



128K × 16 CMOS FLASH MEMORY

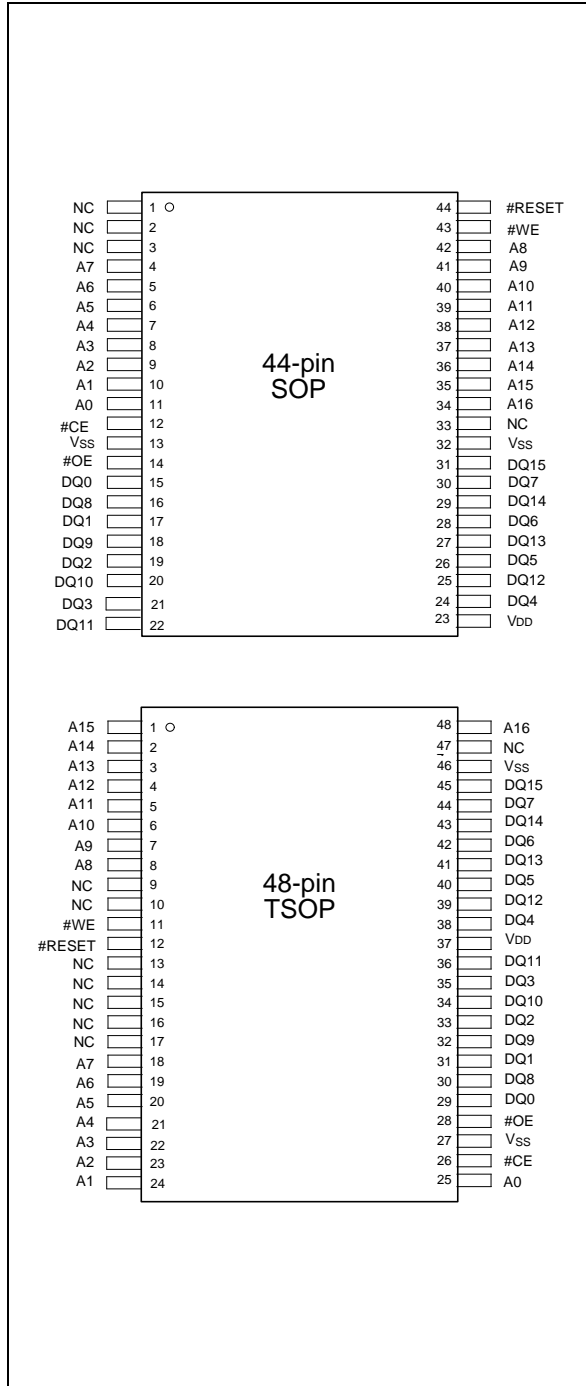
GENERAL DESCRIPTION

The W49F201 is a 2-megabit, 5-volt only CMOS flash memory organized as 128K × 16 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt VPP is not required. The unique cell architecture of the W49F201 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

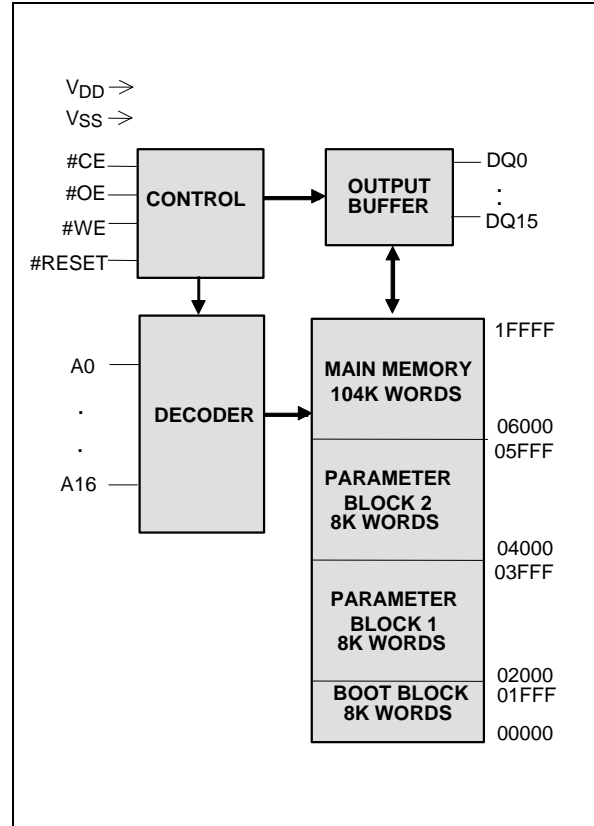
FEATURES

- Single 5-volt operations:
 - 5-volt Read/Erase/Program
- Fast program operation:
 - Word-by-word programming: 50 μS (max.)
- Fast erase operation: 100 mS (typ.)
- Fast read access time: 55/70 nS
- Endurance: 10K cycles (typ.)
- Ten-year data retention
- Hardware data protection
- Sector configuration
 - One 8K word boot block with lockout protection
 - Two 8K word parameter blocks
 - One 104K word main memory block
- Low power consumption
 - Active current: 25 mA (typ.)
 - Standby current: 20 μA (typ.)
- Automatic program and erase timing with internal VPP generation
- End of program or erase detection
 - Toggle bit
 - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard word-wide pinouts
- Available packages: 44-pin SOP, 48-pin TSOP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
#RESET	Reset
A0 – A16	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#WE	Write Enable
VDD	Power Supply
Vss	Ground
NC	No Connection



FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W49F201 is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data to the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for further details.

Reset Operation

The #RESET input pin can be used in some application. When #RESET pin is at high state, the device is in normal operation mode. When #RESET pin is driven low for at least a period of T_{RP} , it will halts the device and all outputs are at high impedance state. The device also resets the internal state machine to read array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence to assure data integrity. As the high state re-asserted to the #RESET pin, the device will return to read or standby mode, it depends on the control signals. The system can read data T_{RH} after the #RESET pin returns to V_{IH} . The other function for #RESET pin is temporary reset the boot block. By applying the 12V to #RESET pin, the boot block can be reprogrammed even though the boot block lockout function is enabled.

Boot Block Operation

There is one 8K-word boot block in this device, which can be used to store boot code. It is located in the first 8K words of the memory with the address range from 0000(hex) to 1FFF(hex).

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout); other memory locations can be changed by the regular programming method.

There is one condition that the lockout feature can be overrides. Just apply 12V to #RESET pin, the lockout feature will temporary be inactivated and the boot block can be erased/programmed. Once the #RESET pin returns to TTL level, the lockout feature will be activated again.

In order to detect whether the boot block feature is set on the 8K-words block, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "0002 hex". If the output data in DQ0 is "1", the boot block programming lockout feature is activated; if the output data in DQ0 is "0", the lockout feature is inactivated and the block can be erased/programmed.

To return to normal operation, perform a three-byte command sequence (or an alternate single-word command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Chip Erase Operation

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycle, the device enters the internal chip erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. The entire memory array will be erased to FF(hex) by the chip erase operation if the boot block programming lockout feature is not activated. Once the boot block lockout feature is activated, the chip erase function will erase all the sectors except the 8Kword boot sector.



Sector Erase Operation

The three sectors, main memory and two parameters blocks, can be erased individually by initiating a six-word command sequence. Sector address is latched on the falling WE edge of the sixth cycle while the 30(hex) data input command is latched at the rising edge of WE. After the command loading cycle, the device enters the internal sector erase mode, which is automatically timed and will be completed in a fast 100 mS (typical). The host system is not required to provide any control or timing during this operation. The device will automatically return to normal read mode after the erase operation completed. Data polling and/or Toggle Bits can be used to detect end of erase cycle.

When the boot block lockout feature is inactivated, the boot block and the main memory block will be erased together. Once the boot block is locked, only the main memory block will be erased by the execution of sector erase operation.

Program Operation

The W49F201 is programmed on a word-by-word basis. Program operation can only change logical data "1" to logical data "0". The erase operation (changed entire data in main memory and/or boot block from "0" to "1" is needed before programming.

The program operation is initiated by a 4-word command cycle (see Command Codes for Word Programming). The device will internally enter the program operation immediately after the word-program command is entered. The internal program timer will automatically time-out (50 μ S max. - TBP) once completed and return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

Hardware Data Protection

The integrity of the data stored in the W49F201 is also hardware protected in the following ways:

- (1) Noise/Glitch Protection: A #WE pulse of less than 15 nS in duration will not initiate a write cycle.
- (2) VDD Power Up/Down Detection: The programming and read operation are inhibited when VDD is less than 2.5V typical.
- (3) Write Inhibit Mode: Forcing #OE low, #CE high, or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.
- (4) VDD power-on delay: When VDD has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

Data Polling (DQ7)- Write Status Detection

The W49F201 includes a data polling feature to indicate the end of a program or erase cycle. When the W49F201 is in the internal program or erase cycle, any attempt to read DQ7 of the last word loaded will receive the complement of the true data. Once the program or erase cycle is completed, DQ7 will show the true data. Note that DQ7 will show logical "0" during the erase cycle, and become logical "1" or true data when the erase cycle has been completed.



Toggle Bit (DQ6)- Write Status Detection

In addition to data polling, the W49F201 provides another method for determining the end of a program cycle. During the internal program or erase cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the program or erase cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software operation. In the software access mode, a six-word (or JEDEC 3-word) command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code, 00DA(hex). A read from address 0001(hex) outputs the device code, 00AE(hex). The product ID operation can be terminated by a three-word command sequence or an alternative one-word command sequence (see Command Definition table).

TABLE OF OPERATING MODES

Operating Mode Selection

(V_{HH} = 12V ±0.5V)

MODE	PINS					
	#CE	#OE	#WE	#RESET	ADDRESS	DQ.
Read	V _{IL}	V _{IL}	V _{IH}	V _{IH}	A _{IN}	D _{out}
Erase/Program	V _{IL}	V _{IH}	V _{IL}	V _{IH}	A _{IN}	D _{in}
Standby	V _{IH}	X	X	V _{IH}	X	High Z
Erase/Program	X	V _{IL}	X	V _{IH}	X	High Z/DOUT
Inhibit	X	X	V _{IH}	V _{IH}	X	High Z/DOUT
Output Disable	X	V _{IH}	X	V _{IH}	X	High Z
Reset	X	X	X	V _{IL}	X	High Z

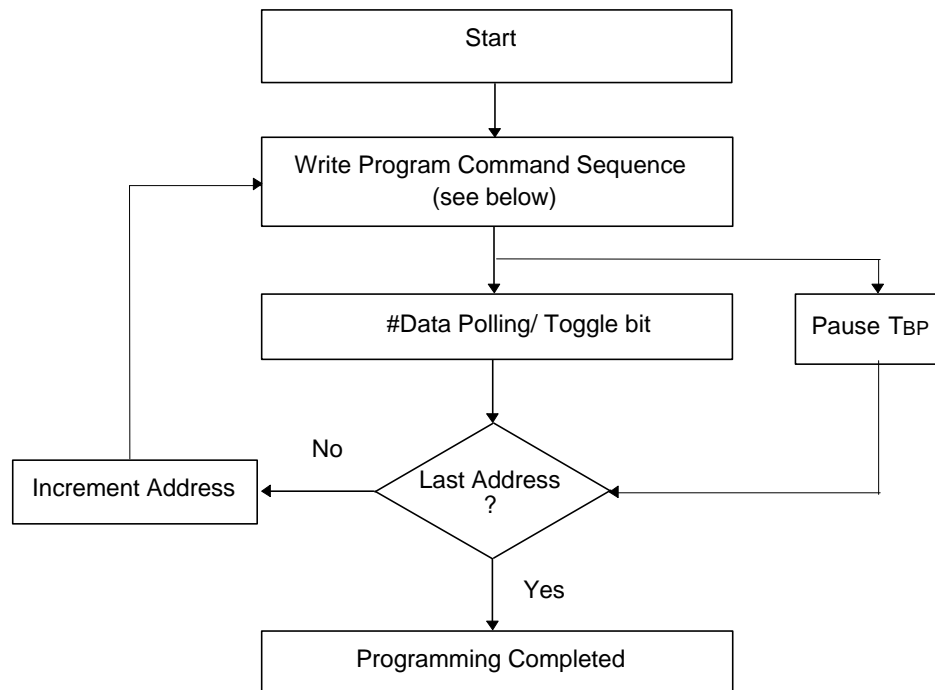
TABLE OF COMMAND DEFINITION

COMMAND DESCRIPTION	NO. OF Cycles	1ST CYCLE	2ND CYCLE	3RD CYCLE	4TH CYCLE	5TH CYCLE	6TH CYCLE
		Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data	Addr. Data
Read	1	A _{IN} D _{OUT}					
Chip Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 10
Sector Erase	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	SA ⁽³⁾ 30
Word Program	4	5555 AA	2AAA 55	5555 A0	A _{IN} D _{IN}		
Boot Block Lockout	6	5555 AA	2AAA 55	5555 80	5555 AA	2AAA 55	5555 40
Product ID Entry	3	5555 AA	2AAA 55	5555 90			
Product ID Exit ⁽¹⁾⁽²⁾	3	5555 AA	2AAA 55	5555 F0			
Product ID Exit ⁽¹⁾⁽²⁾	1	XXXX F0					

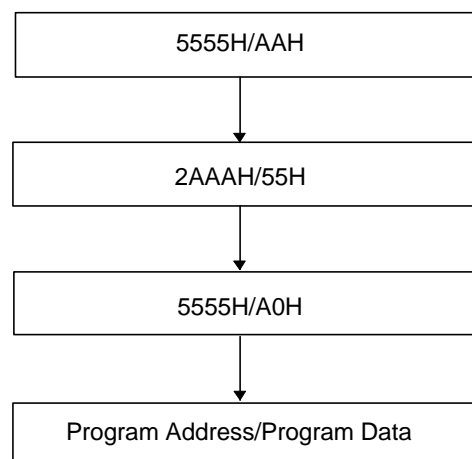
Notes:

1. Data Format: DQ15 – DQ8 (Don't Care); DQ7 – DQ0 (Hex)
2. Either one of the two Product ID Exit commands can be used.
3. SA: Sector Address
 SA = 03XXXh for Parameter Block1
 SA = 05XXXh for Parameter Block2
 SA = 1FXXXh
 - For Main Memory Block when Boot Block lockout feature is activated
 - For both Boot Block and Main Memory Block when Boot Block lockout feature is inactivated

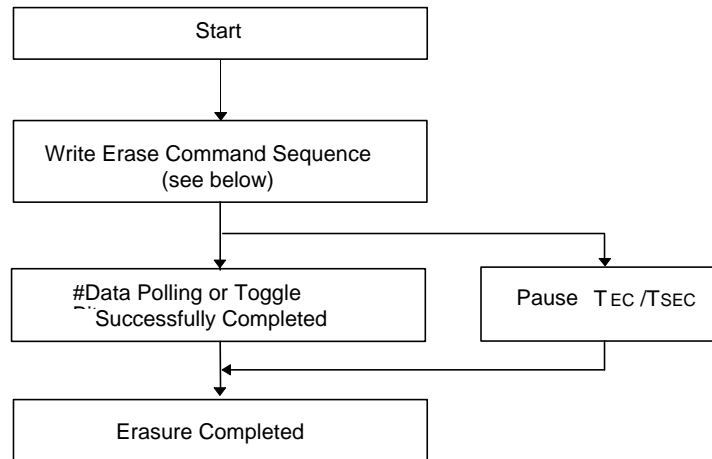
Embedded Programming Algorithm



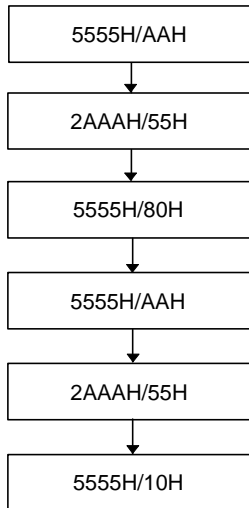
Program Command Sequence (Address/Command):



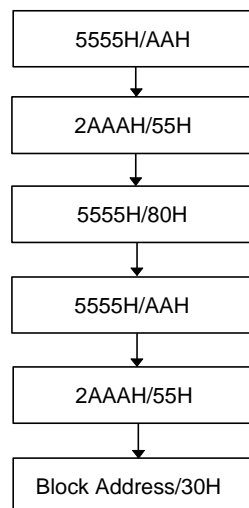
Embedded Erase Algorithm



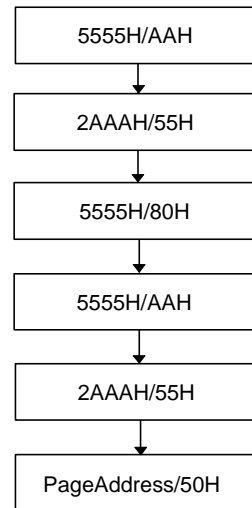
Chip Erase Command Sequence (Address/Command):



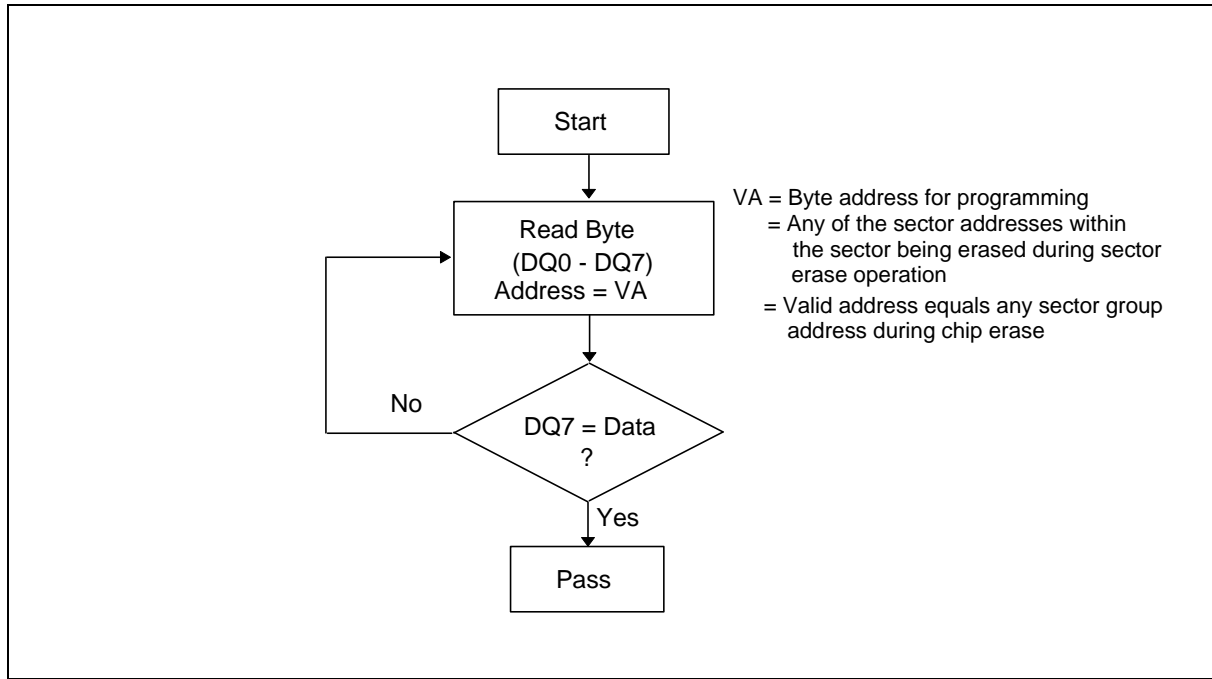
Individual BlockErase Command Sequence (Address/Command):



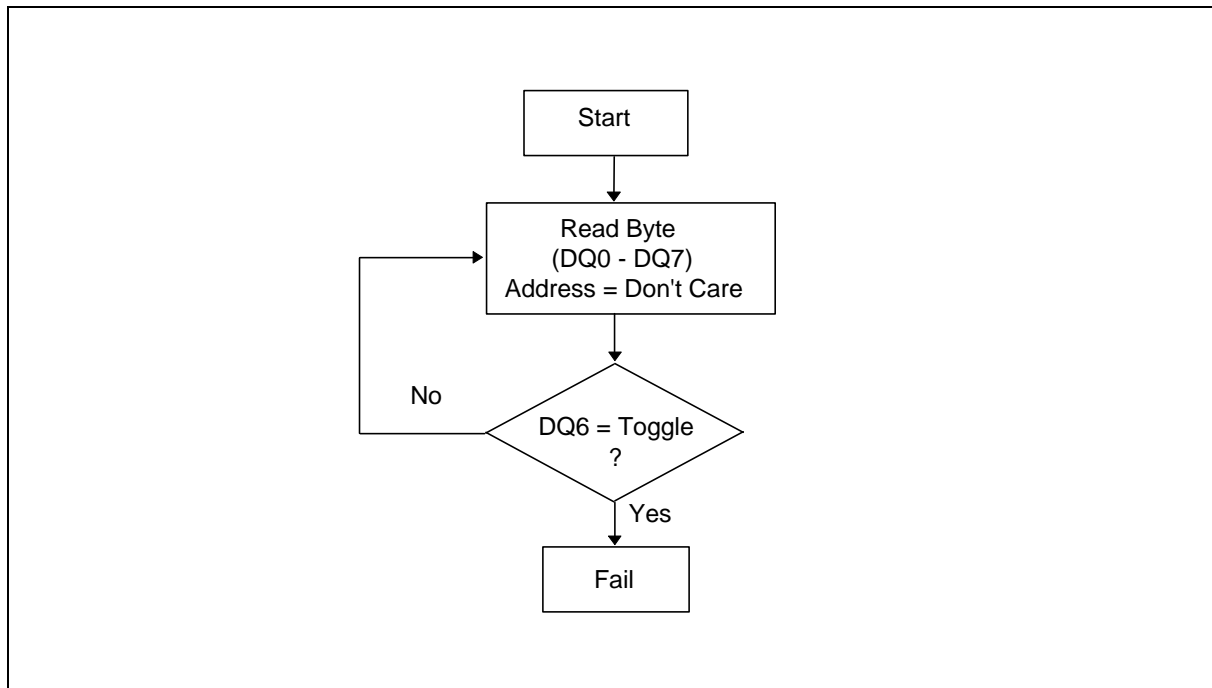
Individual PageErase Command Sequence (Address/Command):



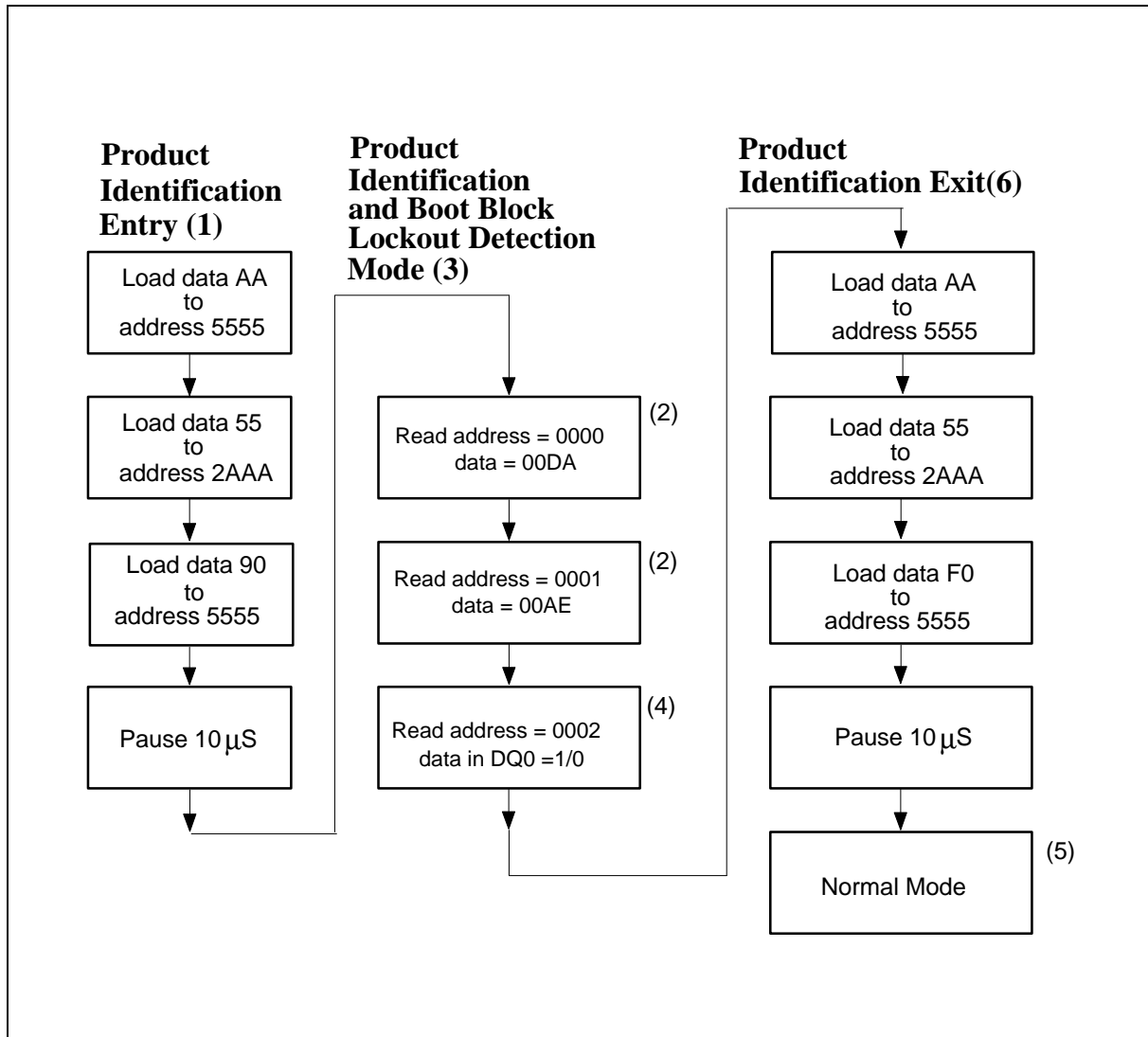
Embedded #Data Polling Algorithm



Embedded Toggle Bit Algorithm

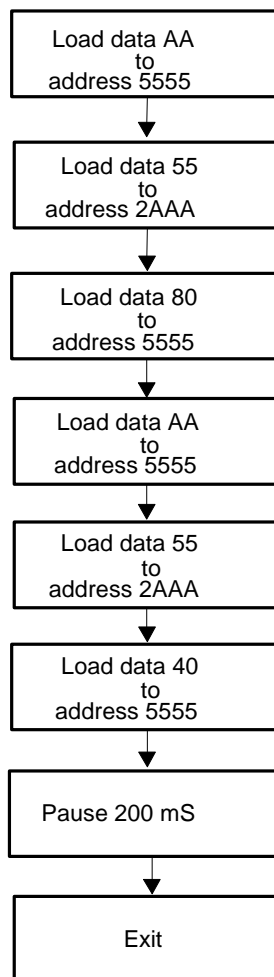


Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

- (1) Data Format: DQ15 – DQ8 (Don't Care), DQ7 – DQ0 (Hex); Address Format: A14 – A0 (Hex)
- (2) A1 – A16 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.
- (3) The device does not remain in identification and boot block lockout detection mode if power down.
- (4) If the output data in DQ0 = 1, the boot block programming lockout feature is activated; if the output data in DQ0 = 0, the lockout feature is inactivated and the block can be programmed.
- (5) The device returns to standard operation mode.
- (6) Optional 1-write cycle (write F0 hex at XXXX address) can be used to exit the product identification/boot block lockout detection.

Boot Block Lockout Enable Acquisition Flow**Boot Block Lockout
Feature Set Flow**



DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to VSS Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential Except #OE	-0.5 to VDD +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to VDD +1.0	V
Voltage on #OE Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(VDD = 5.0V ±10%, VSS = 0V, TA = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	ICC	#CE = #OE = VIL, #WE = VIH, all DQs open Address inputs = VIL/VIH, at f = 5 MHz	-	25	50	mA
Standby VDD Current (TTL input)	ISB1	#CE = VIH, all DQs open Other inputs = VIL/VIH	-	2	3	mA
Standby VDD Current (CMOS input)	ISB2	#CE = VDD -0.3V, all DQs open Other inputs = VDD -0.3V/ VSS	-	20	100	µA
Input Leakage Current	ILI	VIN = VSS to VDD	-	-	10	µA
Output Leakage Current	ILO	VOUT = VSS to VDD	-	-	10	µA
Input Low Voltage	VIL	-	-0.3	-	0.8	V
Input High Voltage	VIH	-	2.0	-	VDD +0.5	V
Output Low Voltage	VOL	IOL = 2.1 mA	-	-	0.45	V
Output High Voltage	VOH	IOH = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU. READ	100	μ S
Power-up to Write Operation	TPU. WRITE	5	mS

CAPACITANCE

($V_{DD} = 5.0V$, $T_A = 25^\circ C$, $f = 1\text{ MHz}$)

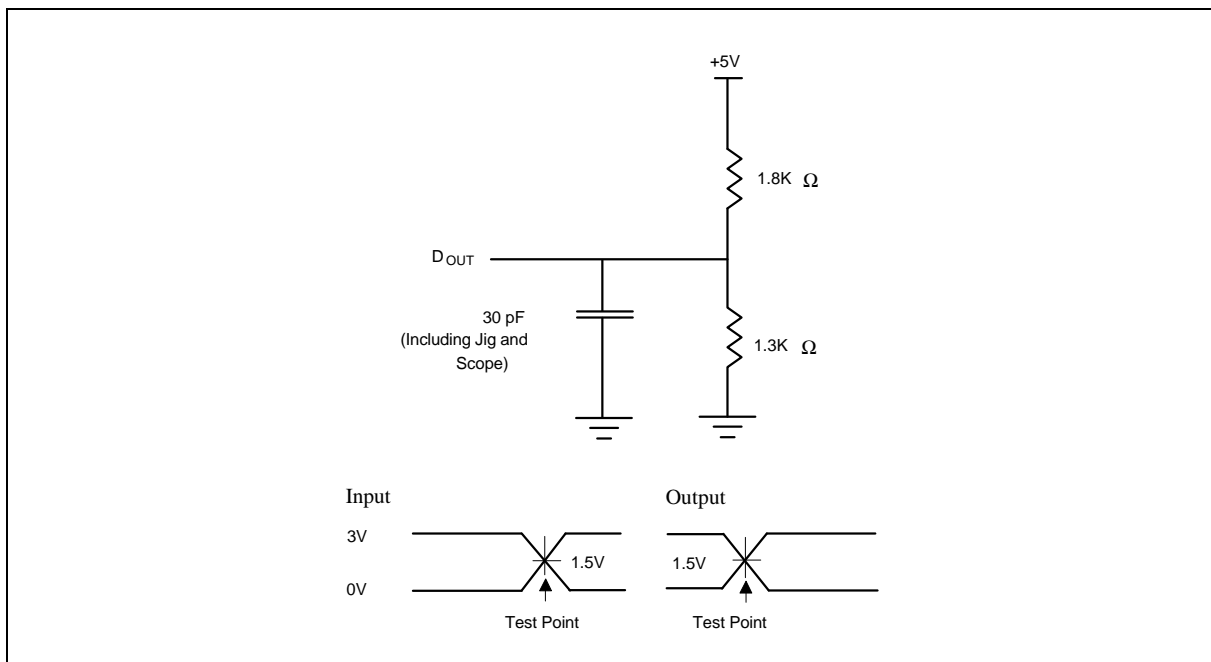
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	C _{I/O}	$V_{I/O} = 0V$	12	pf
Input Capacitance	C _{IN}	$V_{IN} = 0V$	6	pf

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and $C_L = 30\text{ pF}$

AC Test Load and Waveform





AC Characteristics, continued

Read Cycle Timing Parameters(V_{DD} = 5.0V ±10 %, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W49F201-55		W49F201-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	55	-	70	-	nS
Chip Enable Access Time	TCE	-	55	-	70	nS
Address Access Time	TAA	-	55	-	70	nS
Output Enable Access Time	TOE	-	30	-	35	nS
#CE Low to Active Output	TCLZ	0	-	0	-	nS
#OE Low to Active Output	TOLZ	0	-	0	-	nS
#CE High to High-Z Output	TCHZ	-	25	-	25	nS
#OE High to High-Z Output	TOHZ	-	25	-	25	nS
Output Hold from Address Change	TOH	0	-	0	-	nS

Note: The parameter of TCLZ, TOLZ, TCHZ, TOHZ are characterized only and is not 100% tested.

Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Address Setup Time	TAS	0	-	-	nS
Address Hold Time	TAH	50	-	-	nS
#WE and #CE Setup Time	TCS	0	-	-	nS
#WE and #CE Hold Time	TCH	0	-	-	nS
#OE High Setup Time	TOES	0	-	-	nS
#OE High Hold Time	TOEH	0	-	-	nS
#CE Pulse Width	TCP	70	-	-	nS
#WE Pulse Width	TWP	70	-	-	nS
#WE High Width	TWPH	100	-	-	nS
Data Setup Time	TDS	50	-	-	nS
Data Hold Time	TDH	10	-	-	nS
Word programming Time	TBC	-	35	50	μS
Erase Cycle Time	TEC	-	100	200	mS

Note: All AC timing signals observe the following guidelines for determining setup and hold times:

(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.



AC Characteristics, continued

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYMBOL	W49F201-55		W49F201-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
#OE to Data Polling Output Delay	TOEP	-	30	-	35	nS
#CE to Data Polling Output Delay	TCEP	-	55	-	70	nS
#WE High to #OE Low for Data Polling	TOHP	100	-	100	-	nS
#OE to Toggle Bit Output Delay	TOET	-	30	-	35	nS
#CE to Toggle Bit Output Delay	TCET	-	55	-	70	nS
#WE High to #OE Low for Toggle Bit	TOHT	100	-	100	-	nS

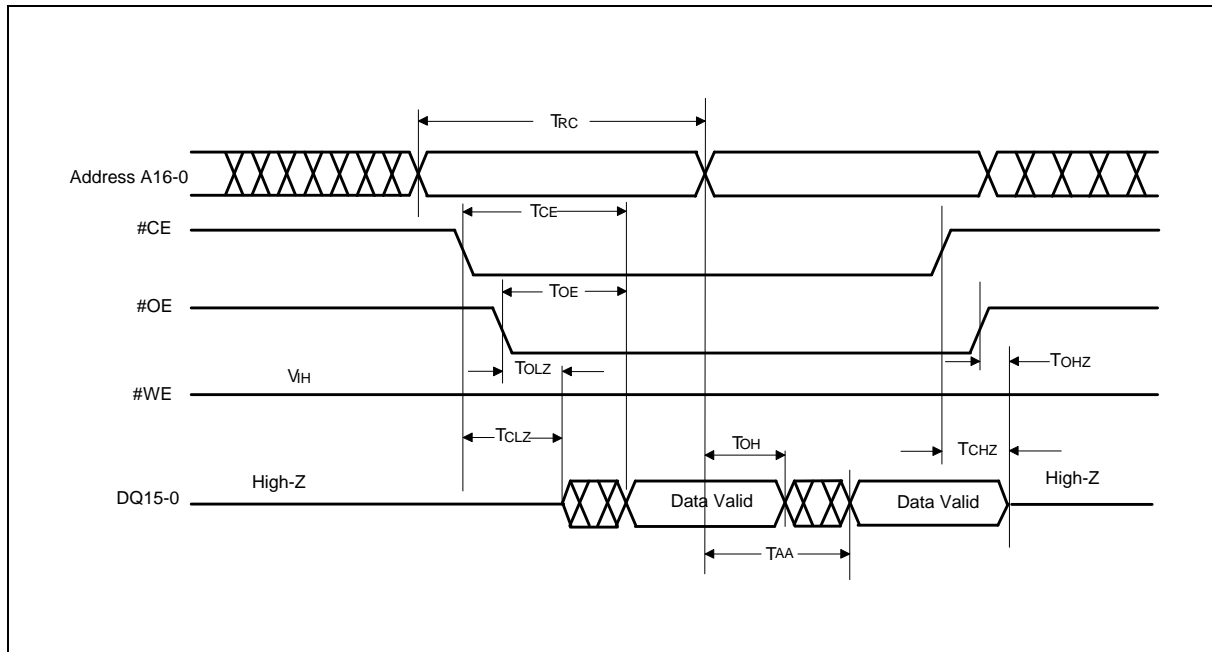
Hardware Reset Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
#RESET Pulse Width	TRP	500	-	nS
#RESET High Time Before Read(1)	TRH	10	-	μS

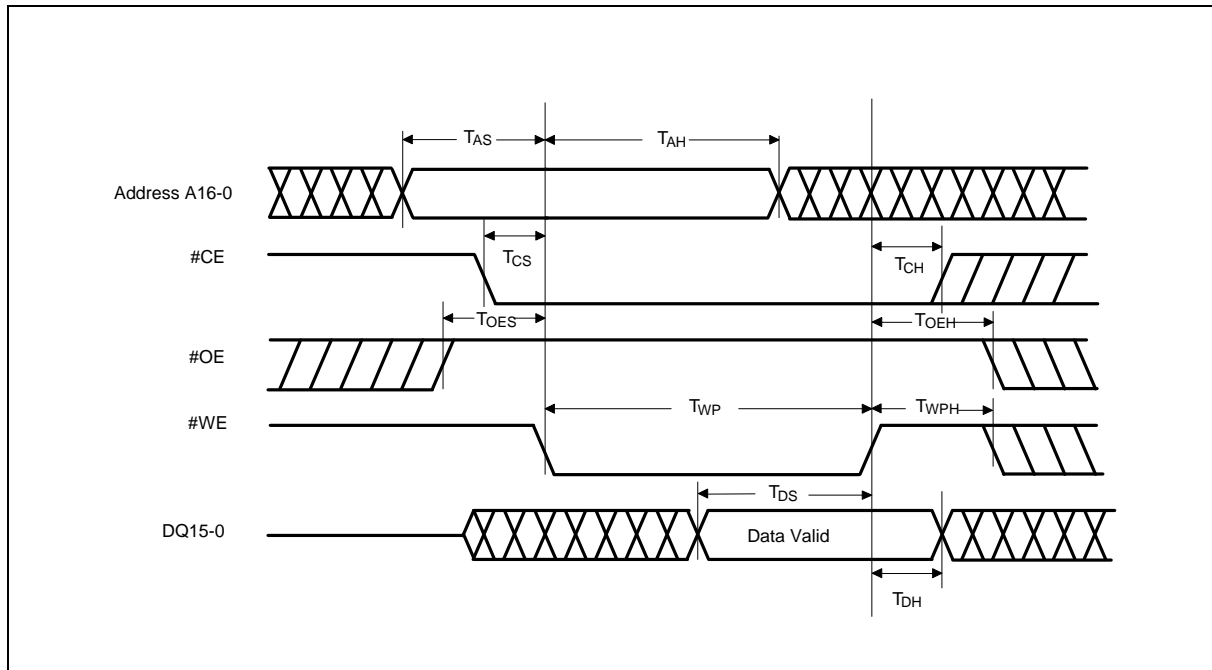
Note: 1. The parameters are characterized only and is not 100% tested.

TIMING WAVEFORMS

Read Cycle Timing Diagram

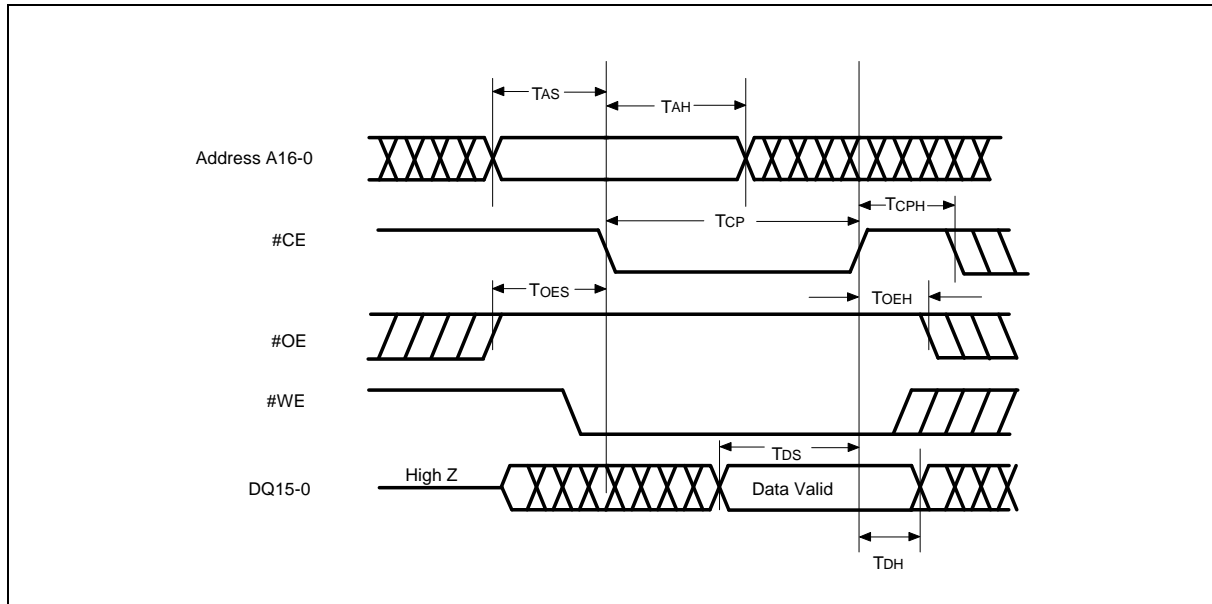


#WE Controlled Command Write Cycle Timing Diagram

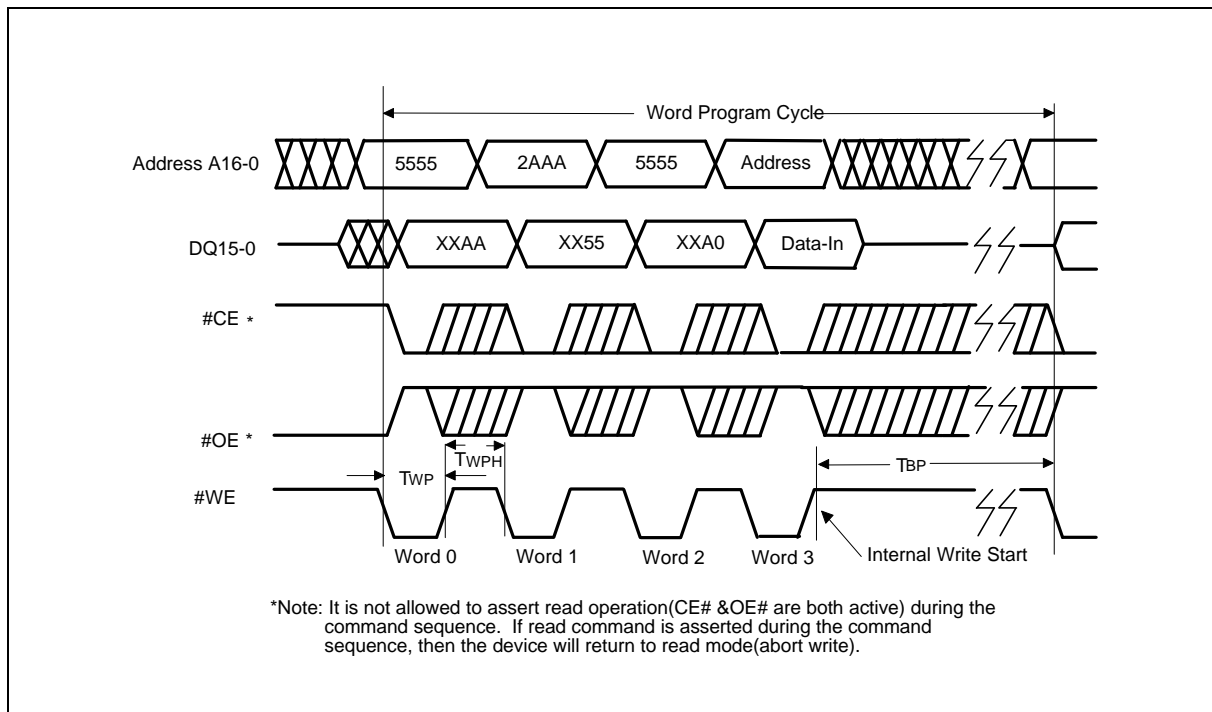


Timing Waveforms, continued

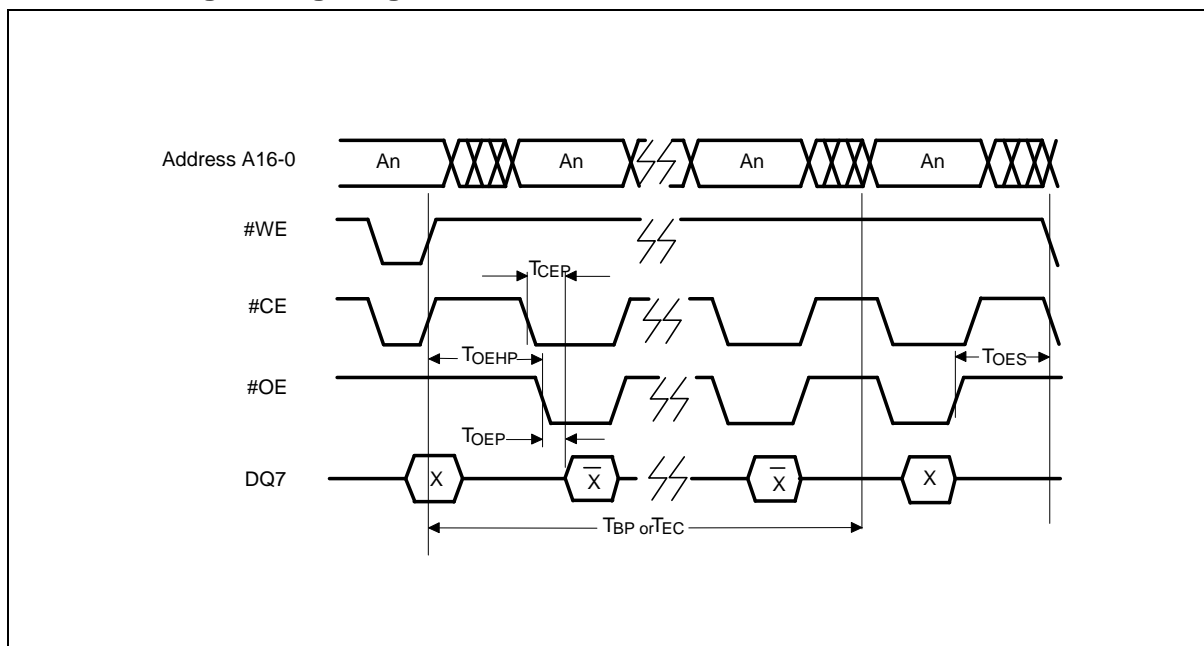
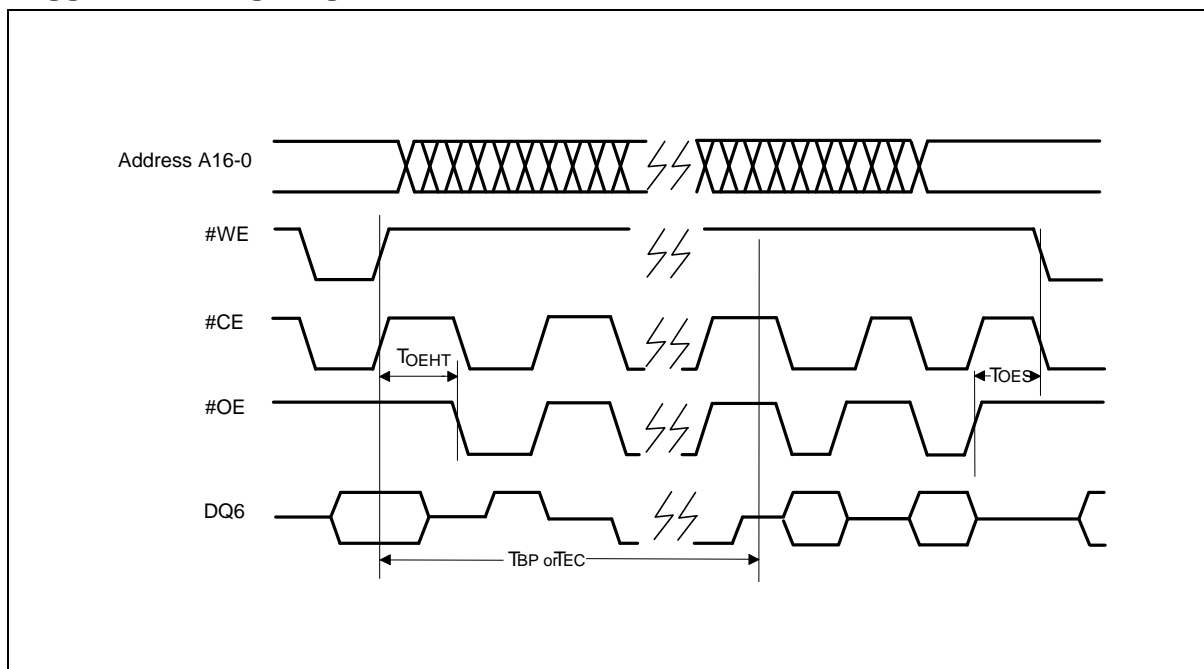
#CE Controlled Command Write Cycle Timing Diagram



Program Cycle Timing Diagram

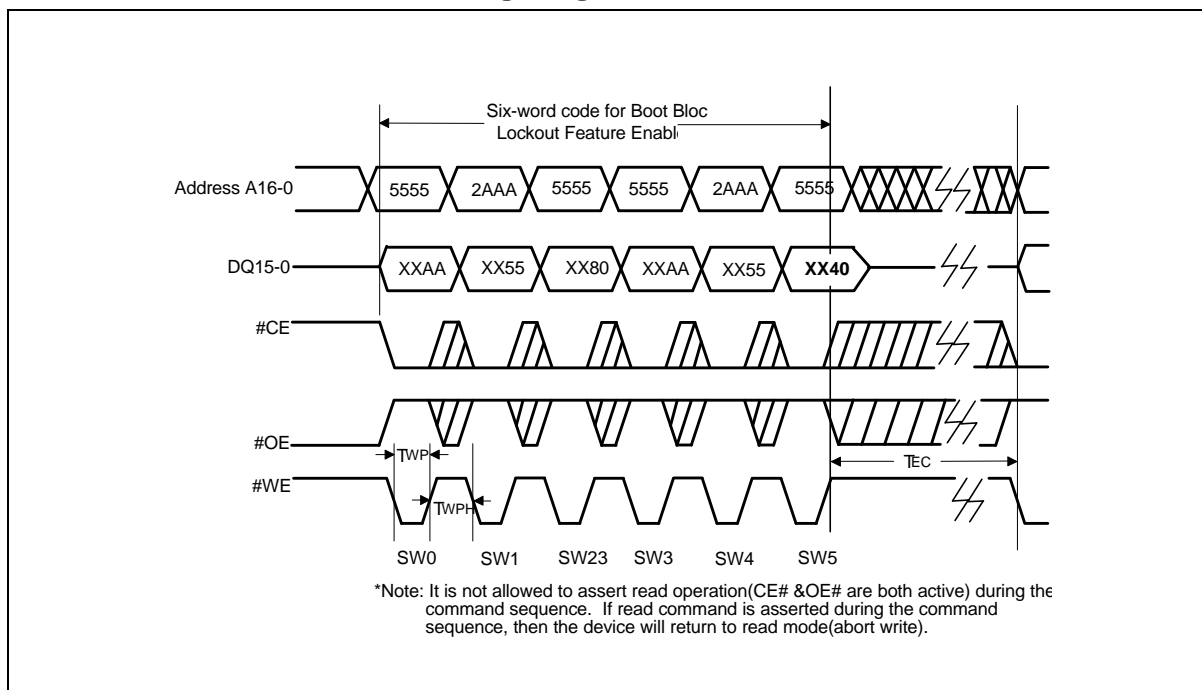


Timing Waveforms, continued

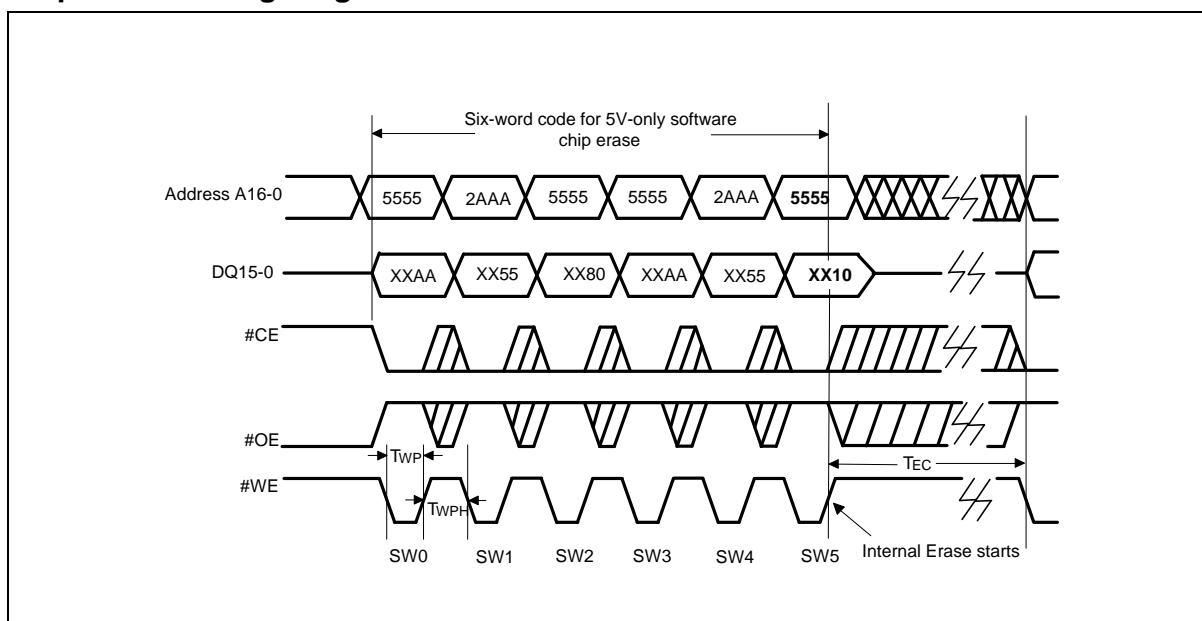
#DATA Polling Timing Diagram**Toggle Bit Timing Diagram**

Timing Waveforms, continued

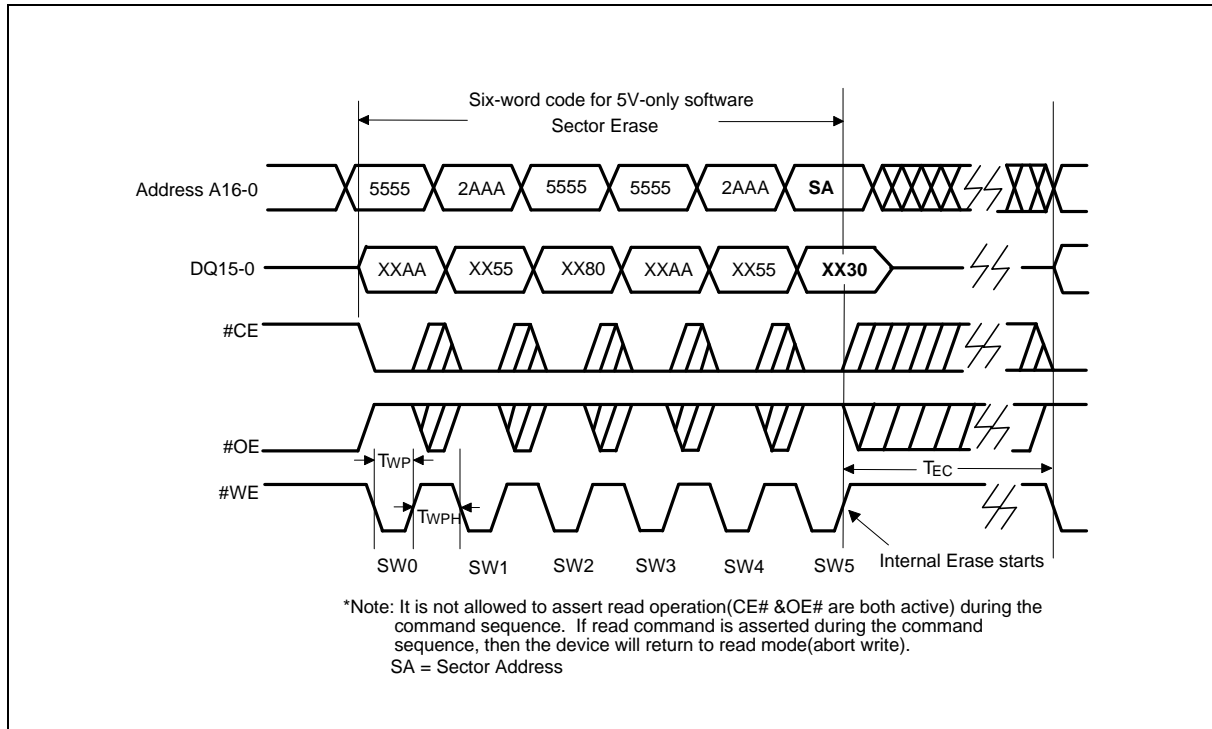
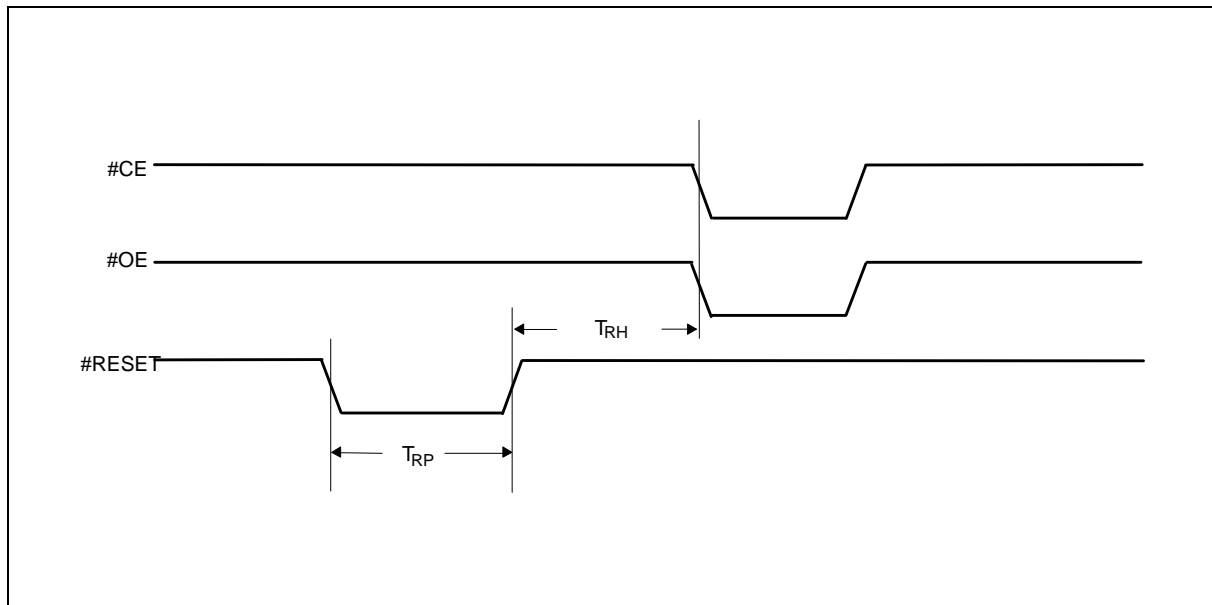
Boot Block Lockout Enable Timing Diagram



Chip Erase Timing Diagram



Timing Waveforms, continued

Sector Erase Timing Diagram**Reset Timing Diagram**



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V _{DD} CURRENT MAX. (mA)	PACKAGE	CYCLE
W49F201S-55B	55	50	100 (CMOS)	44-pin SOP	10K
W49F201S-70B	70	50	100 (CMOS)	44-pin SOP	10K
W49F201T-55B	55	50	100 (CMOS)	48-pin TSOP (12 mm × 20 mm)	10K
W49F201T-70B	70	50	100 (CMOS)	48-pin TSOP (12 mm × 20 mm)	10K

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

HOW TO READ THE TOP MARKING

Example: The top marking of 48-pin TSOP W49F201T-55B



1st line: Winbond logo

2nd line: The part number: W49F201T-55B

3rd line: The lot number

4th line: The tracking code: 149 O B SA

149: Packages made in '01, week 49

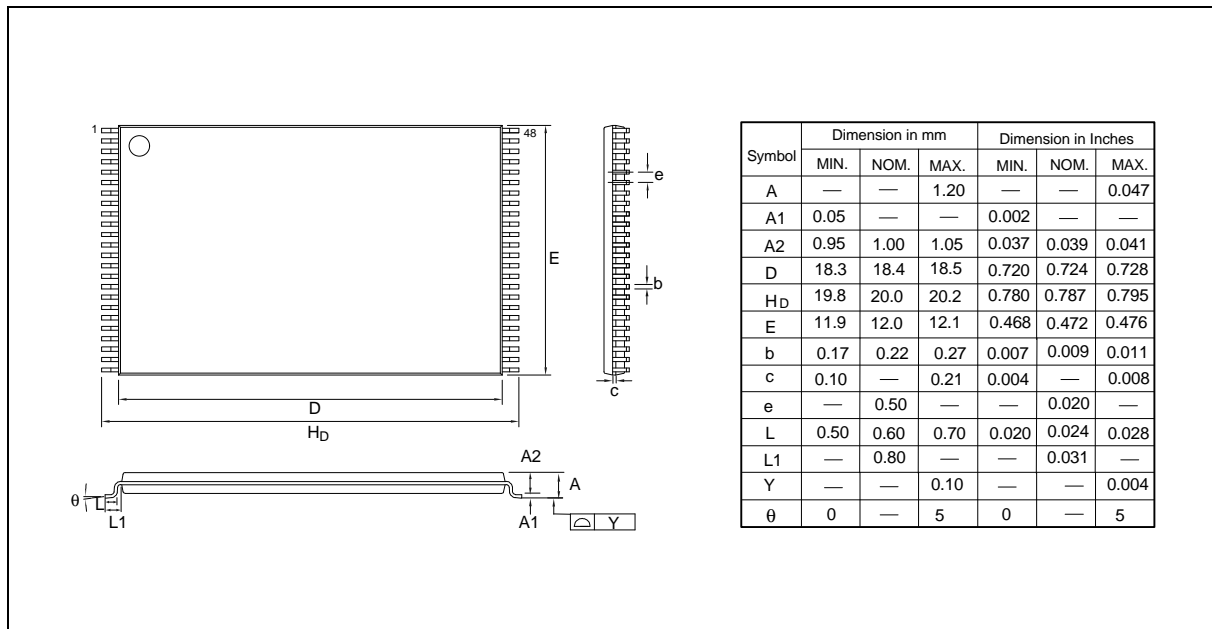
O: Assembly house ID: A means ASE, O means OSE, ..etc.

B: IC revision; A means version A, B means version B, ..etc.

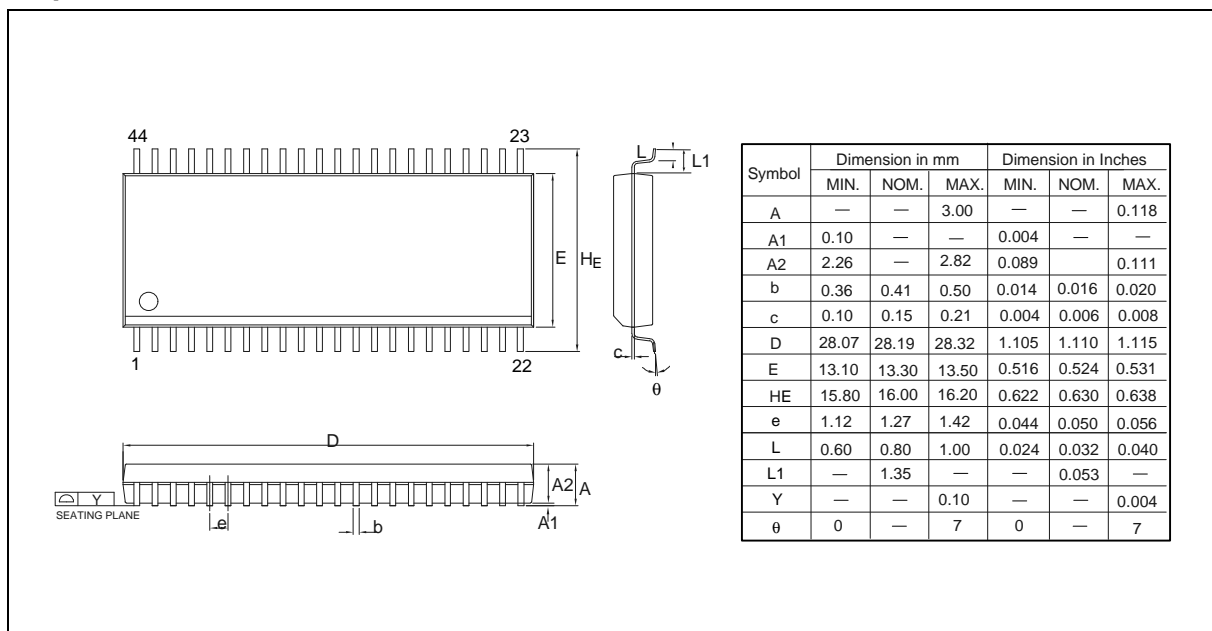
SA: Process code

PACKAGE DIMENSIONS

48-pin TSOP (12 mm × 20 mm)



44-pin SOP



**VERSION HISTORY**

VERSION	DATE	PAGE	DESCRIPTION
A1	Jun. 1999	-	Renamed from W29F201C
A2	May 2001	1	Change Fast Erase Operation from 60 mS to 100 mS
		1, 2, 4, 6, 9, 14, 20	Modify Sector Configuration description
		14, 15	Modify Output Enable Access Time
		1, 14, 15, 22	Add 70 nS bin
		1, 22	Delete Endurance 1K cycles
		5	Delete hardware operation description
A3	July 2001	1, 14, 15, 21	Delete access time of 45 nS
		15	Change TRH from 50 nS to 10 μ S
A4	Jan. 8, 2002	4, 6	Modify Sector Configuration description
		5	Modify $V_{HH} = 12V \pm 5\%$ as $V_{HH} = 12V \pm 0.5V$
A5	Jan. 24, 2002	4	Modify VDD Power Up/Down Detection in Hardware Data Protection
		7 – 11	Modify Embedded Alogorithm
		17	Modify Program Cycle Timing Diagram
		21	Add HOW TO READ THE TOP MARKING



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Revision A5