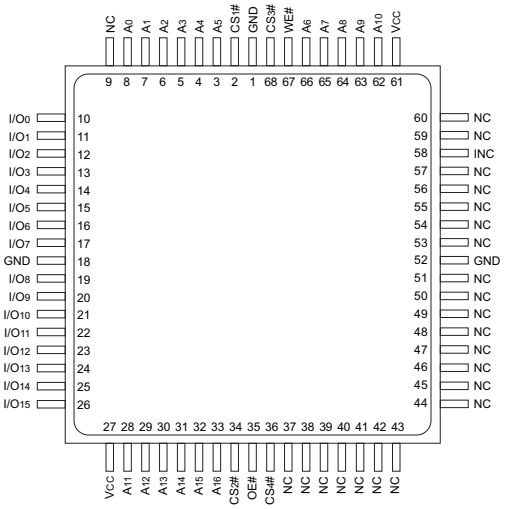
512Kx16 CMOS EEPROM MODULE

FEATURES

- Access Time of 140, 150, 200ns
- Packaging:
  - 68 lead, 40mm Hermetic CQFP (Package 501)
- Organized as 4 banks of 128Kx16
- Write Endurance 10,000 Cycles
- Data Retention Ten Years Minimum
- Military Temperature Range
- Low Power CMOS
- Automatic Page Write Operation
- Page Write Cycle Time: 10ms Max
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- 8 Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight - 20 grams typical

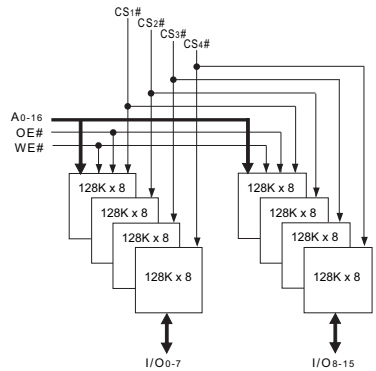
FIGURE 1 – PIN CONFIGURATION
Top View



Pin Description

I/O0-15	Data Input/Output
A0-16	Address Inputs
WE#	Write Enable
CS1-4#	Chip Selects
OE#	Output Enable
V_{CC}	+5.0V Power
GND	Ground
NC	Not Connected

Block Diagram



NOTE: CS1-4# are used as bank selects. During reads, only one CSx# can be active at one time.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Signal Voltage Relative to GND	V_G	-0.6 to + 6.25	V
Voltage on OE# and A9		-0.6 to +13.5	V

NOTE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE capacitance	COE	VIN = 0 V, f = 1.0 MHz	50	pF
WE capacitance	CWE	VIN = 0 V, f = 1.0 MHz	50	pF
CS1-4 capacitance	CCS	VIN = 0 V, f = 1.0 MHz	25	pF
Data I/O capacitance	CI/O	VI/O = 0 V, f = 1.0 MHz	40	pF
Address input capacitance	CAD	VIN = 0 V, f = 1.0 MHz	70	pF

This parameter is guaranteed by design but not tested.

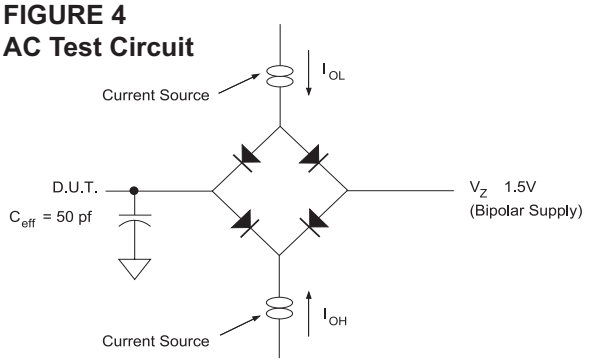
DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, Vout = GND to V_{CC}		10	µA
Operating Supply Current (x16)	I_{CCx16}	CS1# = V_{IL}, OE# = CS2-4# = V_{IH}, f = 5MHz, V_{CC} = 5.5		160	mA
Chip Erase Current	I_{CC1}	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		250	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		5	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5V		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.5V	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

FIGURE 4
AC Test Circuit



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes: V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

WRITE

A write cycle is initiated when OE# is high and a low pulse is on WE# or CS# with CS# or WE# low. The address is latched on the falling edge of CS# or WE# whichever occurs last. The data is latched by the rising edge of CS# or WE#, whichever occurs first. A word write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 3 and 4 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the CS# line low. Write enable consists of setting the WE# line low. The write cycle begins when the last of either CS# or WE# goes low.

The WE# line transition from high to low also initiates an internal 150 µsec delay timer to permit page mode operation. Each subsequent WE# transition from high to low that occurs before the completion of the 150 µsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Write Cycle Parameter	Symbol	Min	Max	Unit
Write Cycle Time, TYP = 6ms	t_{WC}		10	ms
Address Set-up Time	t_{AS}	10		ns
Write Pulse Width (WE# or CS#)	t_{WP}	120		ns
Chip Select Set-up Time	t_{CS}	0		ns
Address Hold Time	t_{AH}	100		ns
Data Hold Time	t_{DH}	10		ns
Chip Select Hold Time	t_{CSH}	0		ns
Data Set-up Time	t_{DS}	100		ns
Output Enable Set-up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width High	t_{WPH}	50		ns

FIGURE 3 – WRITE WAVEFORM WE# CONTROLLED

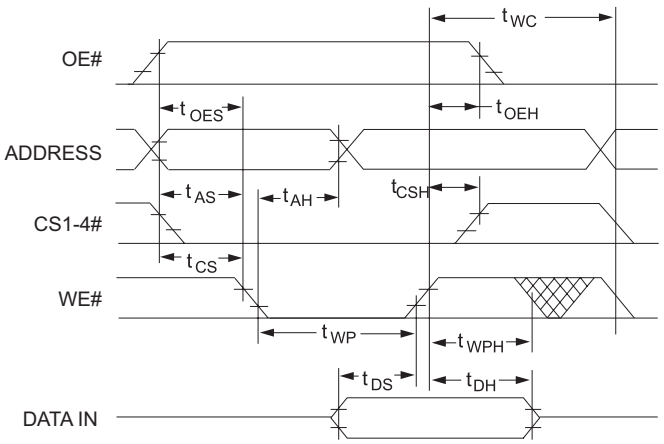
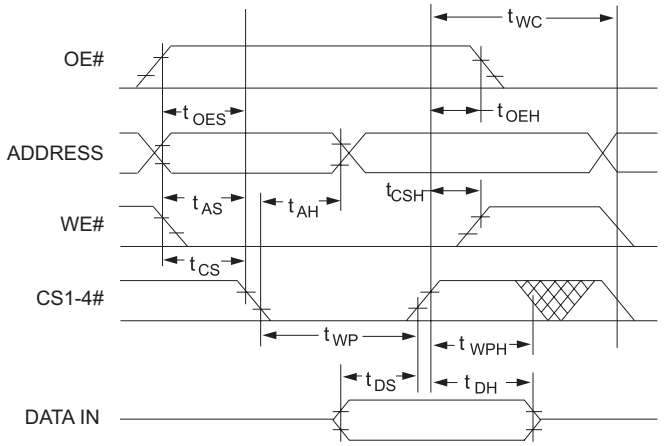


FIGURE 4 – WRITE WAVEFORM CS# CONTROLLED



READ

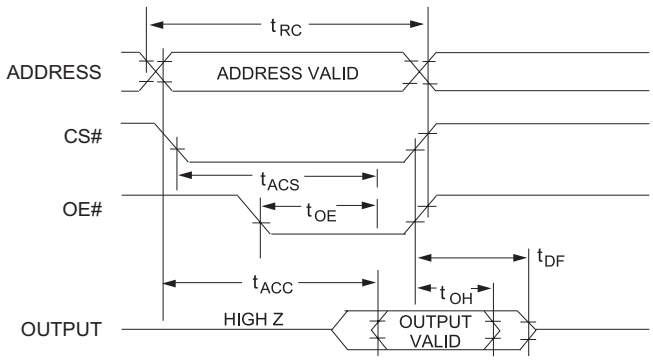
The module stores data at the memory location determined by the address pins. When CS# and OE# are low and WE# is high, this data is present on the outputs. When CS# and OE# are high, the outputs are in a high impedance state. This two line control prevents bus contention.

AC READ CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	-140		-150		-200		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	trc	140		150		200		ns
Address Access Time	tacc		140		150		200	ns
Chip Select Access Time	tacs		140		150		200	ns
Output Hold from Address Change, OE# or CS#	toh	0		0		0		ns
Output Enable to Output Valid	toe	0	50	0	55	0	55	ns
Chip Select or OE# to High Z Output	tdf		50		70		70	ns

FIGURE 5 – READ WAVEFORMS



Notes:
OE# may be delayed up to t_{ACS} - t_{OE} after the falling edge of CS# without impact on t_{OE} or by t_{ACC} - toe after an address change without impact on t_{ACC}.
CS1-4# are used as bank selects.
During reads, only one CSx# can be active at one time.

DATA POLLING

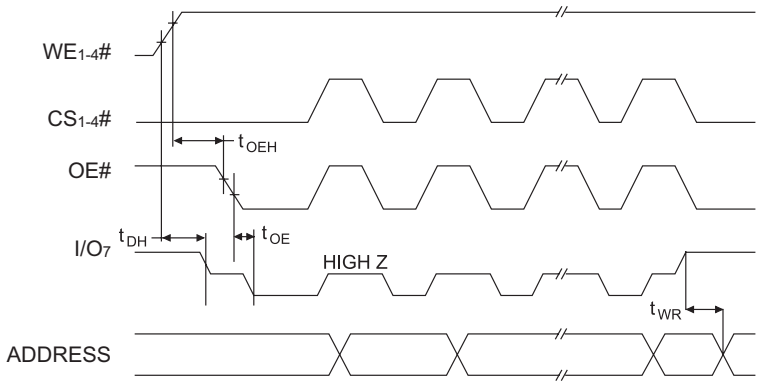
The module offers a data polling feature which allows a faster method of writing to the device. Figure 6 shows the timing diagram for this function. During a word or page write cycle, an attempted read of the last word written will result in the complement of the written data on I/O_7 and I/O_{15}. Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

DATA POLLING CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Min	Max	Unit
Data Hold Time	t_{DH}	10		ns
OE# Hold Time	t_{OEH}	10		ns
OE# To Output Valid	t_{OE}		55	ns
Write Recovery Time	t_{WR}	0		ns

FIGURE 6 – DATA POLLING WAVEFORM



PAGE WRITE OPERATION

The module has a page write operation that allows one to 128 words of data to be written into the device and consecutively loads during the internal programming period. Successive words may be loaded in the same manner after the first data word has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A_0 through A_6 at each write cycle. In this manner a page of up to 128 words can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of words will be written at the same time. The internal programming cycle is the same regardless of the number of words accessed.

PAGE WRITE CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Page Mode Write Characteristics	Symbol			Unit
Parameter		**Min**	**Max**	
Write Cycle Time, TYP = 6ms	t_{WC}		10	ms
Address Set-up Time	t_{AS}	0		ns
Address Hold Time (1)	t_{AH}	50		ns
Data Set-up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	0		ns
Write Pulse Width	t_{WP}	100		ns
Word Load Cycle Time	t_{BLC}		150	µs
Write Pulse Width High	t_{WPH}	50		ns

1. Page address must remain valid for duration of write cycle.

FIGURE 7 – PAGE MODE WRITE WAVEFORM

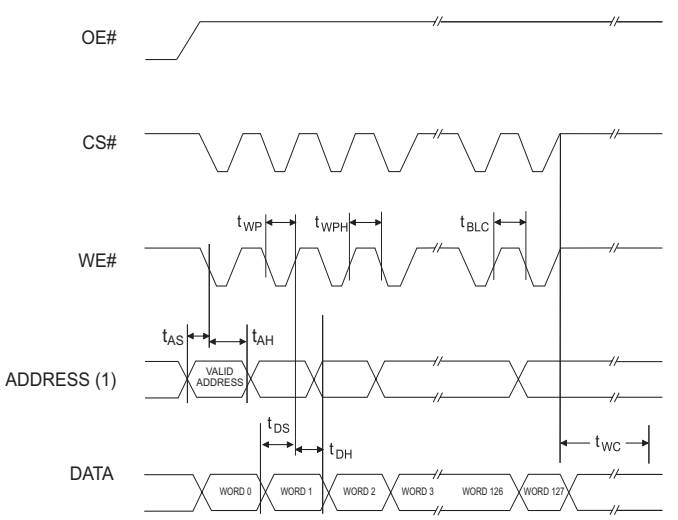
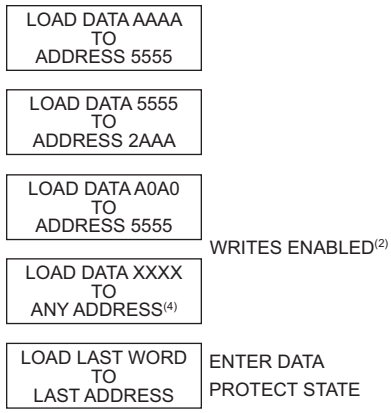
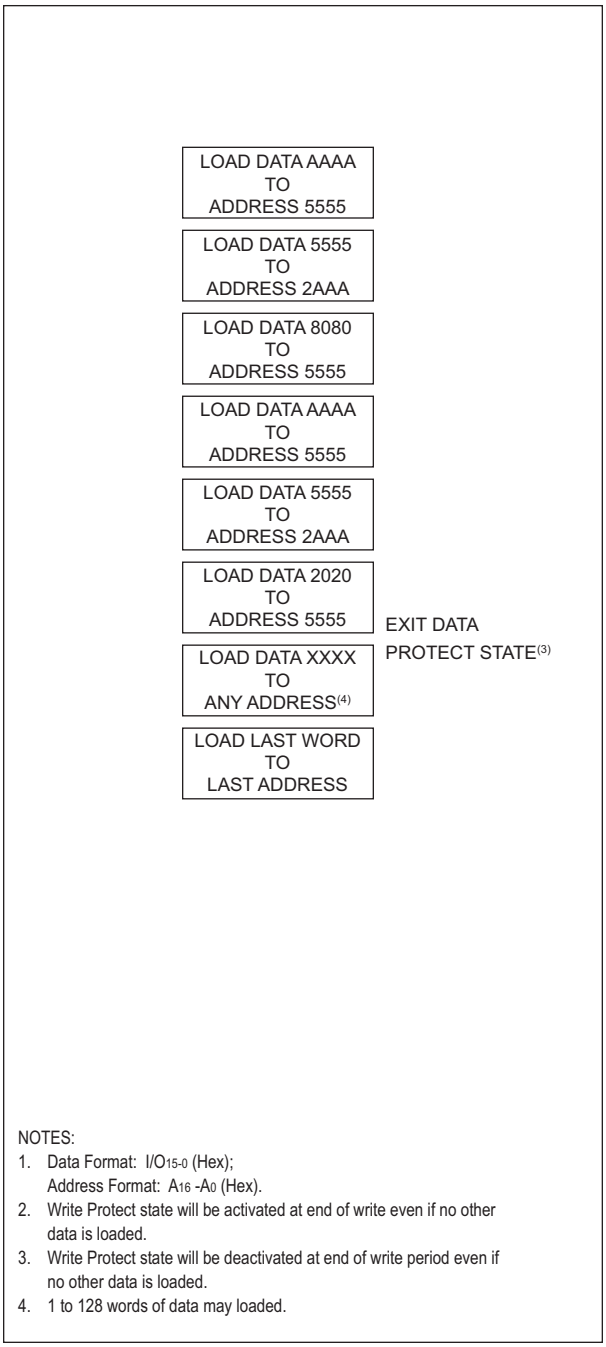


FIGURE 8 – SOFTWARE BLOCK DATA PROTECTION ENABLE ALGORITHM(1)



NOTES:
1. Data Format: I/O_{7-0} (Hex);
   Address Format: A_{14} -A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 words of data to be loaded.

FIGURE 9 –
SOFTWARE BLOCK DATA PROTECTION
DISABLE ALGORITHM(1)



NOTES:
1. Data Format: I/O_{15-0} (Hex);
   Address Format: A_{16} -A_0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 words of data may loaded.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the module has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code words to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three-word write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-word command sequence will start the internal write timers. No data will be written to the device, however, for the duration of t_{WC}. The write protection feature can be disabled by a six-word write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 128K-word block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the module. These are included to improve reliability during normal operation:

a) V_{CC} power on delay

As V_{CC} climbs past 3.8V typical the device will wait 5 msec typical before allowing write cycles.

b) V_{CC} sense

While below 3.8V typical write cycles are inhibited.

c) Write inhibiting

Holding OE# low and either CS# or WE# high inhibits write cycles.

d) Noise filter

Pulses of <8ns (typ) on WE# or CS# will not initiate a write cycle.