2Mx32 FLASH MODULE

DESCRIPTION

The EDI7F342MV and EDI 7F2342MV are organized as one and two banks of 2Mx32 respectively. The modules are based on Intel's 28F016S3- 2Mx8 Flash device in TSOP packages which are mounted on an FR4 substrate.

Both modules offer access times between 120 and 150ns allowing for operation of high-speed microprocessors without wait states.

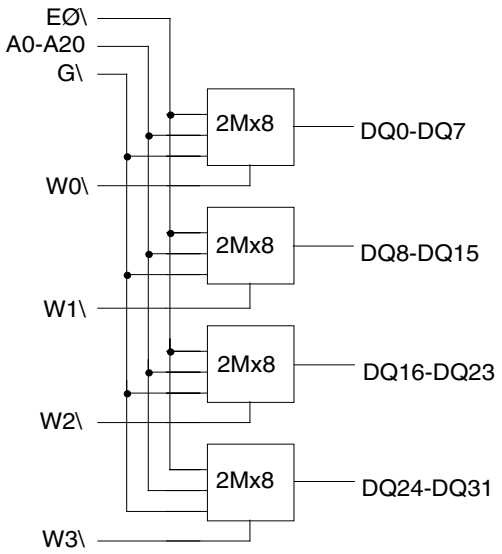
FEATURES

- 2Mx32 and 2x2Mx32 Densities
- Based on Intel's 28F016S3 Flash Device
- Fast Read Access Time - 120ns
- Low Power Dissipation
  - 30mA per Device Active Current
  - 10µA per Device CMOS Standby Current
- Typical Endurance >100,000 Cycles
- Single 3.0 Volt -10% +20% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Range
- Package
  - 80 Pin SIMM (JEDEC)
- Flexible Smart Voltage
  - 2.7-3.6V Program Erase
  - 2.7-3.6V Read Operation
  - 12V Vpp Fast Production Programming

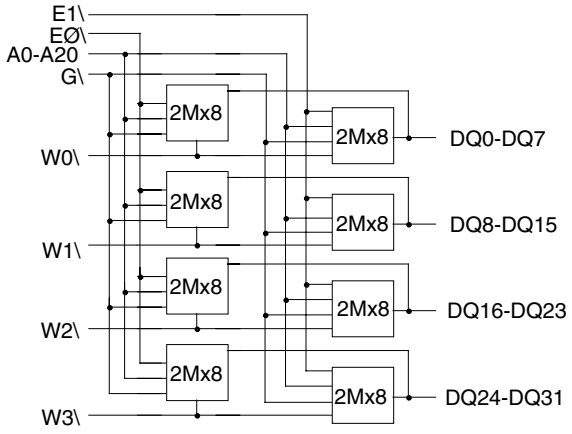
FIG. 1

BLOCK DIAGRAMS

EDI7F342MV-BNC: 2Mx32 80 PIN SIMM



EDI7F2342MV-BNC: 2x2Mx32 80 PIN SIMM



CAPACITANCE

(f=1.0MHz, VIN = VCC or VSS)

Parameter	Sym	2Meg Max	2x2Meg Max	Unit
Address Lines	CA	35	70	pF
Data lines	CDQ	15	30	pF
Chip & Write Enable Lines	CC	15	30	pF
Output Enable lines	CG	35	70	pF

PIN CONFIGURATIONS

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	VSS	21	*	41	A11	61	DQ9
2	VCC	22	*	42	A10	62	DQ8
3	VPP	23	*	43	A9	63	DQ7
4	G\	24	*	44	A8	64	DQ6
5	W0\	25	VSS	45	A7	65	DQ5
6	W1\	26	DQ29	461	A6	66	DQ4
7	NC	27	DQ30	47	A5	67	DQ3
8	DQ16	28	DQ31	48	A4	68	DQ2
9	DQ17	29	W2\	49	A3	69	DQ1
10	DQ18	30	NC	50	A2	70	DQ0
11	DQ19	31	NC	51	A1	71	VPP
12	DQ20	32	A20	52	AO	72	VCC
13	DQ21	33	A19	53	W3\	73	PD1
14	DQ22	34	A18	54	VSS	74	PD2
15	DQ23	35	A17	55	DQ15	75	PD3
16	DQ24	36	A16	56	DQ14	76	PD4
17	DQ25	37	A15	57	DQ13	77	PD5
18	DQ26	38	A14	58	DQ12	78	PD6
19	DQ27	39	A13	59	DQ11	79	PD7
20	DQ28	40	A12	60	DQ10	80	VSS

**TBD*

Simm Density		
Pin	2Meg	2x2Meg
21	NC	NC
22	NC	NC
23	NC	E1\
24	E0\	EO\

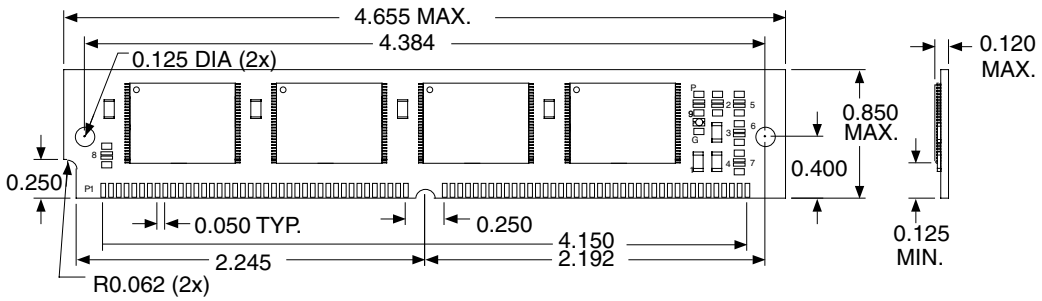
Presence Detect Pin Out		
Pin	2Meg	2x2Meg
PD1	VSS	NC
PD2	NC	VSS
PD3	VSS	VSS
PD4	VSS	VSS

A0-A20	Address input
E0\, E1\	Chip Enable
W0\-W3\	Write Enable
G\	Output Enable
DQ0-DQ31	Data Input/Output
PD	Presence Detect
VCC	Power 3.0V -10% +20%
VSS	Ground
NC	No Connect
VPP	Program Power 2.7V - 12.5V

ORDERING INFORMATION

Part Number	Speed (ns)	Package
EDI7F342MV120BNC	120	364
EDI7F342MV150BNC	150	364

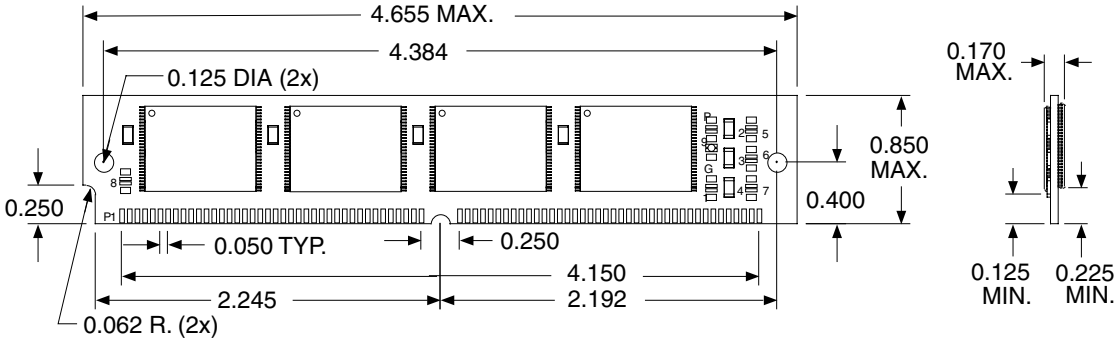
PACKAGE NO. 364: 80 PIN SIMM (JEDEC)



ORDERING INFORMATION

Part Number	Speed (ns)	Package
EDI7F2342MV120BNC	120	365
EDI7F2342MV150BNC	150	365

PACKAGE NO. 365: 80 PIN SIMM (JEDEC)



ALL DIMENSIONS ARE IN INCHES

DATASHEET APPROVALS

EDI PART NO. EDI7F342MV ECO# 15607 NEW REV 3A DATE 9/27/02

APPROVAL:	INITIAL	DATE	CORRECTION ON PAGES
~~JUAN GUZMAN~~ L.K.		9/27/02	
~~MUKESH TRIVEDI~~ M.A.	Mark E. Allen	10/2/02	
PAUL MARIEN			
LARRY WINROTH		10/2/02	
DAVE KELLY			
MARK DOWNEY			
DAVE HARRISON			
TONY LEE			
BOB KHEDERIAN			
LUIS ESTELLA			

	YES	NO
WILL THIS DATASHEET GO ON THE WEB?	☐	☐
IS THIS A NEW DATASHEET?	☐	☐
WILL THIS DATASHEET REPLACE AN EXISTING DATASHEET THAT'S ALREADY ON THE WEB?	☐	☐

LINE:_____
FAMILY:_____
PROD.TYPE:_____
ORG:_____
DENSITY:_____
SPEED:_____
PKG:_____
VOLTAGE:_____

IF YES, WHAT DATASHEET IS IT REPLACING? _____

WHAT SECTION SHOULD THIS DATASHEET BE PLACED IN ON THE WEB? _____

AFTER REVIEWING OR MAKING CORRECTIONS ON THE DATASHEET (S)
PLEASE SIGN-OFF ON THIS SHEET AND ,MAKE YOUR CORRECTIONS –ON **THE ORIGINAL COPY(S).**

AFTER REVIEWING THE DATA SHEET, TEST ENGINEERING WILL COMPLETE THE SECTION BELOW.

TEST PROGRAM CHANGE REQUIRED:
YES:_____☐_____NO_____☐_____DATE:_____

TEST ENGINEER SIGNATURE_____

IF YES, DO NOT RELEASE DATA SHEET UNTIL TEST PROGRAM CHANGE IS COMPLETED.
TEST PROGRAM CHANGE COMPLETION DATE:_____
TEST PROGRAM NAME AND REVISION _____
TEST ENGINEER SIGNATURE_____