

## 4MB SYNCHRONOUS CARD EDGE DIMM

### FEATURES

- 4x128Kx64 Synchronous
- Access Speed(s):  $T_{KHQV} = 9.5, 10, 11, 12, 15ns$
- Flow-Through Architecture
- Clock Controlled Registered Bank Enables (E1#, E2#, E3#, E4#)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW#)
- Asynchronous Output Enable (G#)
- Internally self-timed Write
- Gold Lead Finish
- 3.3V  $\pm 10\%$ , -5% Operation
- Access Speed(s):  $t_{KHQV} = 9.5, 10, 11, 12, 15ns$
- Common Data I/O
- High Capacitance (30pf) drive, at rated Access Speed
- Single total array Clock
- Multiple Vcc and GND

### DESCRIPTION

The EDI2KG64128VxxD is a Synchronous SRAM, 60 position Card Edge DIMM (120 contacts) Module, organized as 4x128Kx64. The Module contains eight (8) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Synchronous Only, Flow-Through, Early Write Device. This module provides High Performance, Ultra Fast access times at a cost per bit benefit over BiCMOS Asynchronous SRAM based devices. As well as improved cost per bit, the use of Synchronous or Synchronous Burst devices or modules can ease the memory subsystem design by reducing or easing the memory controller requirement.

Synchronous operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. All read and write operations to this module are performed on Quad Words (64 bit operations).

Write cycles are internally self timed and are initiated by a rising clock edge. This feature relieves the designer the task of developing external write pulse width circuitry.

### PIN NAMES

DQ0-DQ63	Input/Output Bus
A015	Address Bus
E1#, E2#, E3#, E4#	Synchronous Bank Enables
CK	Array Clock
GW#	Synchronous Global Write Enable
G#	Asynchronous Output Enable
Vcc	3.3V Power Supply
Vss	Ground
NC	No Connect

\*This product is subject to change without notice.

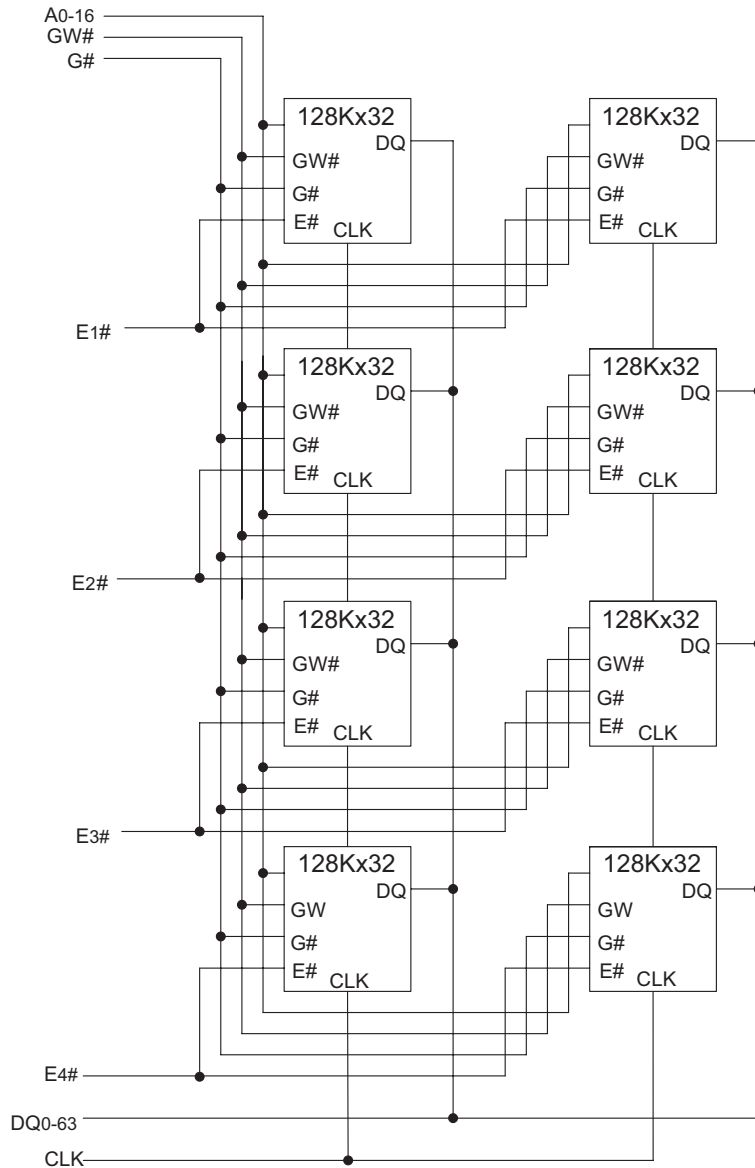


## PIN CONFIGURATION

VSS	1	2	VSS
A0	3	4	A16
A1	5	6	A15
A2	7	8	A14
A3	9	10	A13
VCC	11	12	VCC
A4	13	14	A12
A5	15	16	A11
A6	17	18	A10
A7	19	20	A9
VSS	21	22	VSS
A8	23	24	RFU
VSS	25	26	VSS
CK	27	28	NC
VSS	29	30	VSS
E4#	31	32	E2#
VCC	33	34	VCC
E3#	35	36	E1#
G#	37	38	GW#
VSS	39	40	VSS
DQ0	41	42	DQ7
DQ1	43	44	DQ6
DQ2	45	46	DQ5
DQ3	47	48	DQ4
VCC	49	50	VCC
DQ8	51	52	DQ15
DQ9	53	54	DQ14
DQ10	55	56	DQ13
DQ11	57	58	DQ12
VSS	59	60	VSS
DQ16	61	62	DQ23
DQ17	63	64	DQ22
DQ18	65	66	DQ21
DQ19	67	68	DQ20
VCC	69	70	VCC
DQ24	71	72	DQ31
DQ25	73	74	DQ30
DQ26	75	76	DQ29
DQ27	77	78	DQ28
VSS	79	80	VSS
DQ32	81	82	DQ39
DQ33	83	84	DQ38
DQ34	85	86	DQ34
DQ35	87	88	DQ37
VCC	89	90	VCC
DQ40	91	92	DQ47
DQ41	93	94	DQ46
DQ42	95	96	DQ45
DQ43	97	98	DQ44
VSS	99	100	VSS
DQ48	101	102	DQ55
DQ49	103	104	DQ54
DQ50	105	106	DQ53
DQ51	107	108	DQ52
VCC	109	110	VCC
DQ56	111	112	DQ63
DQ57	113	114	DQ62
DQ58	115	116	DQ61
DQ59	117	118	DQ60
VSS	119	120	VSS



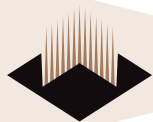
### FUNCTIONAL BLOCK DIAGRAM





## PIN DESCRIPTIONS

DIMM Pins	Symbol	Type	Description
3, 5, 7, 9, 13, 15, 17, 19, 20, 23, 18, 16, 14, 10, 8, 6	A0-A15	Input Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CK. The burst counter generates internal addresses associated with A <sub>0</sub> and A <sub>1</sub> , during burst and wait cycle.
38	GW#	Input Synchronous	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CK.
27	CK	Input Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
36, 32, 35, 31	E1#, E2# E3#, E4#	Input Synchronous	Bank Enables: These active LOW inputs are used to enable each individual Synchronous bank and to gate ADSP#.
37	G#	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
Various	DQ0-63	Input/Output	Data Inputs/Outputs: First byte is DQ <sub>0-7</sub> , second byte is DQ <sub>8-15</sub> , third byte is DQ <sub>16-23</sub> , fourth byte is DQ <sub>24-31</sub> , fifth byte is DQ <sub>32-39</sub> , sixth byte is DQ <sub>40-47</sub> , seventh byte is DQ <sub>48-55</sub> and the eight byte is DQ <sub>56-64</sub> .
Various	Vcc	Supply	Core power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground



## SYNCHRONOUS ONLY – TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	GW#	G#	CK	DQ
Synchronous Write-Bank 1	L	H	H	H	L	H	↑	High-Z
Synchronous Read-Bank 1	L	H	H	H	H	L	↑	
Synchronous Write-Bank 2	H	L	H	H	L	H	↑	High-Z
Synchronous Read-Bank 2	H	L	H	H	H	L	↑	
Synchronous Write-Bank 3	H	H	L	H	L	H	↑	High-Z
Synchronous Read-Bank 3	H	H	L	H	H	L	↑	
Synchronous Write-Bank 4	H	H	H	L	L	H	↑	High-Z
Synchronous Read-Bank 4	H	H	H	L	H	L	↑	
Snooze Mode	X	X	X	X	X	X	X	High-Z

## ABSOLUTE MAXIMUM RATINGS\*

Voltage on Vcc Relative to Vss	-0.5V to +4.6V
V <sub>IN</sub>	-0.5V to Vcc +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	20 mA

\* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

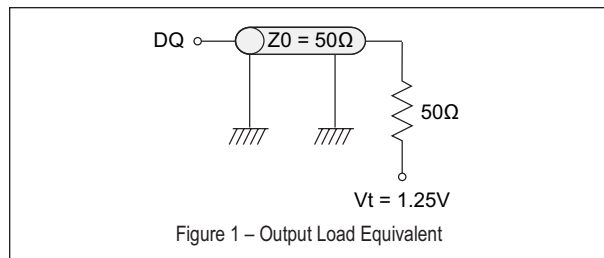
Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V <sub>CC</sub>	3.14	3.3	3.6	V
Supply Voltage	V <sub>SS</sub>	0.0	0.0	0.0	V
Input High	V <sub>IH</sub>	2.2	3.0	V <sub>CC</sub> + 0.3	V
Input Low	V <sub>IL</sub>	-0.3	0.0	0.8	V
Input Leakage	I <sub>LI</sub>	-2	1	2	μA
Output Leakage	I <sub>LO</sub>	-2	1	2	μA
Output High I <sub>OH</sub> = -4ma	V <sub>OH</sub>	2.4	-	-	V
Output Low I <sub>OL</sub> = 8ma	V <sub>OL</sub>	-	-	0.4	V

## DC ELECTRICAL CHARACTERISTICS – READ CYCLE

Description	Symbol	Typ	Max					Units
			9.5	10	11	12	15	
Power Supply Current	I <sub>CC1</sub>	1.55	2.8	2.2	2.2	2.7	2.0	A
Power Supply Current Device Selected, No Operation	I <sub>CC</sub>	.75	1.8	1.5	1.3	1.3	1.0	A
Snooze Mode	I <sub>CCZZ</sub>	200	300	300	300	300	300	mA
CMOS Standby	I <sub>CC3</sub>	400	500	500	500	500	500	mA
Clock Running-Deselect	I <sub>CCK</sub>	600	900	900	900	900	900	mA

\*TBD

## AC TEST LOAD



## AC TEST CONDITIONS

Parameter	I/O	Unit
Input Pulse Levels	V <sub>SS</sub> to 3.0V	V
Input and Output Timing Ref.	1.25	V
Output Test Equivalencies	See figure at left	V



## READ CYCLE TIMING PARAMETERS

Description	Sym	9.5ns		10ns		11ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t <sub>KHKH</sub>	*	*	12		12		15		20		ns
Clock High Time	t <sub>KHKL</sub>	*	*	5		5		5		6		ns
Clock Low Time	t <sub>KLKH</sub>	*	*	5		5		5		6		ns
Clock to Output Valid	t <sub>KHQV</sub>	*	*		10		11		12		15	ns
Clock to Output Invalid	t <sub>KHGX1</sub>	*	*	3		3		3		3		ns
Clock to Output Low-Z	t <sub>KHGX</sub>	*	*	2		2		2		2		ns
Output Enable to Output Valid	t <sub>GLQV</sub>	*	*		4		5		5		6	ns
Output Enable to Output Low-Z	t <sub>GLGX</sub>	*	*	0		0		0		0		ns
Output Enable to Output High-Z	t <sub>GHQZ</sub>	*	*		4		5		5		5	ns
Address Setup	t <sub>AVKH</sub>	*	*	2.5		2.5		2.5		2.5		ns
Bank Enable Setup	t <sub>EVKH</sub>	*	*	2.5		2.5		2.5		2.5		ns
Address Hold	t <sub>KHAX</sub>	*	*	1.0		1.0		1.0		1.0		ns
Bank Enable Hold	t <sub>KHEX</sub>	*	*	1.0		1.0		1.0		1.0		ns

\*TBD

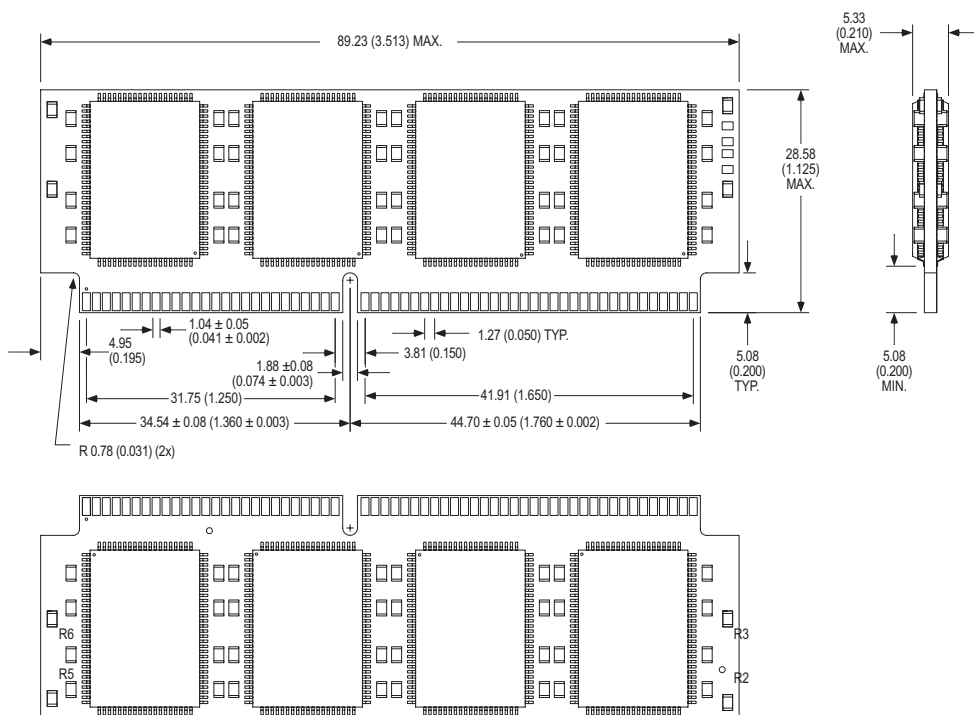
## WRITE CYCLE TIMING PARAMETERS

Description	Sym	9.5ns		10ns		11ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t <sub>KHKH</sub>	*	*	12		12		15		20		ns
Clock High Time	t <sub>KHKL</sub>	*	*	5		5		5		6		ns
Clock Low Time	t <sub>KLKH</sub>	*	*	5		5		5		6		ns
Address Setup	t <sub>AVKH</sub>	*	*	2.5		2.5		2.5		2.5		ns
Address Hold	t <sub>KHAX</sub>	*	*	1.0		1.0		1.0		1.0		ns
Bank Enable Setup	t <sub>EVKH</sub>	*	*	2.5		2.5		2.5		2.5		ns
Bank Enable Hold	t <sub>KHEX</sub>	*	*	1.0		1.0		1.0		1.0		ns
Global Write Enable Setup	t <sub>WVKH</sub>	*	*	2.5		2.5		2.5		2.5		ns
Global Write Enable Hold	t <sub>KHWX</sub>	*	*	1.0		1.0		1.0		1.0		ns
Data Setup	t <sub>DVKH</sub>	*	*	2.5		2.5		2.5		2.5		ns
Data Hold	t <sub>KHDX</sub>	*	*	1.0		1.0		1.0		1.0		ns

\*TBD



Part Number	Organization	Voltage	Speed (ns)	Package	Height*
EDI2GG464128V95D*	4x128Kx64	3.3	9.5	120 Card Edge DIMM	28.58 (1.125")
EDI2GG464128V10D*	4x128Kx64	3.3	10	120 Card Edge DIMM	28.58 (1.125")
EDI2GG464128V11D	4x128Kx64	3.3	11	120 Card Edge DIMM	28.58 (1.125")
EDI2GG464128V12D	4x128Kx64	3.3	12	120 Card Edge DIMM	28.58 (1.125")
EDI2GG464128V15D*	4x128Kx64	3.3	15	120 Card Edge DIMM	28.58 (1.125")

**PACKAGE DESCRIPTION: 120 LEAD CARD EDGE DIMM**

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### Document Title

4MB SYNCHRONOUS CARD EDGE DIMM

### Revision History

Rev #	History	Release Date	Status
Rev 0	Created	July 1999	
Rev 1	Corrected block diagram specs	10-25-04	