Overview

The VG4632321A SGRAM is a high-speed CMOS synchronous graphic RAM containing 32M bits. It is internally configured as a dual 512K x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 32 bit bank is organized as 2048 rows by 256 columns by 32 bits. Read and write accesses to the SGRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command.

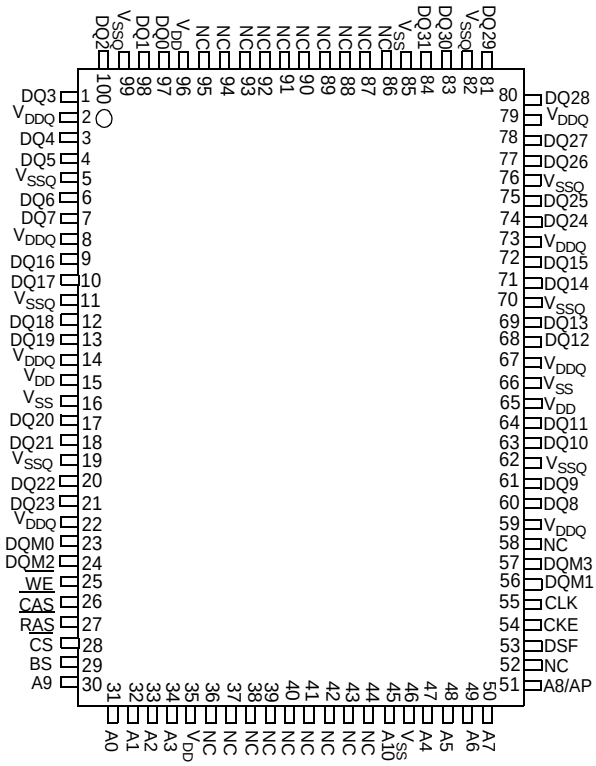
The VG4632321A provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with burst termination option. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. In addition, it features the write per bit and the masked block write functions.

By having a programmable Mode register and special mode register, the system can choose the best suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth, and when combined with special graphics functions result in a device particularly well suited to high performance graphics applications.

Features

- Fast access time from clock: 4.5/5/5.5/6/7ns
- Fast clock rate: 222/200/183/166/143MHz
- Fully synchronous operation
- Internal pipelined architecture
- Dual internal banks(512K x 32-bit x 2-bank)
- Programmable Mode and Special Mode registers
  - CAS Latency: 1, 2, or 3
  - Burst Length: 1, 2, 4, 8, or full page
  - Burst Type: interleaved or linear burst
  - Burst Read Single Write
  - Load Color or Mask register
- Burst stop function
- Individual byte controlled by DQM0-3
- Block write and write-per-bit capability
- Auto Refresh and Self Refresh
- 2048 refresh cycles/32ms
- Single + 3.3V ±0.3V power supply
- Interface: LVTTL
- JEDEC 100-pin Plastic QFP package

Pin Assignment (Top View)



Key Specifications

VG4632321A		-4.5/-5/-5.5/-6/-7
t_{CK}	Clock Cycle time(min.)	4.5/5/5.5/6/7 ns
t_{RAS}	Row Active time(min.)	40/40/40/42/42 ns
t_{AC}	Access time from CLK(max.)	4/4.5/5/5.5/6 ns
t_{RC}	Row Cycle time(min.)	55/55/56.5/60/62 ns

Block Diagram

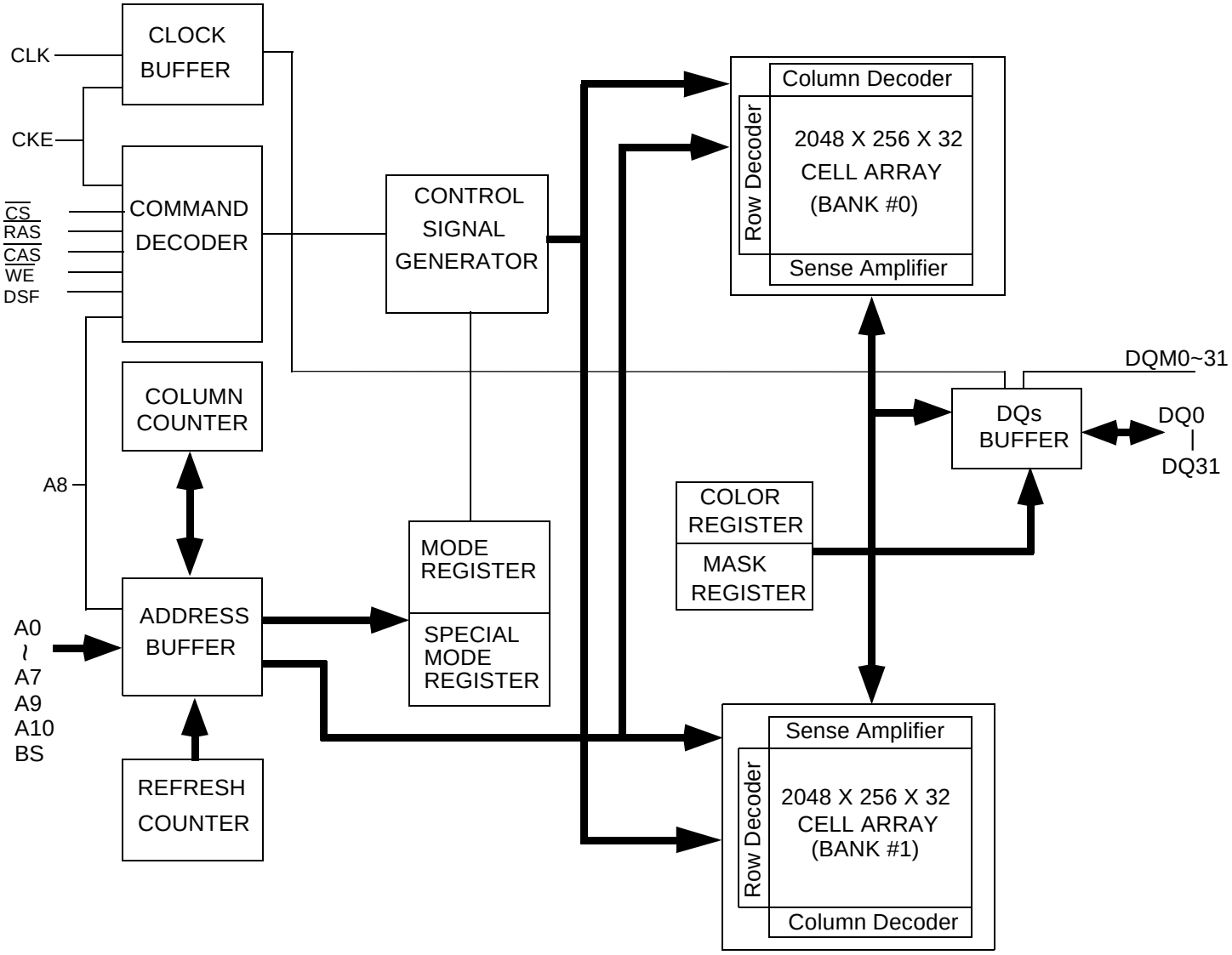


Table 1 shows the details for pin number, symbol, type, and description.

Table 1. Pin Description of VG4632321A

Pin Number	Symbol	Type	Description
55	CLK	Input	**Clock:** CLK is driven by the system clock. All SGRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and control the output registers.
54	CKE	Input	**Clock Enable:** CKE activates(HIGH) and deactivates(LOW) the CLK signal. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When both banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes providing low standby power.
29	BS	Input	**Bank Select:** BS defines to which bank the BankActivate, Read, Write, or Bank-Precharge command is being applied. BS is also used to program the 10th bit of the Mode and Special Mode registers.
30-34, 45,47-51	A0-A10	Input	**Address Inputs:** A0-A10 are sampled during the BankActivate command (row address A0-A10) and Read/Write command (column address A0-A7 with A8 defining Auto Precharge) to select one location out of the 512K available in the respective bank. During a Precharge command, A8 is sampled to determine if both banks are to be precharged (A8 = HIGH). The address inputs also provide the op-code during a Mode Register Set or Special Mode Register Set command.
28	$\overline{CS}$	Input	**Chip Select:** $\overline{CS}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when $\overline{CS}$ is sampled HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
27	$\overline{RAS}$	Input	**Row Address Strobe:** The $\overline{RAS}$ signal defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ signals, and is latched at the positive edges of CLK. When $\overline{RAS}$ and $\overline{CS}$ are asserted “LOW” and $\overline{CAS}$ is asserted “HIGH”, either the BankActivate command or the Precharge command is selected by the $\overline{WE}$ signal. When the $\overline{WE}$ is asserted “HIGH” the BankActivate command is selected and the bank designated by BS is turned on to the active state. When the $\overline{WE}$ is asserted "LOW", the Precharge command is selected and the bank designated by BS is switched to the idle state after precharge operation.
26	$\overline{CAS}$	Input	**Column Address Strobe:** The $\overline{CAS}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ signals, and it is latched at the positive edges of CLK. When $\overline{RAS}$ is held “HIGH” and $\overline{CS}$ is asserted “LOW”, the column access is started by asserting $\overline{CAS}$ “LOW”. Then, the Read or Write command is selected by asserting $\overline{WE}$ “LOW” or “HIGH”.
25	$\overline{WE}$	Input	**Write Enable:** The $\overline{WE}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ signals, and it is latched at the positive edges of CLK. The $\overline{WE}$ input is used to select the BankActivate or Precharge command and Read or Write command.
53	DSF	Input	**Define Special Function:** The DSF signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ and $\overline{WE}$ signals, and it is latched at the positive edges of CLK. The DSF input is used to select the masked write disable/enable command and block write command, and the Special Mode Register Set cycle.

23,56,24, 57	DQM0-DQM3	Input	**Data Input/Output Mask:** DQM0-DQM3 are byte specific, nonpersistent I/O buffer controls. The I/O buffers are placed in a high-z state when DQM is sampled HIGH. Input data is masked when DQM is sampled HIGH during a write cycle. Output data is masked (two-clock latency) when DQM is sampled HIGH during a read cycle. DQM3 masks DQ31-DQ24, DQM2 masks DQ23-DQ16, DQM1 masks DQ15-DQ8, and DQM0 masks DQ7-DQ0.
97,98,100, 1,3,4,6,7, 60,61,63, 64,68,69, 71,72,9, 10,12,13, 17,18,20, 21,74,75, 77, 78,80, 81, 83, 84	DQ0-DQ31	Input/ Output	**Data I/O:** The DQ0-31 input and output data are synchronized with the positive edges of CLK. The I/Os are byte-maskable during Reads and Writes. The DQs also serve as column/byte mask inputs during Block Writes.
30,36-45, 52,58, 86-95	NC	-	**No Connect:** These pins should be left unconnected.
2,8,14,22, 59,67,73, 79	V_{DDQ}	Supply	**DQ Power:** Provide isolated power to DQs for improved noise immunity.
5,11,19, 62,70,76, 82,99	V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
15,35,65, 96	V_{DD}	Supply	**Power Supply:** +3.3V $\pm$0.3V
16,46,66, 85	V_{SS}	Supply	**Ground**

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 2 shows the truth table for the operation commands.

Table 2. Truth Table (Note(1), (2))

Command	State	CKEn-1	CKEn	DQM(7)	BS	A8	A0-7 A9, A10	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF
BankActivate & Masked Write Disable	Idle(3)	H	X	X	V	V	V	L	L	H	H	L
BankActivate & Masked Write Enable	Idle(3)	H	X	X	V	V	V	L	L	H	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L	L
Write	Active(3)	H	X	X	V	L	V	L	H	L	L	L
Block Write Command	Active(3)	H	X	X	V	L	V	L	H	L	L	H
Write and AutoPrecharge	Active(3)	H	X	X	V	H	V	L	H	L	L	L
Block Write and AutoPrecharge	Active(3)	H	X	X	V	H	V	L	H	L	L	H
Read	Active(3)	H	X	X	V	L	V	L	H	L	H	L
Read and AutoPrecharge	Active(3)	H	X	X	V	H	V	L	H	L	H	L
Mode Register Set	Idle	H	X	X	V	L	V	L	L	L	L	L
Special Mode Register Set	Idle(5)	H	X	X	X	X	V	L	L	L	L	H
No-Operation	Any	H	X	X	X	X	X	L	H	H	H	X
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H	L
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H	L
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X	X
								L	H	H	H	X
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(6)	H	L	X	X	X	X	H	X	X	X	X
								L	H	H	H	L
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (Power-Down)	L	H	X	X	X	X	H	X	X	X	X
								L	H	H	H	L
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X	X

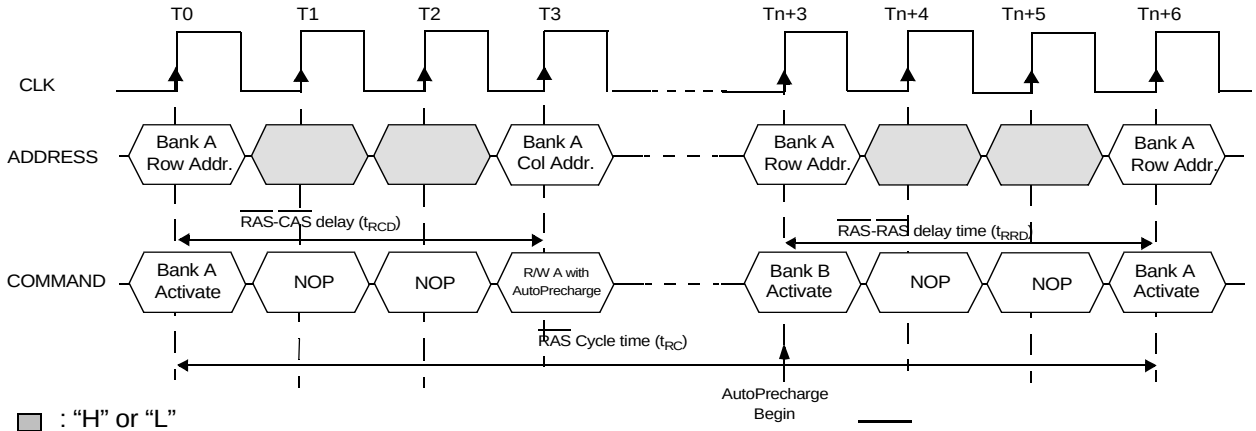
Note: 1. V = Valid X = Don't Care L = Low level H = High level

2. CKEn signal is input level when commands are provided.
   CKEn-1 signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BS signal.
4. Device state is 1, 2, 4, 8, and full page burst operation.
5. The Special Mode Register Set is also available in Row Active State.
6. Power Down Mode can not entry in the burst operation.
   When this command assert in the burst cycle, device state is clock suspend mode.
7. DQM0-3

Commands

1 BankActivate & Masked Write Disable command
(RAS = "L", CAS = "H", WE = "H", DSF = "L", BS = Bank, A0-A10 = Row Address)

The BankActivate command activates the idle bank designated by the BS (Bank Select) signal. By latching the row address on A0 to A10 at the time of this command, the selected row access is initiated. The read or write operation in the same bank can occur after a time delay of t_{RCD}(min.) from the time of bank activation. A subsequent BankActivate command to a different row in the same bank can only be issued after the previous active row has been precharged (refer to the following figure). The minimum time interval between successive BankActivate commands to the same bank is defined by t_{RC}(min.). The SGRAM has two internal banks on the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the back-to-back activation of both banks. t_{RRD}(min.) specifies the minimum time required between activating different banks. After this command is used, the Write command and the Block Write command perform the no mask write operation.



BankActivate Command Cycle (Burst Length = n, CAS Latency = 3)

2 BankActivate & Masked Write Enable command (refer to the above figure)
(RAS = "L", CAS = "H", WE = "H", DSF = "H", BS = Bank, A0-A10 = Row Address)

The BankActivate command activates the idle bank designated by BS signal. After this command is performed, the Write command and the Block Write command perform the masked write operation. In the masked write and the masked block write functions, the I/O mask data that was stored in the write mask register is used.

3 BankPrecharge command
(RAS = "L", CAS = "H", WE = "L", DSF = "L", BS = Bank, A8 = "L", A0-A7,A9,A10 = Don't care)

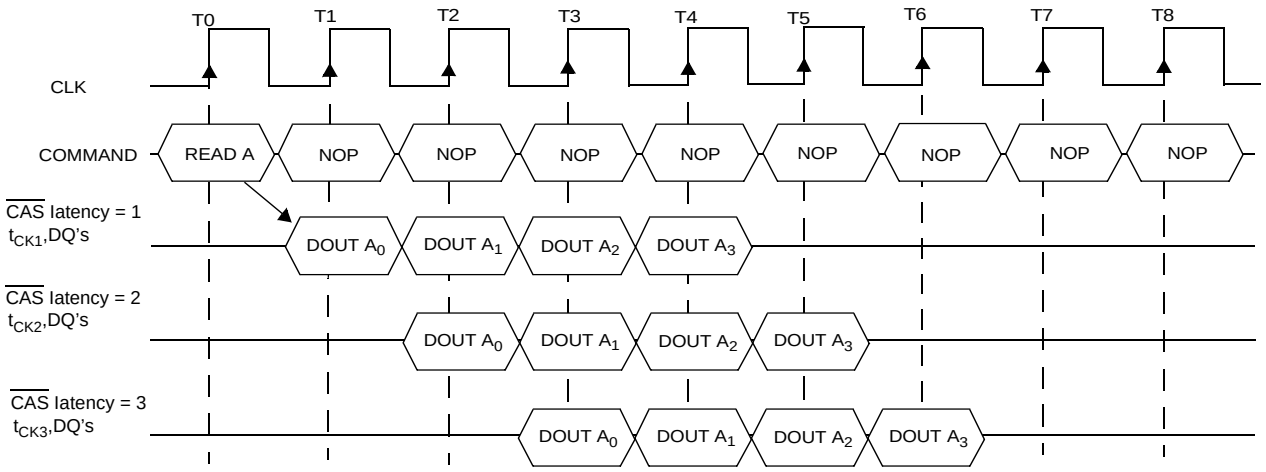
The BankPrecharge command precharges the bank designated by BS signal. The precharged bank is switched from the active state to the idle state. This command can be asserted anytime after t_{RAS}(min.) is satisfied from the BankActivate command in the desired bank. The maximum time any bank can be active is specified by t_{RAS}(max.). Therefore, the precharge function must be performed in any active bank within t_{RAS}(max.). At the end of precharge, the precharged bank is still the idle state and ready to be activated again.

4 PrechargeAll command
(RAS = "L", CAS = "H", WE = "L", DSF = "L", BS = Don't care, A8 = "H", A0-A7,A9,A10 = Don't care)

The PrechargeAll command precharges both banks simultaneously. Even if both banks are not in the active state, the PrechargeAll command can be issued. Both banks are then switched to the idle state.

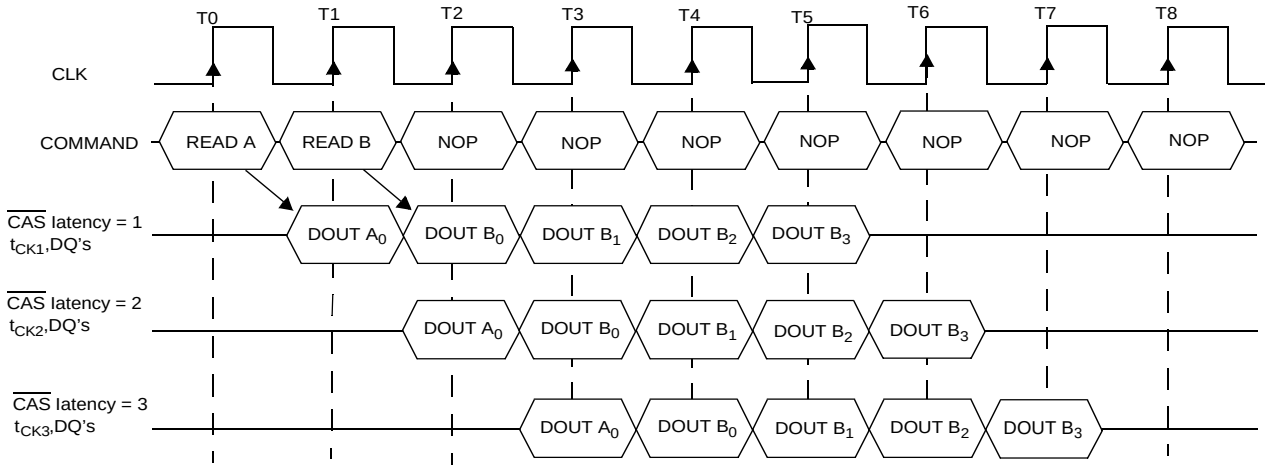
5 Read command
(RAS = "H", CAS = "L", WE = "H", DSF = "L", BS = Bank, A8 = "L", A0-A7 = Column Address, A9,A10 = Don't care)

The Read command is used to read burst of data on consecutive clock cycles from an active row in an active bank. The bank must be active for at least t_{RCD}(min.) before Read command is issued. During read bursts, the valid data-out element from the starting column address will be available following the CAS latency after the issue of Read command. Each subsequent data-out element will be valid by the next positive clock edge (refer to the following figure). The DQs goes into high-impedance at the end of the burst, unless other command was initiated. The burst length, burst sequence, and CAS latency are determined by the mode register which is already prgrammed.A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).



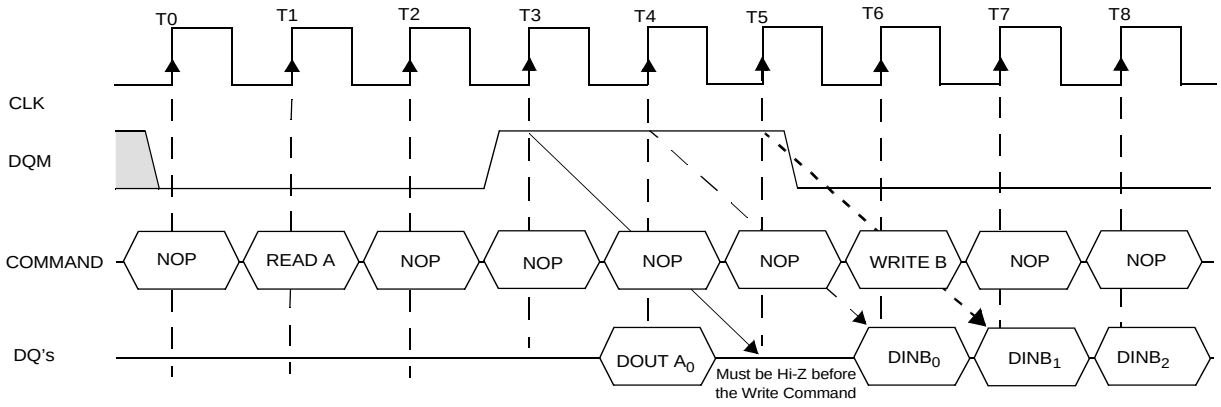
Burst Read Operation (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 1, 2, 3)

The read data appears on the DQs subjects to the values on the DQM inputs two clocks early (i.e. DQM latency is two clocks for output buffers). A read burst without auto precharge function may be interrupted by a subsequent Read or Write/Block Write command to the same bank or the other active bank before the end of burst length. It may be interrupted by a BankPrecharge/PrechargeAll command to the same bank too. The interrupt comes from Read command can occur on any clock cycle following a previous Read command (refer to the following figure).

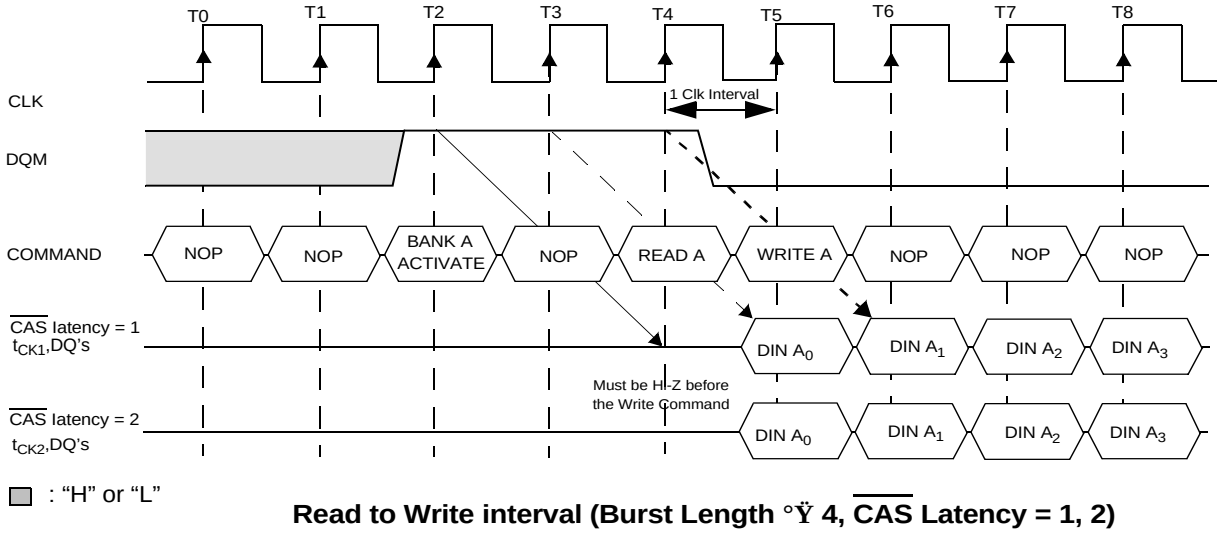


Read Interrupted by a Read (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 1, 2, 3)

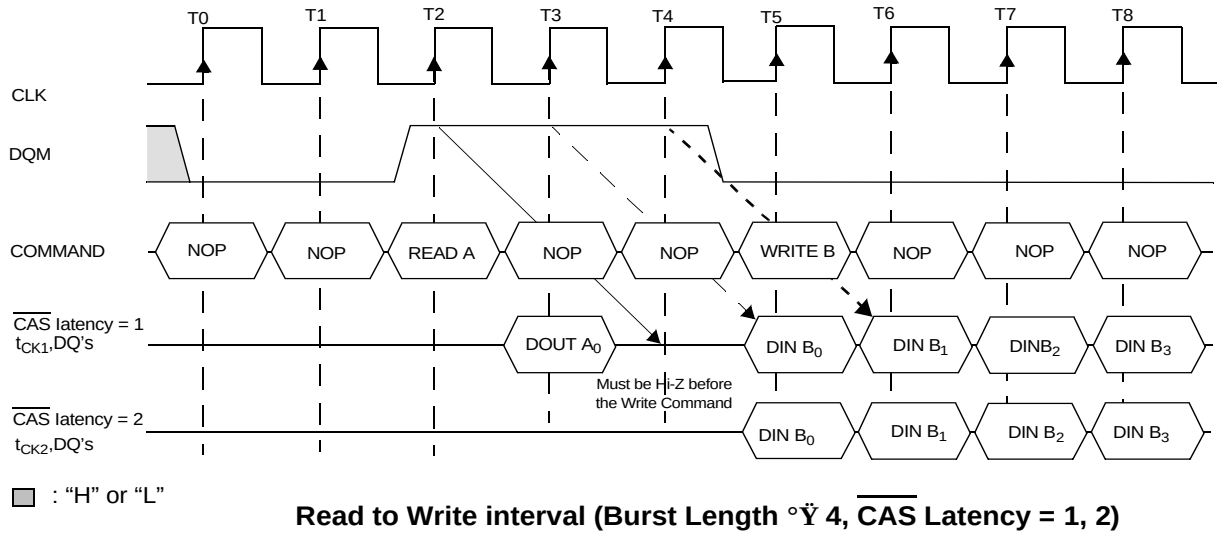
The DQM inputs are used to avoid I/O contention on DQ pins when the interrupt comes from Write/Block Write command. The DQMs must be asserted (High) at least two clocks prior to the Write/Block Write command to suppress data-out on DQ pins. To guarantee DQ pins against the I/O contention, a single cycle with high-impedance on DQ pins must occur between the last read data and the Write/Block Write command (refer to the following three figures). If the data output of burst read occurs at the second clock of burst write, the DQMs must be asserted (High) at least one clock prior to the Write/Block Write command to avoid internal bus contention.



Read to Write interval (Burst Length °Ÿ 4, $\overline{\text{CAS}}$ Latency = 3)

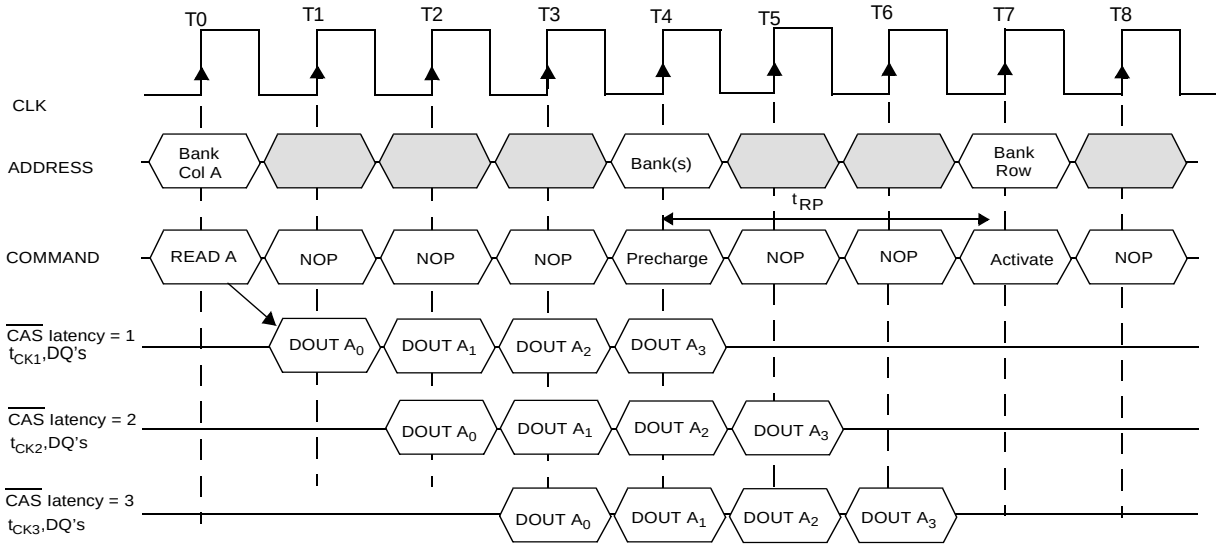


Read to Write interval (Burst Length °Ÿ 4, $\overline{\text{CAS}}$ Latency = 1, 2)



Read to Write interval (Burst Length °Ÿ 4, $\overline{\text{CAS}}$ Latency = 1, 2)

A read burst without auto precharge function may be interrupted by a BankPrecharge/ PrechargeAll command to the same bank. The following figure shows the optimum time that BankPrecharge/PrechargeAll command is issued in different $\overline{\text{CAS}}$ latency.



Read to Precharge ($\overline{CAS}$ Latency = 1, 2, 3)

6 Read and AutoPrecharge command

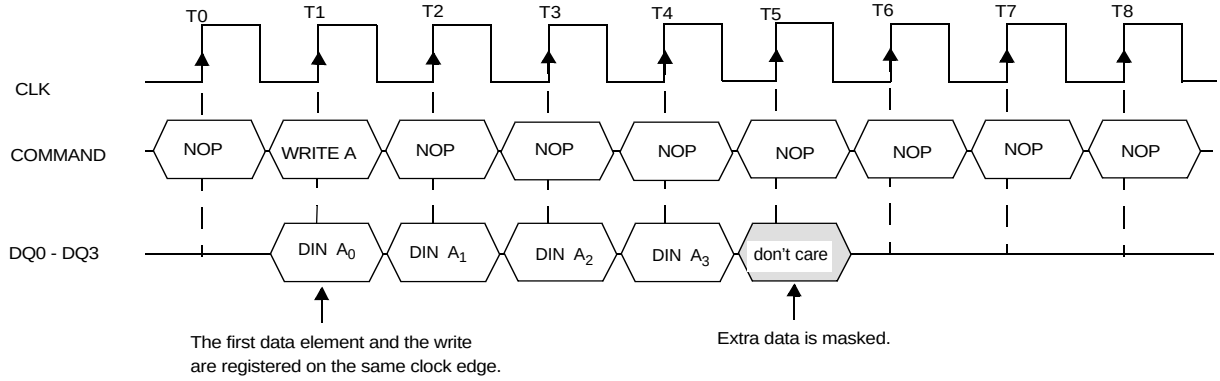
($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", DSF = "L", BS = Bank, A8 = "H", A0-A7 = Column Address, A9,A10 = Don't care)

The Read and AutoPrecharge command automatically performs the precharge operation after the read operation. Once this command is given, any subsequent command can not occur within a time delay of {t_{RP}(min.) + burst length}. At full-page burst, only read operation is performed in this command and the auto precharge function is ignored.

7 Write command

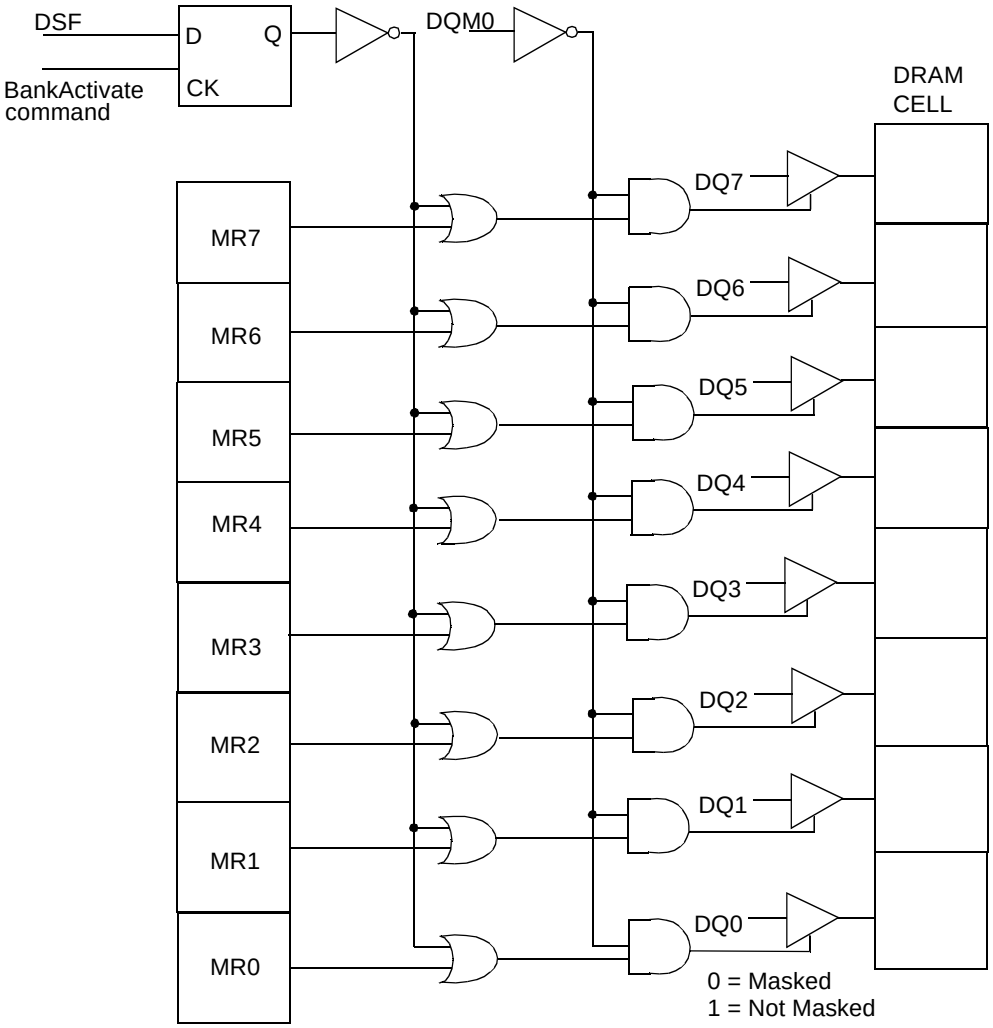
($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", DSF = "L", BS = Bank, A8 = "L", A0-A7 = Column Address, A9,A10 = Don't care)

The Write command is used to write burst of data on consecutive clock cycles from an active row in an active bank. The bank must be active for at least t_{RCD}(min.) before Write command is issued. During write bursts, the first valid data-in element will be registered coincident with the Write command. Subsequent data elements will be registered on each successive positive clock edge (refer to the following figure). The DQs remains high-impedance at the end of the burst, unless other command was initiated. The burst length and burst sequence are determined by the mode register which is already programmed. A full-page burst will continue until terminated (at the end of the page it will wrap to column 0 and continue).



Burst Write Operation (Burst Length = 4, $\overline{CAS}$ Latency = 1, 2, 3)

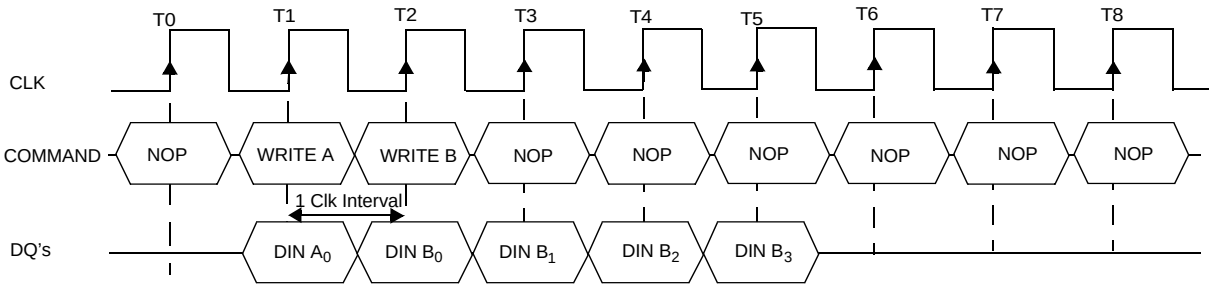
Any Write performed to a row that was opened via an BankAcitvate & Masked Write Enable command is a masked write (Write-Per-Bit). Data is written to the 32 cells (bits) at the selected column location subject to the data stored in the Mask register. The overall mask consists of the DQM inputs, which mask on a per-byte basis, and the Mask register, which masks on a per-bit basis. This is shown in the following block diagram.



Note: Only lower byte is shown. The operation is identical for other bytes.

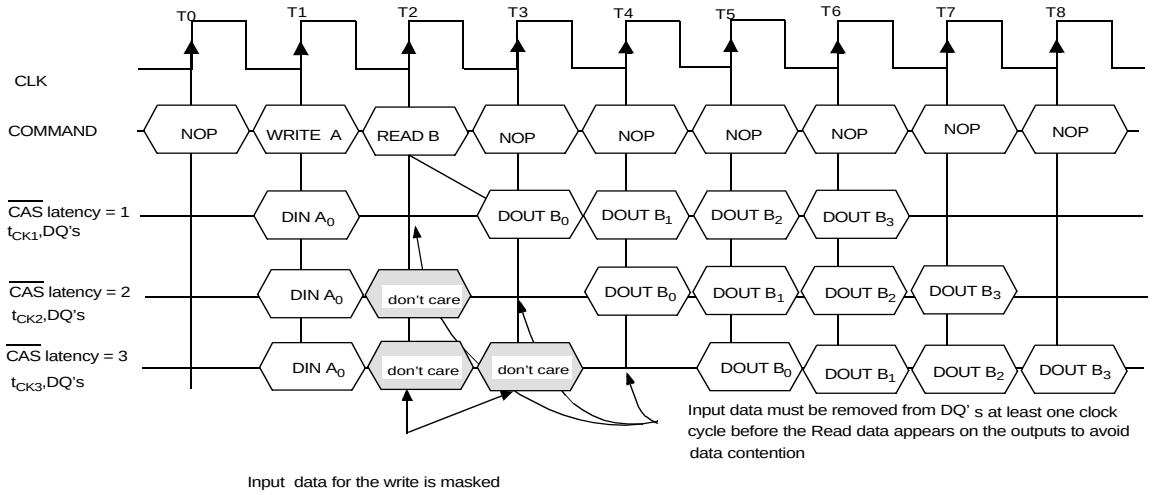
Write Per Bit (I/O Mask) Block Diagram

A write burst without auto precharge function may be interrupted by a subsequent Write/Block Write, BankPrecharge/PrechargeAll, or Read command before the end of burst length. The interrupt comes from Write/Block Write command can occur on any clock cycle following the previous Write command (refer to the following figure).



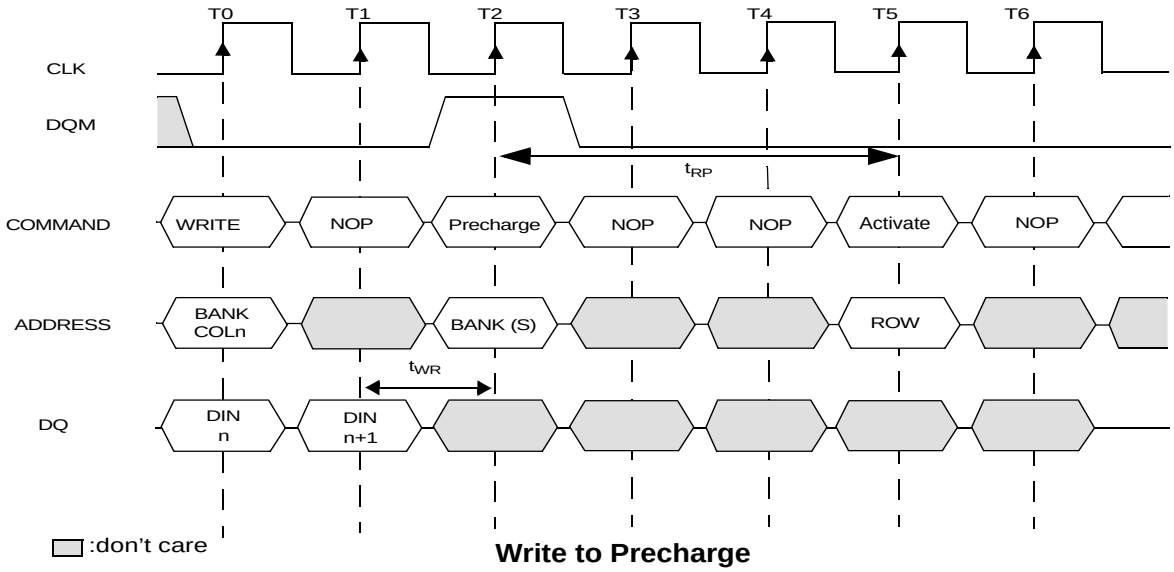
Write Interrupted by a Write (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 1, 2, 3)

The Read command that interrupts a write burst without auto precharge function should be issued one cycle after the clock edge at which the last data-in element is registered. In order to avoid data contention, input data must be removed from the DQs at least one clock cycle before the first read data appears on the outputs (refer to the following figure). Once the Read command is registered, the data inputs will be ignored, and writes will not be executed.



Write Interrupted by a Read (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 1, 2, 3)

The BankPrecharge/PrechargeAll command that interrupts a write burst without auto precharge function should be issued m cycles after the clock edge at which the last data-in element is registered, where m equals t_{WR}/t_{CK} rounded up to the next whole number. In addition, the DQM signals must be used to mask input data, starting with the clock edge following the last data-in element and ending with the clock edge on which the BankPrecharge/PrechargeAll command is entered (refer to the following figure).



Write to Precharge

When Burst-Read and Single-Write mode is selected , the write burst length is 1 regardless of the read burst length (refer to Figures 21 and 22 in Timing Waveforms).

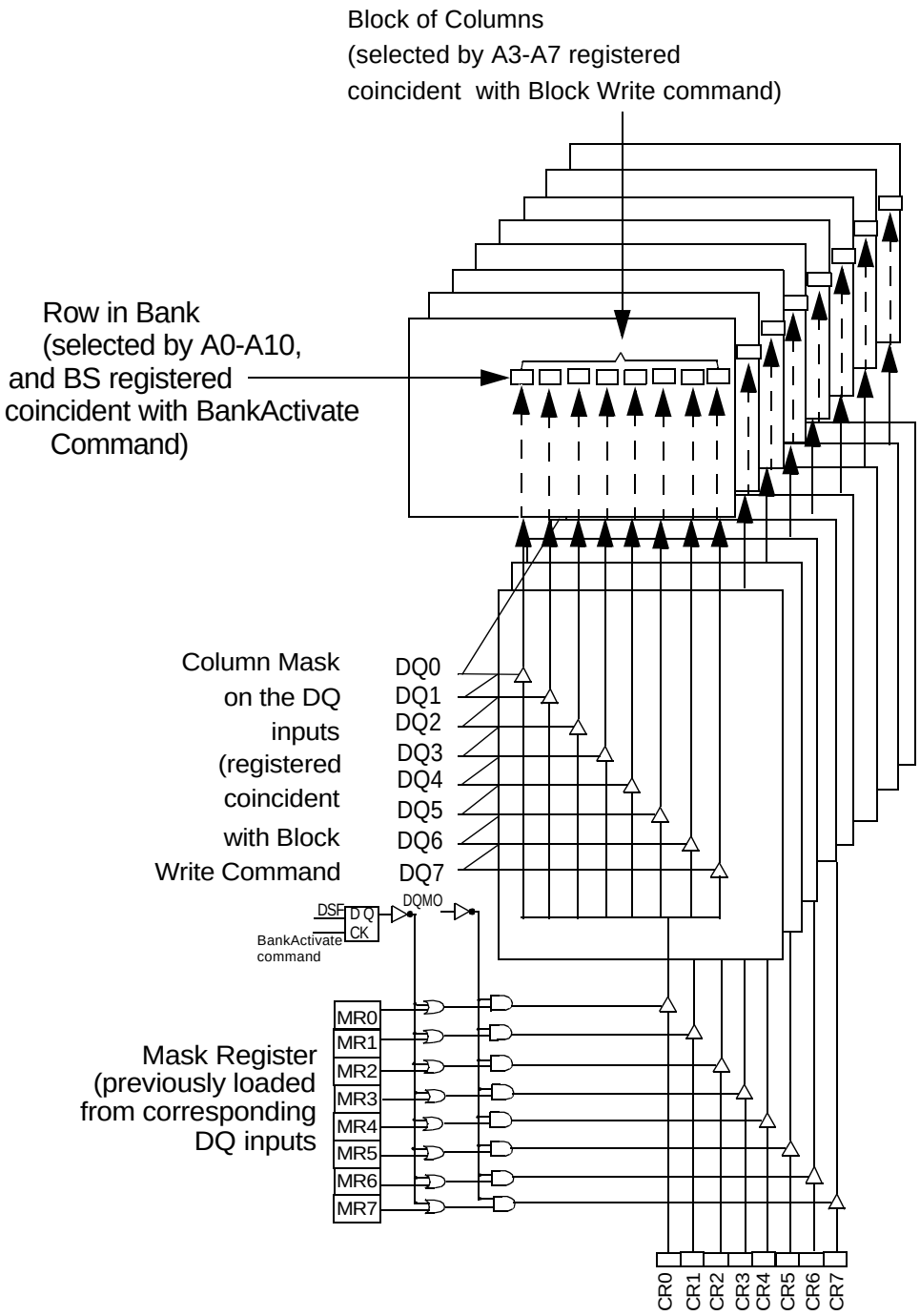
8 Block Write command
($\overline{\text{RAS}}$ = "H" , $\overline{\text{CAS}}$ = "L" , $\overline{\text{WE}}$ = "L", DSF = "H" , BS =Bank , A8 = "L" , A3-A7 = Column Address, DQ0-DQ31 = Column Mask)

The block writes are non-burst accesses that write to eight column locations simultaneously. A single data value, which was previously loaded in the Color register, is written to the block of eight consecutive column locations addressed by inputs A3-A7. The information on the DQs which is registered coincident with the Block Write command is used to mask specific column/byte combinations within the block . The mapping of the DQ inputs to the column/byte combinations is shown in following table.

DQ inputs	Column Address			DQ Planes Controlled		DQ Inputs	Column Address			DQ Planes Controlled
	A2	A1	A0				A2	A1	A0	
DQ0	0	0	0	0~7		DQ16	0	0	0	16~23
DQ1	0	0	1	0~7		DQ17	0	0	1	16~23
DQ2	0	1	0	0~7		DQ18	0	1	0	16~23
DQ3	0	1	1	0~7		DQ19	0	1	1	16~23
DQ4	1	0	0	0~7		DQ20	1	0	0	16~23
DQ5	1	0	1	0~7		DQ21	1	0	1	16~23
DQ6	1	1	0	0~7		DQ22	1	1	0	16~23
DQ7	1	1	1	0~7		DQ23	1	1	1	16~23
DQ8	0	0	0	8~15		DQ24	0	0	0	24~31
DQ9	0	0	1	8~15		DQ25	0	0	1	24~31
DQ10	0	1	0	8~15		DQ26	0	1	0	24~31
DQ11	0	1	1	8~15		DQ27	0	1	1	24~31
DQ12	1	0	0	8~15		DQ28	1	0	0	24~31
DQ13	1	0	1	8~15		DQ29	1	0	1	24~31
DQ14	1	1	0	8~15		DQ30	1	1	0	24~31
DQ15	1	1	1	8~15		DQ31	1	1	1	24~31

The overall Block Write mask consists of a combination of the DQM inputs, the Mask register, and the column/byte mask information, as shown in the following diagram. The DQM and Mask register masking operates as for normal Write command, with the exception that the mask information is applied simultaneously to all eight columns. Therefore, in a Block Write, a given bit is written only if a ”0” was registered for the corresponding DQM input, a ”1” was registered for the corresponding DQ signal, and the corresponding bit in the Mask register is ”1”.

A block write access requires a time period of t_{BWC} to execute, so in general, there should be m NOP cycles, m equals (t_{BWC}-t_{CK}) /t_{CK} rounded up to the next whole number, after the Block Write command. However, BankActivate or BankPrecharge commands to the other bank are allowed. When following a Block Write with a BankPrecharge or PrechargeAll command to the same bank, t_{BPL} must be met.

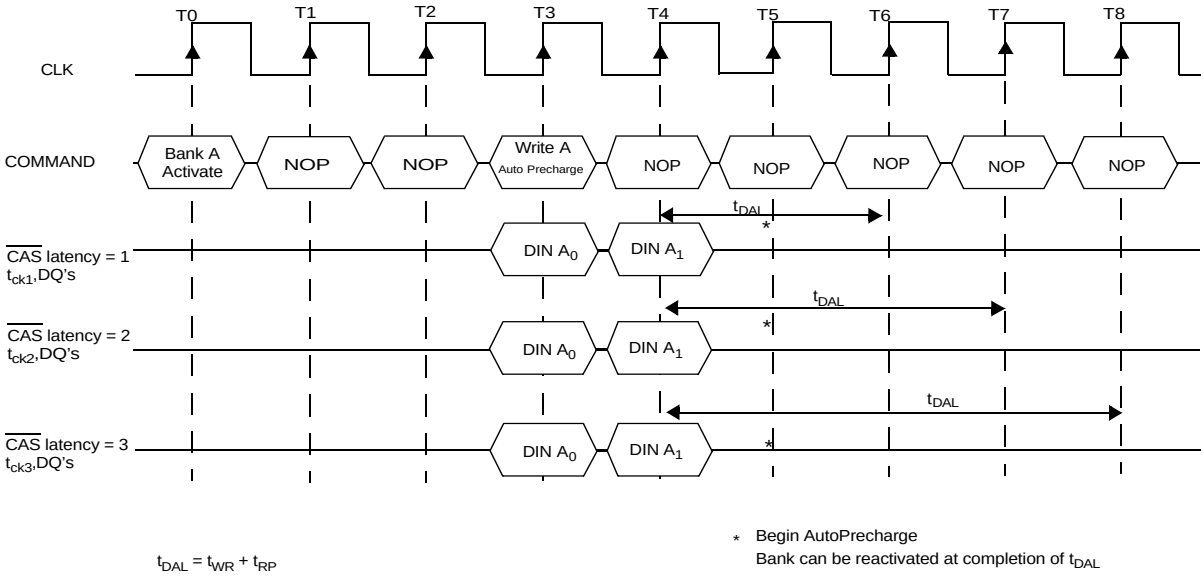


Note: Only lower byte is shown. The operation is identical for other bytes.

Block-Write Masking Block Diagram

9 Write and AutoPrecharge command (refer to the following figure)
(RAS = "H" , CAS = "L" , WE = "L" , DSF="L" , BS = Bank, A8 = "H", A0-A7 = Column Address, A9,A10 = Don't care)

The Write and AutoPrecharge command performs the precharge operation automatically after the write operation. Once this command is given, any subsequent command can not occur within a time delay of {burst length + t_{WR} + t_{RP}(min.)}. At full-page burst, only write operation is performed in this command and the auto precharge function is ignored.



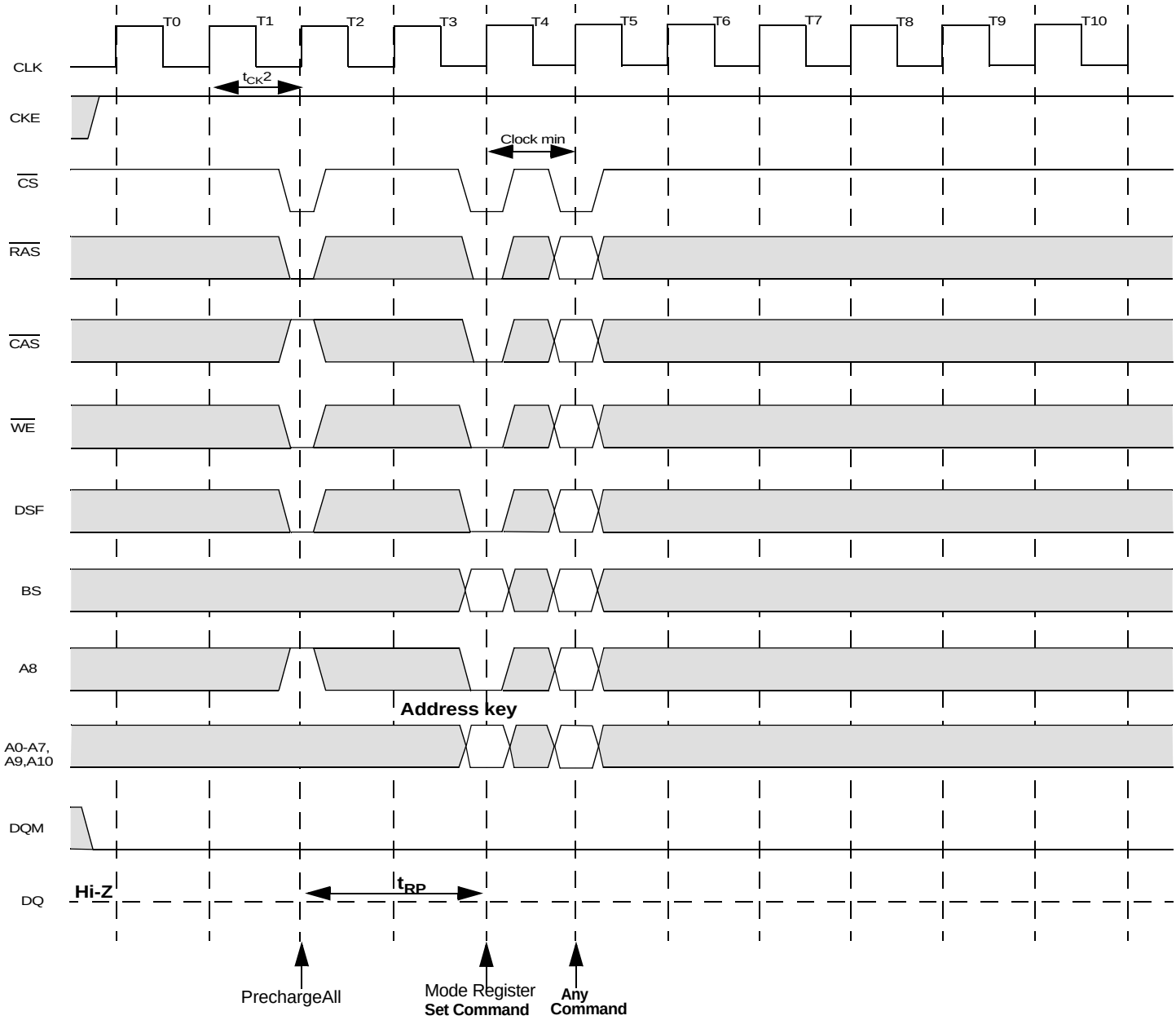
Burst Write with Auto-Precharge (Burst Length = 2, $\overline{\text{CAS}}$ Latency = 1, 2, 3)

10 Block Write and AutoPrecharge command
(RAS = "H" , CAS = "L" , WE = "H", DSF = "H" , BS = Bank , A8 = "H" , A3-A7 = Column Address, A9,A10 = Don't care DQ0-DQ31 = Column Mask)

The Block Write and AutoPrecharge command performs the precharge operation automatically after the block write operation. Once this command is given, any subsequent command can not occur within a time delay of {t_{BPL} + t_{RP} (min.)}.

11 Mode Register Set command
(RAS = "L" , CAS = "L", WE = "L" , DSF = "L" , BS , A0-A10 = Register Data)

The mode register stores the data for controlling the various operating modes of SGRAM. The Mode Register Set command programs the values of $\overline{\text{CAS}}$ latency. Addressing Mode and Burst Length in the Mode register to make SGRAM useful for variety of different applications. The default values of the Mode Register after power-up are undefined, therefore this command must be issued at the power-up sequence. The state of pins A0-A10 and BS in the same cycle is the data written in the mode register. One clock cycle is required to complete the write in the mode register (refer to the following figure). The mode register contents can be changed using the same command and the clock cycle requirements during operation as long as both banks are in the idle state.



Mode Register Set Cycle ($\overline{\text{CAS}}$ Latency = 1, 2, 3)

The mode register is divided into various fields depending on functionality.

- Burst Length Field (A2~A0)

  This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 1, 2, 4, 8, or full page.

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full Page

- Addressing Mode Select Field (A3)
  The Addressing Mode can be one of two modes, Interleave Mode or Sequential Mode.
  Sequential Mode supports burst length of 1, 2, 4, 8, or full page. But, Interleave Mode only supports burst length of 4 and 8.

A3	Addressing Mode
0	Sequential
1	Interleave

--- Addressing Sequence of Sequential Mode

An internal column address is performed by increasing the address from the column address which is input to the device. The internal column address is varied by the Burst Length as shown in the following table. When the value of column address, (n+m), in the table is larger than 255, only the least significant 8 bits are effective.

Data n	0	1	2	3	4	5	6	7	-	255	256	257	-
Column Address	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	-	n+255	n	n+1	-
Burst Length	2 words:												
	4 words:												
	8 words:												
	Full Page: Column address is repeated until terminated.												

--- Addressing Sequence of Interleave Mode
A column access is started in the input column address and is performed by inverting the address bits in the sequence shown in following table.

Data n	Column Address								Burst Length	
Data 0	A7	A6	A5	A4	A3	A2	A1	A0	**4 Words**	**8 Words**
Data 1	A7	A6	A5	A4	A3	A2	A1	$\overline{A0}$		
Data 2	A7	A6	A5	A4	A3	A2	$\overline{A1}$	A0		
Data 3	A7	A6	A5	A4	A3	A2	$\overline{A1}$	$\overline{A0}$		
Data 4	A7	A6	A5	A4	A3	$\overline{A2}$	A1	A0		
Data 5	A7	A6	A5	A4	A3	$\overline{A2}$	A1	$\overline{A0}$		
Data 6	A7	A6	A5	A4	A3	$\overline{A2}$	$\overline{A1}$	A0		
Data 7	A7	A6	A5	A4	A3	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$		

- $\overline{CAS}$ Latency Field (A6 ~ A4)
  This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum value of $\overline{CAS}$ Latency depends on the frequency of CLK. And this value satisfying the following formula must be programmed into this field.

  $t_{CAC\ (min)} \leq \overline{CAS}$ Latency x t_{CK}

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	1 clock
0	1	0	2 clocks
0	1	1	3 clocks
1	X	X	Reserved

- Mode field (A8~A7)

  A7 and A8 must be programmed to “00” in normal operation.

A8	A7	Test Mode
0	0	normal mode
0	1	Vendor Use Only
1	x	Vendor Use Only

- Single Write Mode (A9)

  This bit is used to select the write mode. When the A9 bit is “0”, Burst Read and Burst Write mode is selected. When the A9 bit is ”1”, Burst Read and Single Write mode is Selected.

A9	Single Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

12 Special Mode Register Set command
(RAS = ”L”, CAS = ”L”, WE = ”L”, DSF = ”H”, BS, A0-A10 = Register Data)

The special mode register is used to load the Color and Mask registers, which are used in Block Write and masked Write cycles. The control information being written to the Special Mode register is applied to the address inputs and the data to be written to either the Color register or the Mask register is applied to the DQs. When A6 is “high” during a Special Mode Register Set cycle, the Color register will be loaded with the data on the DQs. Similarly, when A5 is “high” during a Special Mode Register Set cycle, the Mask register will be loaded with the data on the DQs. A6 = A5 = 1 in the Special Mode Register Set cycle is illegal.

Functions	BS	A10~A7	A6	A5	A4~A0
Leave Unchanged	X	X	0	0	X
Load Mask Register	X	X	0	1	X
Load Color Register	X	X	1	0	X
Illegal	X	X	1	1	X

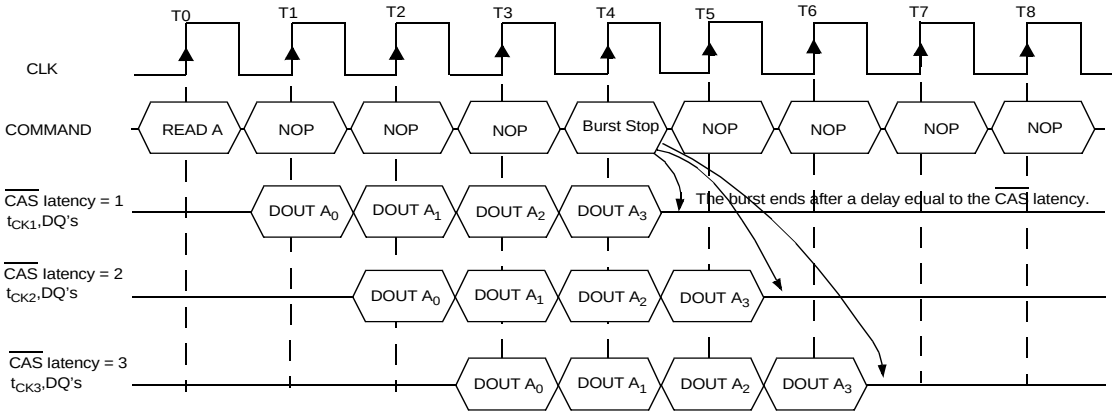
One clock cycle is required to complete the write in the Special Mode register. This command can be issued at the active state. As in write operation, this command accepts the data needed through DQ pins. Therefore it should be attended not to induce bus contention.

13 No-Operation command
(RAS = ”H”, CAS = ”H”, WE = ”H”)

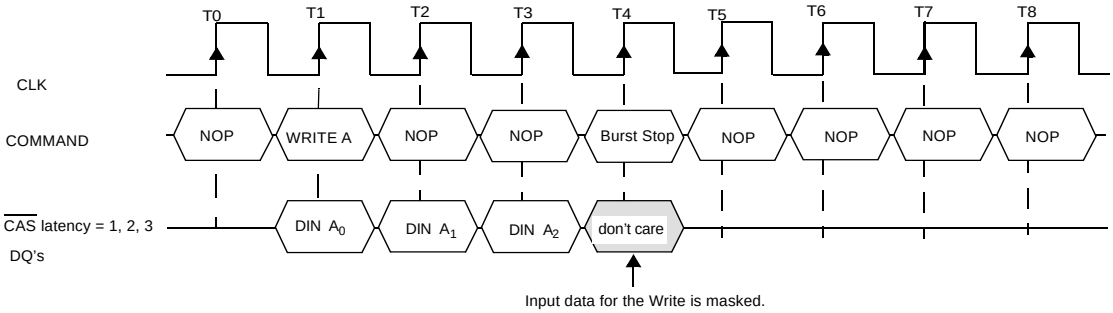
The No-Operation command is used to perform a NOP to SGRAM which is selected (CS is Low). This prevents unwanted commands from being registered during idle or wait states.

14 Burst Stop command
(RAS = ”H”, CAS = ”H”, WE = ”L’, DSF = ”L”)

Burst Stop command is used to terminate either fixed-length or full-page bursts. This command is only effective in a read/write burst without auto precharge function. The terminated read burst ends after a delay equal to the CAS latency (refer to the following figure). The termination of a write burst is shown in the following figure.



Termination of a Burst Write Operation (Burst Length > 4, $\overline{\text{CAS}}$ Latency = 1, 2, 3)



Termination of a Burst Write Operation (Burst Length = X, $\overline{\text{CAS}}$ Latency = 1, 2, 3)

15 Device Deselect command
($\overline{\text{CS}}$ = "H")

The Device Deselect command disables the command decoder so that the $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and Address inputs are ignored, regardless of whether the CLK is enabled. This command is similar to the No Operation command.

16 AutoRefresh command (refer to Figures 3 & 4 in Timing Waveforms)
($\overline{\text{RAS}}$ = "L", $\overline{\text{CAS}}$ = "L", $\overline{\text{WE}}$ = "H", DSF = "L", CKE = "H", BS, A0-A10 = Don't care)

The AutoRefresh command is used during normal operation of the SGRAM and is analagous to CAS-before-RAS(CBR) Refresh in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "don't care" during an AutoRefresh command. The internal refresh counter increments automatically on every auto refresh cycle to all of the rows. The refresh operation must be performed 2048 times within 32ms. The time required to complete the auto refresh operation is specified by t_{RP}(min.). To provide the AutoRefresh command, both banks need to be in the idle state and the device is not in power down mode (CKE is high in the previous cycle). This command must be followed by NOPs until the auto refresh operations is completed. The precharge time requirement, t_{RP}(min.) must be met befor successive auto refresh operations are performed.

17 SelfRefresh Entry command (refer to Figure 5 in Timing Waveforms)
($\overline{\text{RAS}}$ = "L", $\overline{\text{CAS}}$ = "L", $\overline{\text{WE}}$ = "H", DSF = "L", CKE = "L", BS, A0-A10 = Don't care)

The SelfRefresh is another refresh mode available in the SGRAM. It is the preferred refresh mode for data retention and low power operation. Once the SelfRefresh command is registered, all the inputs to the SGRAM becomes "don't care" with the exception of CKE, which must remain LOW. The refresh addressing and timing is internally generated to reduce power comsumption. The SGRAM may remain in SelfRefresh mode for an indefinite period. Once the SGRAM enters the SelfRefresh mode , t_{RAS}(min.) is required before exit from SelfRefresh mode. The SelfRefresh mode is exited by restarting the external clock and then asserting high on CKE(Self-Refresh Exit command).

18 SelfRefresh Exit command (refer to Figure 5 in Timing Waveforms)
(CKE = ”H”, $\overline{CS}$ = ”H” or CKE = ”H”, $\overline{RAS}$ = ”H”, $\overline{CAS}$ = ”H”, $\overline{WE}$ = ”H”)

The command is used to exit from the SelfRefresh mode. Once this command is registered, NOP or Device Deselect commands must be issued for t_{RC}(min), because time is required for the completion of any bank currently being internally refreshed. If auto refresh cycles in bursts are performed during normal operation, a burst of 1024 auto refresh cycles should be completed just prior to entering, and just after exiting the SelfRefresh mode.

19 Clock Suspend Mode Entry/PowerDown Mode Entry command (refer to Figures 6, 7, and 8 in Timing Waveforms)
(CKE = ”L”)

When SGRAM operating the burst cycle, the internal CLK is suspended (masked) from the subsequent cycle by issuing this command (asserting CKE ”low”). The device operation is held intact while CLK is suspended. On the other hand, when both banks are in the idle state, this command performs entry into the PowerDown mode. All input and output buffers (except the CKE buffer) are turned off in the PowerDown mode. The device may not remain in the Clock Suspend or PowerDown state longer than the refresh period (16ms) since the command does not perform any refresh operations.

20 Clock Suspend Mode Exit/PowerDown Mode Exit command (refer to Figures 6, 7, and 8 in Timing Waveforms)
(CKE = ”H”)

When the internal CLK has been suspended, the operation of the internal CLK is resumed from the subsequent cycle by providing this command (asserting CKE “high”). When the device is in the PowerDown mode, the device exits this mode and all disabled buffers are turned on to the active state. t_{PDE}(min.) is required when the device exit from the PowerDown mode. Any subsequent commands can be issued after one clock cycle from the end of this command.

21 Data Write/Output Enable, Data Mask/Output Disable command
(DQM = ”L”, ”H”)

During a write cycle, the DQM signal functions as Data Mask and can control every word of the input data. During a read cycle, the DQM functions as the control of output buffers. DQM is also used for device selection, byte selection and bus control in a memory system. DQM0 controls DQ0 to DQ7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, DQM3 controls DQ24 to DQ31, DQM masks the DQ’s by a byte regardless that the corresponding DQ’s are in a state of write-per-bit masking or pixel masking. the byte control. The each DQM0-3 corresponds to DQ0-7, DQ8-15, DQ16-23, DQ24-31.

Absolute Maximum Rating

Symbol	Item	Rating	Unit
V_{IN}, V_{OUT}	Input, Output Voltage	-0.3~V_{DD} + 0.3	V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.3~4.6	V
T_{OPR}	Operating Temperature	0~70	**°C**
T_{STG}	Storage Temperature	-55~150	**°C**
T_{SOLDER}	Soldering Temperature(10s)	260	**°C**
P_D	Power Dissipation	1	W
I_{OUT}	Short Circuit Output Current	50	mA

Recommended D.C. Operating Conditions (Ta = 0~70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V
V_{IH}	LVTTL Input High Voltage	2.0	-	V_{DD}+ 0.3	V
V_{IL}	LVTTL Input Low Voltage	-0.3	-	0.8	V

Capacitance (VDD = 3.3V, f = 1MHz, Ta = 25°C)

Symbol	Parameter	Min.	Max.	Unit
C_I	Input Capacitance	-	5	pF
$C_{I/O}$	Input/Output Capacitance	-	7	pF

Note: These parameters are periodically sampled and are not 100% tested.

Recommended D.C. Operating Conditions (V_{DD} = 3.3V ±0.3V, Ta = 0 ~ 70°C)

Description/test condition	Symbol	-4.5		-5		-5.5		-6		-7		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Max.	Min.	Max.		
Operating Current $t_{RC} \geq t_{RC(min)}$, Outputs Open Address changed once during $t_{CK(min)}$. Burst Length = 1, One bank active	I_{DD1}		230		220		210		200		180	mA	3,4
Precharge Standby Current in non power-down mode t_{CK} = 15ns, $\overline{CS} \geq V_{IH(min)}$, $CKE \geq V_{IH(min)}$ Input signals are changed once during 30ns.	I_{DD2N}		45		45		45		45		45		3
Precharge Standby Current in non power-down mode $t_{CK} = \infty$, $CKE \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$ Input signals are stable	I_{DD2NS}		20		20		20		20		20		
Precharge Standby Current in power-down mode t_{CK} =15ns, $CKE \leq V_{IL(max)}$	I_{DD2P}		2		2		2		2		2		3
Precharge Standby Current in power-down mode $t_{CK} = \infty$, $CKE \leq V_{IL(max)}$, $CLK \leq V_{IL(max)}$	I_{DD2PS}		2		2		2		2		2		
Active Standby Current in non power down mode $CKE \geq V_{IH(min)}$, t_{CK} = 15ns(Both Bank Active) Input signals are changed once during 30ns.	I_{DD3N}		50		50		50		50		50		3
Active Standby Current in power-down mode $CKE \leq V_{IL(max)}$, t_{CK} = 15ns, $\overline{CS} \geq V_{IH(min)}$(Both Bank Active)	I_{DD3P}		5		5		5		5		5		
Operating Current (Page Burst, and All Bank activated) $t_{CCD} = t_{CCD(min)}$, Outputs Open, Multi-bank interleave, gapless data	I_{DD4}		310		290		275		260		230		4,5
Refresh Current $t_{RC} \geq t_{RC(min)}$ (t_{REF} = 32ms)	I_{DD5}		230		220		210		200		180		3
Self Refresh Current $CKE \leq 0.2V$	I_{DD6}		3.5		3.5		3.5		3.5		3.5		
Operating Current (One Bank Block Write) $t_{CK} = t_{CK(min)}$, Outputs Open, $t_{BWC} = t_{BWC(min)}$	I_{DD7}		230		210		200		180		150		

Parameter	Description	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current ($0V \leq V_{IN} \leq V_{DD}$ All other pins not under test = 0V)	-5	5	µA	
I_{OL}	Output Leakage Current Output disable, ($0V \leq V_{OUT} \leq V_{DDQ}$)	-5	5	µA	
V_{OH}	LVTTL Output "H" Level Voltage (I_{OUT} = -2mA)	2.4	-	V	

V_{OL}	LVTTL Output "L" Level Voltage (I_{OUT} = 2mA)	-	0.4	V	

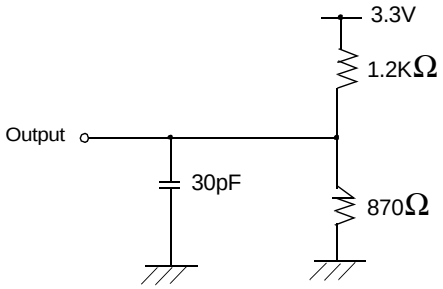
Electrical Characteristics and Recommended A.C. Operating Conditions
(V_{DD} = 3.3V±0.3V, Ta = 0~70°C) (Note: 6, 7, 8, 9, 10) * CL is CAS Latency.**

symbol	A.C. Parameter		-4.5		-5		-5.5		-6		-7		unit	note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Row cycle time		55		55		56.5		60		62		ns	10
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay		15		15		16.5		18		20			10
t_{RP}	Precharge to refresh/row activate command		15		15		16.5		18		20			10
t_{RRD}	Row activate to row activate delay		9		10		11		12		14			10
t_{RAS}	Row activate to precharge time		40	100K	40	100K	40	100K	42	100K	42	100K		
t_{WR}	Write recovery time		7		7		7		7		7			
t_{CK1}	Clock cycle time	CL* = 1	-		-		-		18		18			
t_{CK2}		CL* = 2	-		-		-		8		9			
t_{CK3}		CL* = 3	4.5		5		5.5		6		7			
t_{CH}	Clock high time		2		2		2		2		2.5			
t_{CL}	Clock low time		2		2		2		2		2.5			
t_{AC1}	Access time from CLK (positive edge)	CL* = 1		-		-		-		17		17		
t_{AC2}		CL* = 2		-		-		-		6		6		
t_{AC3}		CL* = 3		4		4.5		5		5.5		6		
t_T	Transition time of CLK (Rise and Fall)		0.5	10	0.5	10	0.5	10	0.5	10	0.5	10		
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay time		1		1		1		1		1		CLK	
t_{OH}	Data output hold time		1.5		2		2		2		2		ns	
t_{LZ}	Data output low impedance		2		2		2		2		2			
t_{HZ1}	Data output high impedance(CL = 1)		-	-	-	-	-	-	2	5	3	6		9
t_{HZ2}	Data output high impedance(CL = 2)		-	-	-	-	-	-	2	5	3	6		9
t_{HZ3}	Data output high impedance(CL = 3)		2	4	2	4.5	2	4.5	2	5	3	5		9
t_{IS}	Data/Address/Control Input setup time		1.5		1.5		1.5		1.5		2			
t_{IH}	Data/Address/Control Input hold time		0.8		0.8		1		1		1			
t_{SRX}	Minimum CKE "High"for Self-Refresh exit		1		1		1		1		1		CLK	
t_{PDE}	Power Down Exit set-up time		4		4		4		5		5		ns	
t_{RSC}	(Special) Mode Register Set Cycle time		2		2		2		2		2		CLK	10
t_{BWC}	Block Write Cycle time		1		1		1		1		1		CLK	
t_{DAL2}	Data-in to ACT (REF) Command (CL = 2)		-		-		-		1clk+ t_{RP}		1clk+ t_{RP}		ns	
t_{DAL3}	Data-in to ACT (REF) Command (CL = 3)		1clk+ t_{RP}		1clk+ t_{RP}		1clk+ t_{RP}		1clk+ t_{RP}		1clk+ t_{RP}			
t_{BPL}	Block Write to Precharge command		1		1		1		1		1		CLK	
t_{REF}	Refresh time			32		32		32		32		32	ms	

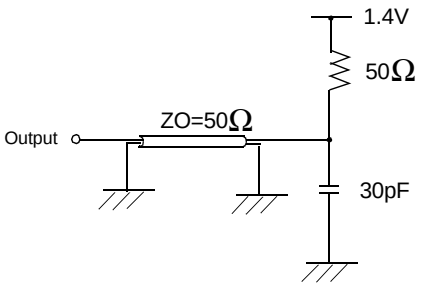
Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}. Assume that there is only one read/write cycle during t_{RC} (min).
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. Assume minimum column address update cycle t_{CCD} (min).
6. Power-up sequence is described in Note 11.
7. A.C. Test Conditions

Reference Level of Output Signals	1.4V / 1.4V
Output Load	Reference to the Under Output Load (B)
Input Signal Levels	3.0V / 0.0V
Transition Time (Rise and Fall) of Input Signals	1ns
Reference Level of Input Signals	1.4V



LVTTL D.C. Test Load (A)



LVTTL A.C. Test Load (B)

8. Transition times are measured between V_{IH} and V_{IL}. Transition (rise and fall) of input signals are fixed slope (1 ns).
9. t_{HZ} defines the time at which the outputs achieve the open circuit condition and are not reference levels.
10. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows:

    the number of clock cycles = specified value of timing/Clock cycle time (count fractions as a whole number)

Latency relationship to frequency (Unit : clock cycles)
-4.5 Version (Calculation with t_{CK} = 4.5ns ~ 30ns)

Clock period (t_{CK})	**t_{RC}**	**t_{RP}**	**t_{RRD}**	**t_{RAS}**	**t_{RSC}**	**t_{RCD}**
	55ns	**15ns**	**9ns**	**40ns**	**9ns**	**15ns**
30ns	2	1	1	2	1	1
20ns	3	1	1	2	1	1
15ns	4	1	1	3	1	1
10ns	6	2	1	4	1	2
4.5ns	13	4	2	9	2	4

-5 Version (Calculation with t_{CK} = 5ns ~ 30ns)

Clock period (t_{CK})	t_{RC}	t_{RP}	t_{RRD}	t_{RAS}	t_{RSC}	t_{RCD}
	55ns	15ns	10ns	40ns	10ns	15ns
30ns	2	1	1	2	1	1
20ns	3	1	1	2	1	1
15ns	4	1	1	3	1	1
10ns	6	2	1	4	1	2
5ns	11	3	2	8	2	3

-5.5 Version (Calculation with t_{CK} = 5.5ns ~ 30ns)

Clock period (t_{CK})	t_{RC}	t_{RP}	t_{RRD}	t_{RAS}	t_{RSC}	t_{RCD}
	56.5ns	16.5ns	11ns	40ns	11ns	16.5ns
30ns	2	1	1	2	1	1
20ns	3	1	1	2	1	1
15ns	4	2	1	3	1	2
10ns	6	2	2	4	2	2
5.5ns	11	3	2	8	2	3

-6 Version (Calculation with t_{CK} = 6ns ~ 30ns)

Clock period (t_{CK})	t_{RC}	t_{RP}	t_{RRD}	t_{RAS}	t_{RSC}	t_{RCD}
	60ns	18ns	12ns	42ns	12ns	18ns
30ns	2	1	1	2	1	1
20ns	3	1	1	3	1	1
15ns	4	2	1	3	1	2
10ns	6	2	2	5	2	2
6ns	10	3	2	7	2	3

-7 Version (Calculation with t_{CK} = 7ns ~ 30ns)

Clock period (t_{CK})	t_{RC}	t_{RP}	t_{RRD}	t_{RAS}	t_{RSC}	t_{RCD}
	62ns	20ns	14ns	42ns	14ns	20ns
30ns	3	1	1	2	1	1
20ns	4	1	1	3	1	1
15ns	5	2	1	3	1	2
10ns	7	2	2	5	2	2
7ns	10	3	2	6	2	3

11. Power up Sequence

Power up must be performed in the following sequence.

1) Power must be applied to V_{DD} and V_{DDQ} (simultaneously) when all input signals are held "NOP" state and CKE = "H", DQM = "H". The CLK signal must be started at the same time.
2) After power-up, a pause of 200u secouds minimum is required. Then, it is recommended that DQM is held "high" (V_{DD} levels) to ensure DQ output to be in the high impedance.
3) Both banks must be precharged.
4) Mode Register Set command must be asserted to initialize the Mode register.
5) A minimum of 8 Auto-Refresh dummy cycles must be required to stabilize the internal circuitry of the device. Sequence of 4 and 5 may be changed.

Timing Waveforms

Figure 1. AC Parameters for Write Timing (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2)

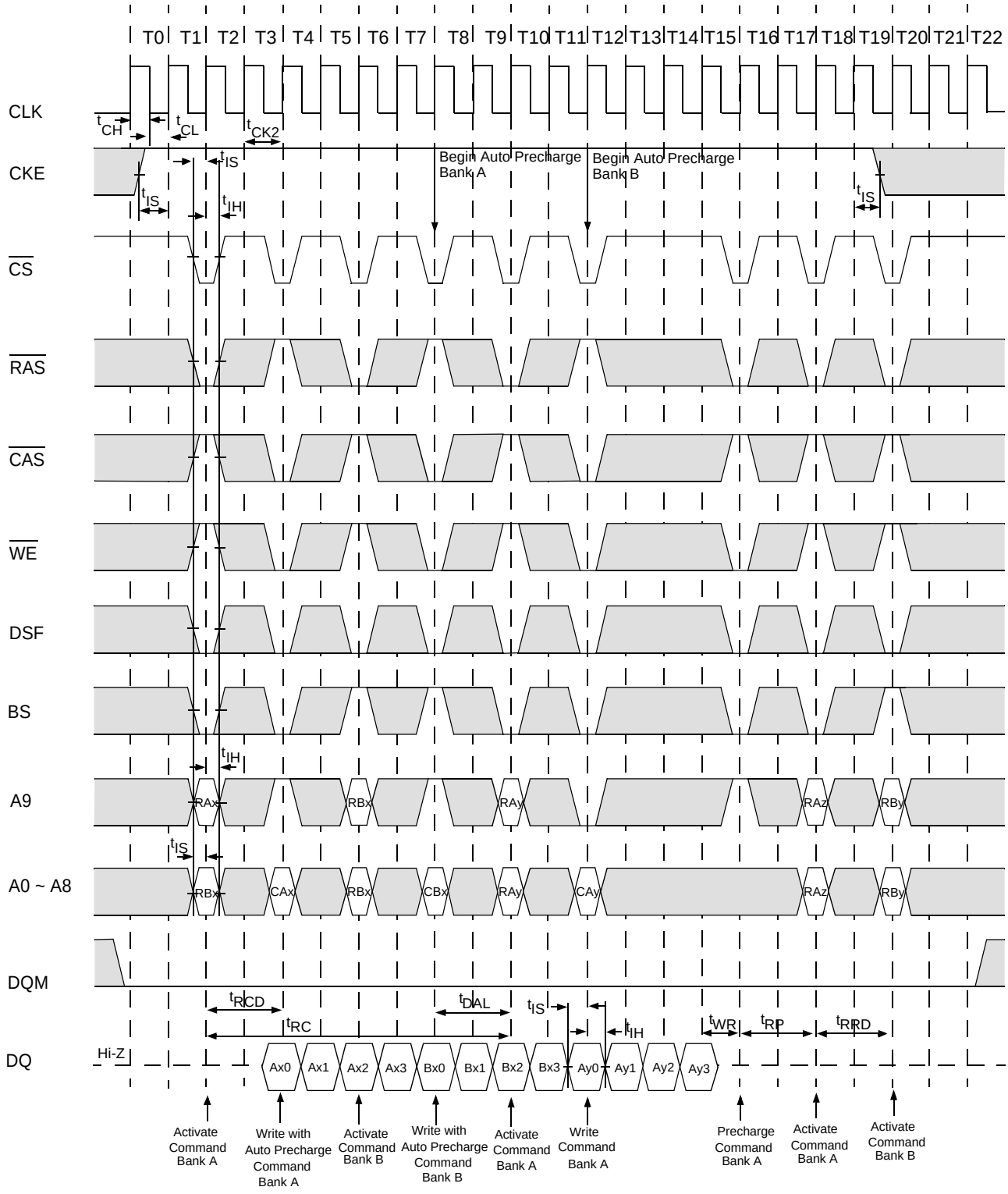


Figure 2. AC Parameters for Read Timing (Burst Length = 2, $\overline{\text{CAS}}$ Latency = 2)

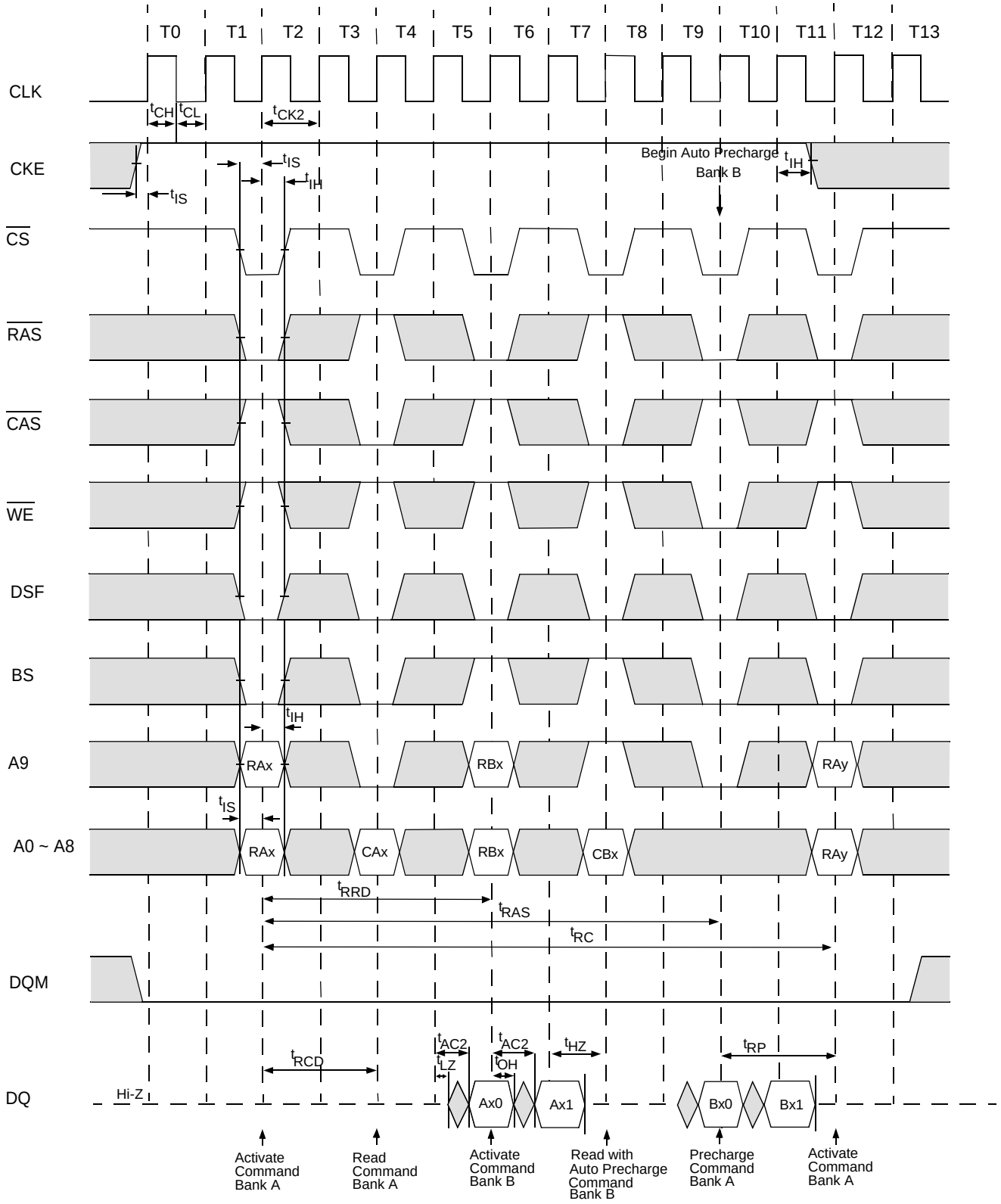


Figure 3. Auto Refresh (CBR) (Burst Length = 4, $\overline{CAS}$ Latency = 2)

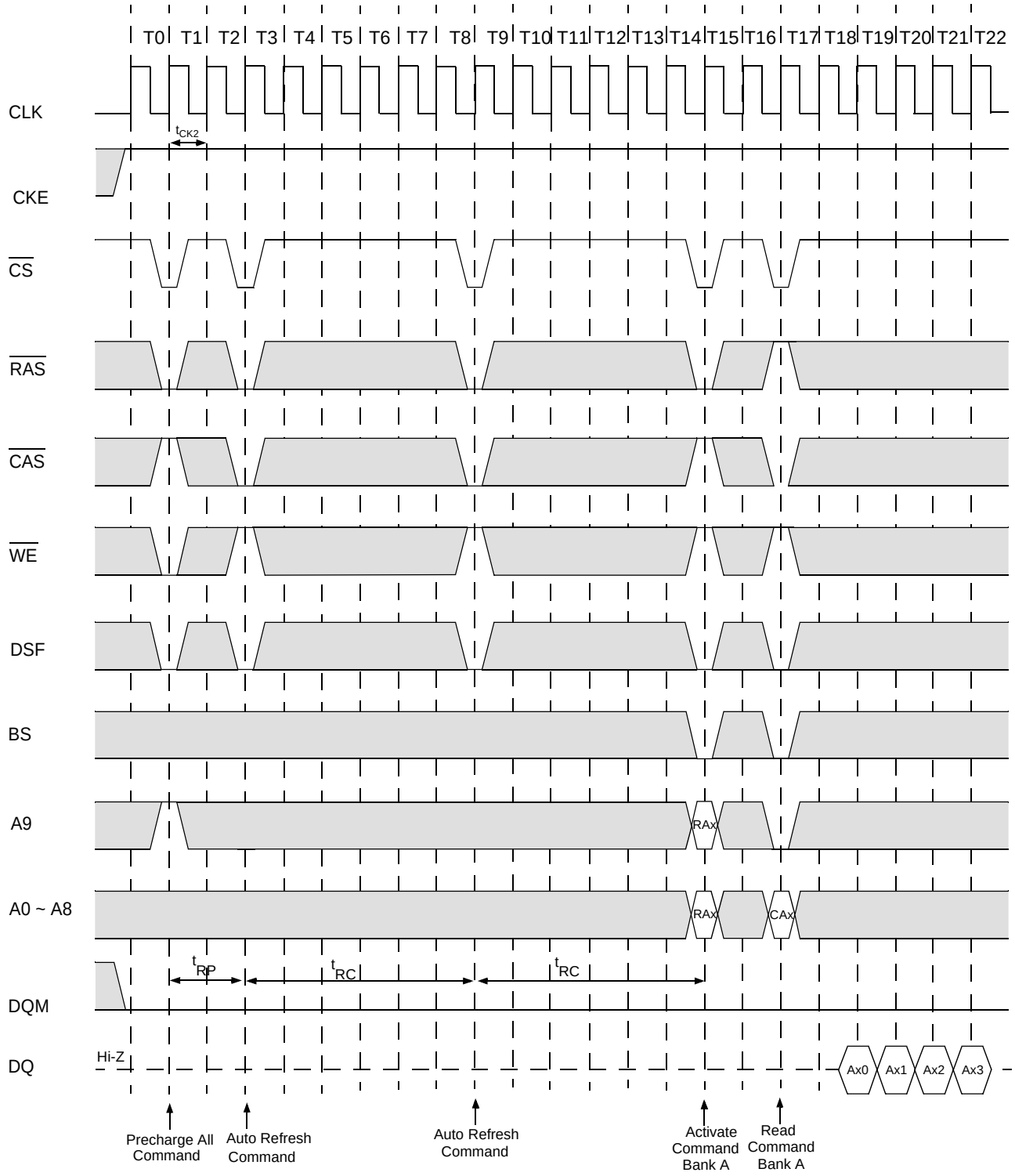


Figure 4. Power on Sequence and Auto Refresh (CBR)

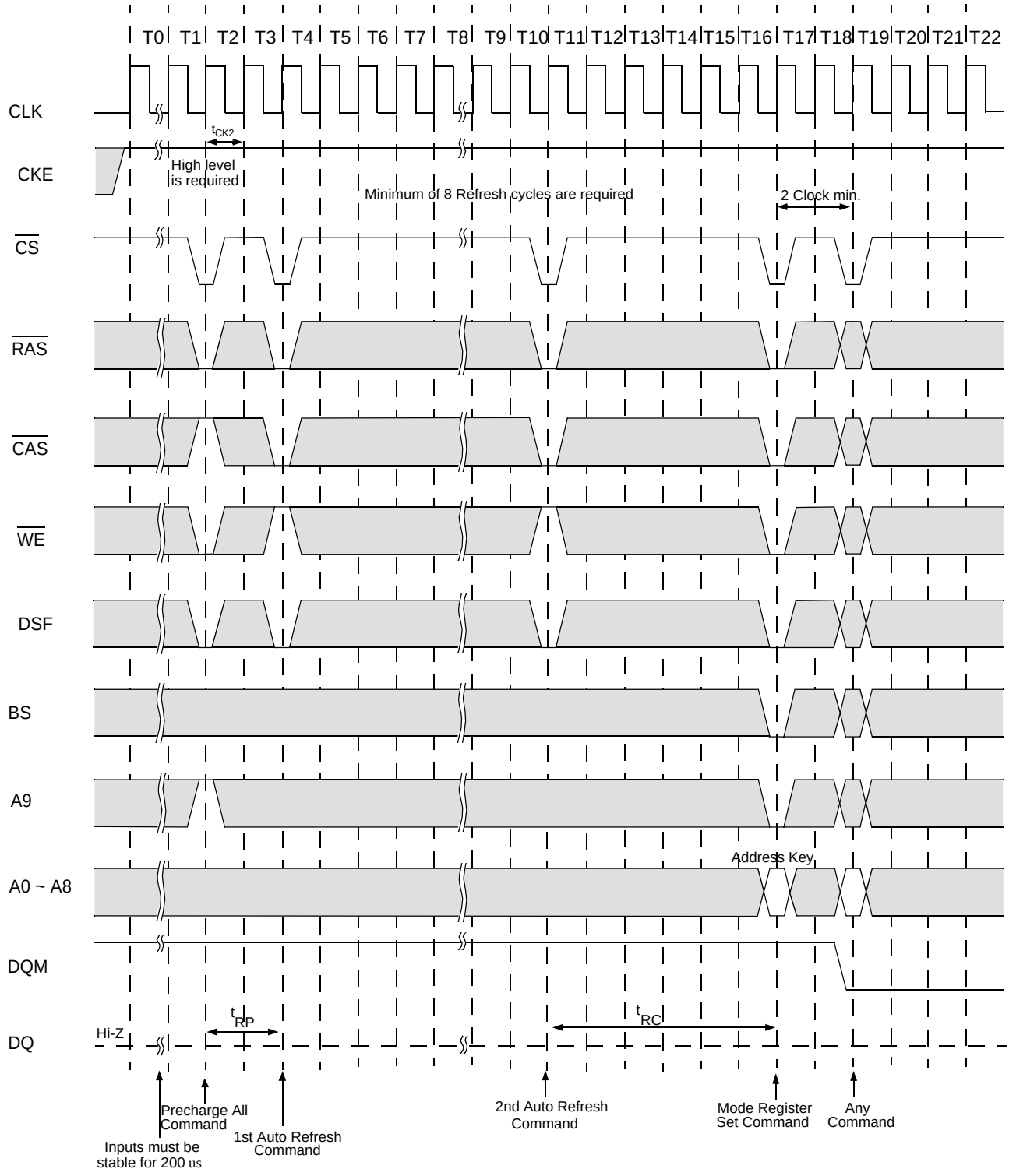
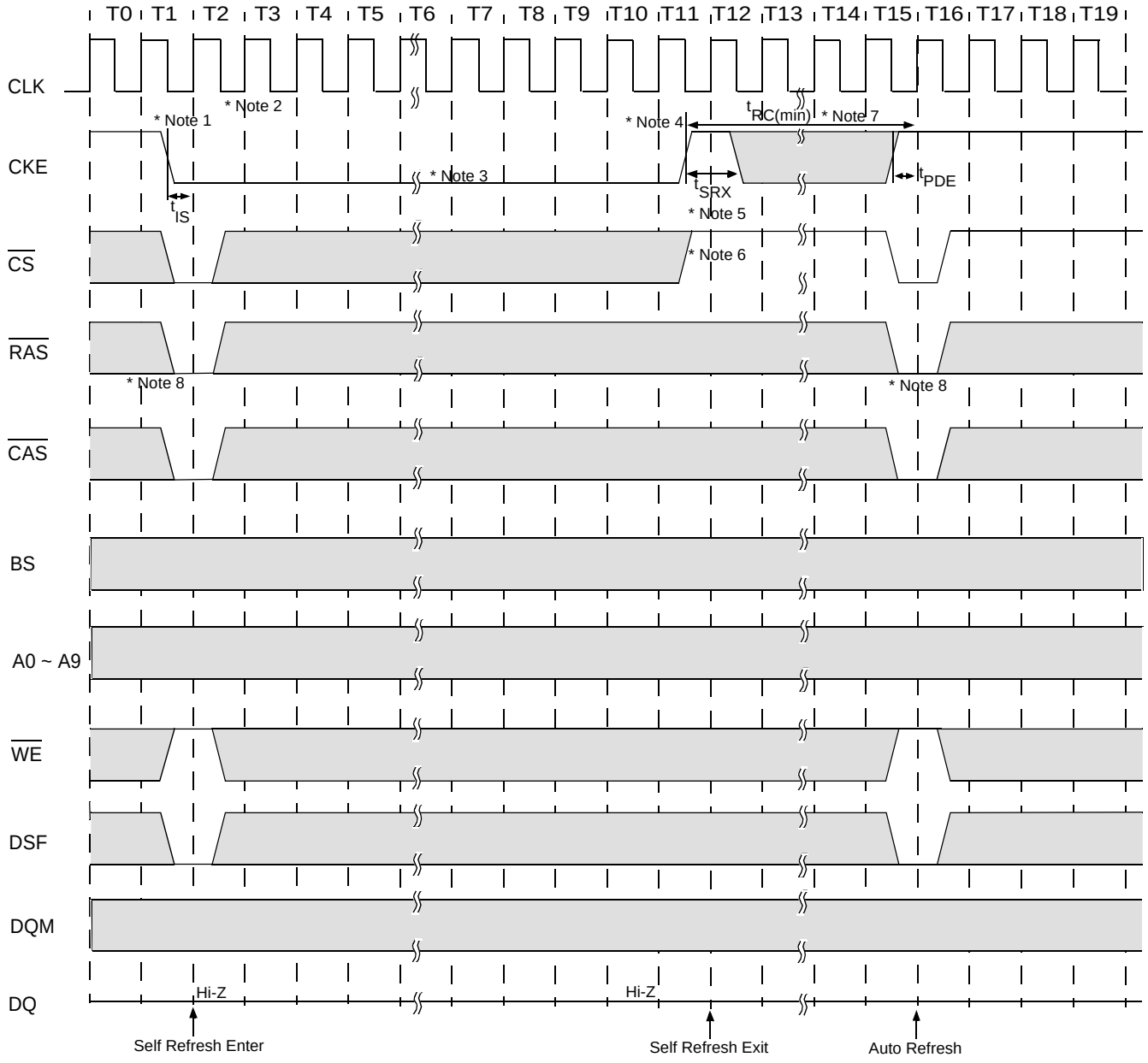


Figure 5. Self Refresh Entry & Exit Cycle



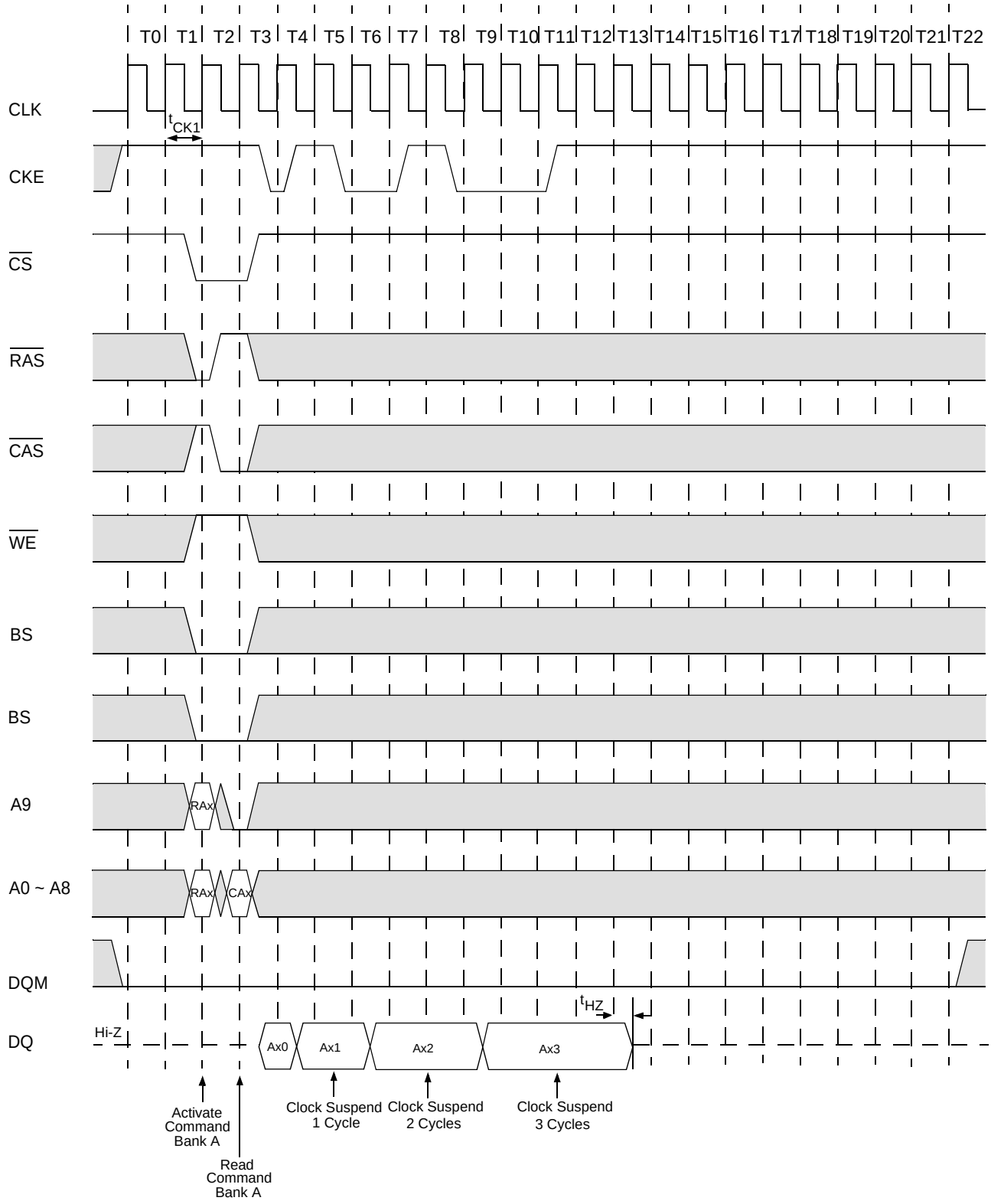
Note: To Enter SelfRefresh Mode

1. CS, RAS & CAS with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in SelfRefresh mode as long as CKE stays "low".
   Once the device enters SelfRefresh mode, Minimum t_{RAS} is required before exit from SelfRefresh.

Note: To Exit SelfRefresh Mode

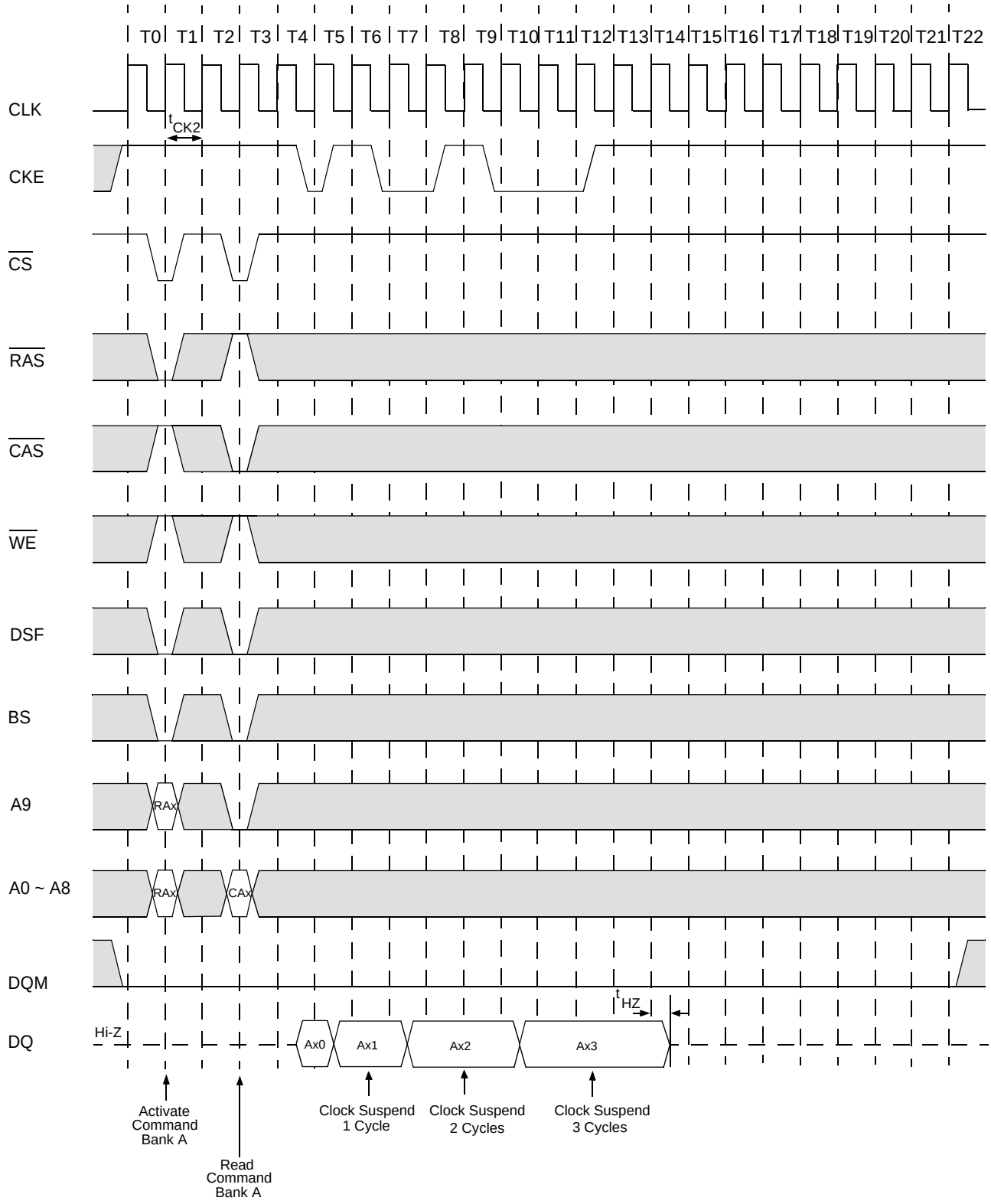
4. System clock restart and be stable before returning CKE high.
5. Enable CKE and CKE should be set high for minimum time of t_{SRX}.
6. $\overline{CS}$ starts from high.
7. Minimum t_{RC} is required after CKE going high to complete SelfRefresh exit.
8. 1024 cycles of burst AutoRefresh is required before SelfRefresh entry and after SelfRefresh exit if the system uses burst refresh.

Figure 6.1 Clock Suspension During Burst Read (Using CKE)
(Burst Length = 4, CAS Latency = 1)



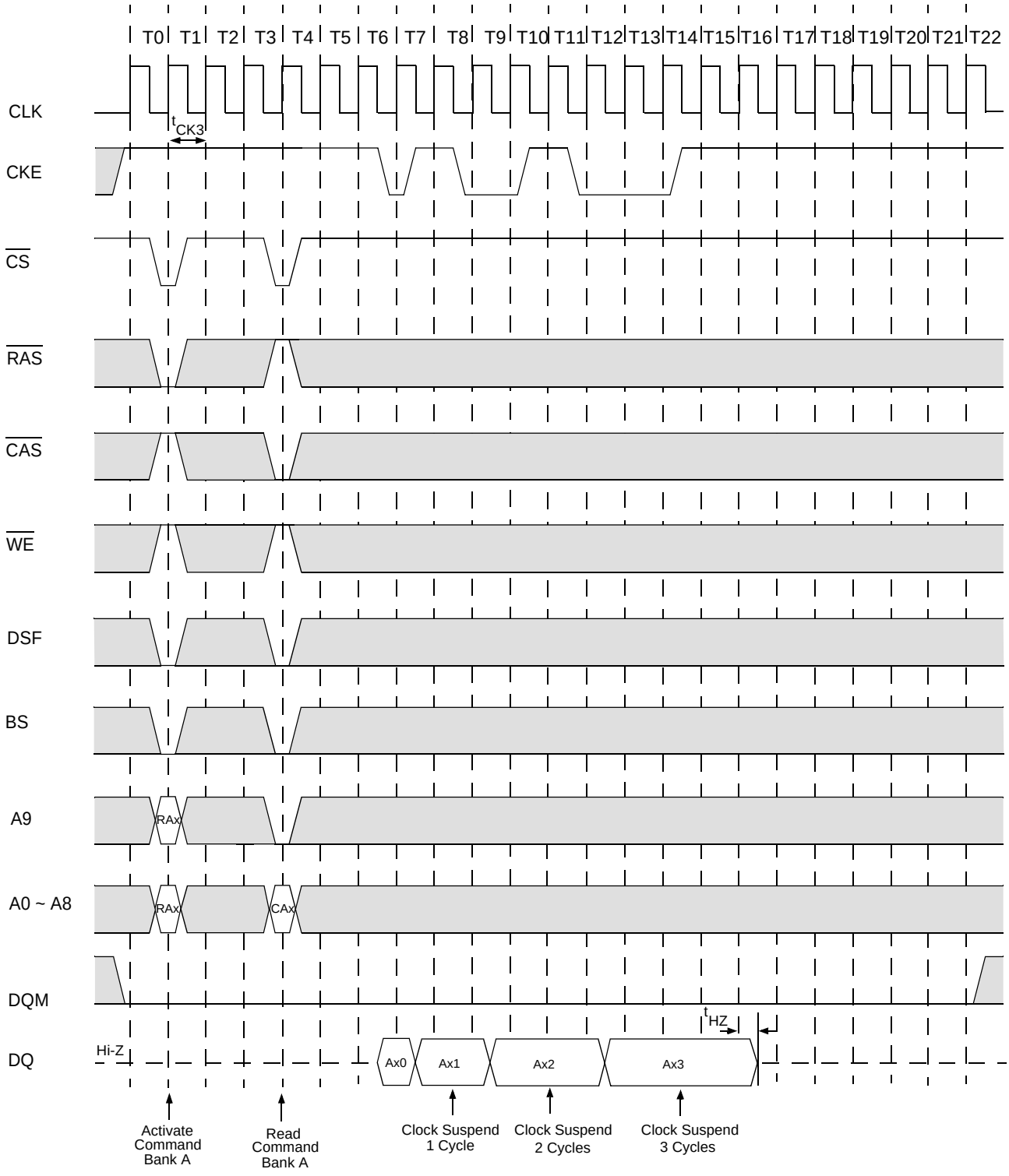
Note: CKE to CLK disable/enable = 1 clock

Figure 6.2 Clock Suspension During Burst Read (Using CKE)
(Burst Length = 4, CAS Latency = 2)



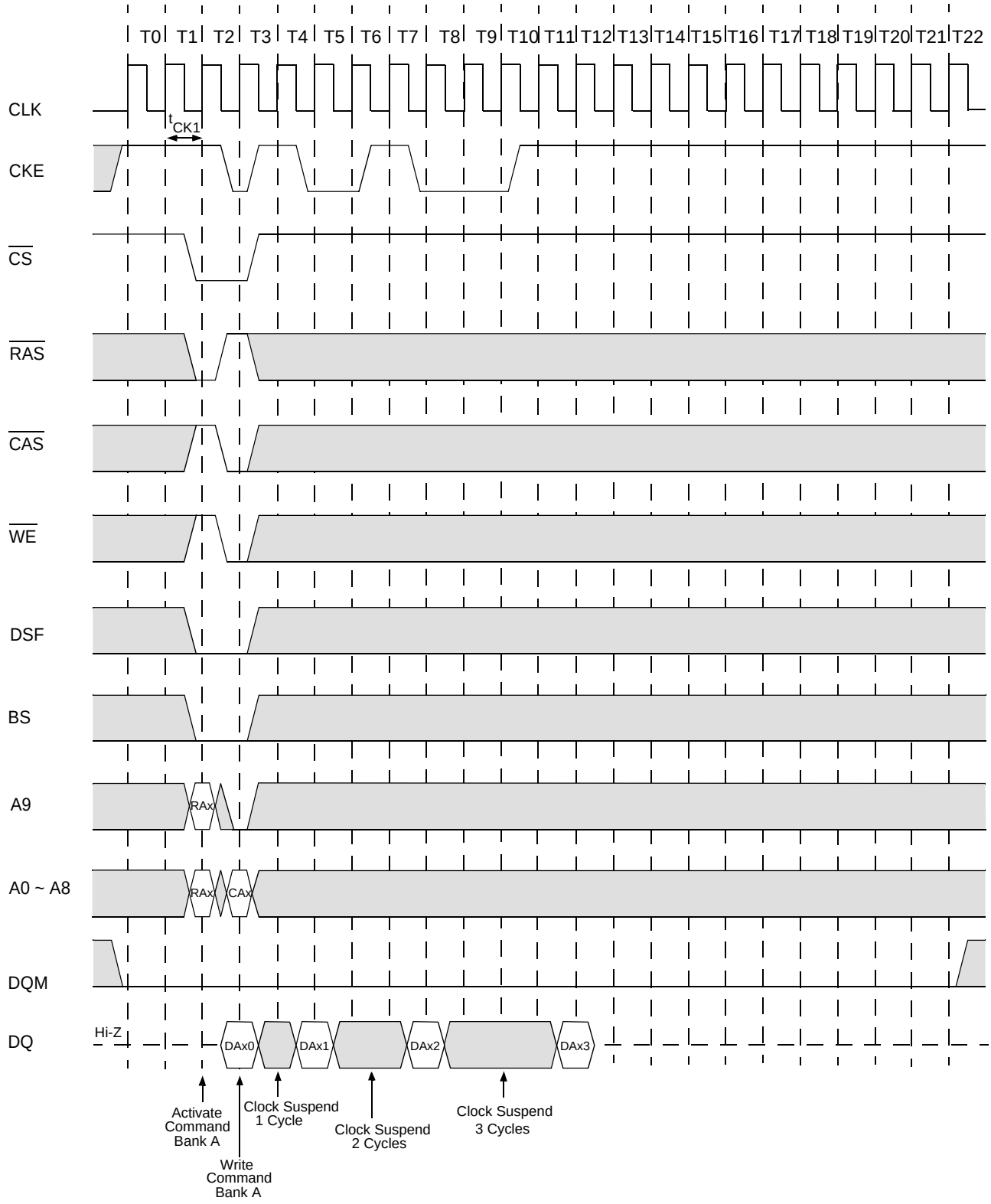
Note: CKE to CLK disable/enables = 1 clock

Figure 6.3 Clock Suspension During Burst Read (Using CKE)
(Burst Length = 4, CAS Latency = 3)



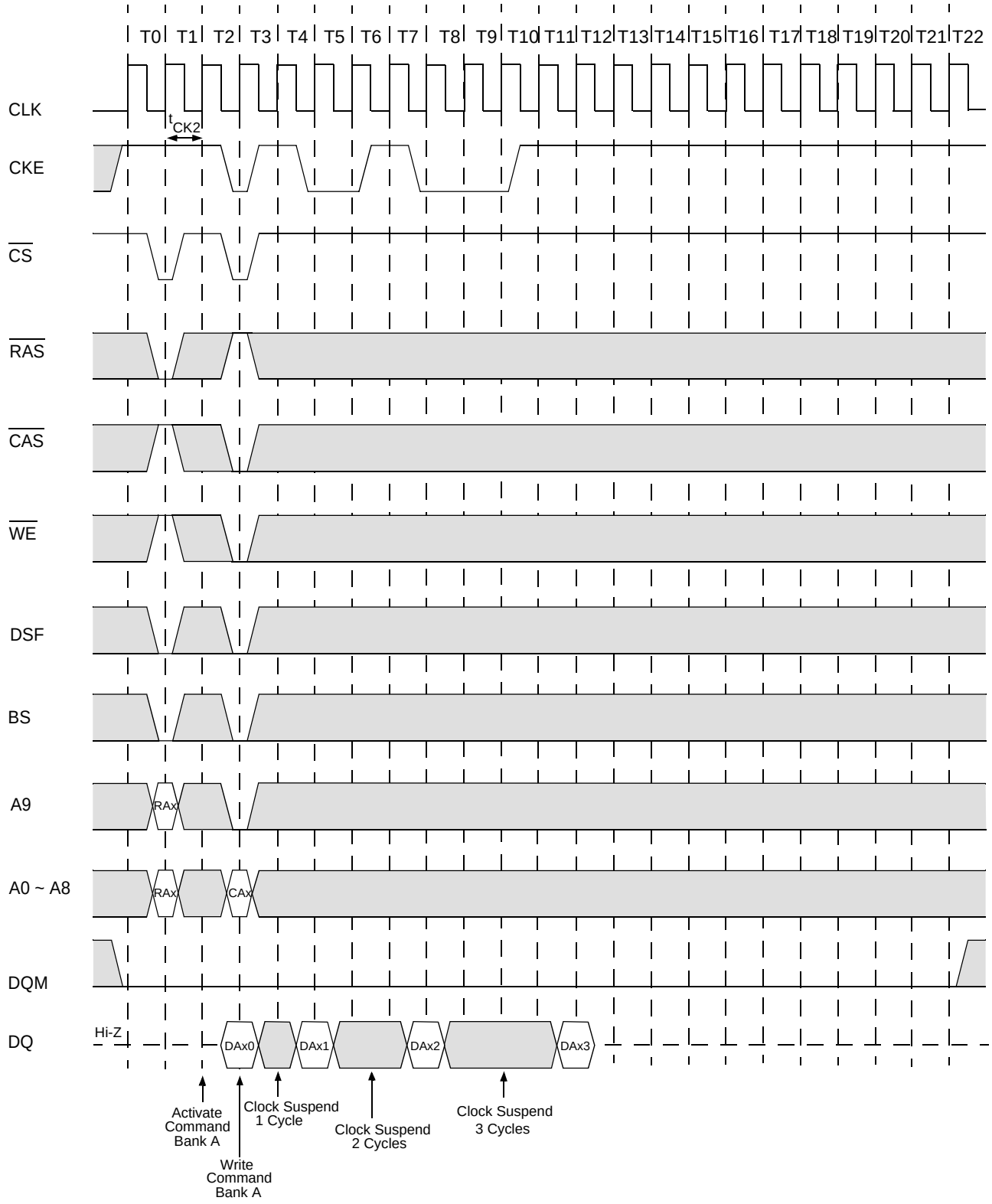
Note: CKE to CLK disable/enable = 1 clock

Figure 7.1 Clock Suspension During Burst Write (Using CKE)
(Burst Length = 4, CAS Latency = 1)



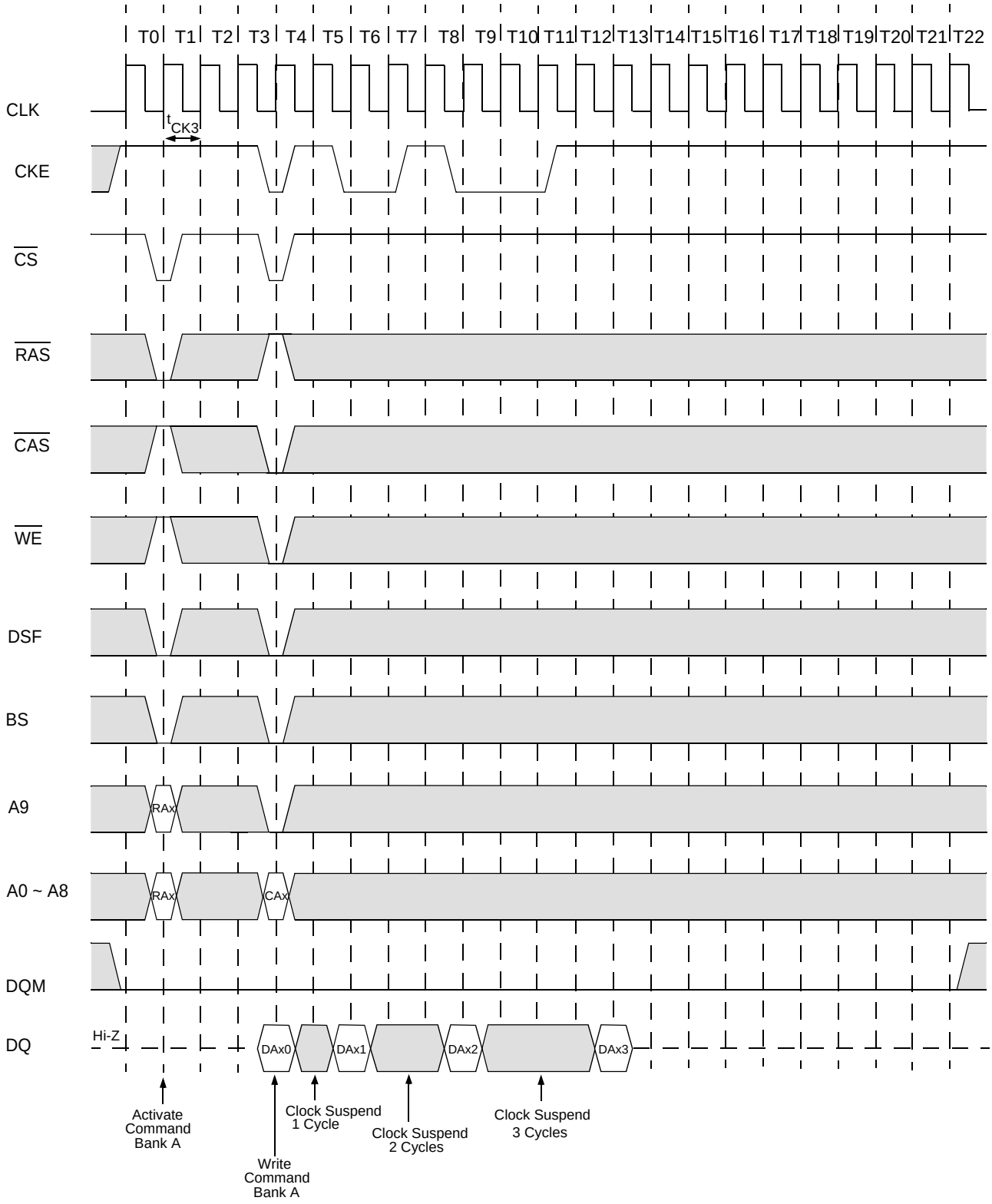
Note: CKE to CLK disable/enable = 1 clock

Figure 7.2 Clock Suspension During Burst Write (Using CKE)
(Burst Length = 4, CAS Latency = 2)



Note: CKE to CLK disable/enable = 1 clock

Figure 7.3 Clock Suspension During Burst Write (Using CKE)
(Burst Length = 4, CAS Latency = 3)



Note: CKE to CLK disable/enable = 1 clock

Figure 8. Power Down Mode and Clock Mask
(Burst Length = 4, $\overline{\text{CAS}}$ Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2)

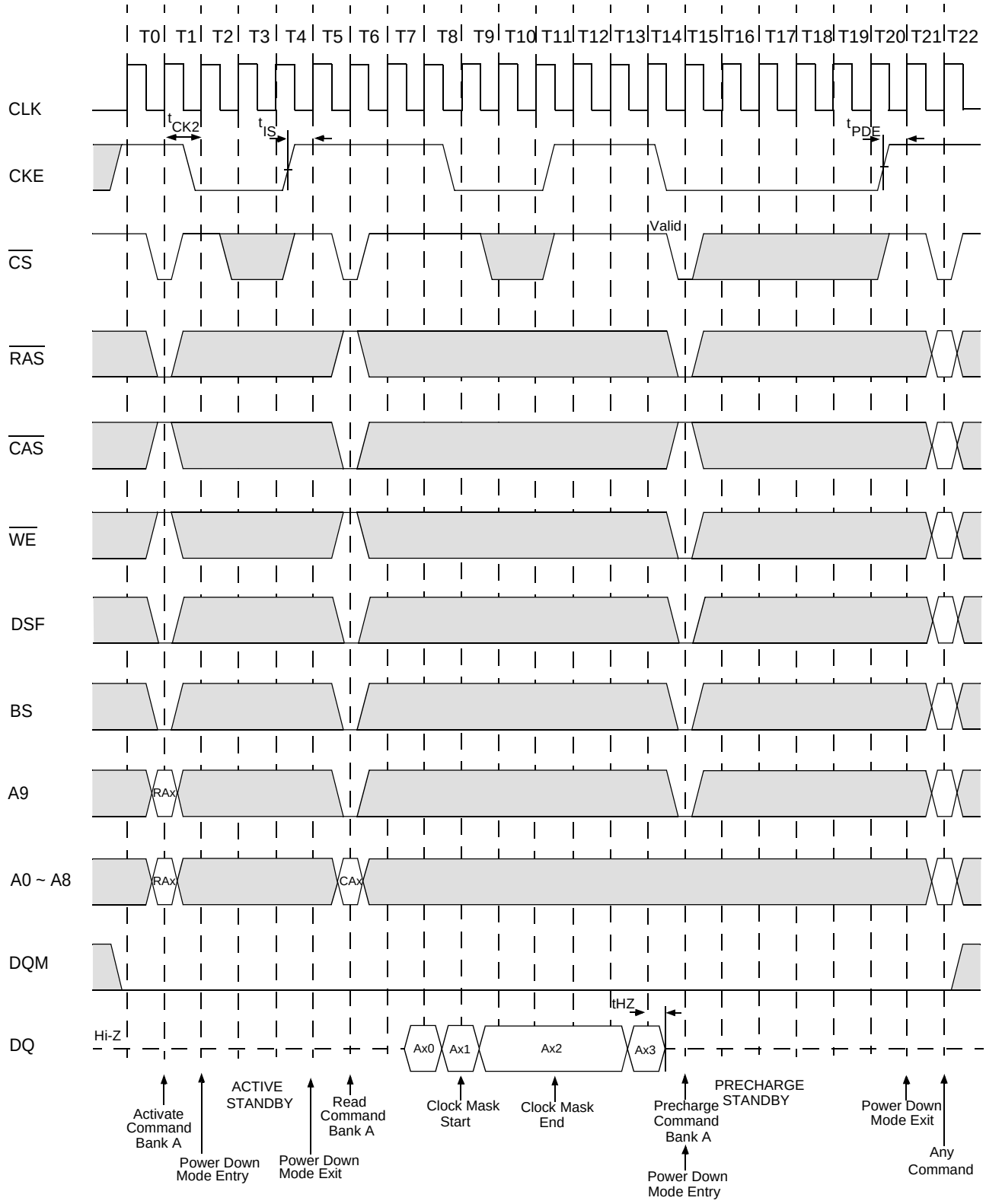


Figure 9.1 Random Column Read (Page within same Bank)
(Burst Length = 4, CAS Latency = 1)

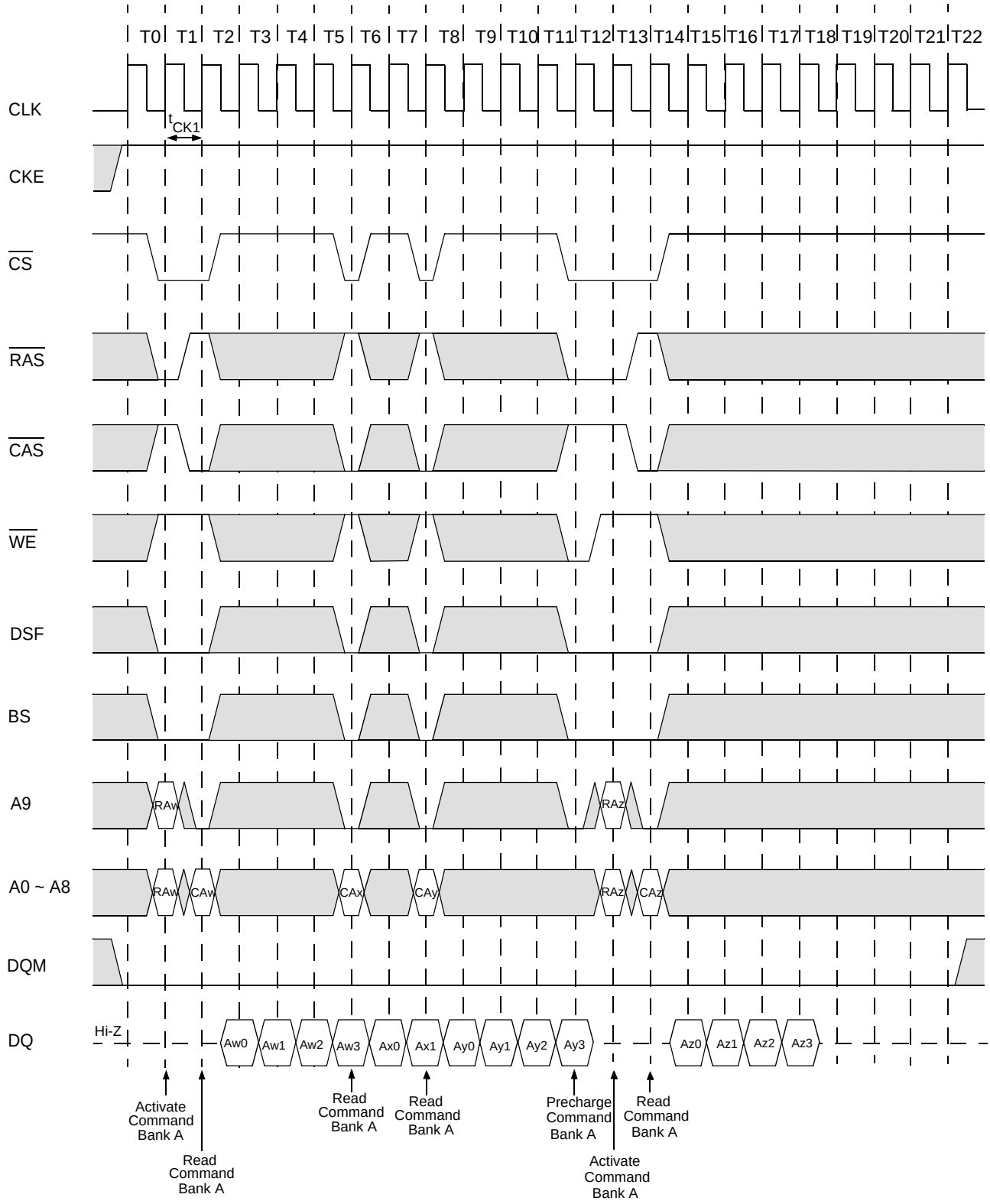


Figure 9.2 Random Column Read (Page within same Bank)
(Burst Length = 4, CAS Latency = 2)

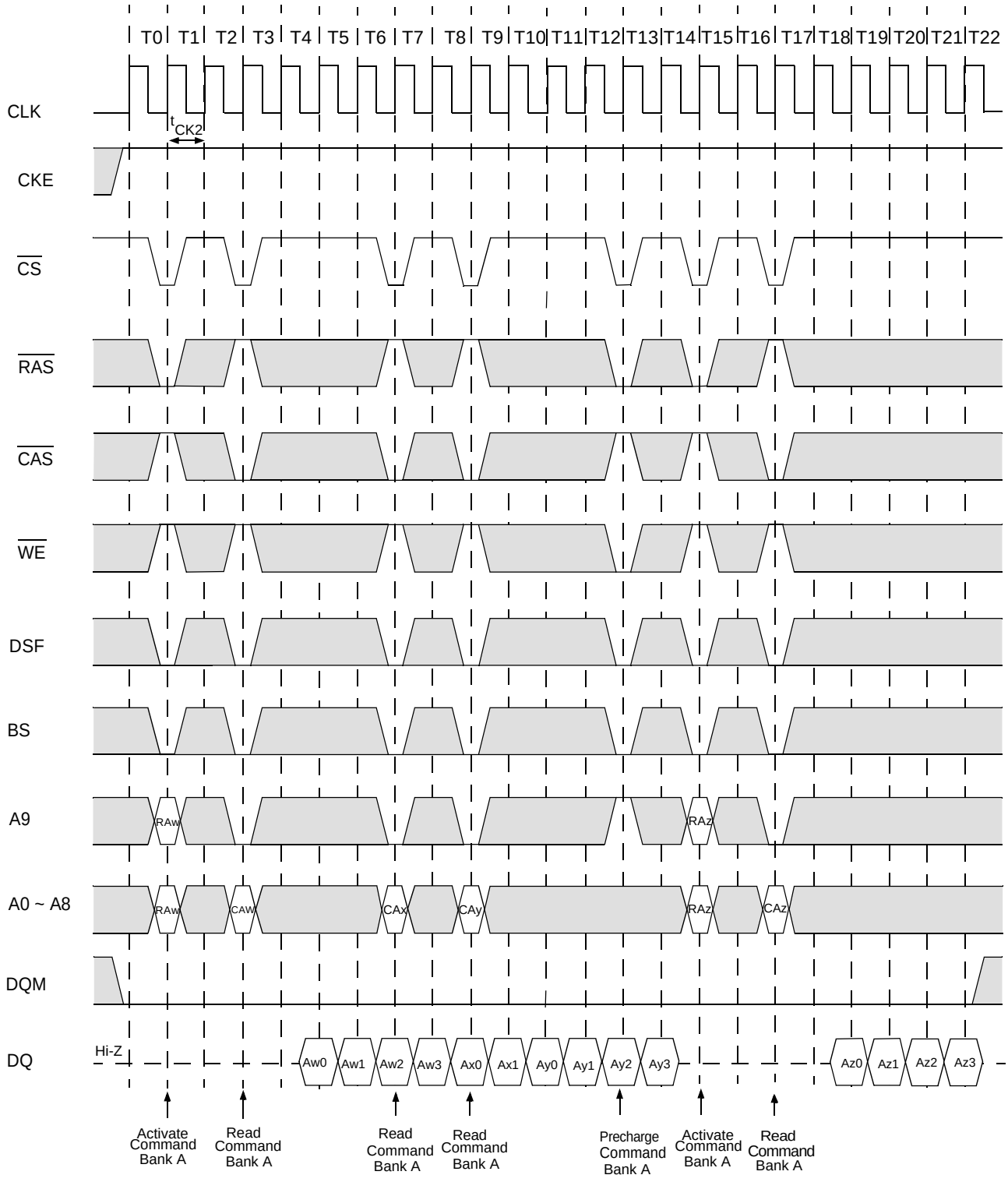
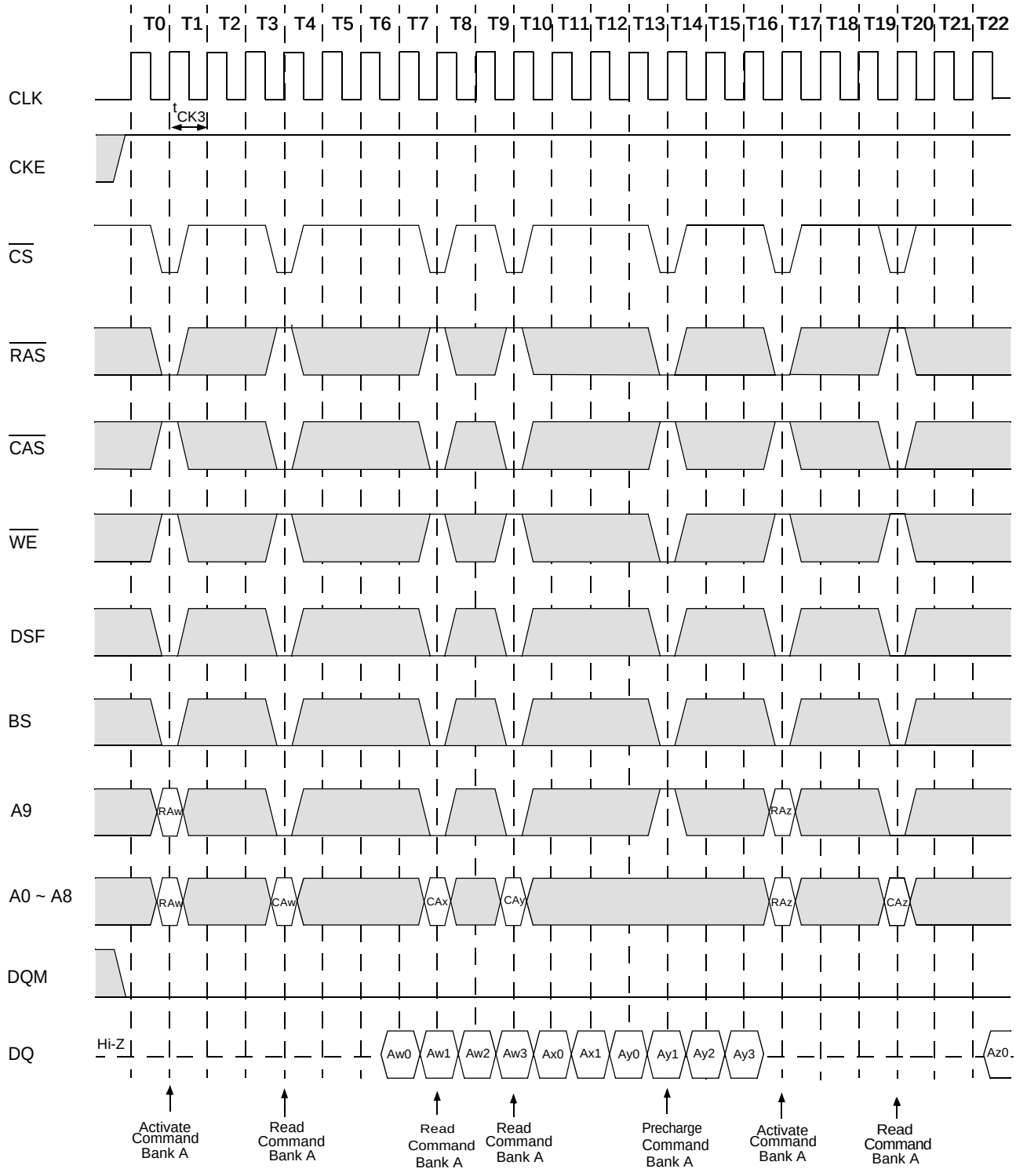


Figure 9.3 Random Column Read (Page within same Bank)
(Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3)



Note: CKE to CLK disable/enable = 1 clock

Figure 10.1 Random Column Write (Page within same Bank) (Burst Length = 4, CAS Latency = 1)

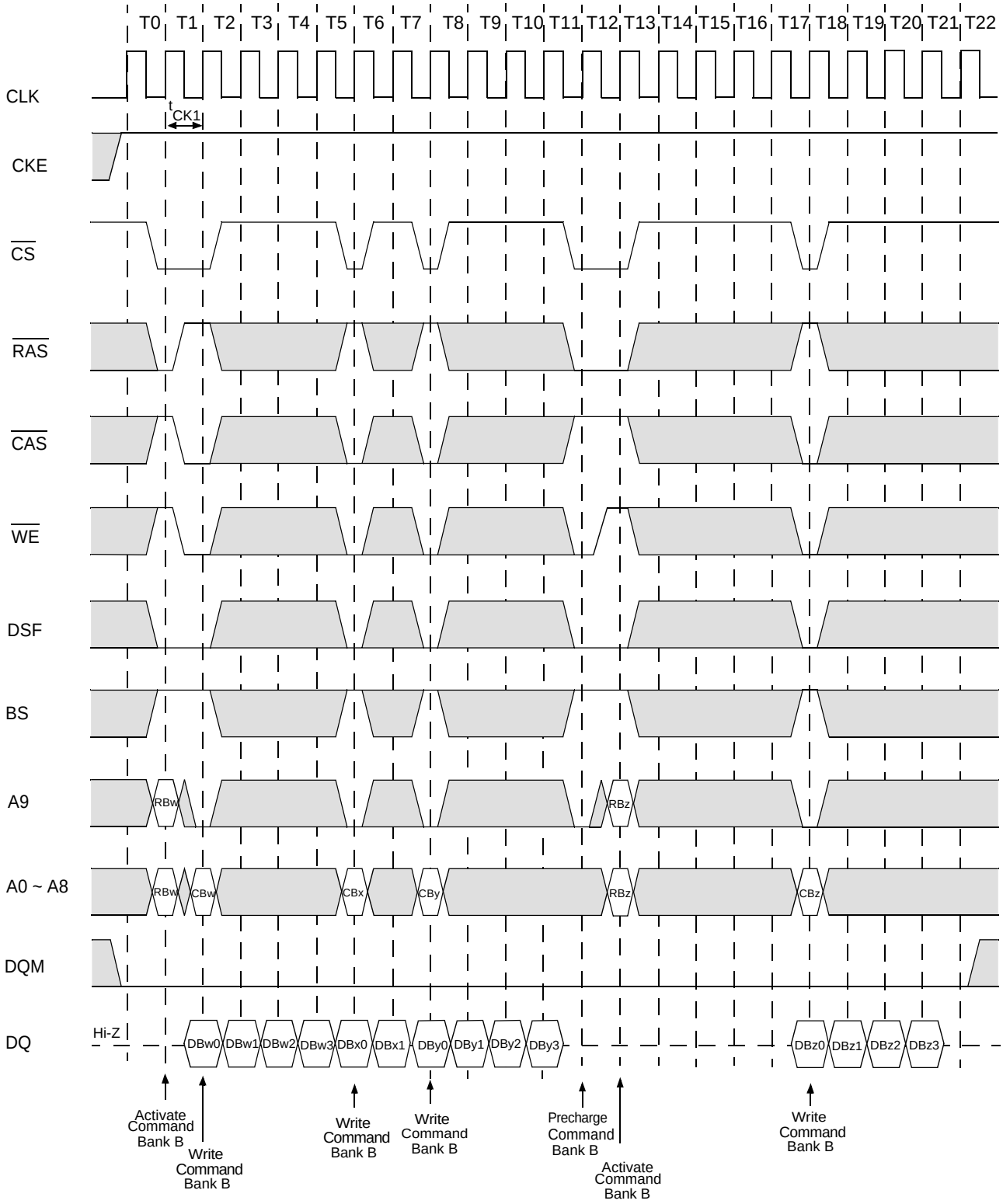


**Figure 10.2 Random Column Write (Page within same Bank)
(Burst Length = 4, CAS Latency = 2)**

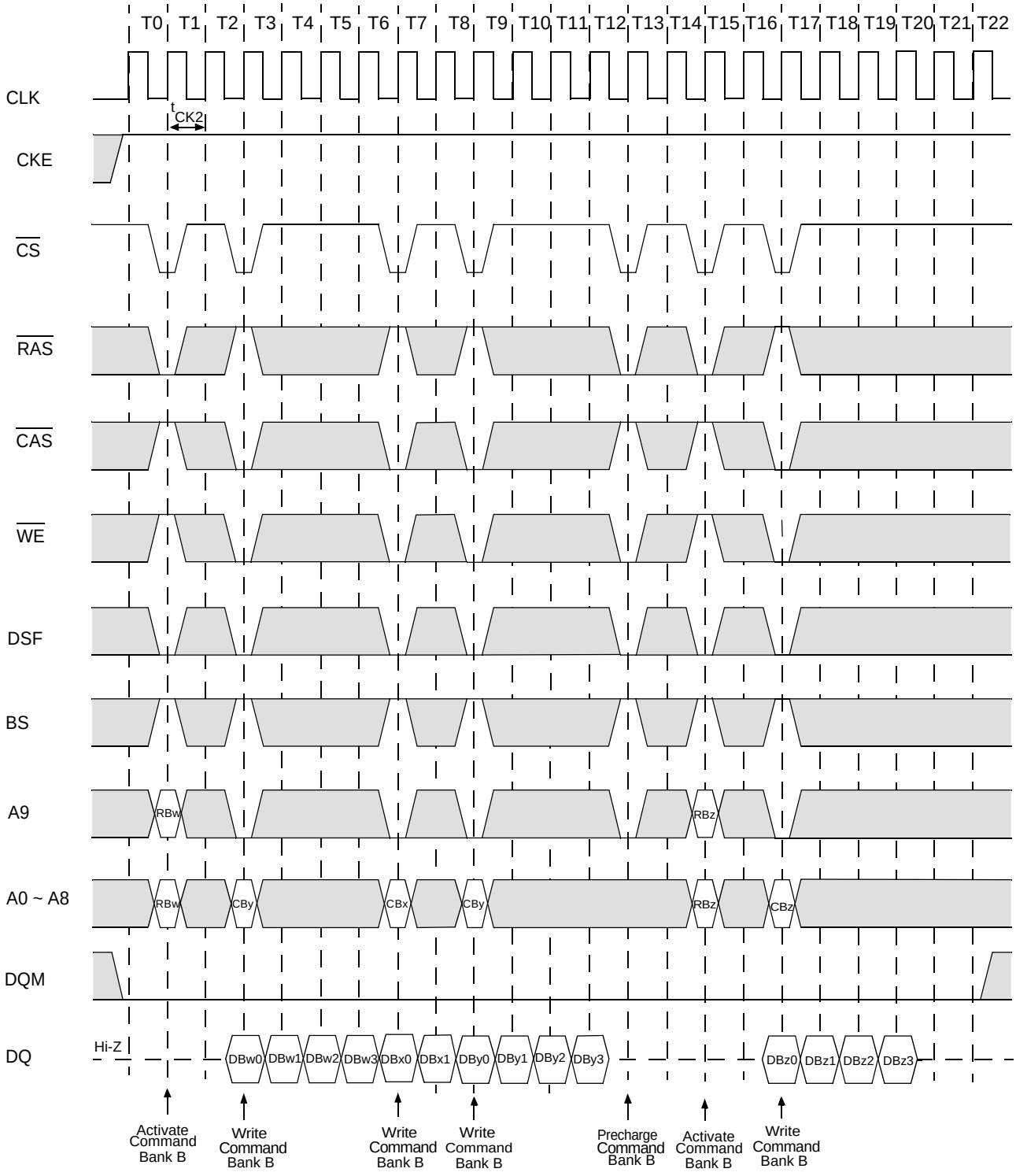


Figure 10.3 Random Column Write (Page within same Bank)
(Burst Length = 4, CAS Latency = 3)

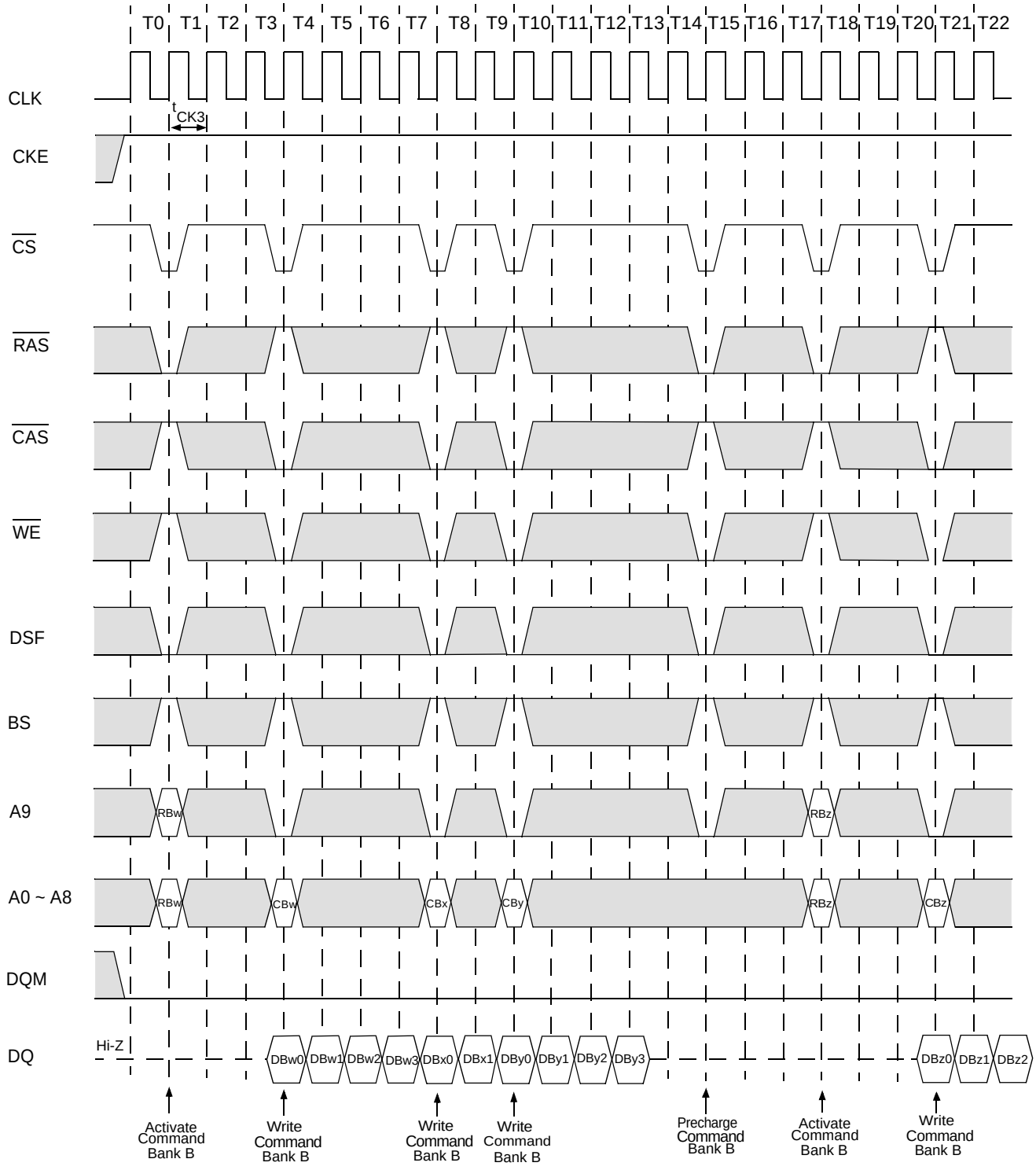


Figure 11.1 Random Row Read (Interleaving Banks)
(Burst Length = 8, CAS Latency = 2)

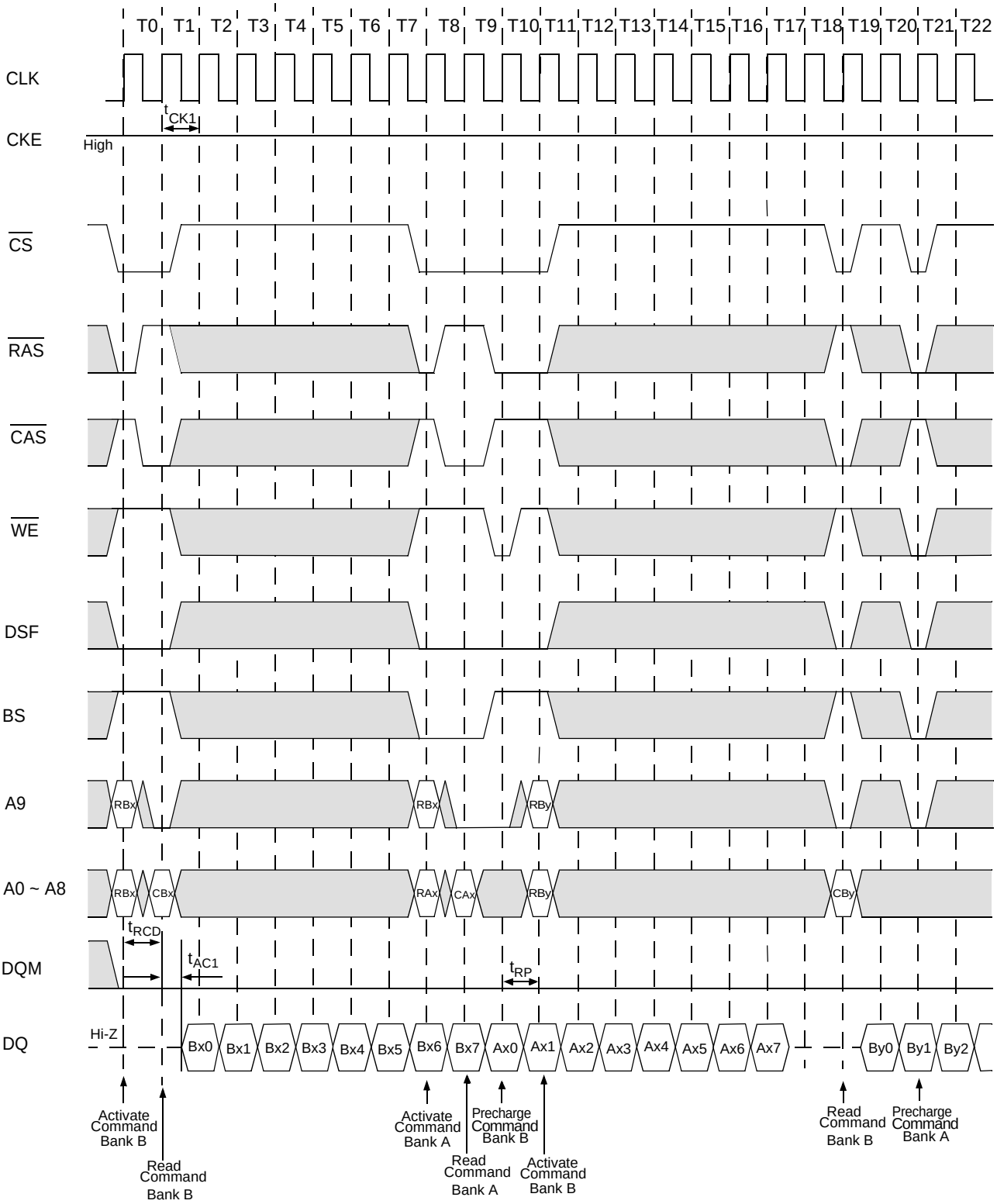


Figure 11.2 Random Row Read (Interleaving Banks)
(Burst Length = 8, CAS Latency = 2)

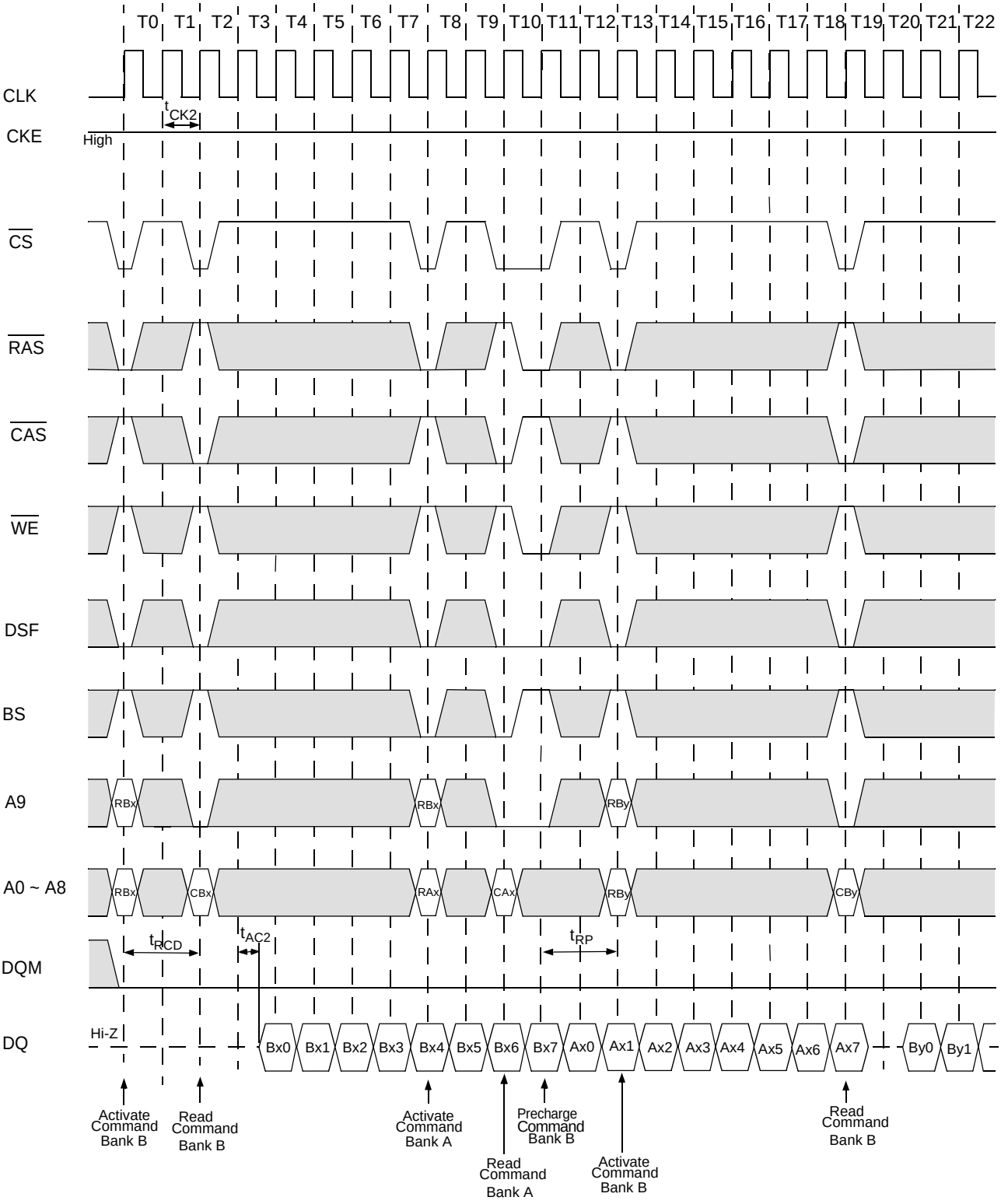


Figure 11.3 Random Row Read (Interleaving Banks)
(Burst Length = 8, CAS Latency = 3)

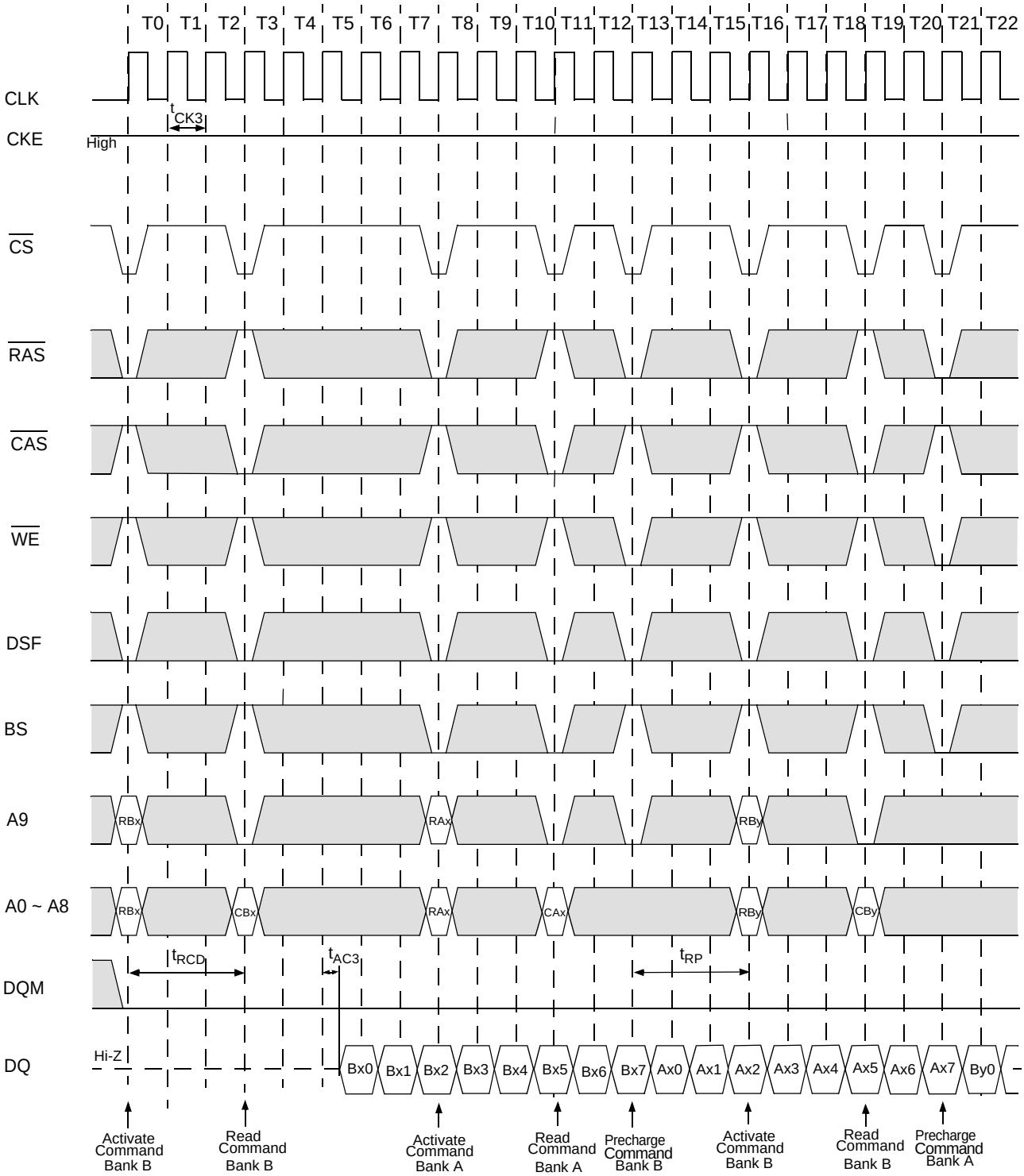


Figure 12.1 Random Row Read (Interleaving Banks)
(Burst Length = 8, CAS Latency = 1)

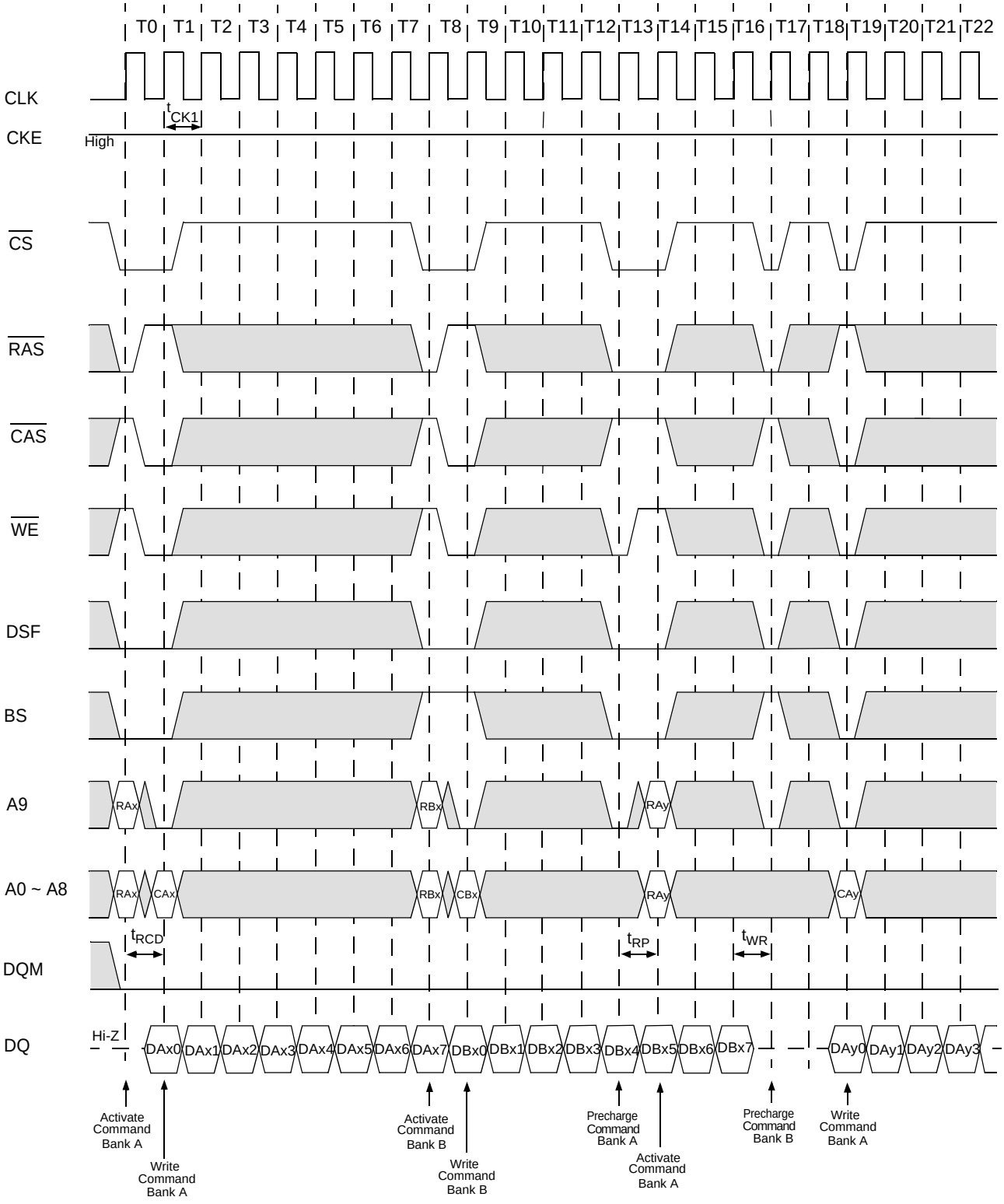
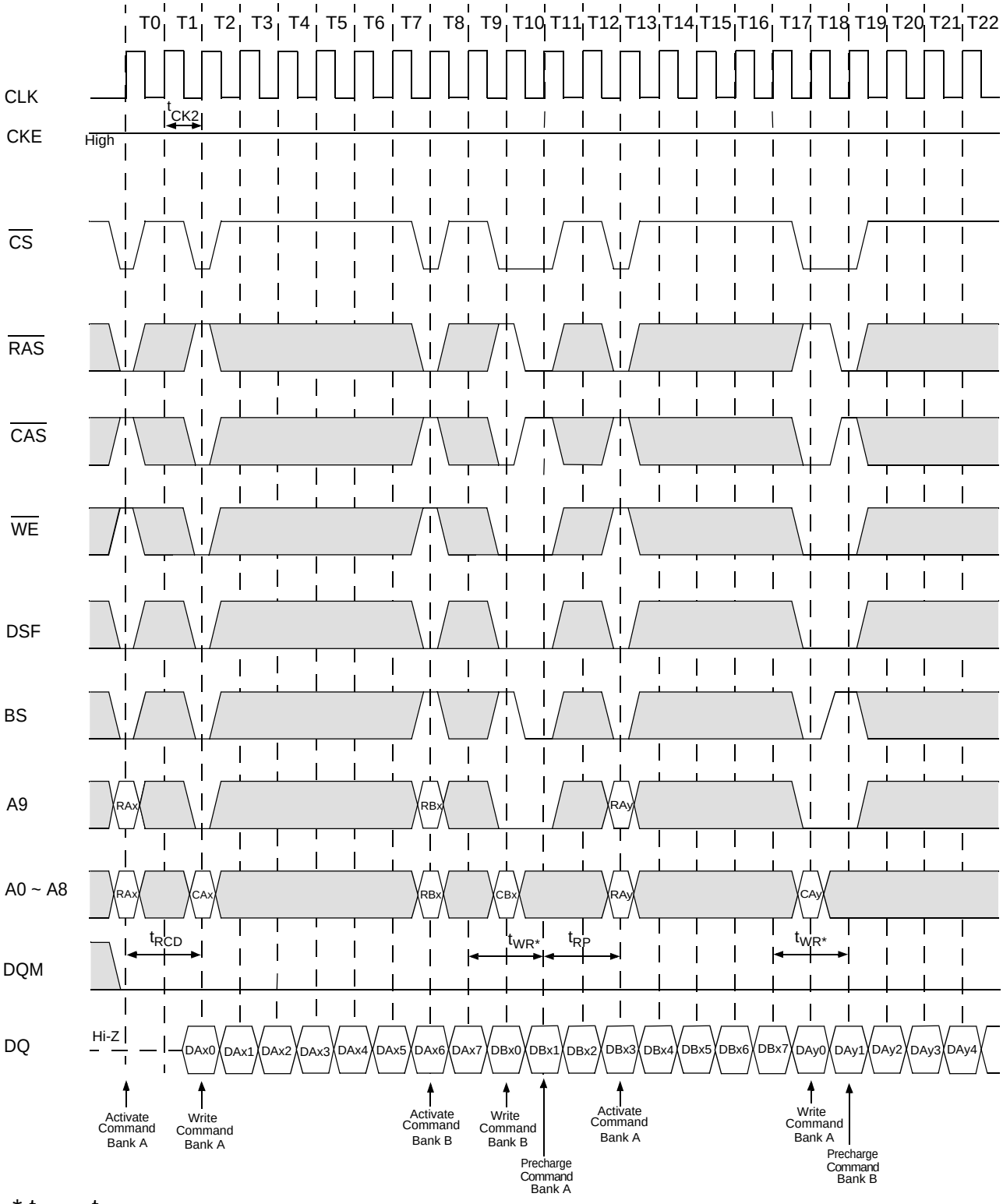
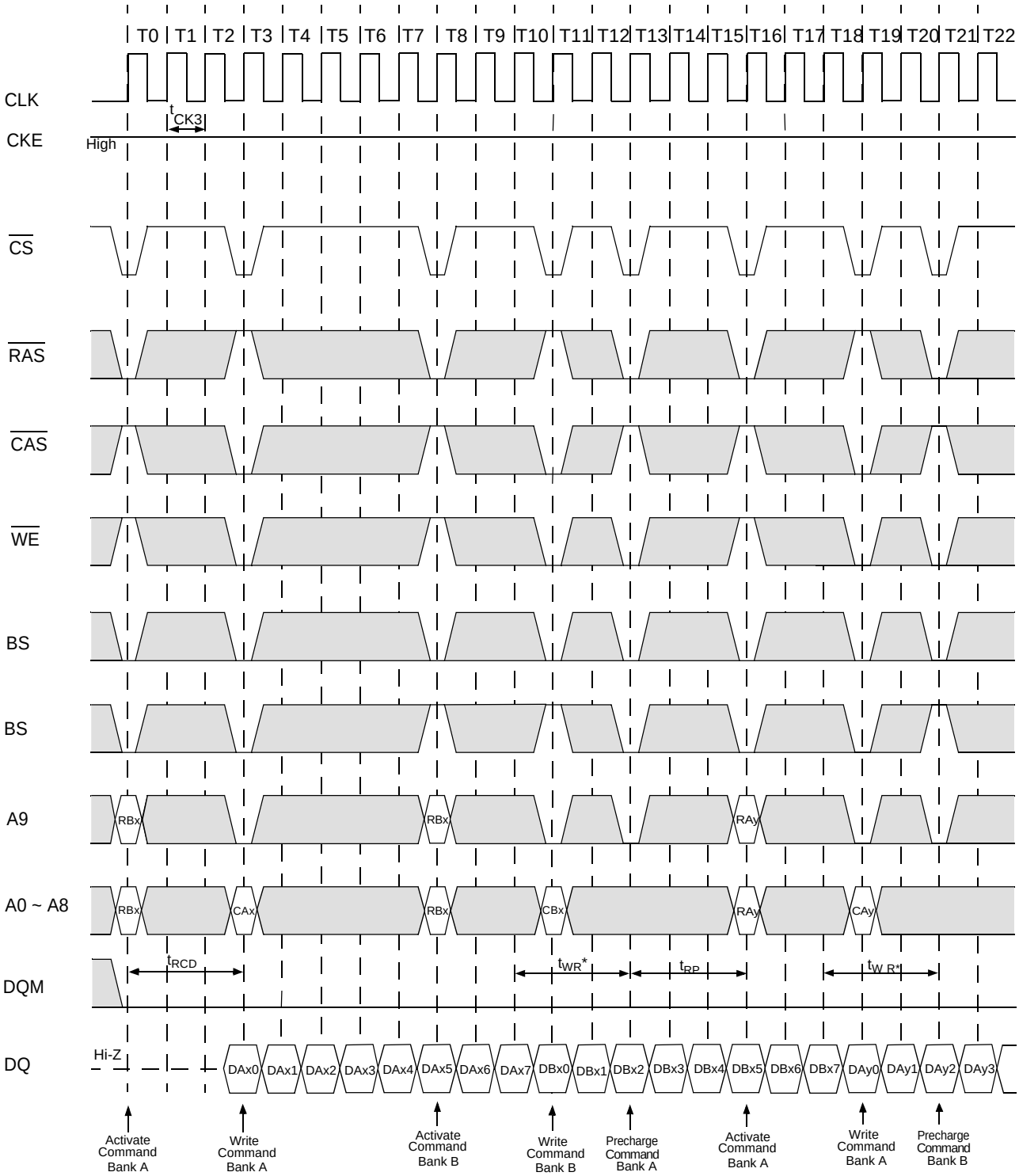


Figure 12.2 Random Row Write (Interleaving Banks)
(Brust Length = 4, CAS Latency = 2)



* $t_{WR} > t_{WR(min.)}$

Figure 12.3 Random Row Write (Interleaving Banks)
(Burst Length = 8, CAS Latency = 3)



*t_{WR} > t_{WR} (min)

Figure 13.1 Read and Write Cycle (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 1)

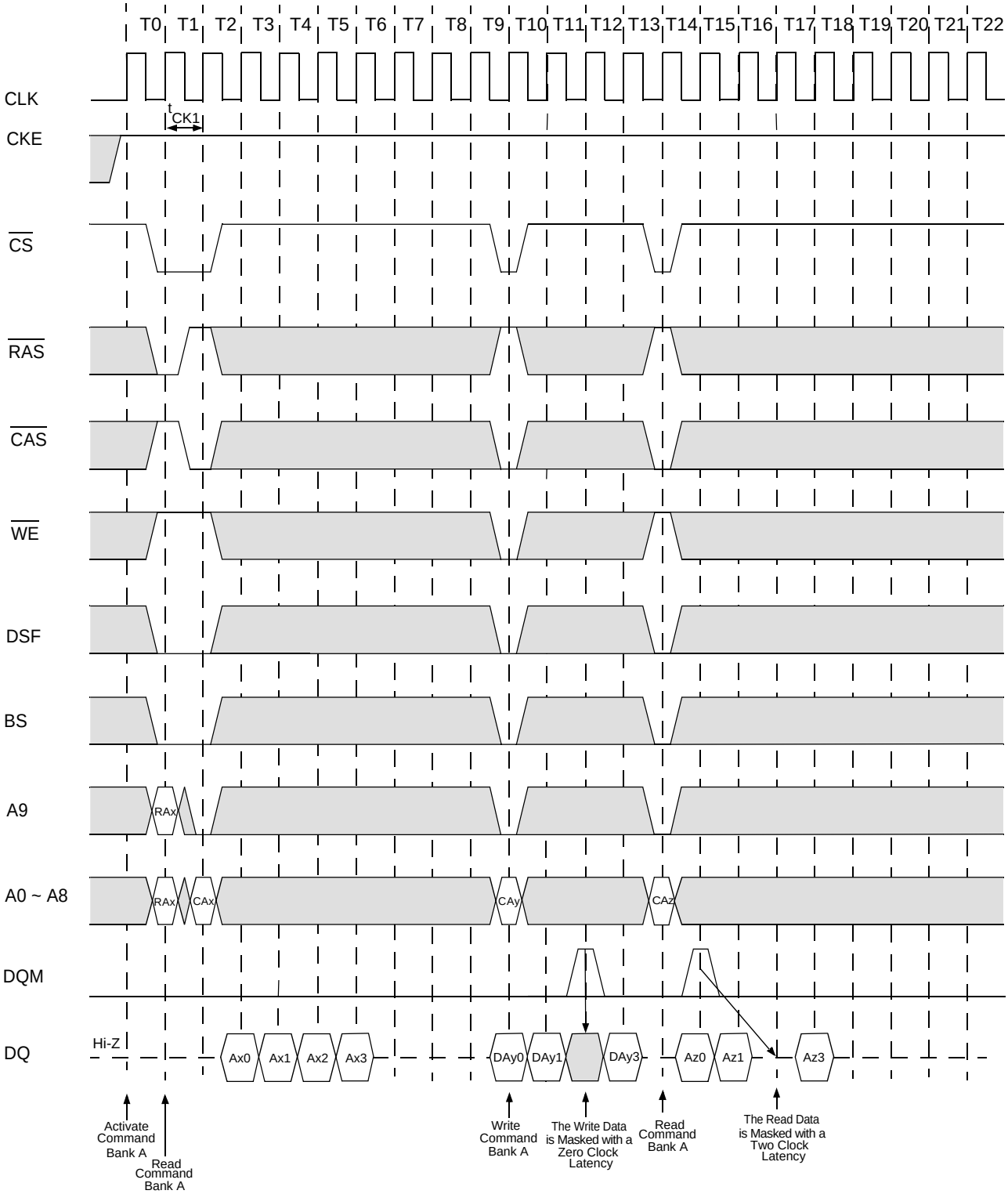


Figure 13.2 Read and Write Cycle (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2)

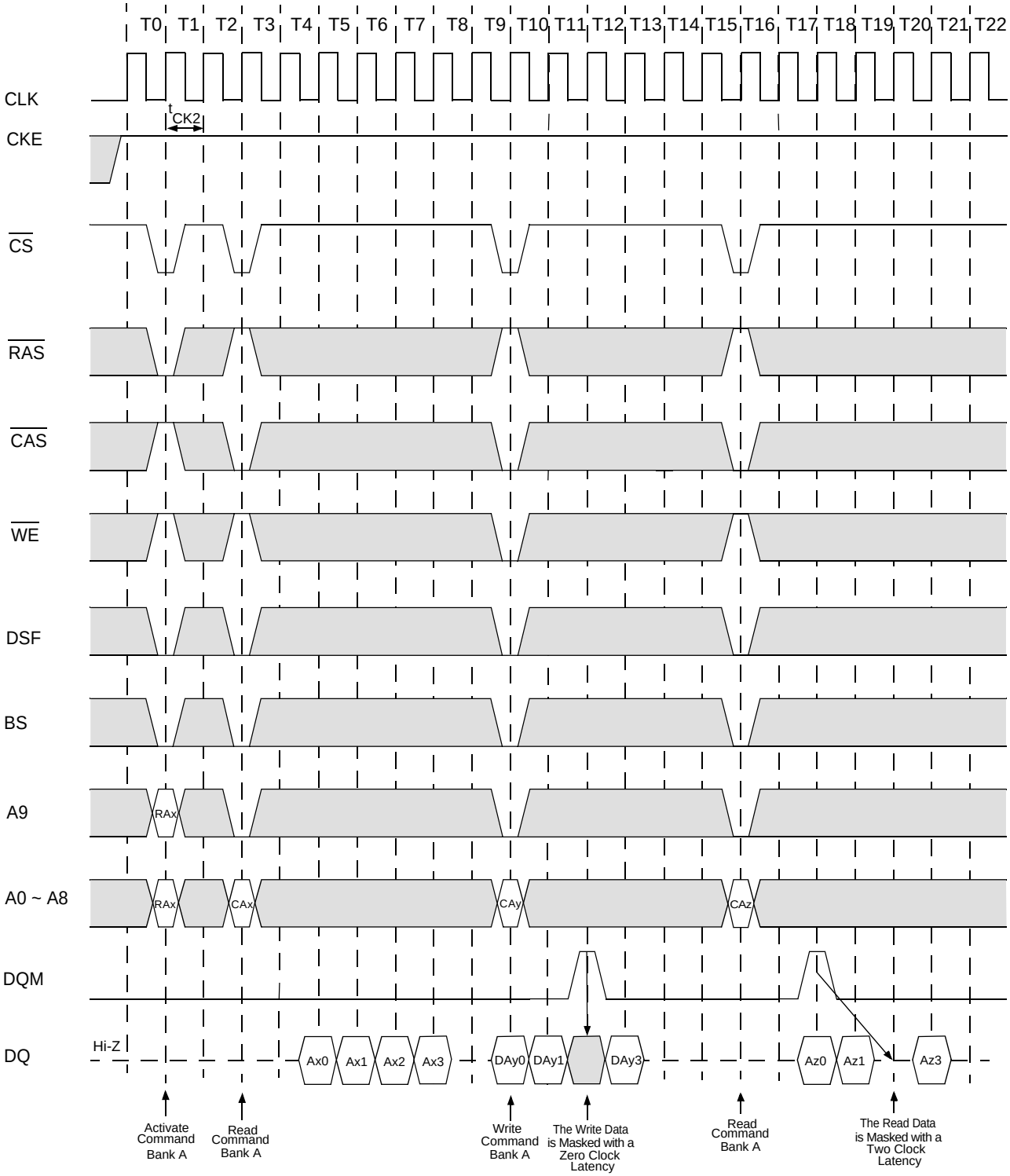


Figure 13.3 Read and Write Cycle (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3)

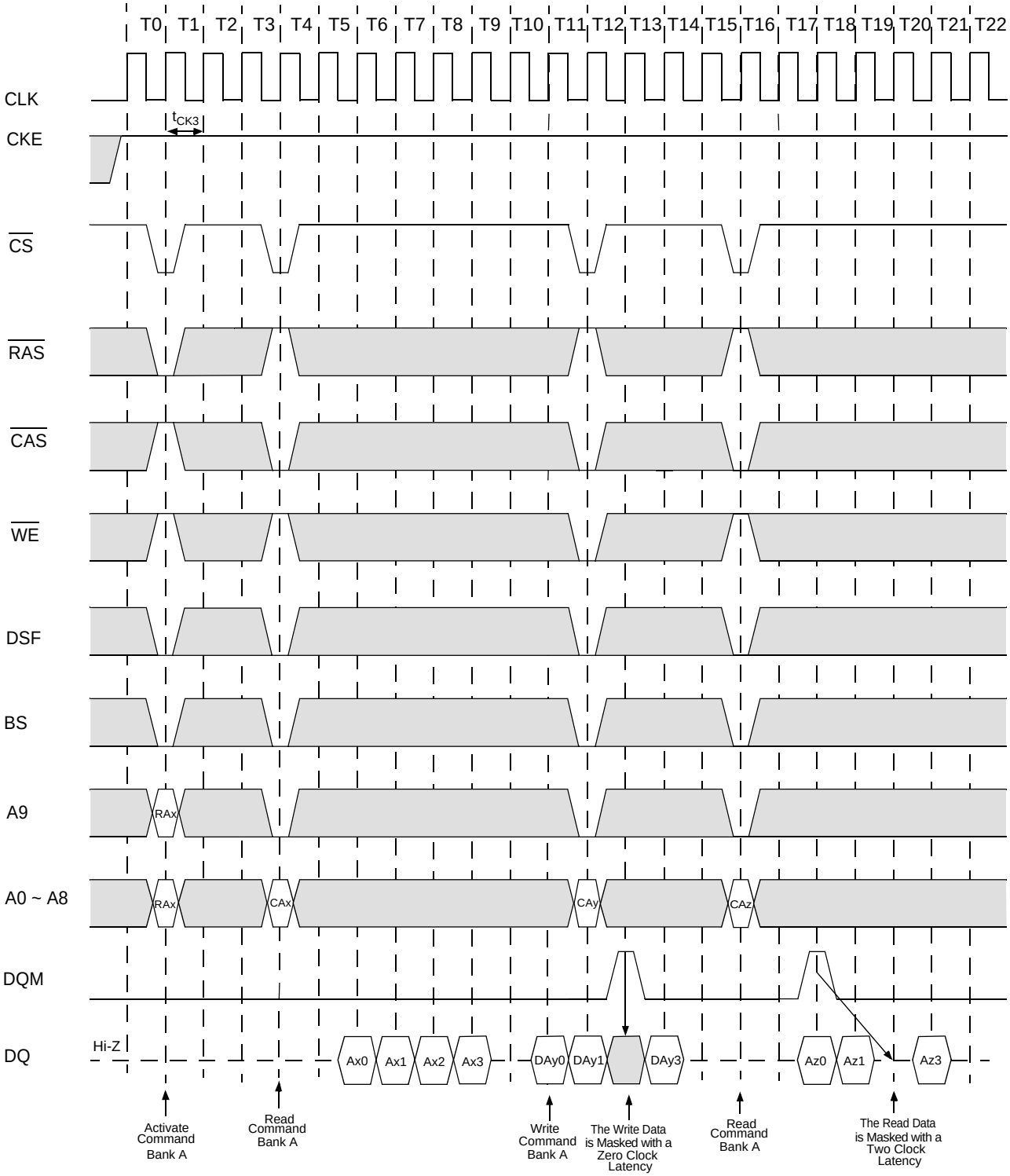


Figure 14.1 Interleaving Column Read Cycle (Burst Length = 4, CAS Latency = 1)

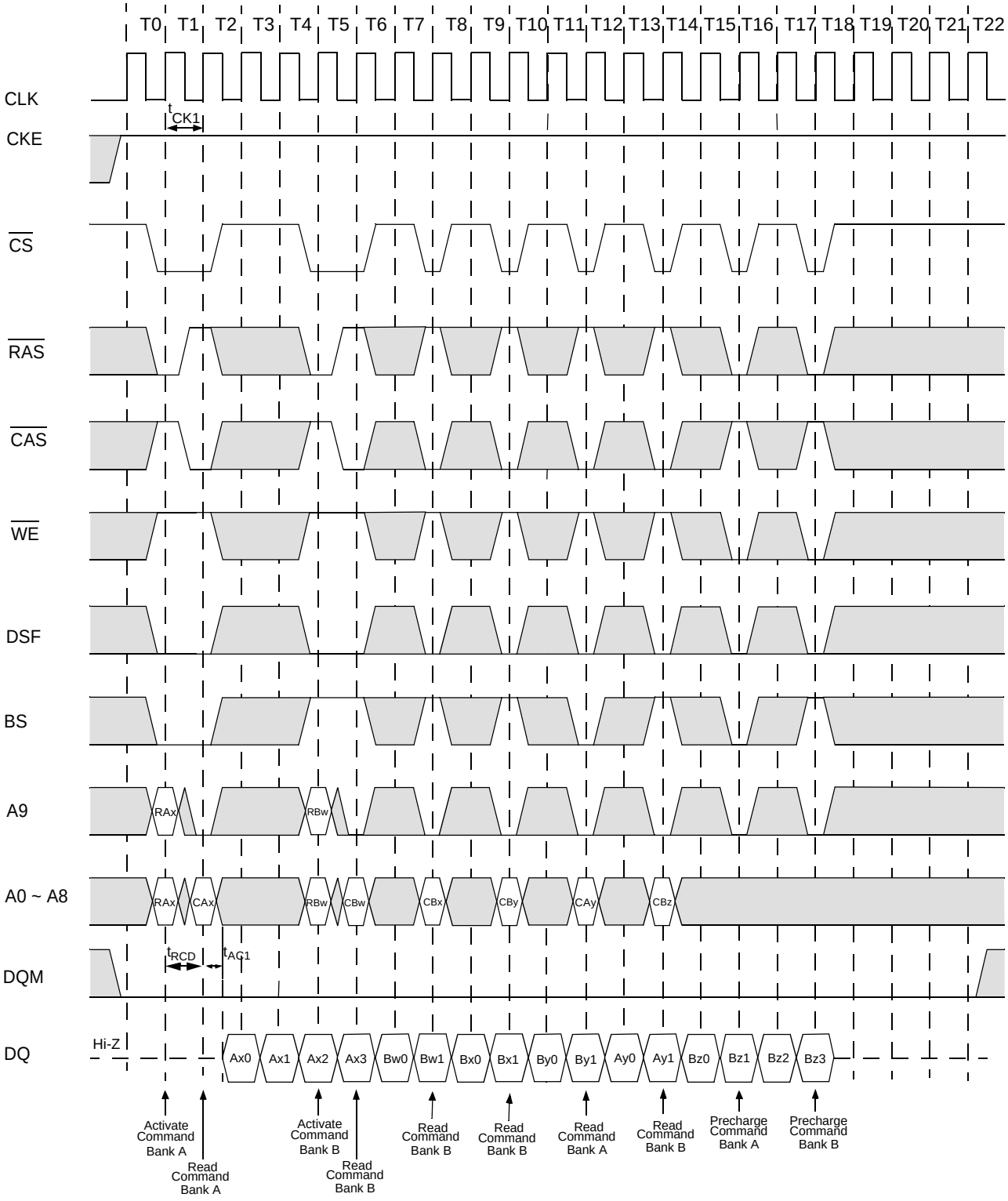


Figure 14.2 Interleaving Column Read Cycle
(Burst Length = 4, CAS Latency = 2)

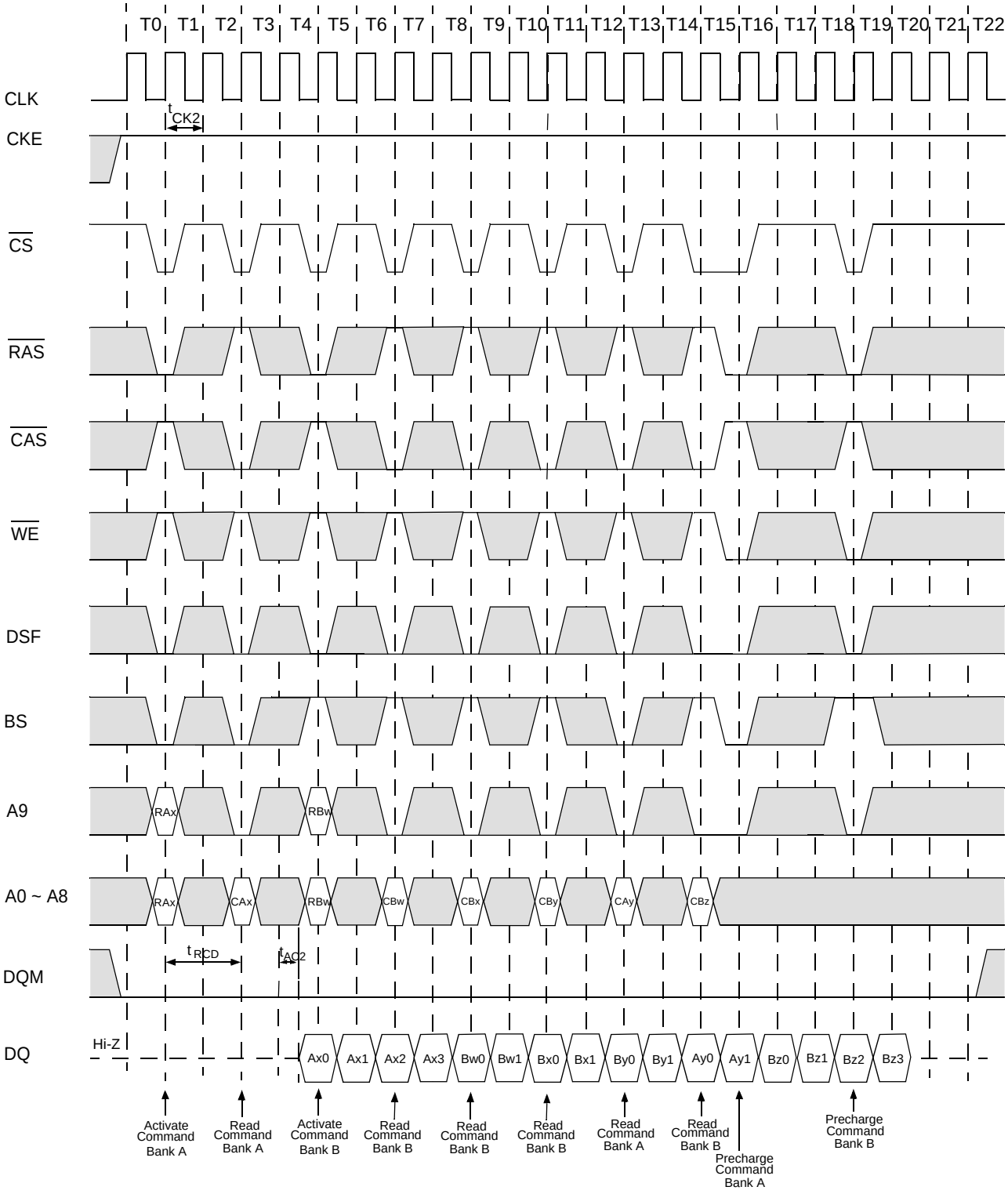


Figure 14.3. Interleaved Column Read Cycle (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3)

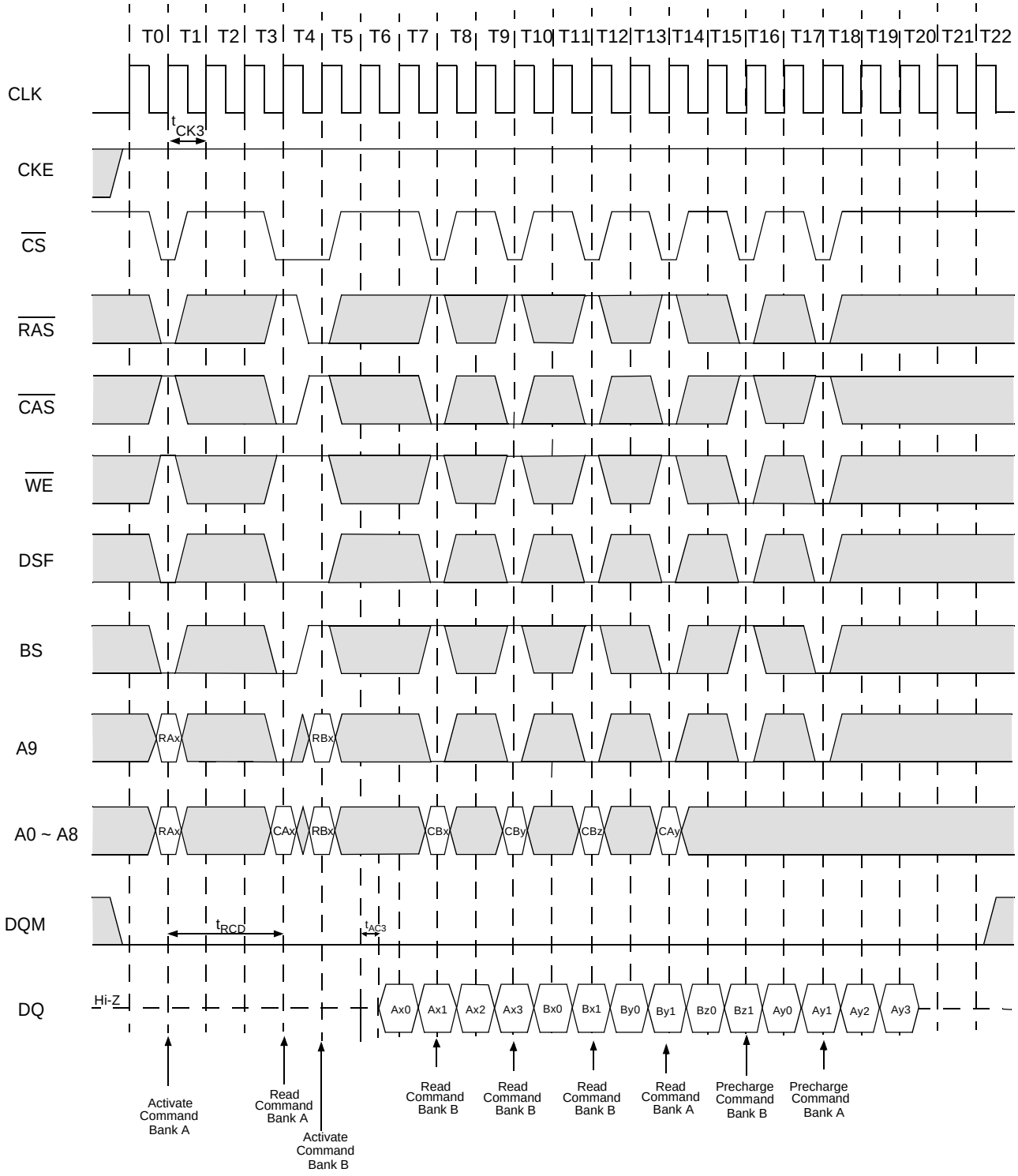


Figure 15.1. Interleaved Column Write Cycle (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 1)

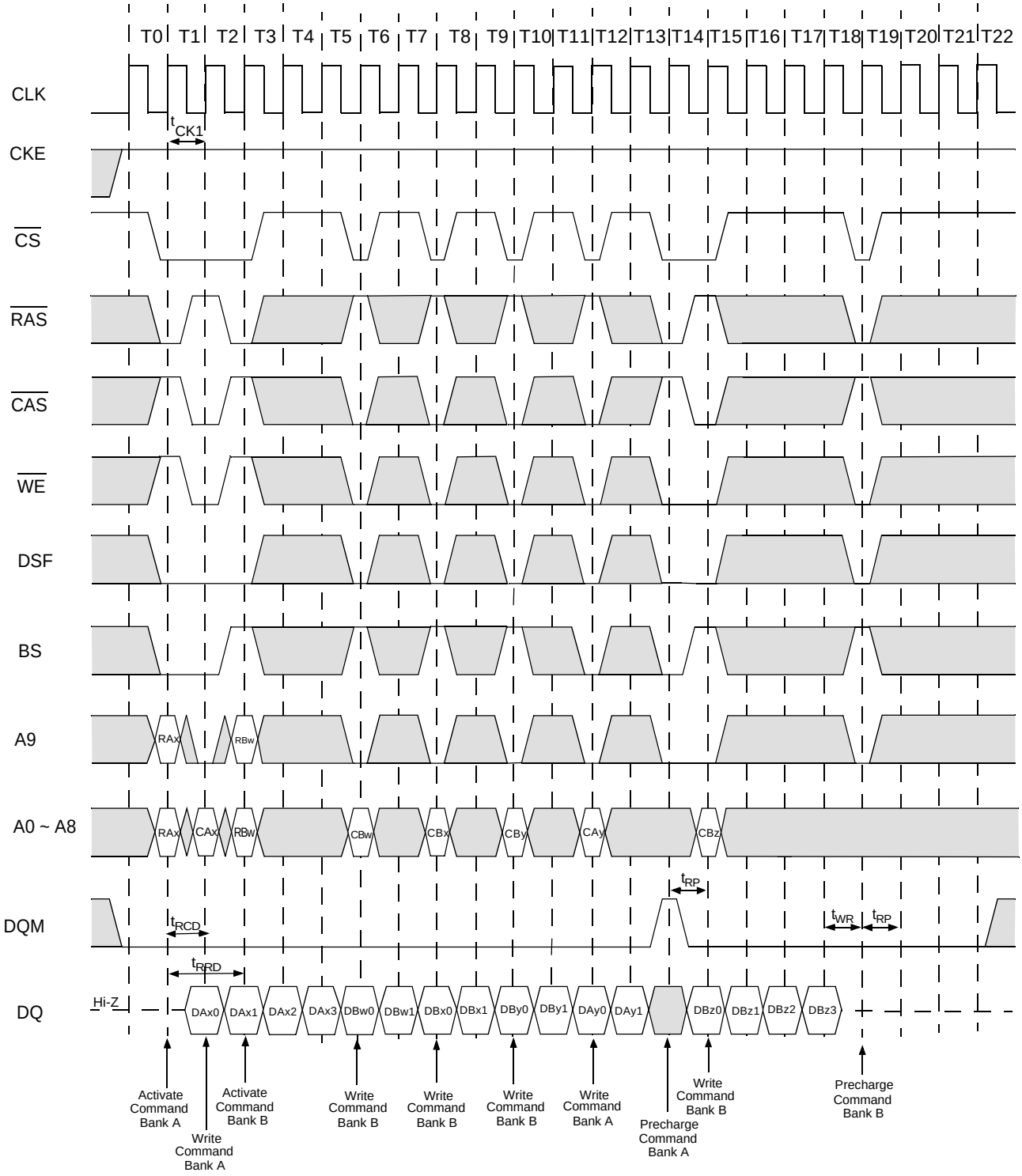


Figure 15.2. Interleaved Column Write Cycle (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2)

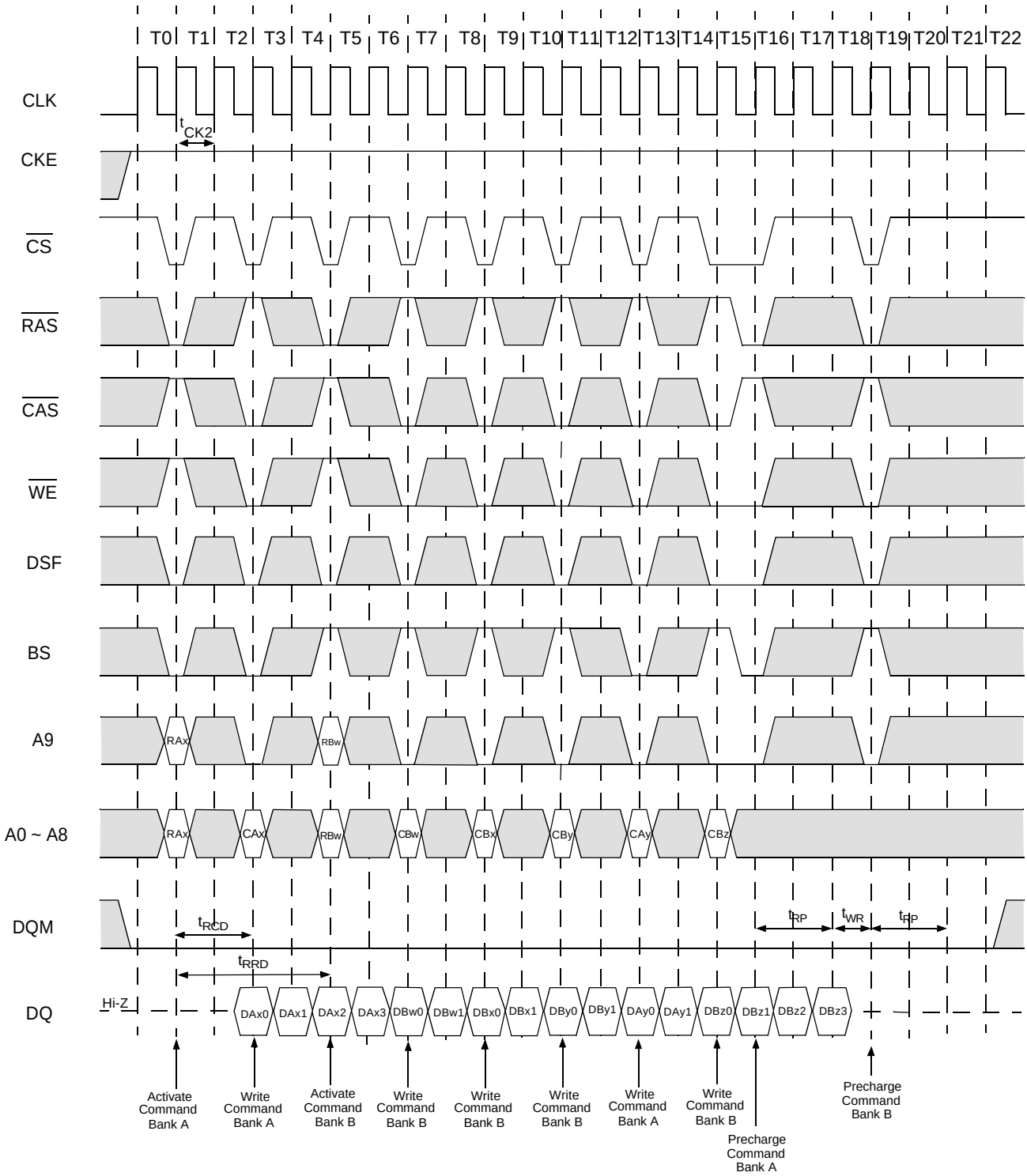


Figure 15.3. Interleaved Column Write Cycle (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3)

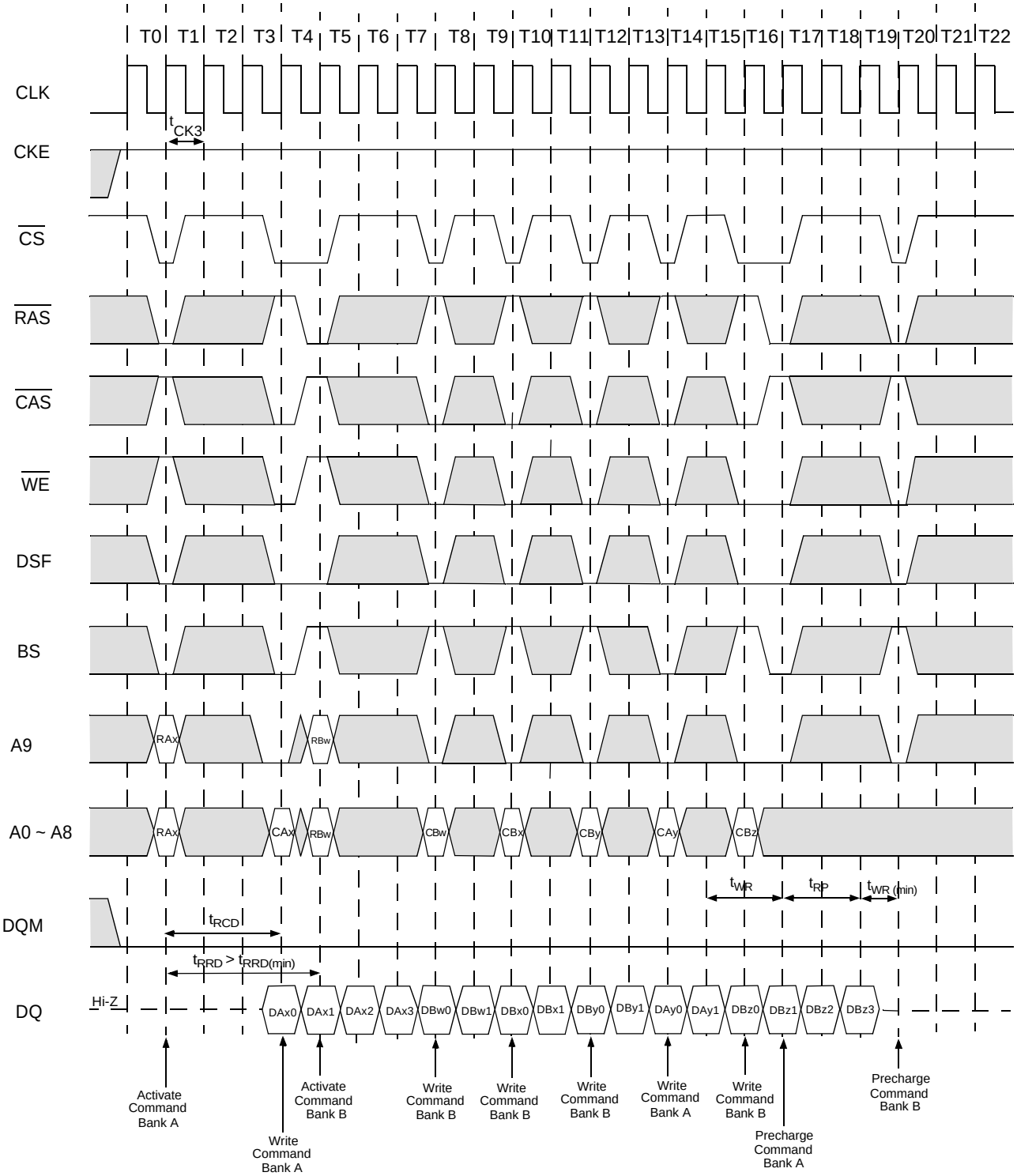


Figure 16.1. Auto Precharge after Read Burst (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 1)

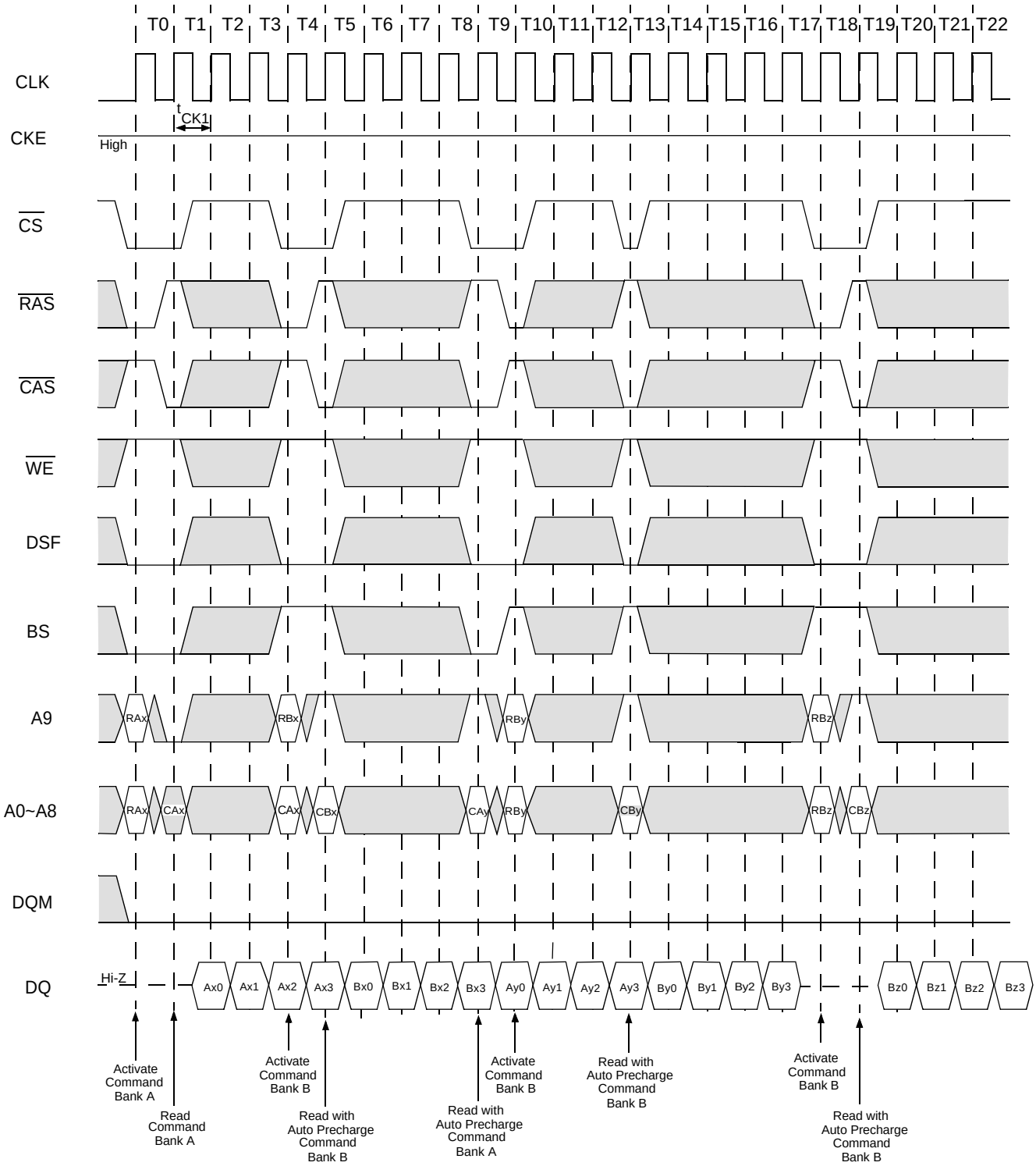


Figure 16.2 Auto Precharge after Read Burst (Burst Length = 4, $\overline{CAS}$ Latency = 2)

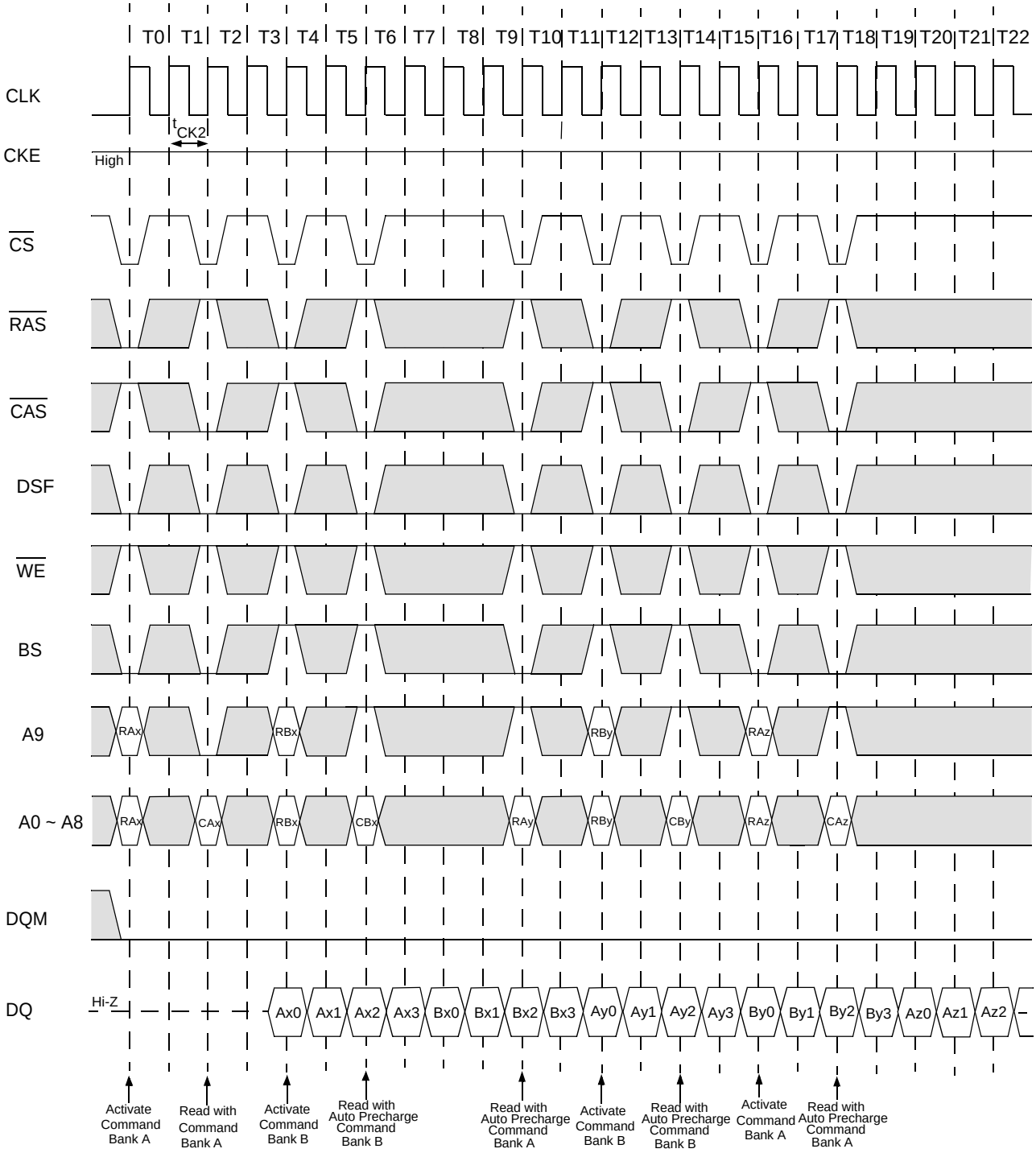


Figure 16.3 Auto Precharge after Read Burst (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3)

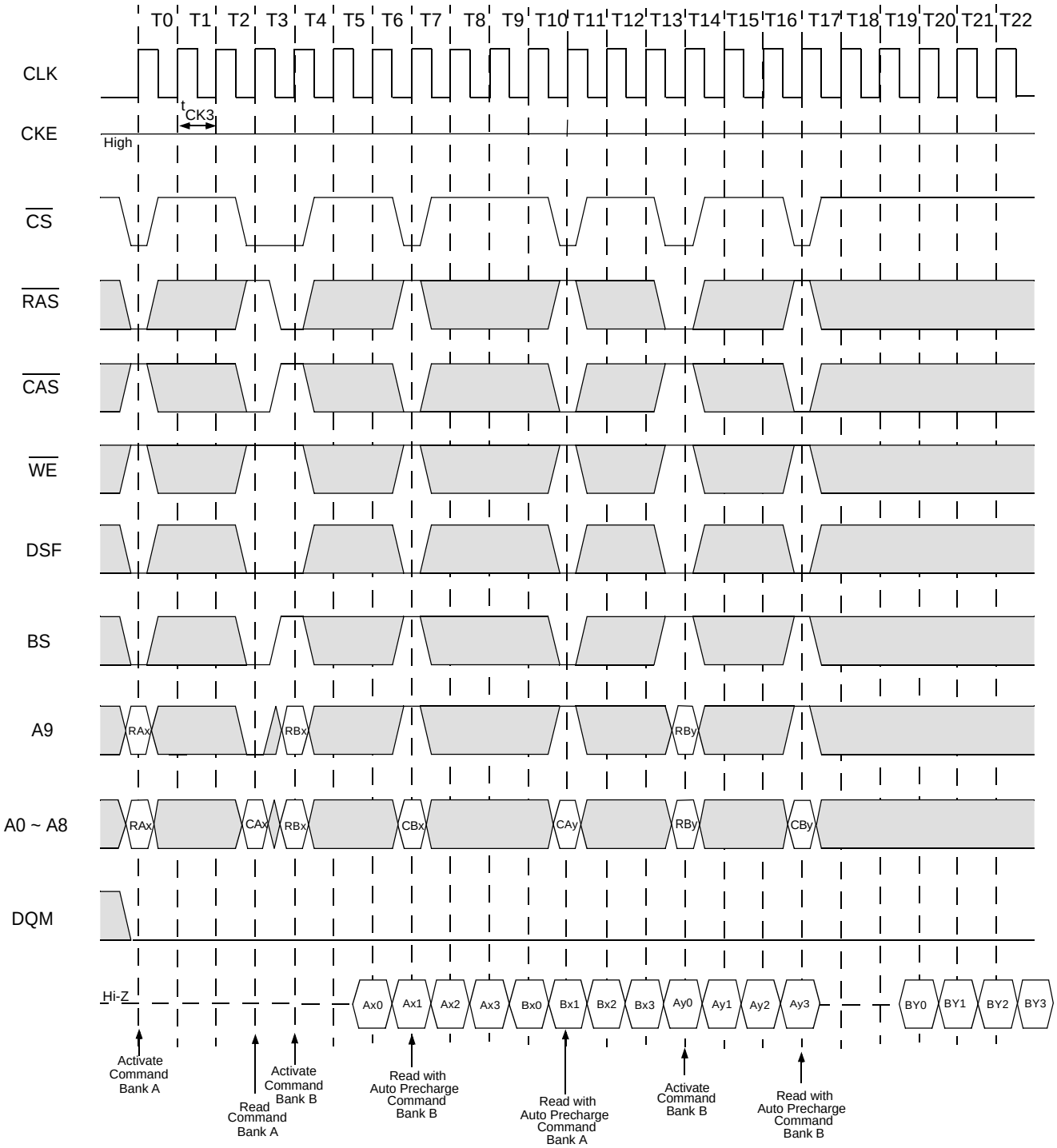


Figure 17.1 Auto Precharge after Write Burst (Burst Length = 4, $\overline{CAS}$ Latency = 1)

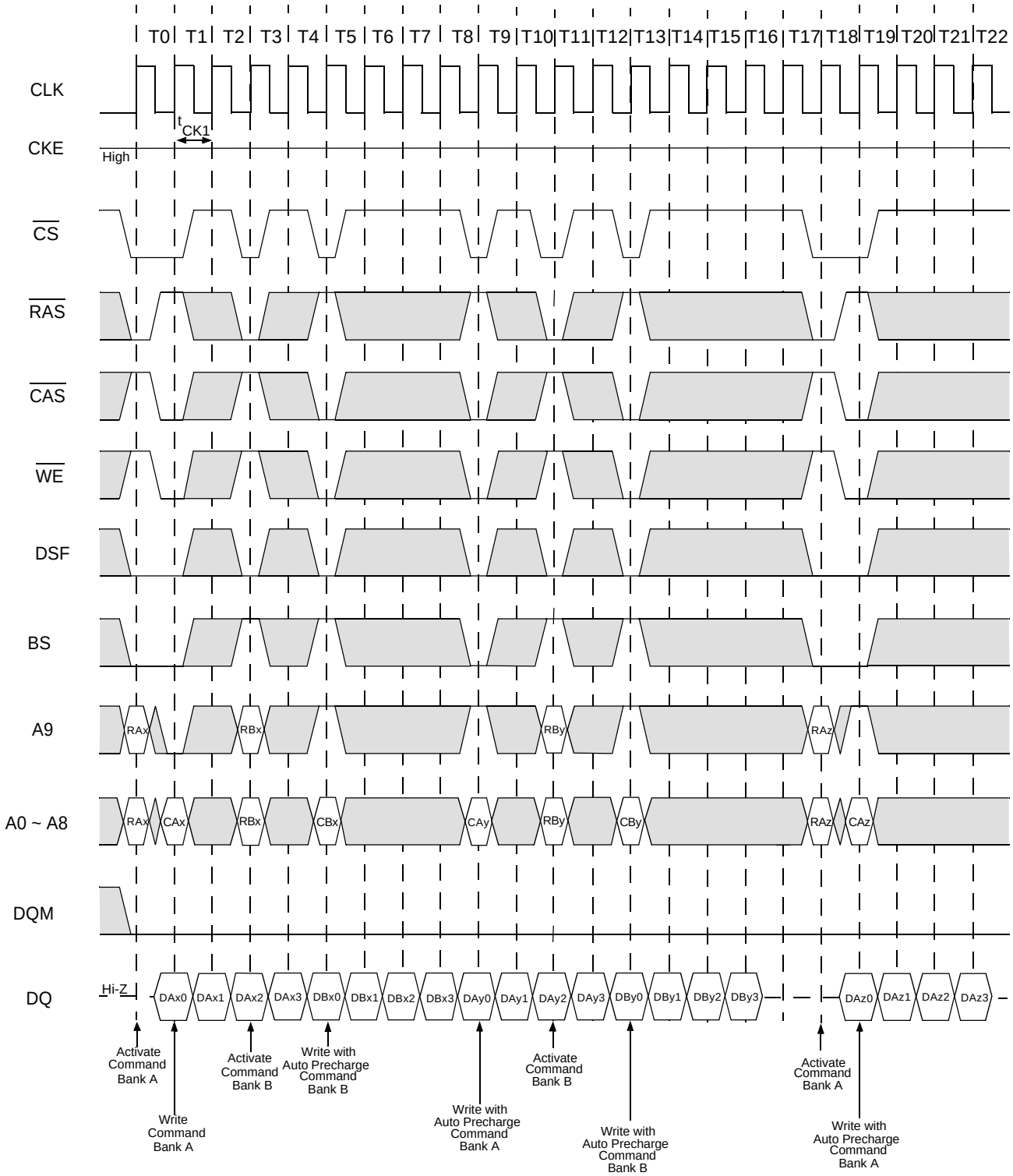


Figure 17.2. Auto Precharge after Write Burst (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2)

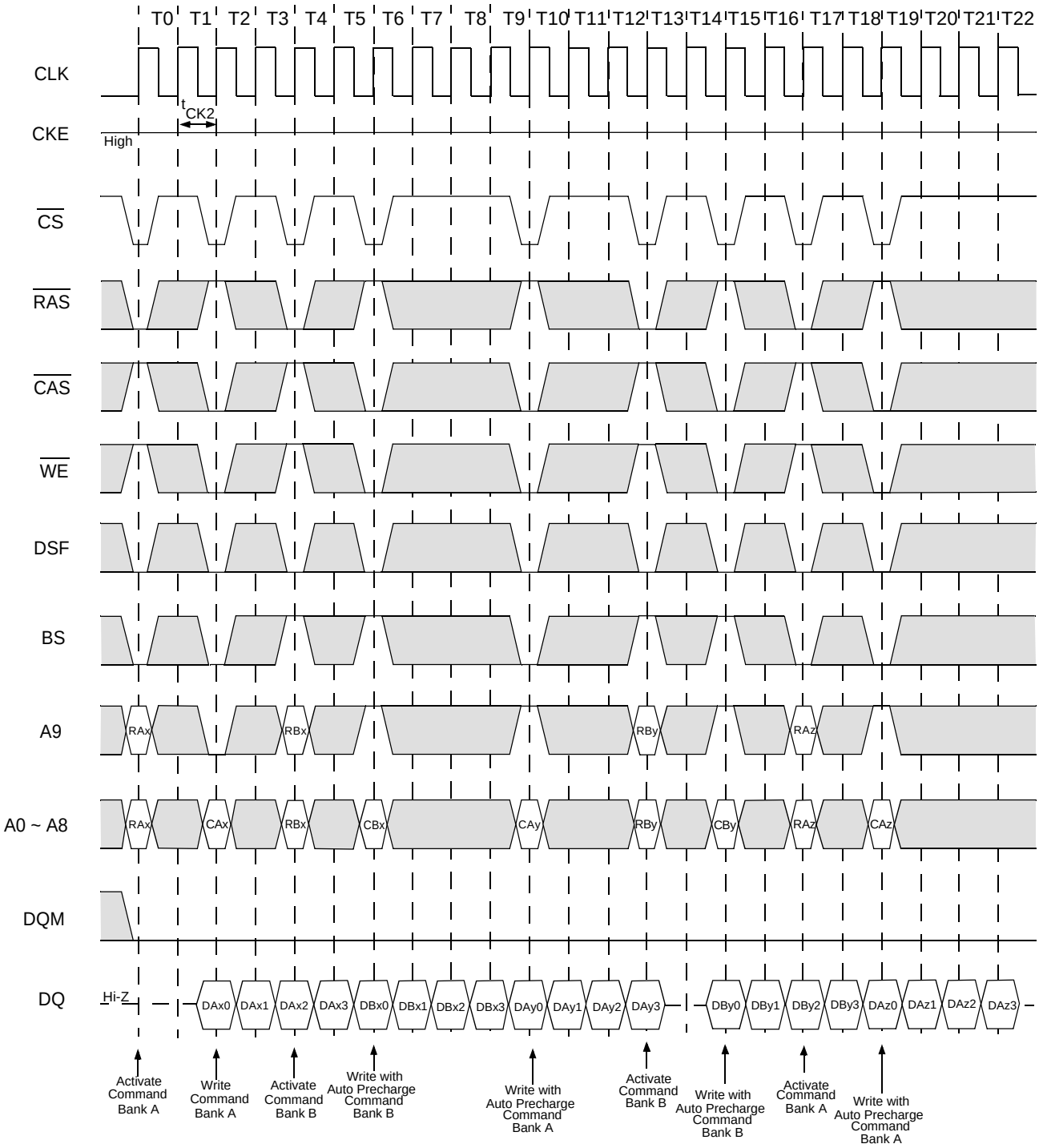


Figure 17.3. Auto Precharge after Write Burst (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 3)

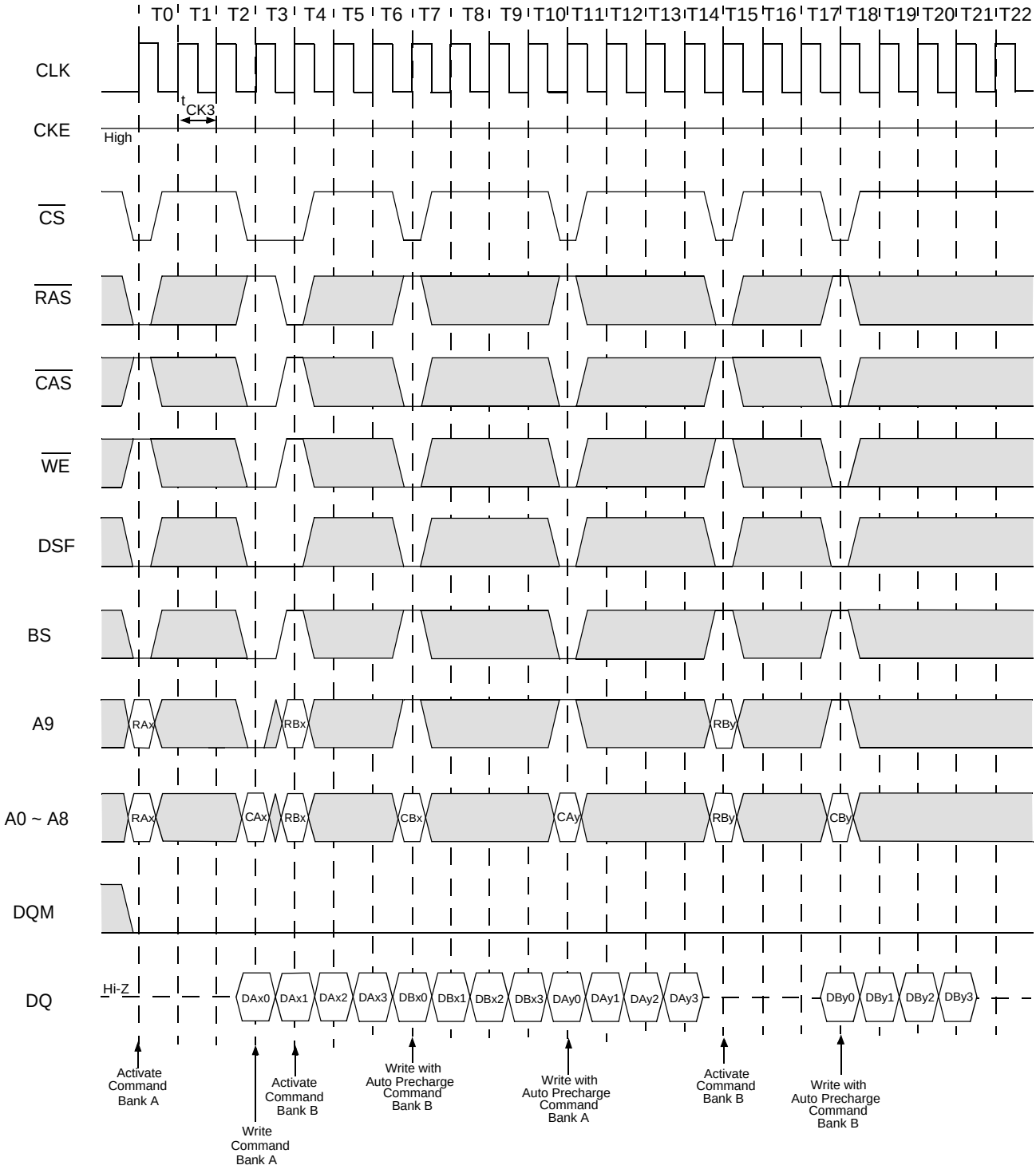


Figure 18.1. Full Page Read Cycle (Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 1)

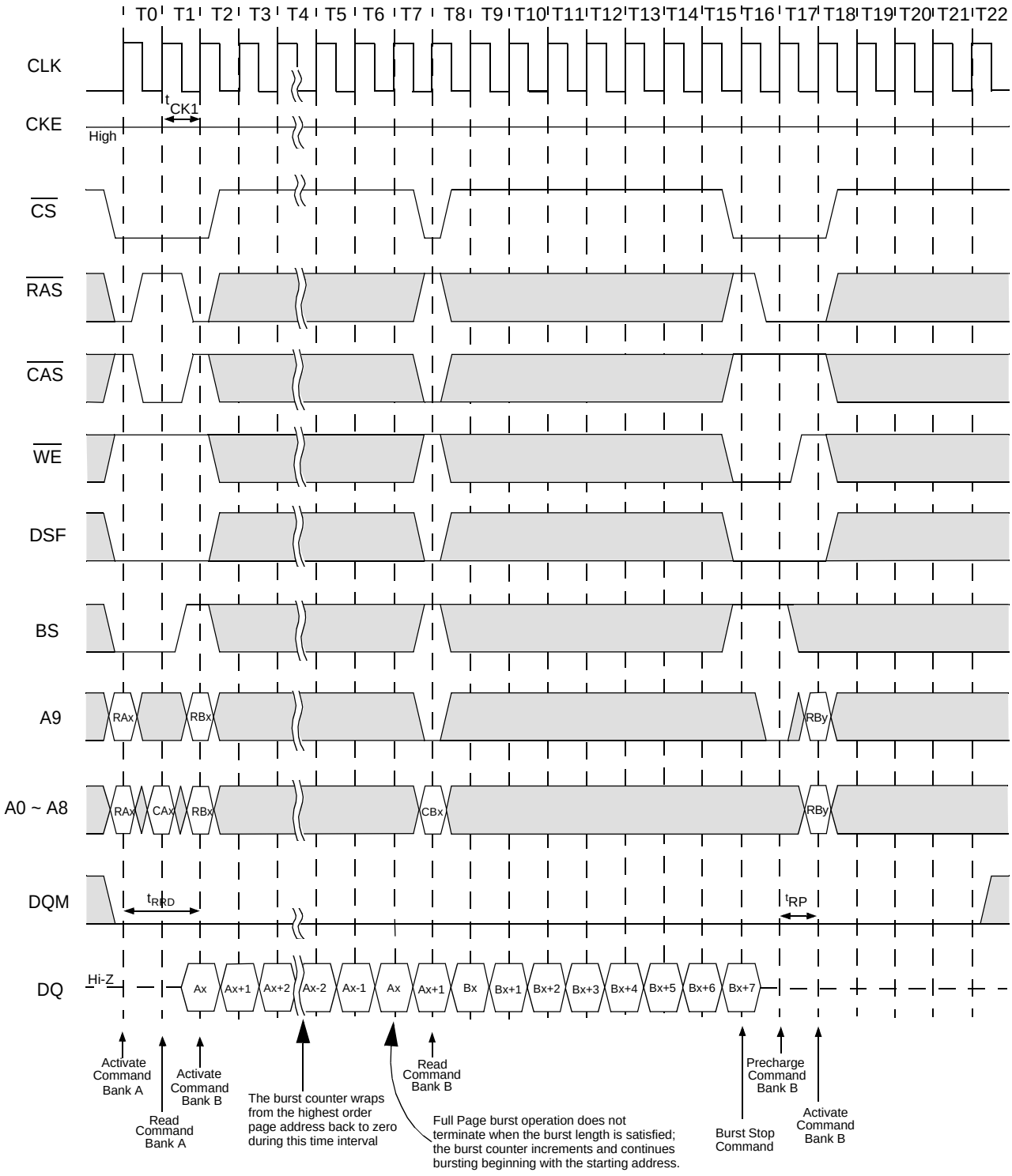


Figure 18.2. Full Page Read Cycle (Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2)

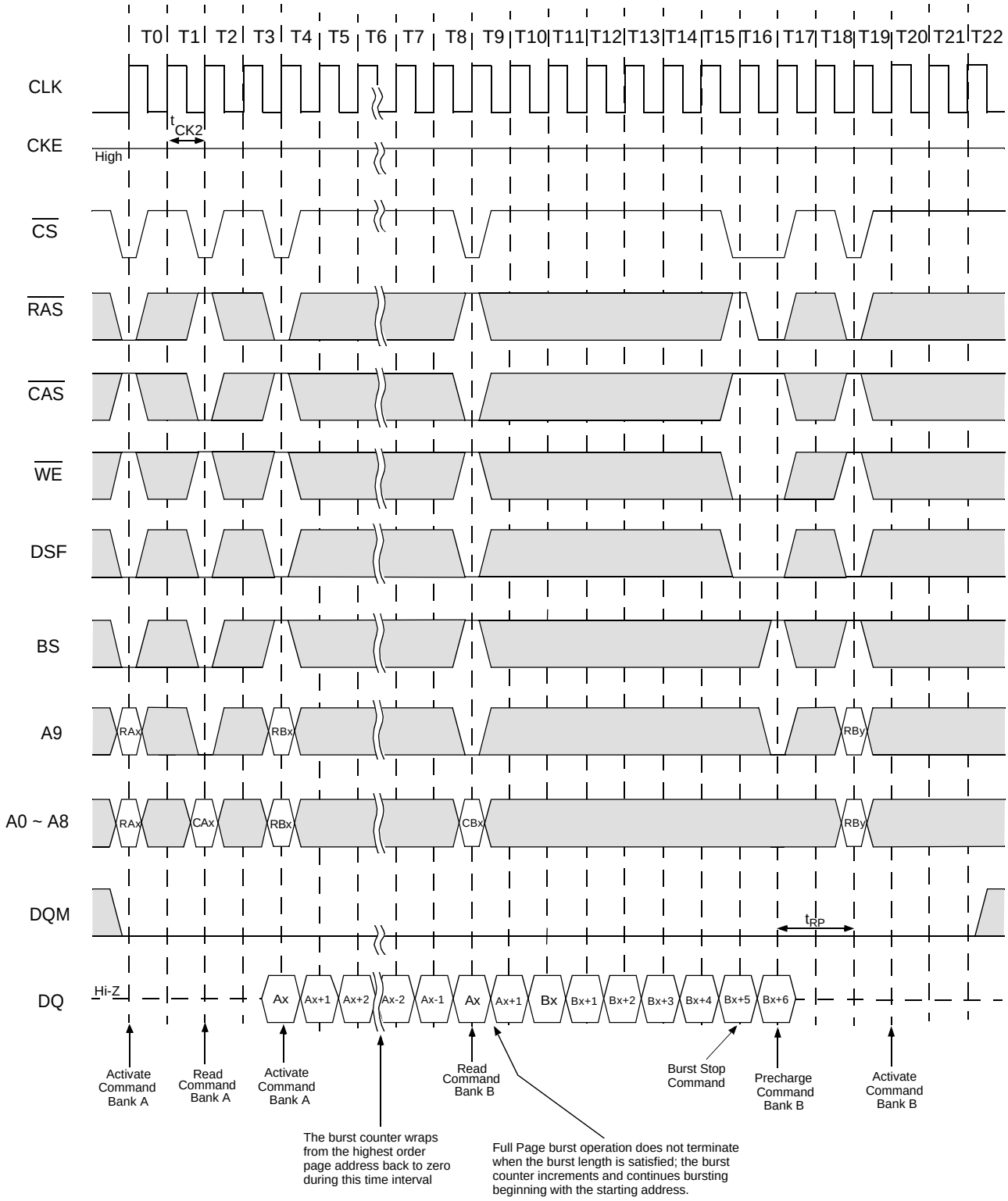


Figure 18.3. Full Page Read Cycle (Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 3)

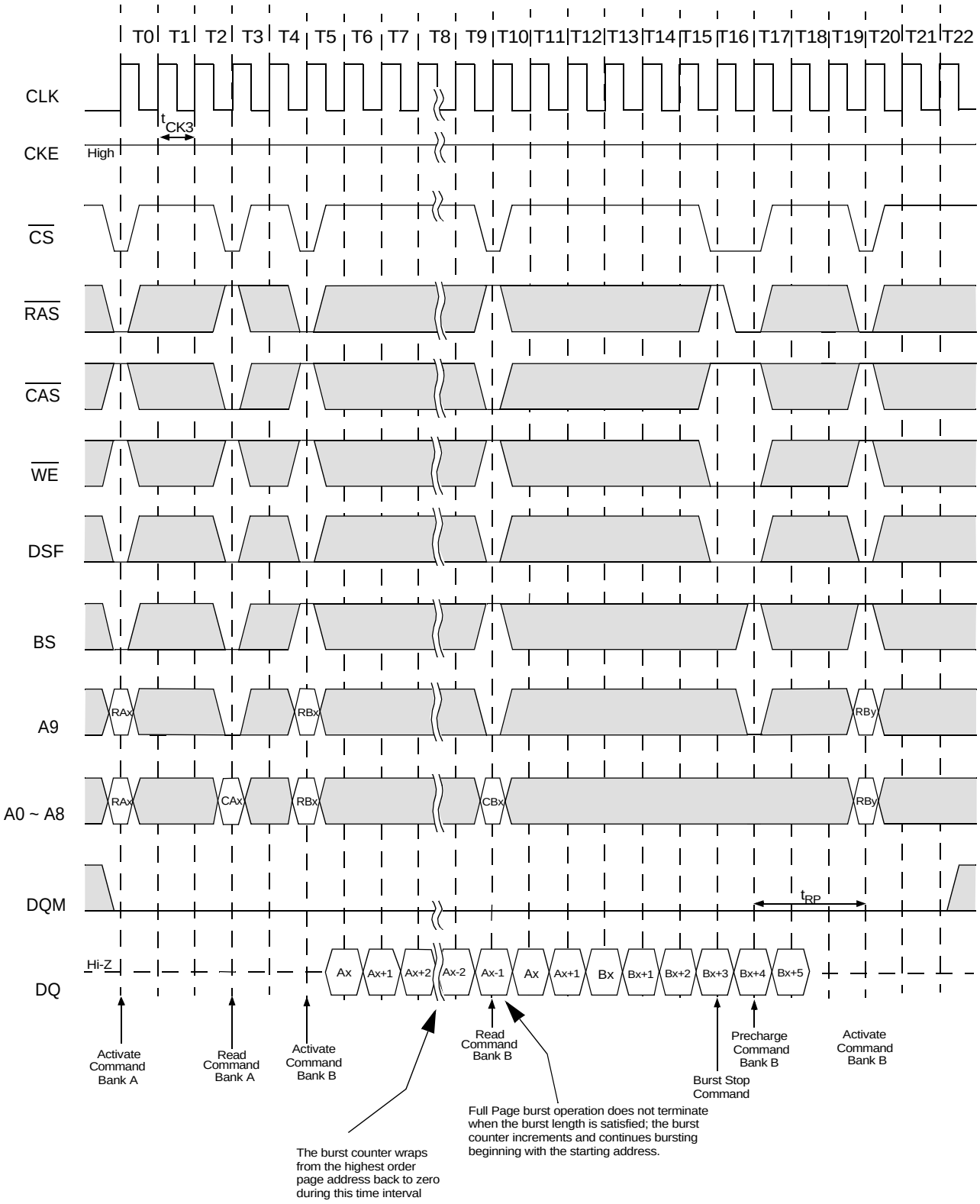


Figure 19.1 Full Page Write Cycle (Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 1)

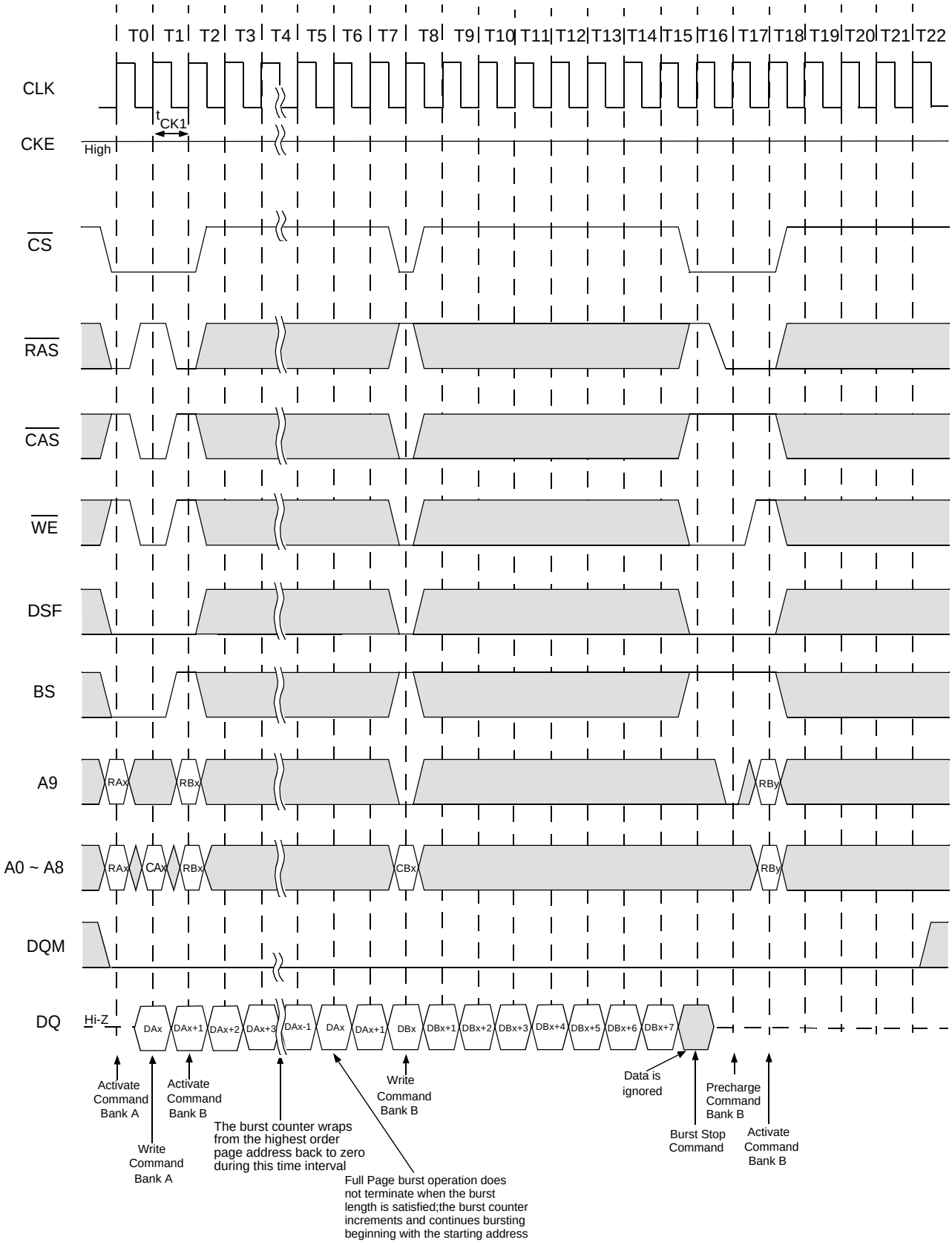


Figure 19.2 Full Page Write Cycle (Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2)

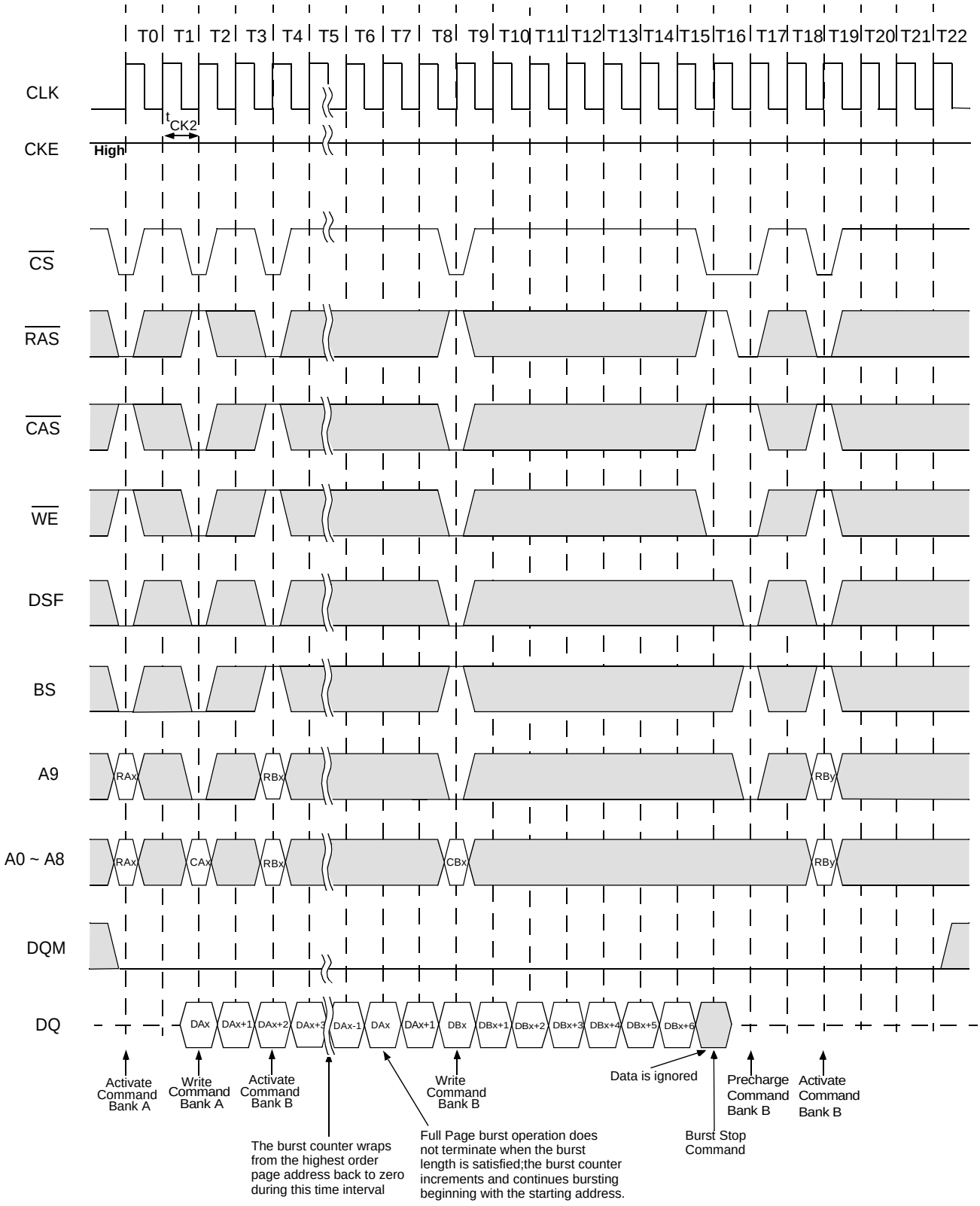


Figure19.3 Full Page Write Cycle (Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 3)

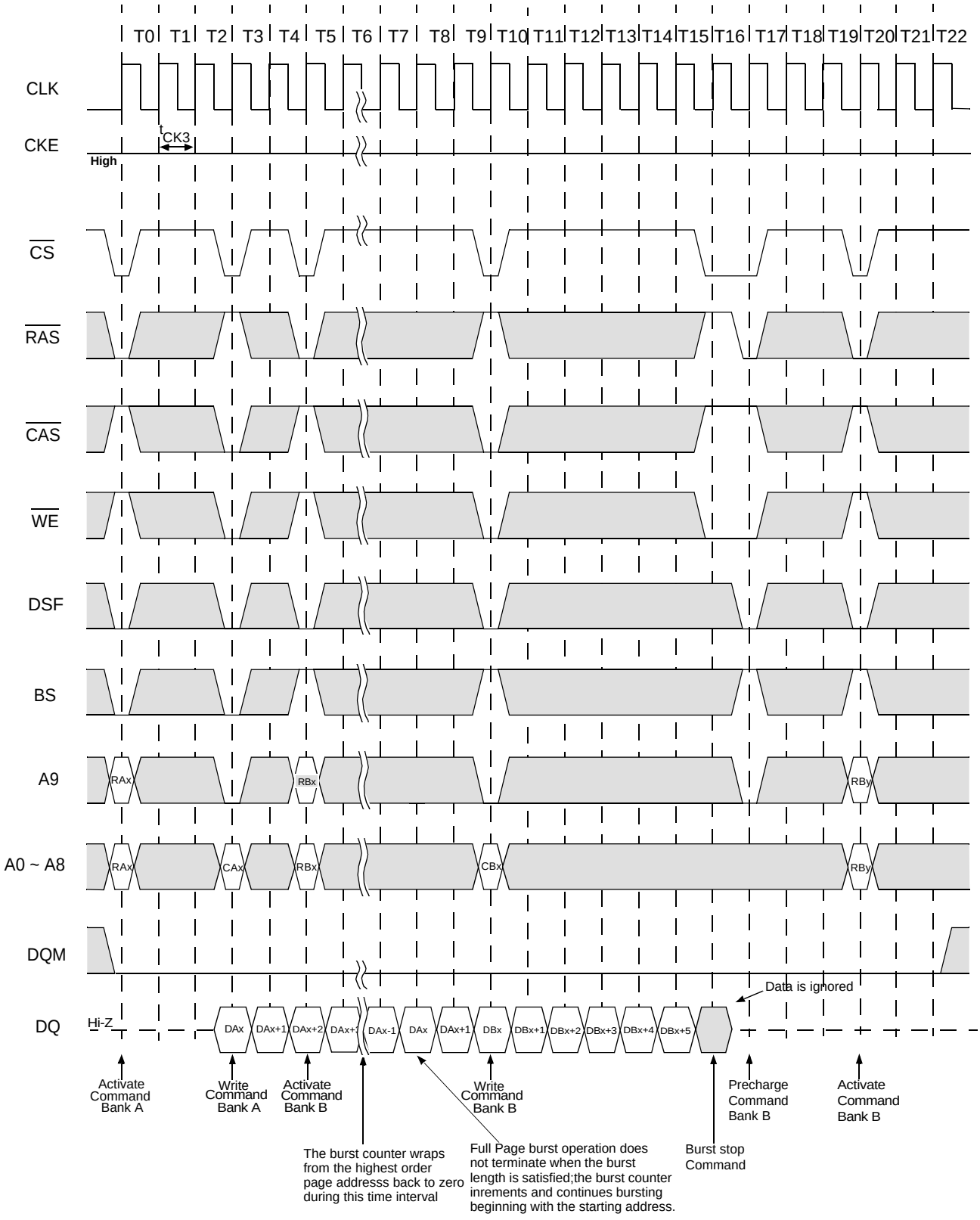


Figure 20. Byte Write Operation (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2)

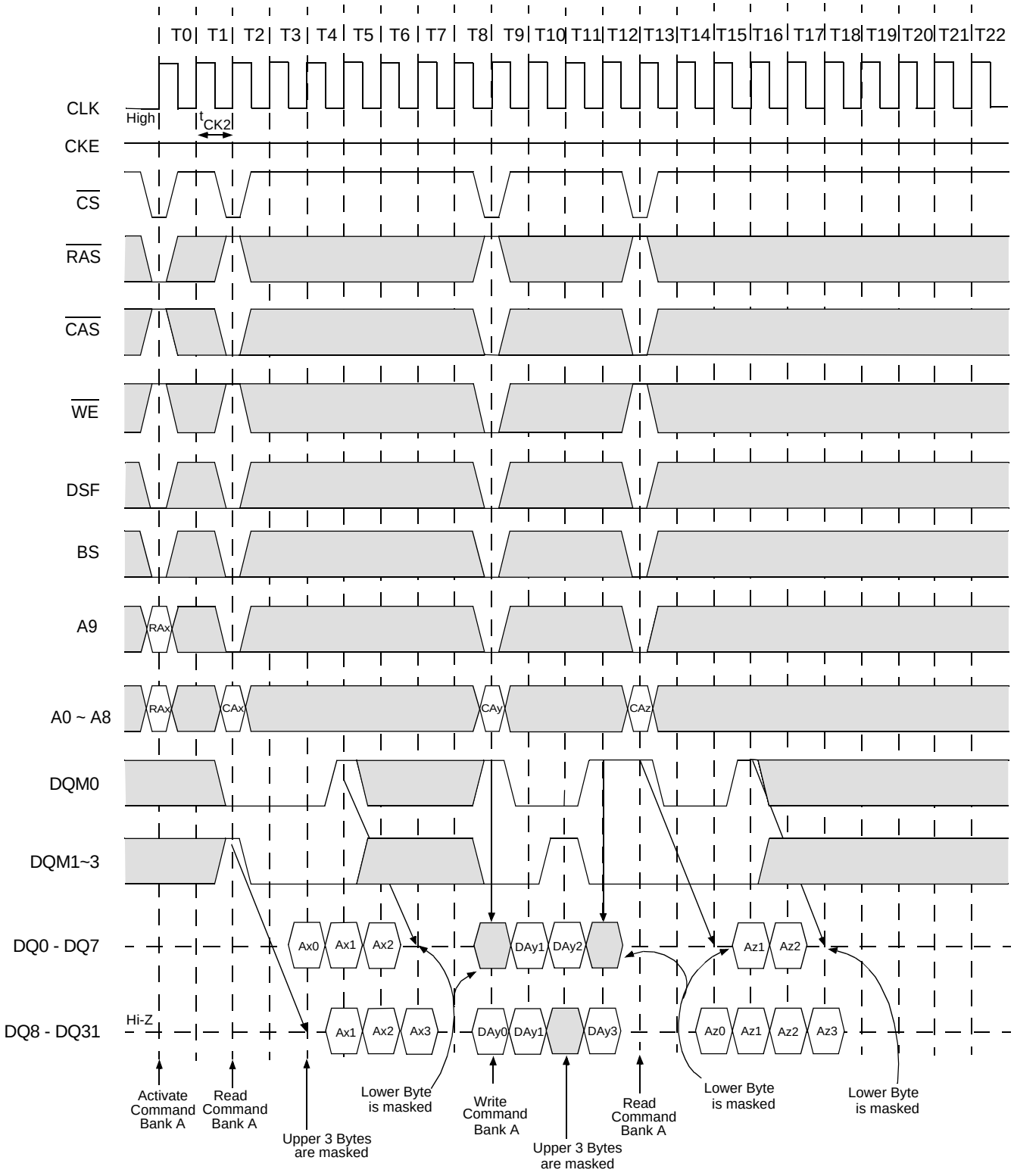


Figure 21. Burst Read and Single Write Operation (Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2)

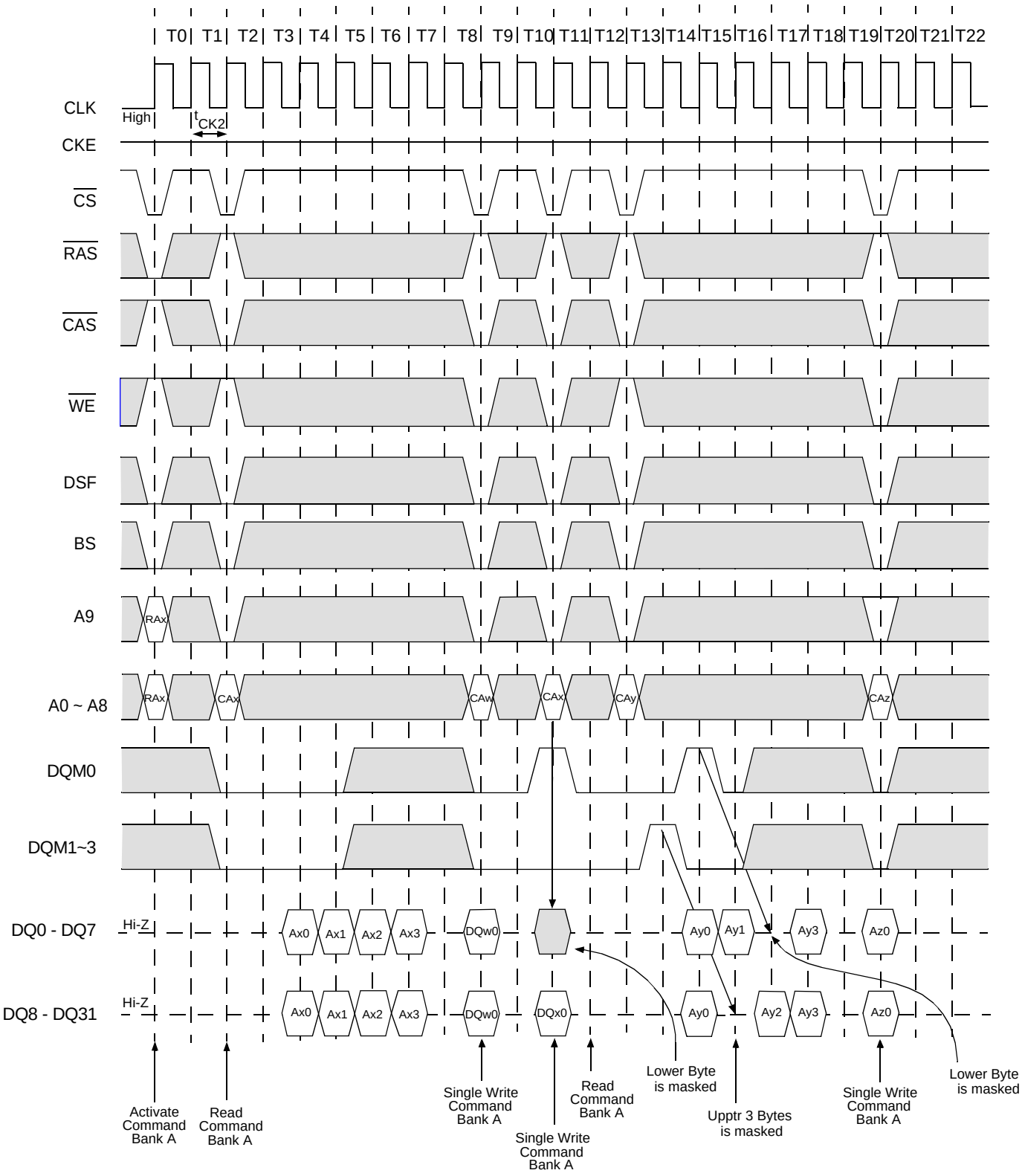


Figure 22. Full Page Burst Read and Single Write Operation

(Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 3)

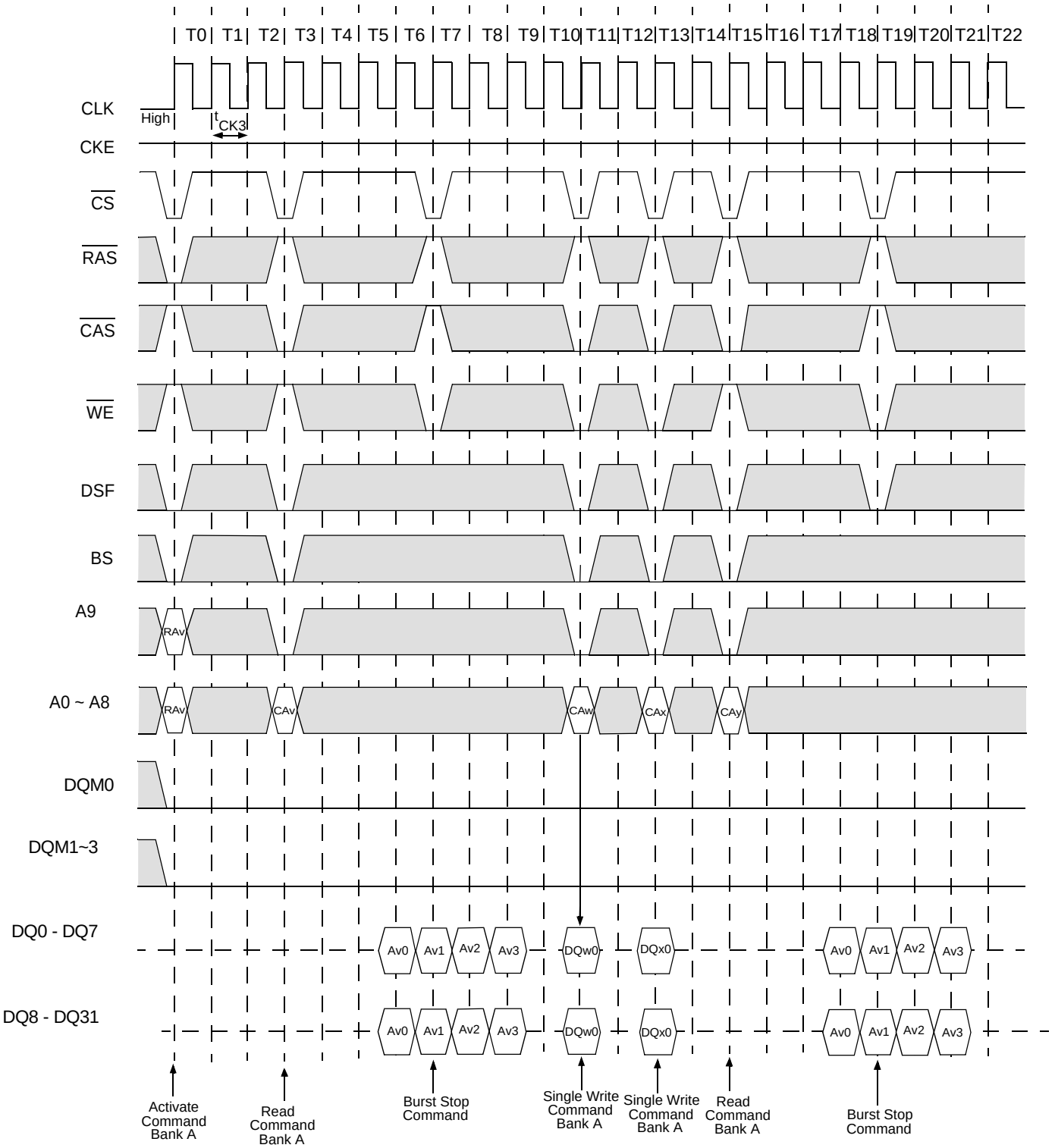


Figure 23. Random Row Read (Interleaving Banks)

(Burst Length = 2, $\overline{\text{CAS}}$ Latency = 1)

Figure 24. Full Page Random Column Read (Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2)

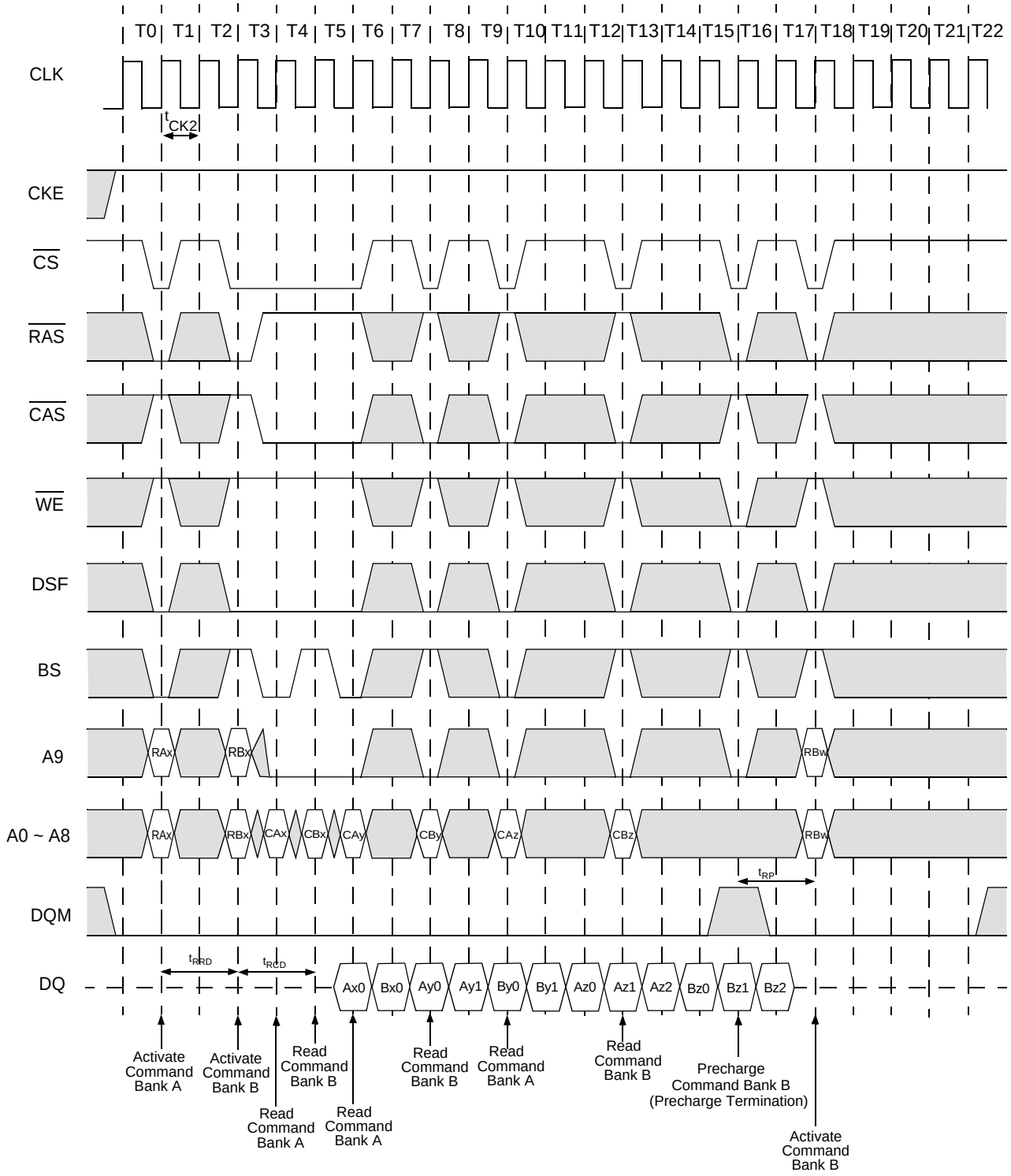


Figure 25. Full Page Random Column Write (Burst Length = Full Page, $\overline{CAS}$ Latency = 2)

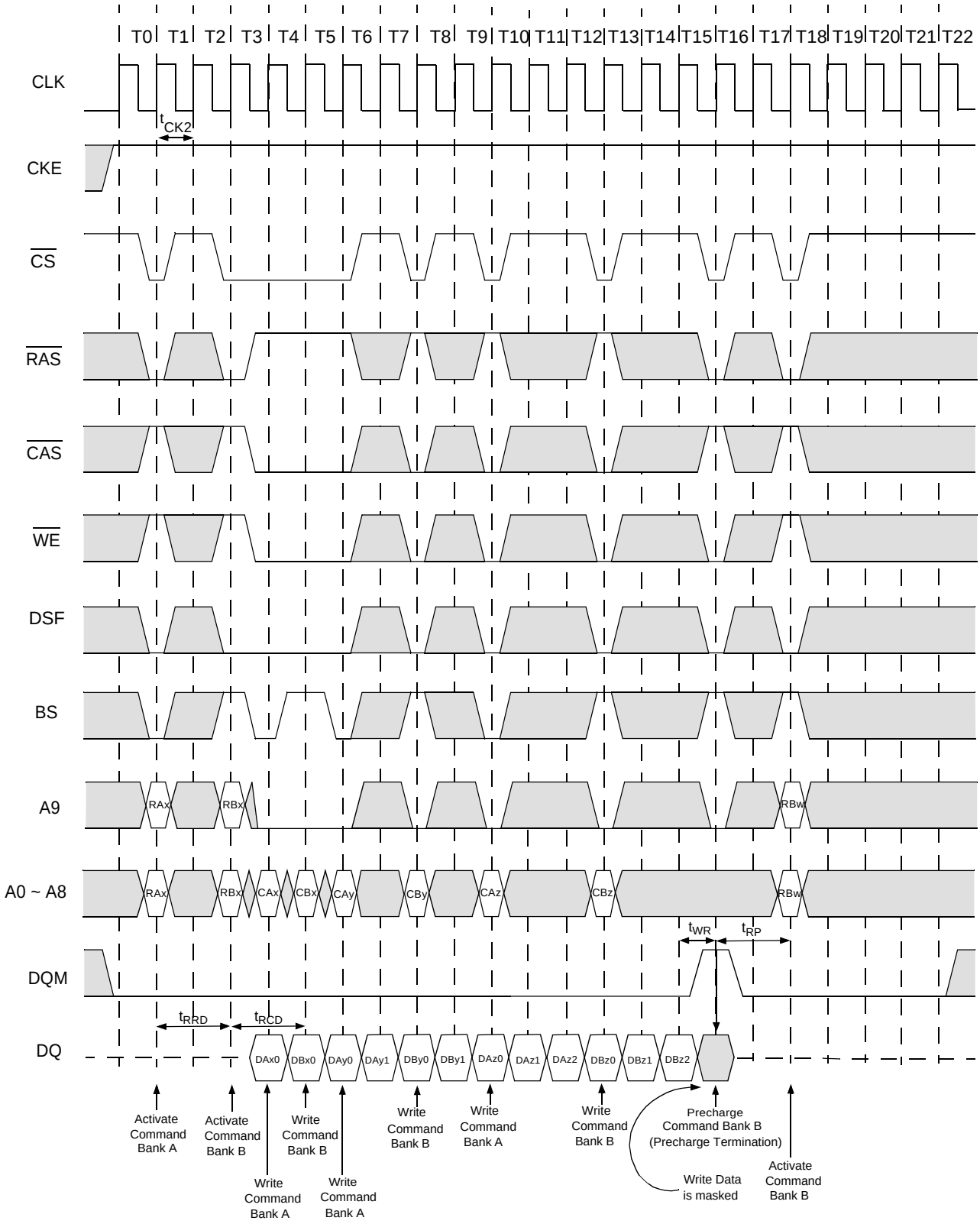


Figure 26.1. Precharge Termination of a Burst (Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 1)

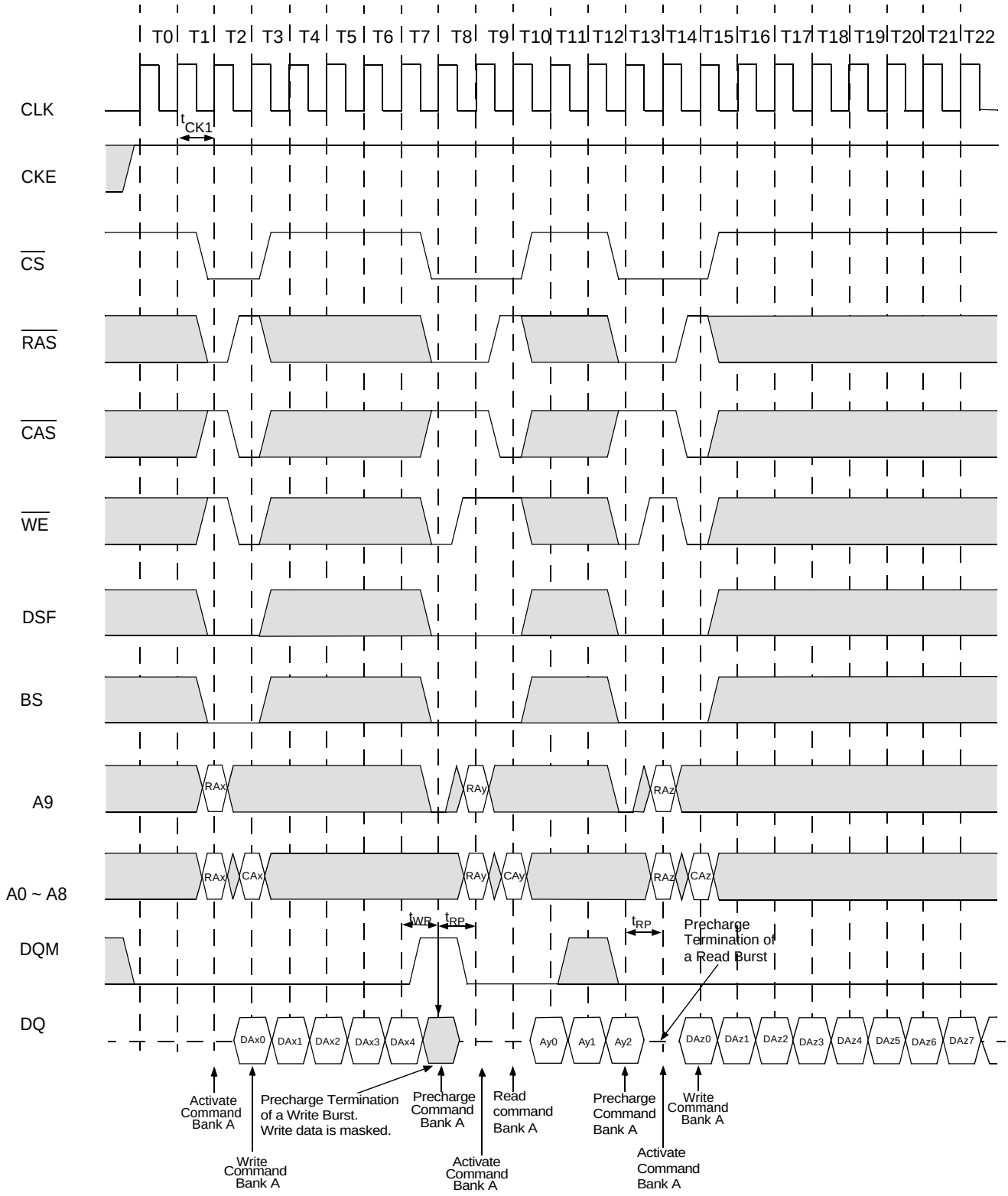


Figure 26.2. Precharge Termination of a Burst
(Burst Length = 8 or Full Page, CAS Latency = 2)

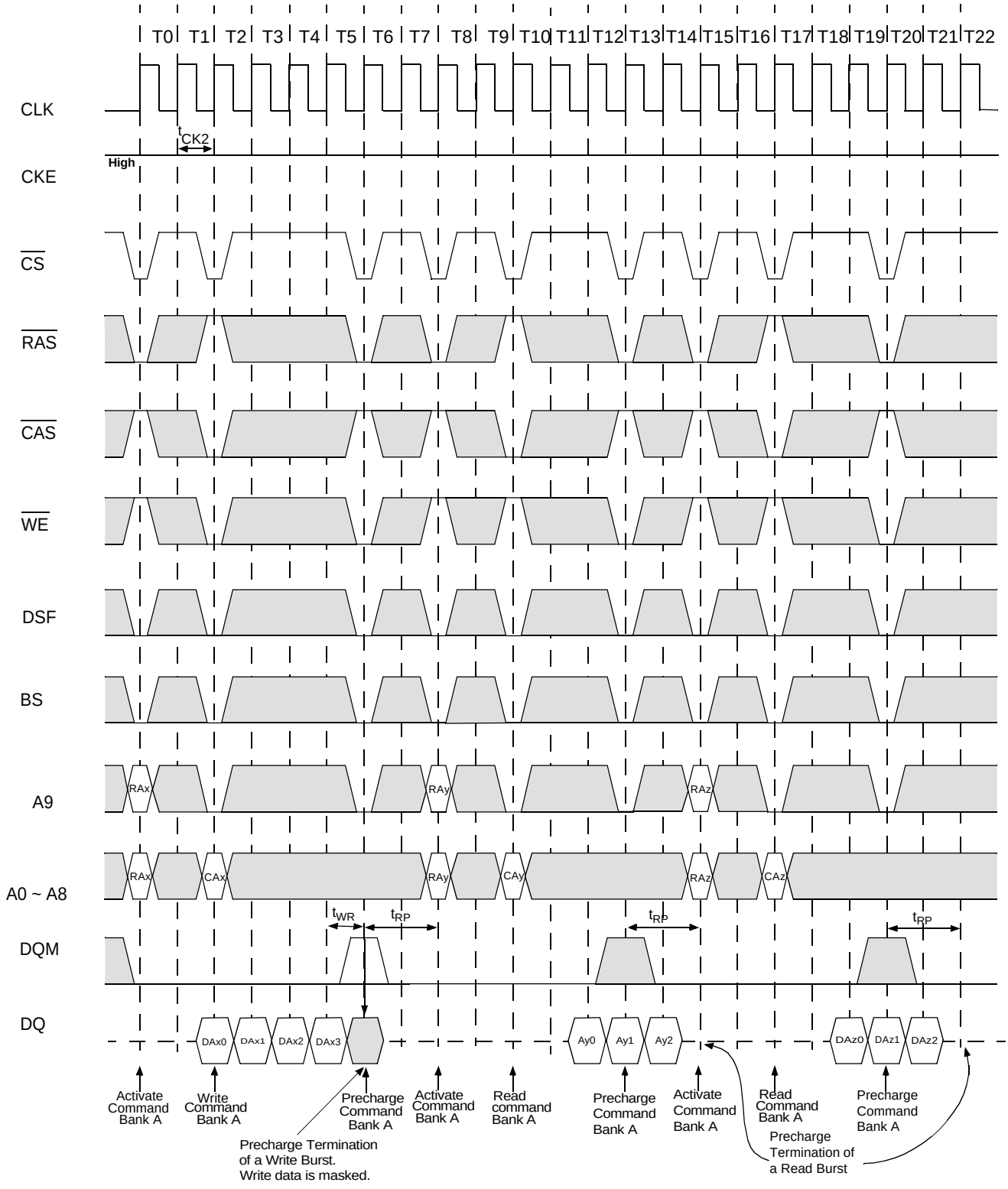
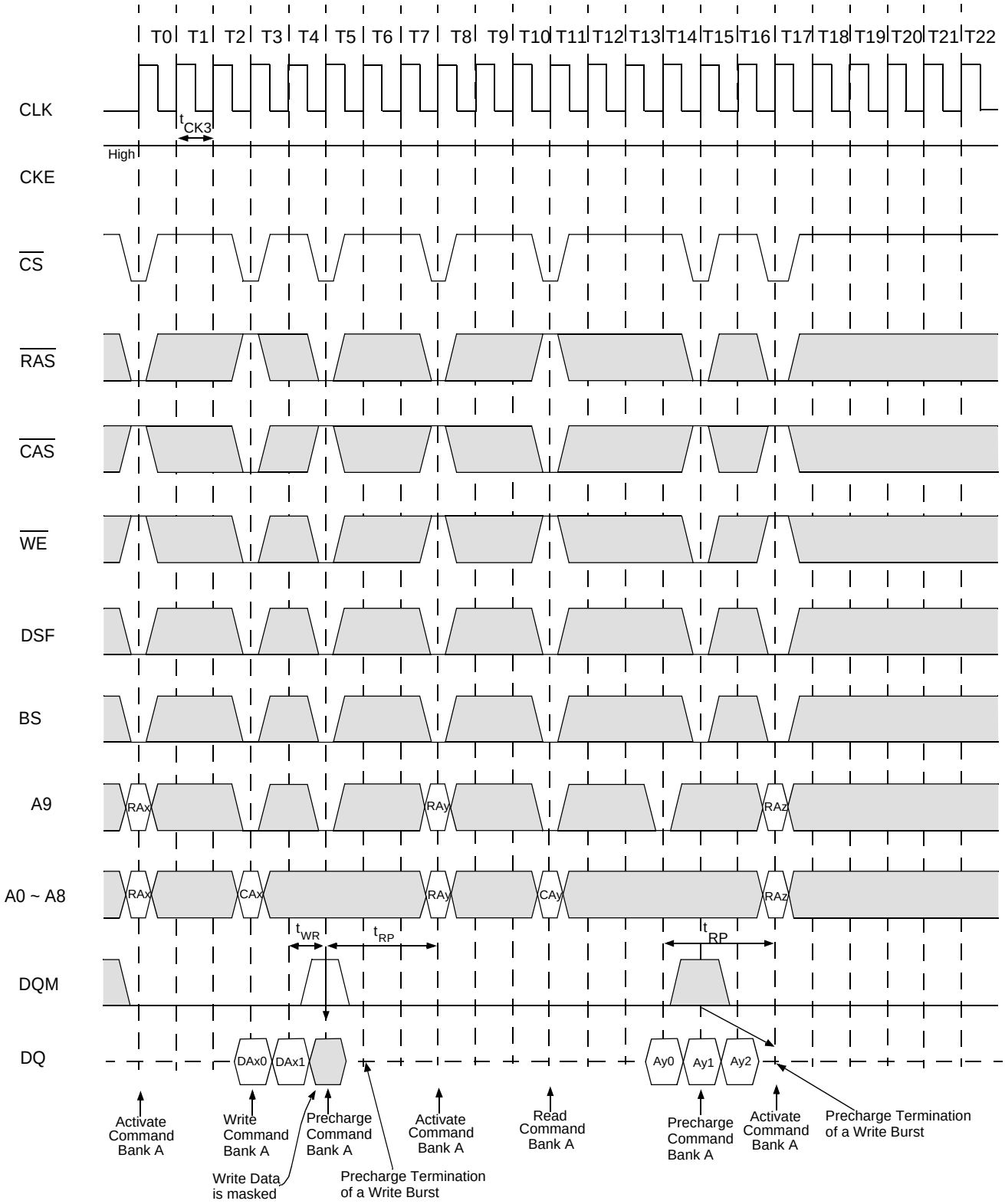


Figure 26.3 Precharge Termination of a Burst
(Burst Length = 4, 8 or Full page, CAS Latency = 3)



Ordering Information

Part Number	Frequency	Package	Packing Type
VG4632321AQ - 7	143MHz	QFP	Tray
VG4632321AQ - 7R	143MHz	QFP	Tape & Reel
VG4632321AQ - 6	166MHz	QFP	Tray
VG4632321AQ - 6R	166MHz	QFP	Tape & Reel
VG4632321AQ - 55	183MHz	QFP	Tray
VG4632321AQ - 55R	183MHz	QFP	Tape & Reel
VG4632321AQ - 5	200MHz	QFP	Tray
VG4632321AQ - 5R	200MHz	QFP	Tape & Reel
VG4632321AQ - 45	222MHz	QFP	Tray
VG4632321AQ - 45R	222MHz	QFP	Tape & Reel

VG4632321AQ - 7

- VG → VIS Memory Product
- 46 → Synchronous Graphic
- 32321 → Sync, 2k self - ref. 1M x 32 SGRAM
- A → Revision
- Q → Package Type (Q : QFP)
- 7 → Speed (7 : 7ns, 6 : 6ns, 5 : 5ns)
- R → Packing Type (R : Tape & Reel, Blank : Tray)

Outline Drawing Information