VSC9188

VITESSE

VSC9188 Stratton - 2.5 Gb/s VT1.5 Pointer Processor Path Terminator and Column Aligner

(2.5V/1.8V Power Supply, 0.18μm Technology

(Compliant with SONET Requirements as Stated in ANSI T1.105 and Telcordia GR-253-CORE

(Facilitates Hardware-based UPSR Switching in Accordance with Telcordia GR-1400-CORE

(Provides JTAG TAP Controller Conforming to the IEEE 1149.1 Standard

(Thermally-enhanced 552-pin CCGA Package

SPECIFICATIONS:

(2.5V/1.8V power supply, 0.18μm technology

APPLICATIONS:

(VT1.5 Pointer Processing

(Column Aligning

(Performance Monitoring

(Interface to a Large-scale VT1.5 Crossconnect.

BENEFITS:

(Low Cost

(Low Power

(High Functionality

FEATURES:

(Bidirectional 2.5 Gb/s VT1.5 Pointer Processor, Path Terminator and Column Aligner

(VT1.5 Pointer Processing on 4 x 336 VT1.5 Groups within 4 x STS-12 Backplane Signals

(Path Termination and Generation of STS-1 Traffic

(4 x 622 Mb/s STS-12 LVDS Backplane Interface Inputs with Integrated CDR and Realignment

(Two 4 x 622 Mb/s STS-12 LVDS Backplane Interface Outputs for Working and Protection Fan-out

(Interfaces with VSC9186 10 Gb/s Pointer Processor and VSC9187 3024 x 3024 VT1.5 TSI

(Generates In-band VT Signalling of UPSR Performance Monitoring Information for Hardware-based Protection Switching in VSC9187 3024 x 3024 VT1.5 TSI

KEY SPECIFICATIONS:

PARAMETERS	DESCRIPTION	Min	Max	Conditions
Vdd_core	Voltage for Core	2.97V	3.63V	Recommended 3.3V
Vdd_IO	Voltage of IO cells	2.3V	2.7V	Recommended 2.5V
POWER DISSIPATION				
IDD_2.5	Peak power supply current from 2.5V VDD	–	0.3A	Nominal
PD_typical	Typical power dissipation		3 W	Nominal
PD_peak	Peak power dissipation		5 W	Nominal
Backplane Data I/Os	622 Mb/s LVDS			

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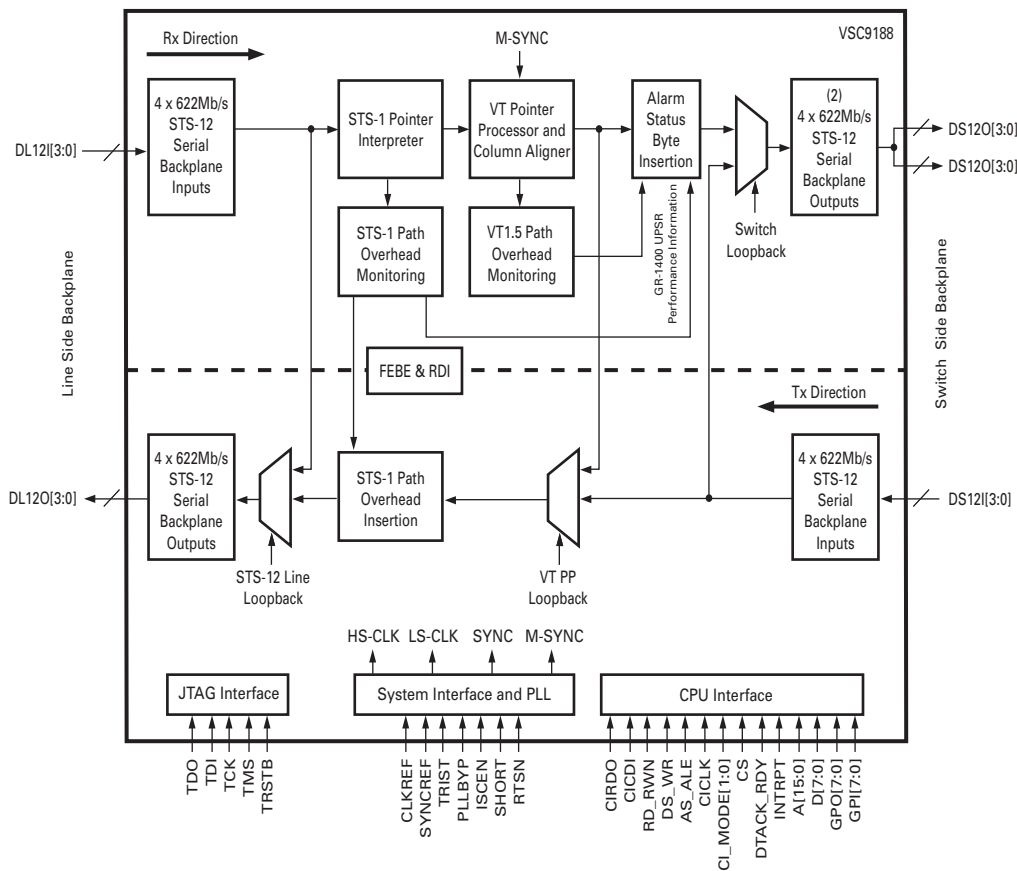
GENERAL DESCRIPTION:

The VSC9188 is a VT1.5 Pointer Processor and Column Aligner. The primary application for this device is to provide column alignment and performance monitoring for VT1.5 payloads and interface these tributaries to a large-scale VT1.5 crossconnect. The VSC9188 receives four serial STS-12 622 Mb/s signals from a VSC9186 10Gb/s Pointer Processor or VSC9182 STS-1 grooming crossconnect. These signals are terminated at the path level, monitored at the VT1.5 level, and column-aligned at the VT1.5 level in a deterministic fashion to a local SYNC signal. GR-1400 UPSR performance information is aggregated and placed in the VT overhead for use in the VT crossconnect. The four processed serial STS-12 622 Mb/s signals are duplicated on working and protection STS-12 622 Mb/s outputs for fan-out to protected VT fabrics. Four serial STS-12 622 Mb/s signals are received from the switch and the Path Overhead (POH) is reconstructed prior to transmission. Various loopback and test modes are also available.

VSC9188 BLOCK DIAGRAM:

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