High-Speed, Low r_{ON}, SPST Analog Switch
(1-Bit Bus Switch with Level-Shifter)

FEATURES

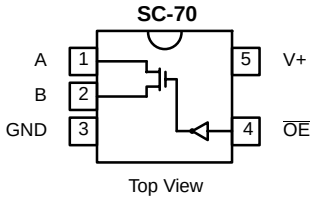
- SC-70 5-Lead Package
- 5-Ω Switch Connection Between Two Ports
- Minimal Propagation Delay Through The Switch
- Low I_{CC}
- Zero Bounce In Flow-Through Mode
- Control Inputs Compatible with TTL Level

DESCRIPTION

The DG2302 is a high-speed, 1-bit, low power, TTL-compatible bus switch. Using sub-micron CMOS technology, DG2302 achieves low on-resistance and negligible propagation delay.

The DG2302 consist of a bi-directional input/output pins A and B. When the output enable ($\overline{OE}$) is low, the input/output pins are connected. When the $\overline{OE}$ is high, the switch is open and a high-impedance state exists between input/output pins A and B.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View

Device Marking: E5

TRUTH TABLE		
$\overline{OE}$	B	Function
L	A	Connect
H	HiZ State	Disconnect

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	SC70-5	DG2302DL

ABSOLUTE MAXIMUM RATINGS

Reference to GND
V+ ..... -0.3 to +6 V
$\overline{OE}$, A, B[a] ..... -0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal) ..... ±50 mA
Peak Current ..... ±200 mA
(Pulsed at 1 ms, 10% duty cycle)
Storage Temperature (D Suffix) ..... -65 to 150°C

Power Dissipation (Packages)[b]
5-Pin SC70[c] ..... 250 mW

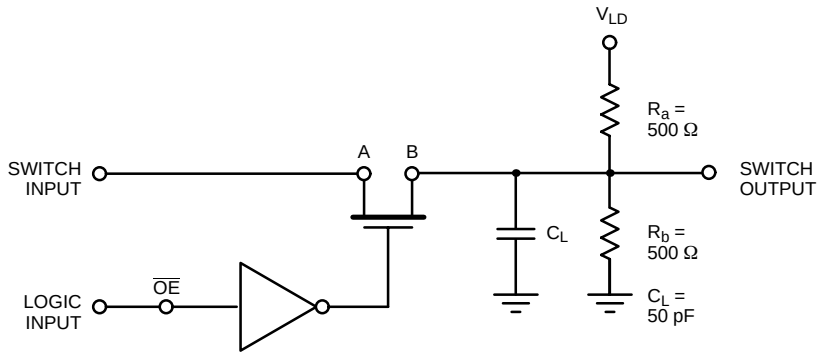
Notes:
a. Signals on A, or B or $\overline{OE}$ exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 3.1 mW/°C above 70°C

SPECIFICATIONS (V+ = 5.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, V_{IN} = 0.8 or 2.0 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
DC Characteristics							
On-Resistance	r_{ON}	V+ = 4.5 V, V_A = 0 V, I_B = 64 mA	Full			7	Ω
		V+ = 4.5 V, V_A = 0 V, I_B = 30 mA	Full			7	
		V+ = 4.5 V, V_A = 2.4 V, I_B = 15 mA	Full			50	
Switch Off Leakage Current	$I_{(off)}$	V+ = 5.5 V, V_A = 1 V/4.5 V, V_B = 4.5 V/1 V	Full	-10		10	µA
Switchl-On Leakage Current	$I_{(on)}$	V+ = 5.5 V, V_A = V_B = 1 V/4.5 V	Full	-10		10	
Input High Voltage	V_{IH}		Full	2.0			V
Input Low Voltage	V_{IL}		Full			0.8	
Input Current	I_{IL} or I_{IH}	$V_{\overline{OE}}$ = 0 or V+	Full	-1		1	µA
Dynamic Characteristics							
Prop Delay Bus-to-Bus[f]	t_{PHL}	V_{LD} = Open (Figure 1 and 2)	Full			1	ns
	t_{PLH}		Full			1	
Output Enable Time[d]	t_{PZL}	V_{LD} = 7 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		5.0		
	t_{PZH}	V_{LD} = Open, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		5.0		
Output Disable Time[d]	t_{PLZ}	V_{LD} = 7 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		3.9		
	t_{PHZ}	V_{LD} = Open, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		1.0		
Input Capacitance	C_{in}		Room		3.5		pF
Channel-Off Capacitance[d]	$C_{(off)}$	$V_{\overline{OE}}$ = 0 or V+, f = 1 MHz	Room		5		
Channel-On Capacitance[d]	C_{ON}		Room		11		
Power Supply							
Power Supply Range	V+			4.0		5.5	V
Power Supply Current	I+	$V_{\overline{OE}}$ = 0			0.9	1.5	mA
		$V_{\overline{OE}}$ = V+				1.0	µA

Notes:
a. Room = 25°C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

AC LOADING AND WAVEFORMS



Input driven by 50-Ω source terminated in 50 Ω
C_L includes load and stray capacitance
Input PRR = 1.0 MHz, t_W = 50 ns

Figure 1. AC Test Circuit

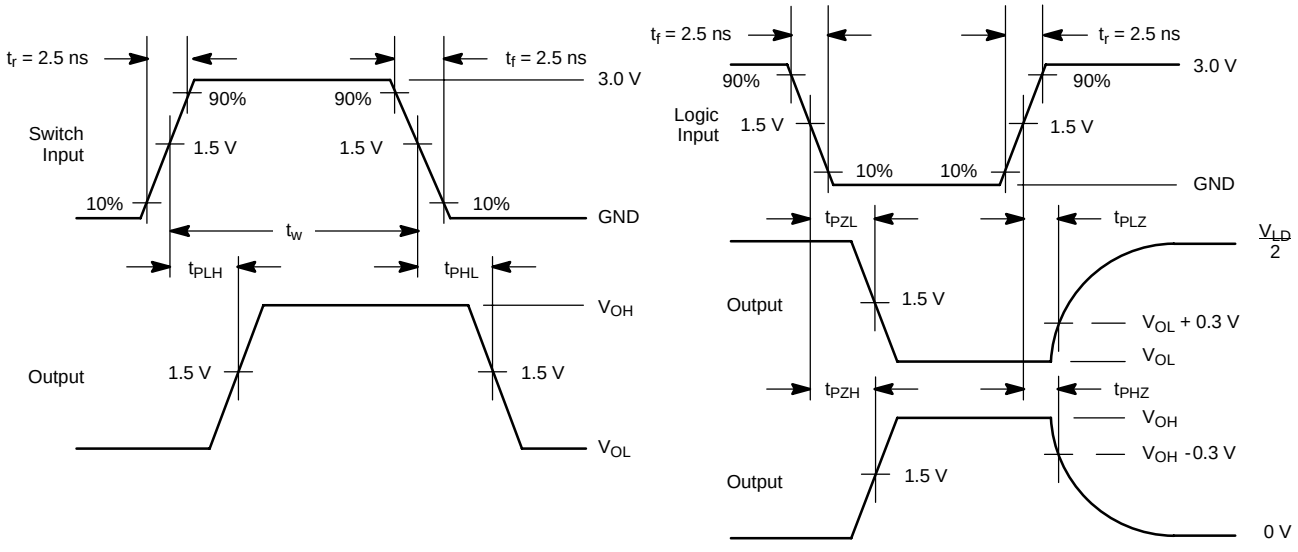


Figure 2. AC Waveforms

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)