REVISION HISTORY

REVISION	DESCRIPTION	Date
Preliminary Rev. 0.1	Original	May 4,2001
Rev. 1.0	Sample ready and release	Jul 16,2001
Rev. 1.1	1.Add 28-pin 8x20 mm TSOP-I 2.Add 28L 8x20mm TSOP-I outline dimension	Jul 16,2002
Rev. 1.2	Add order information for lead free product	May 13,2003

FEATURES

- Fast access time : 35/70ns (max.)
- Low power consumption:
  Operating current : 40/20 mA (max)
  Standby current : 1 μA (typical) L-version
  0.5μA(typical) LL-version
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min.)
- Package : 28-pin 600 mil PDIP
  28-pin 330 mil SOP
  28-pin 8x13.4mm STSOP
  28-pin 8x20 mm TSOP-I

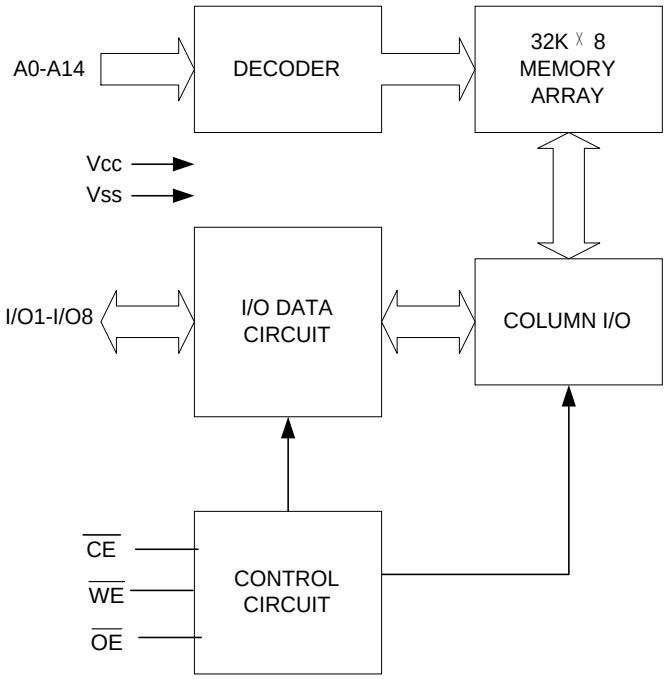
GENERAL DESCRIPTION

The UT62L256C is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

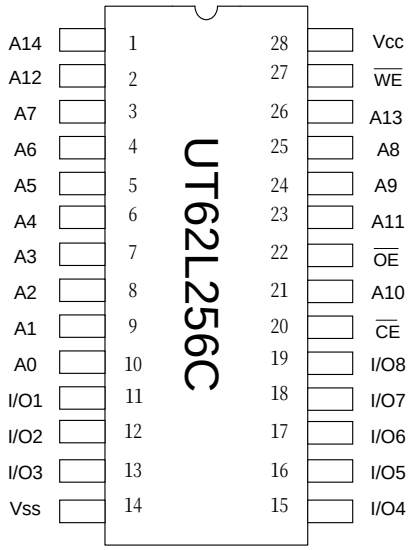
The UT62L256C is designed for high-speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application.

The UT62L256C operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible

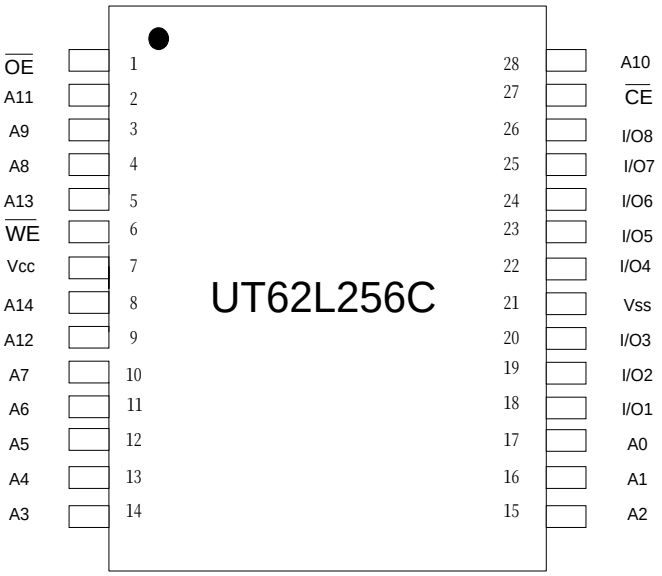
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PDIP/SOP



STSOP/TSOP-I

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to 4.5	V
Operating Temperature	T_A	0 to 70	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	High - Z	I_{CC}, I_{cc1}, I_{cc2}
Read	L	L	H	D_{OUT}	I_{CC}, I_{cc1}, I_{cc2}
Write	L	X	L	D_{IN}	I_{CC}, I_{cc1}, I_{cc2}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V ~ 3.6V, T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}*1			2.0	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}*2			- 0.5	-	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ $\overline{CE}$=V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH}= - 1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time=Min., $\overline{CE}$ = V_{IL} ,$I_{I/O}$ = 0mA ,	- 35	-	-	40	mA
			- 70	-	-	20	mA
	Icc1	Cycle time=1us $\overline{CE}$=0.2V; $I_{I/O}$ = 0mA other pins at 0.2V or Vcc-0.2V;		-	-	6	mA
	Icc2	Cycle time=500ns $\overline{CE}$=0.2V; $I_{I/O}$ = 0mA other pins at 0.2V or Vcc-0.2V		-	-	12	mA
Standby Power Supply Current	I_{SB}	$\overline{CE}$ =V_{IH}		-	-	3	mA
	I_{SB1}	$\overline{CE} \geqq V_{CC}$-0.2V	-L	-	1	40	µA
			-LL	-	0.5	20	µA

Notes:
1. Overshoot : Vcc+3.0v for pulse width less than 10ns.
2. Undershoot : Vss-3.0v for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 100pF, I_{OH}/I_{OL} = -1mA/4mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V~3.6V , T_A = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L256C-35		UT62L256C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	70	ns
Chip Enable Access Time	t_{ACE}	-	35	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	35	ns
Chip Enable to Output in Low Z	t_{CLZ*}	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	25	-	35	ns
Output Disable to Output in High Z	t_{OHZ*}	-	25	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns

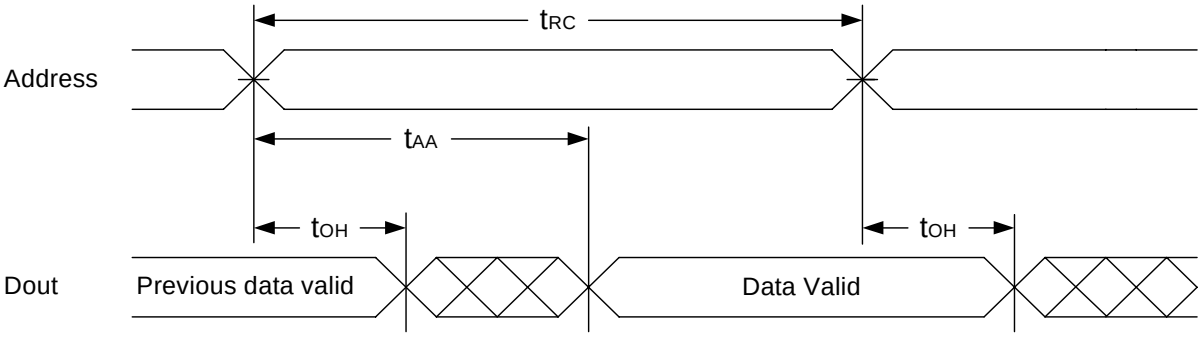
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L256C-35		UT62L256C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	60	-	ns
Chip Enable to End of Write	t_{CW}	30	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	50	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	ns
Write to Output in High Z	t_{WHZ*}	-	15	-	25	ns

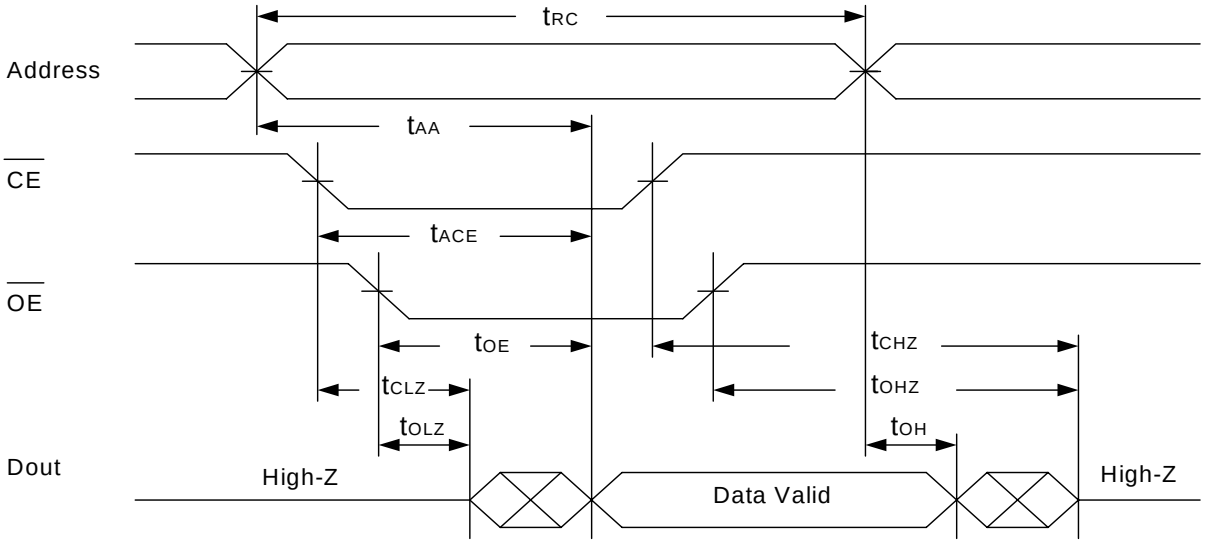
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



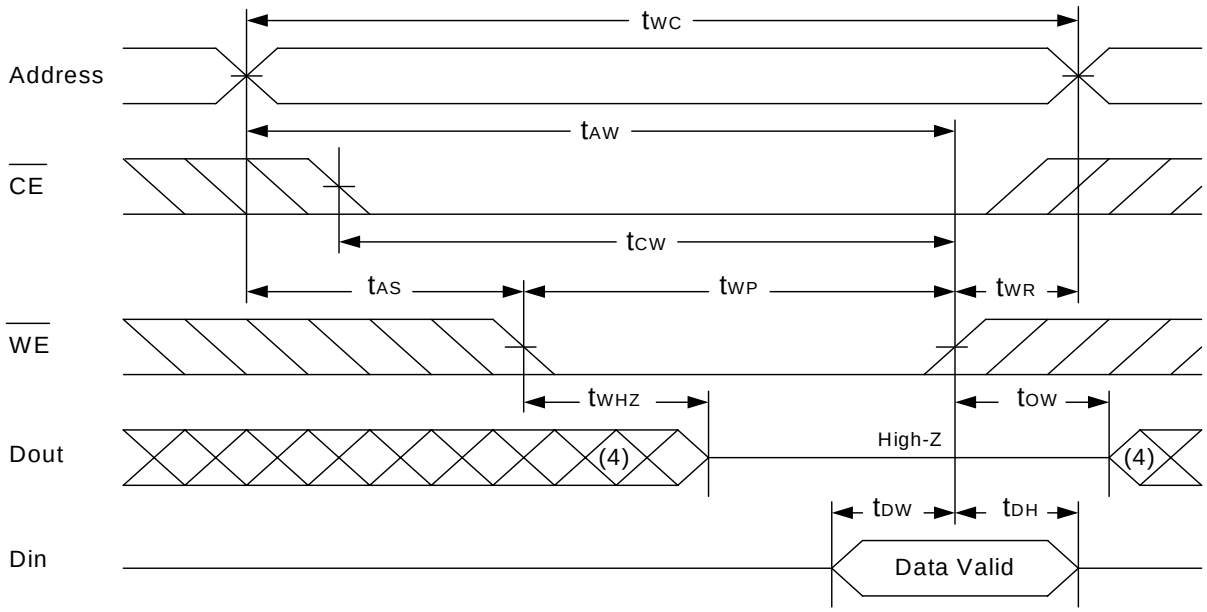
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,4,5)



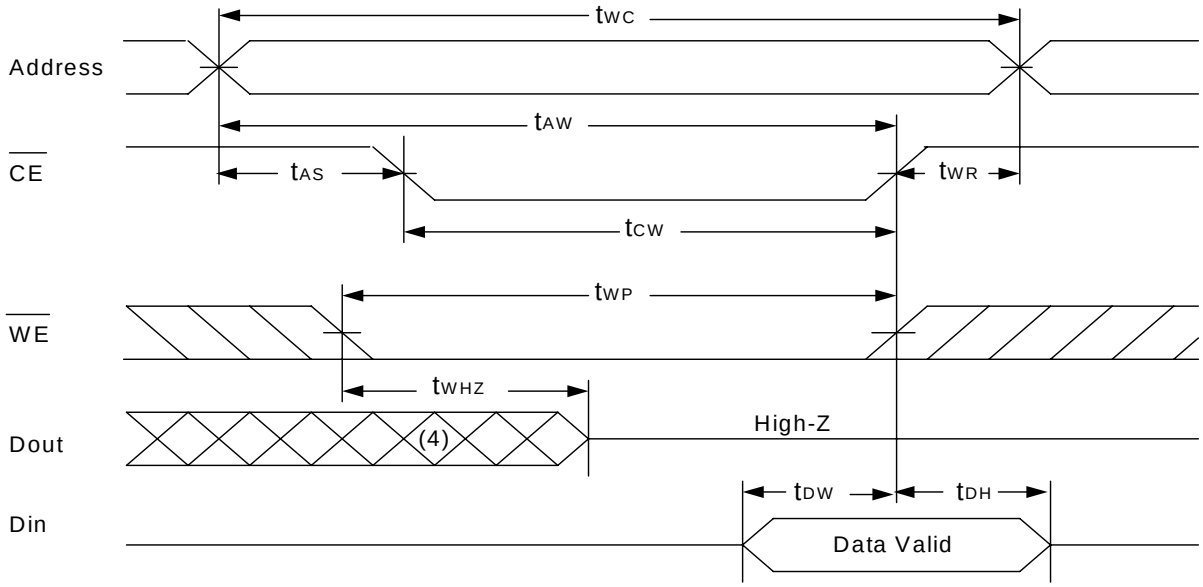
Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{OE}$ =low, $\overline{CE}$ =low.
3. Address must be valid prior to or coincident with $\overline{CE}$ =low,; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L=5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5,6)



Notes :

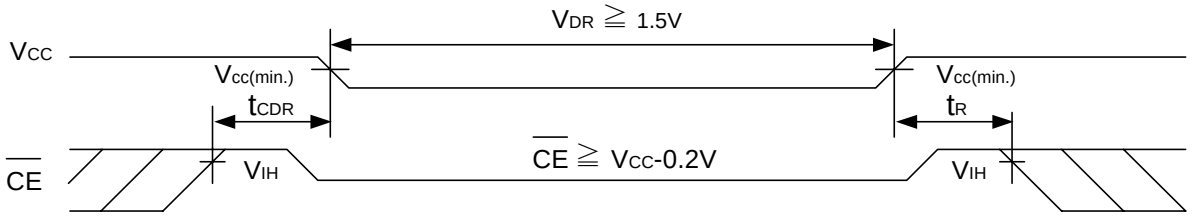
1. $\overline{WE}$, $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, low $\overline{WE}$.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ low, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS (T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	Vcc=2.5V	- L	-	1	20	µA
		$\overline{CE} \geqq V_{CC}$-0.2V	- LL	-	0.5	10	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

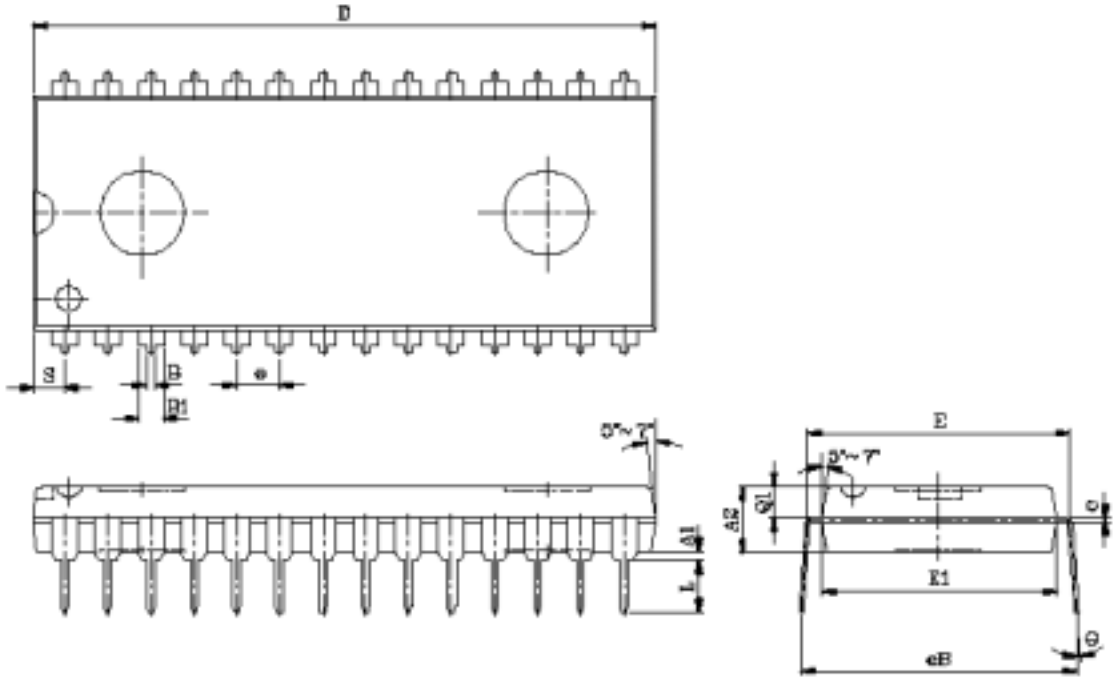
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM



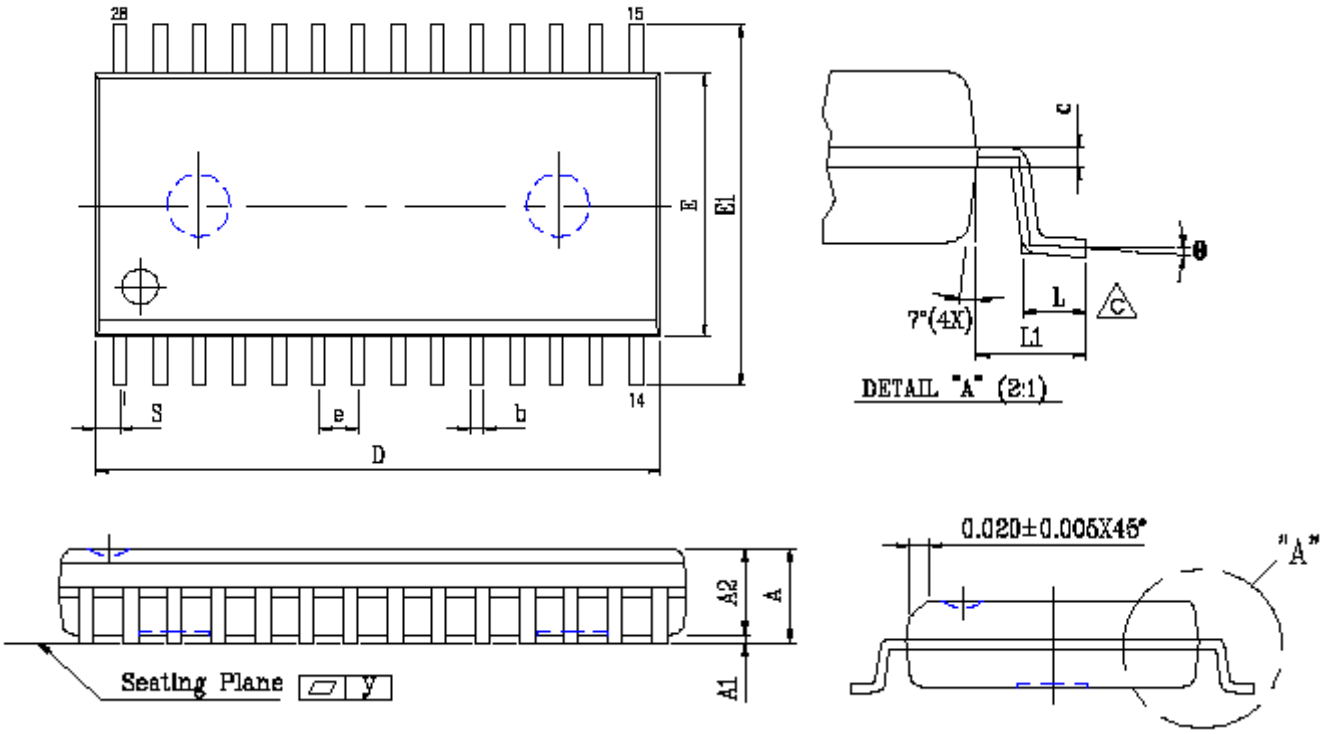
PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP PACKAGE OUTLINE DIMENSION



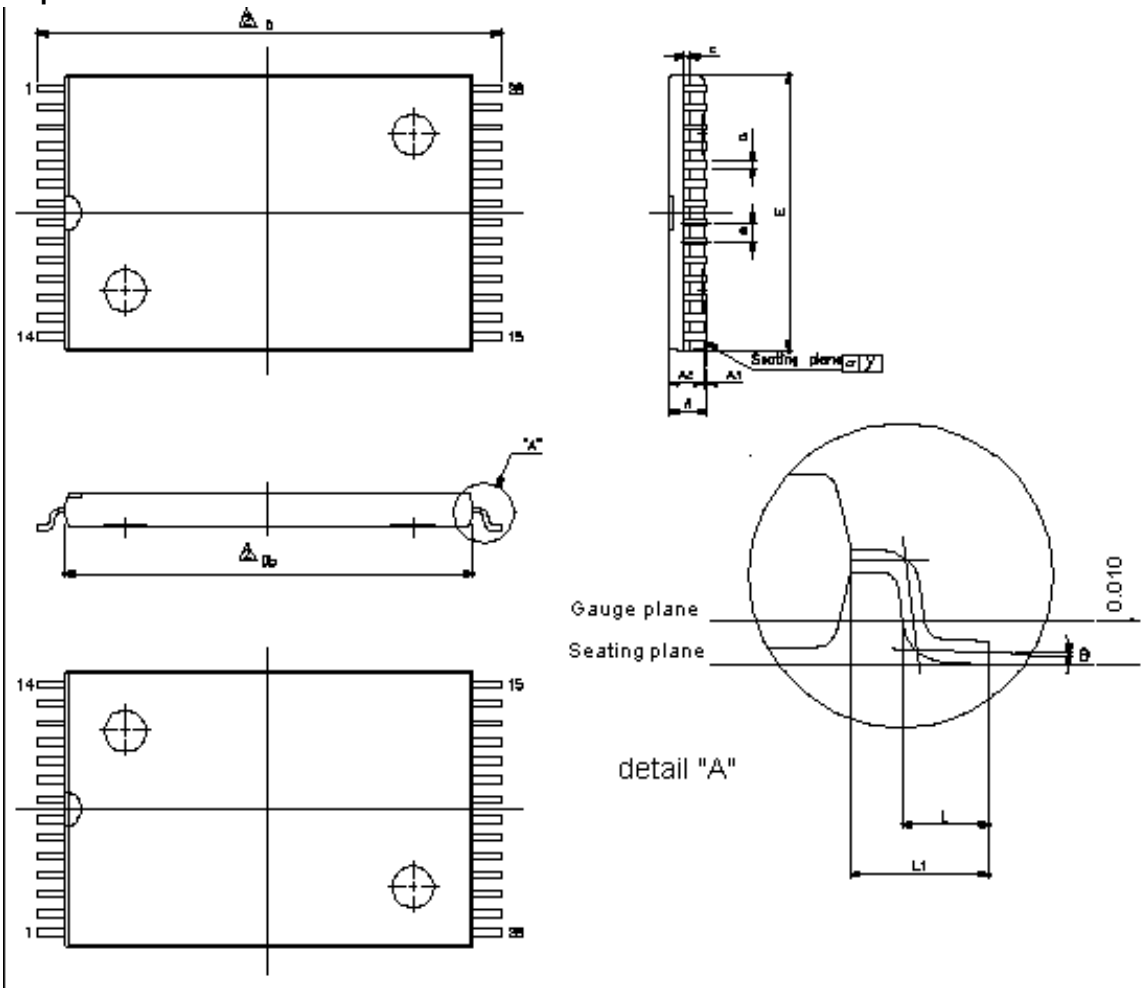
UNIT / SYMBOL	INCH(BASE)	MM(REF)
A1	0.010 (MIN)	0.254 (MIN)
A2	0.150±0.005	3.810±0.127
B	0.020 (MAX)	0.508(MAX)
B1	0.055 (MAX)	1.397(MAX)
c	0.012 (MAX)	0.304 (MAX)
D	1.430 (MAX)	36.322 (MAX)
E	0.6 (TYP)	15.24 (TYP)
E1	0.52 (MAX)	13.208 (MAX)
e	0.100 (TYP)	2.540(TYP)
eB	0.625 (MAX)	15.87 (MAX)
L	0.180(MAX)	4.572(MAX)
S	0.06 (MAX)	1.524 (MAX)
Q1	0.08(MAX)	2.032(MAX)
Θ	15^{o}(MAX)	15^{o}(MAX)

28 pin 330 mil SOP PACKAGE OUTLINE DIMENSION



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.120 (MAX)	3.048 (MAX)
A1	0.002(MIN)	0.05(MIN)
A2	0.098±0.005	2.489±0.127
b	0.0016 (TYP)	0.406(TYP)
c	0.010 (TYP)	0.254(TYP)
D	0.728 (MAX)	18.491 (MAX)
E	0.340 (MAX)	8.636 (MAX)
E1	0.465±0.012	11.811±0.305
e	0.050 (TYP)	1.270(TYP)
L	0.05 (MAX)	1.270 (MAX)
L1	0.067±0.008	1.702 ±0.203
S	0.047 (MAX)	1.194 (MAX)
y	0.003(MAX)	0.076(MAX)
Θ	0^o 10^o	0^o 10^o

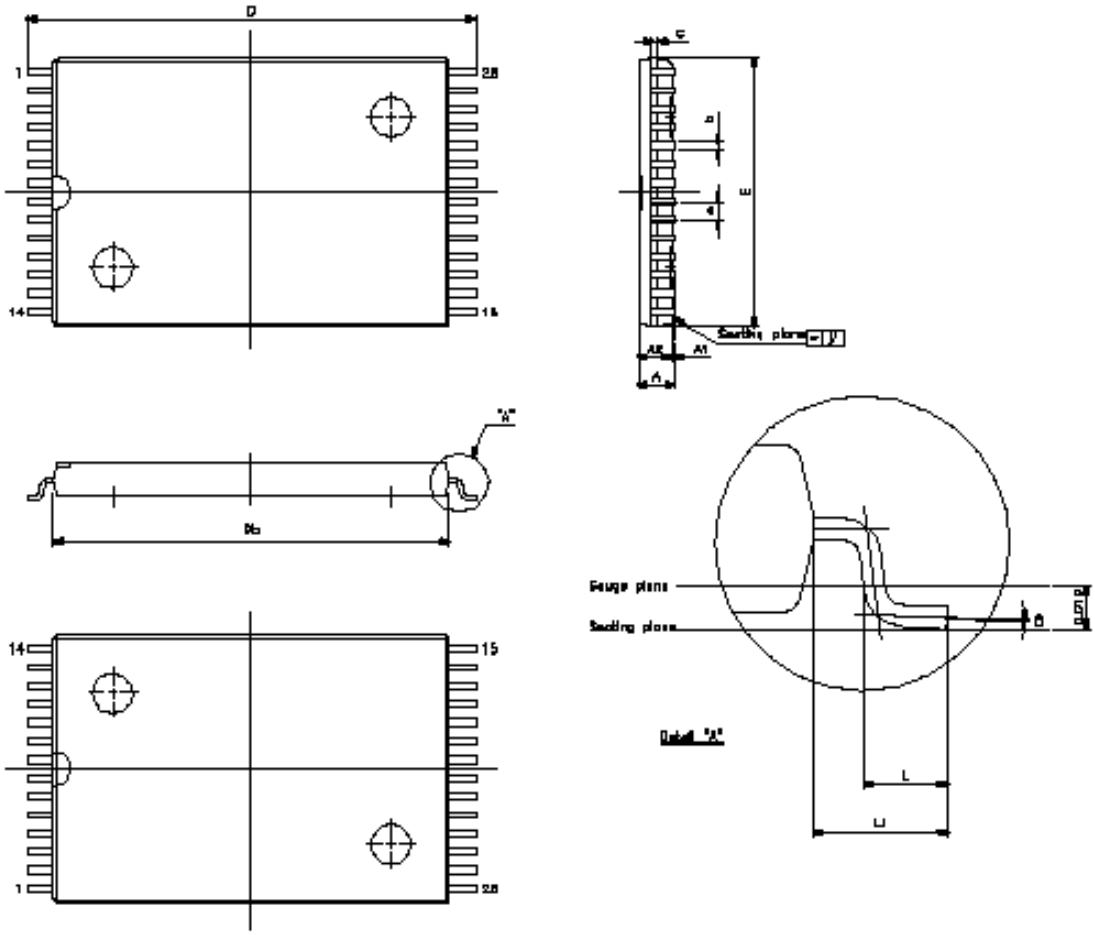
28 pin 8x13.4mm STSOP PACKAGE OUTLINE DIMENSION



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.006 (TYP)	0.15(TYP)
c	0.010 (TYP)	0.254(TYP)
Db	0.465±0.004	11.80±0.10
E	0.315±0.004	8.00±0.10
e	0.022 (TYP)	0.55(TYP)
D	0.528±0.008	13.40±0.20
L	0.020±0.004	0.50±0.10
L1	0.0315±0.004	0.80±0.10
y	0.08(MAX)	0.003(MAX)
Θ	0^o 5^o	0^o 5^o

Note：
E dimension is not including end flash
The total of both sides' end flash is
Not above 0.3mm.

28 pin 8x20mm TSOP-I PACKAGE OUTLINE DIMENSION



Note：
E dimension is not including end flash
The total of both sides' end flash is
Not above 0.3mm.

SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.008 (TYP)	0.20(TYP)
c	0.008 (TYP)	0.15(TYP)
Db	0.465±0.004	11.80±0.10
E	0.315±0.004	8.00±0.10
e	0.022 (TYP)	0.55(TYP)
D	0.528±0.008	13.40±0.20
L	0.020±0.004	0.50±0.10
L1	0.0315±0.004	0.80±0.10
y	0.003(MAX)	0.08(MAX)
Θ	0^o 5^o	0^o 5^o

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) typ.	PACKAGE
UT62L256CPC-35L	35	1 μA	28PIN PDIP
UT62L256CPC-35LL	35	0.5 μA	28PIN PDIP
UT62L256CPC-70L	70	1 μA	28PIN PDIP
UT62L256CPC-70LL	70	0.5 μA	28PIN PDIP
UT62L256CSC-35L	35	1 μA	28PIN SOP
UT62L256CSC-35LL	35	0.5 μA	28PIN SOP
UT62L256CSC-70L	70	1 μA	28PIN SOP
UT62L256CSC-70LL	70	0.5 μA	28PIN SOP
UT62L256CLS-35L	35	1 μA	28PIN STSOP
UT62L256CLS-35LL	35	0.5 μA	28PIN STSOP
UT62L256CLS-70L	70	1 μA	28PIN STSOP
UT62L256CLS-70LL	70	0.5 μA	28PIN STSOP
UT62L256CLC-35L	35	1 μA	28PIN TSOP-I
UT62L256CLC-35LL	35	0.5 μA	28PIN TSOP-I
UT62L256CLC-70L	70	1 μA	28PIN TSOP-I
UT62L256CLC-70LL	70	0.5 μA	28PIN TSOP-I

ORDERING INFORMATION (for lead free product)

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) typ.	PACKAGE
UT62L256CPCL-35L	35	1 μA	28PIN PDIP
UT62L256CPCL-35LL	35	0.5 μA	28PIN PDIP
UT62L256CPCL-70L	70	1 μA	28PIN PDIP
UT62L256CPCL-70LL	70	0.5 μA	28PIN PDIP
UT62L256CSCL-35L	35	1 μA	28PIN SOP
UT62L256CSCL-35LL	35	0.5 μA	28PIN SOP
UT62L256CSCL-70L	70	1 μA	28PIN SOP
UT62L256CSCL-70LL	70	0.5 μA	28PIN SOP
UT62L256CLSL-35L	35	1 μA	28PIN STSOP
UT62L256CLSL-35LL	35	0.5 μA	28PIN STSOP
UT62L256CLSL-70L	70	1 μA	28PIN STSOP
UT62L256CLSL-70LL	70	0.5 μA	28PIN STSOP
UT62L256CLCL-35L	35	1 μA	28PIN TSOP-I
UT62L256CLCL-35LL	35	0.5 μA	28PIN TSOP-I
UT62L256CLCL-70L	70	1 μA	28PIN TSOP-I
UT62L256CLCL-70LL	70	0.5 μA	28PIN TSOP-I

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