# UM61512A Series

## 64K X 8 BIT HIGH SPEED CMOS SRAM

### Features

- Single +5V power supply
- Access times: 15/20/25ns (max.)
- Current: Operating: 160mA (max.)
  Standby: 10mA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 3V (min.)
- Available in 32-pin SKINNY DIP, TSOP, SOP, SOJ and both 300/400 mil packages

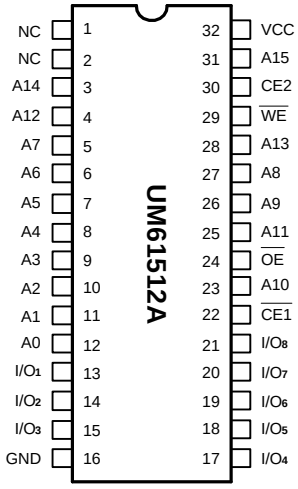
### General Description

The UM61512A is a low operating current 524,288-bit static random access memory organized as 65,536 words by 8 bits and operates on a single 5V power supply. It is built using UMC's high performance CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

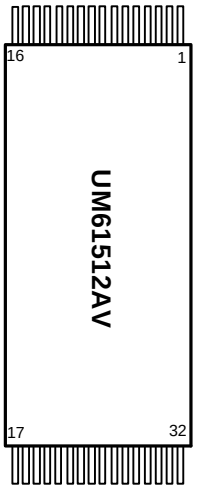
Two chip enable inputs are provided for POWER-DOWN and device enable and an output enable input is included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 3V.

### Pin Configurations

■ **SKINNY/SOJ/SOP**

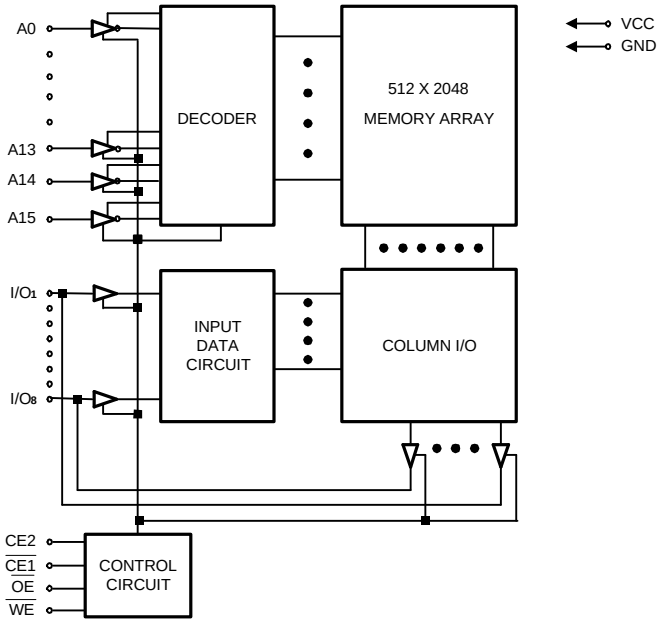



■ **TSOP (forward type)**




| Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|
| 1 | A11 | 17 | A3 |
| 2 | A9 | 18 | A2 |
| 3 | A8 | 19 | A1 |
| 4 | A13 | 20 | A0 |
| 5 | $\overline{WE}$ | 21 | $I/O_1$ |
| 6 | CE2 | 22 | $I/O_2$ |
| 7 | A15 | 23 | $I/O_3$ |
| 8 | VCC | 24 | GND |
| 9 | NC | 25 | $I/O_4$ |
| 10 | NC | 26 | $I/O_5$ |
| 11 | A14 | 27 | $I/O_6$ |
| 12 | A12 | 28 | $I/O_7$ |
| 13 | A7 | 29 | $I/O_8$ |
| 14 | A6 | 30 | $\overline{CE1}$ |
| 15 | A5 | 31 | A10 |
| 16 | A4 | 32 | $\overline{OE}$ |

## Block Diagram




## Pin Descriptions SKINNY/SOJ/SOP

| Pin No. | Symbol | Description |
|---|---|---|
| 1, 2 | NC | No Connection |
| 3 - 12, 23, 25 - 28, 31 | A0 - A15 | Address Inputs |
| 13 - 15, 17 - 21 | $I/O_1$ - $I/O_8$ | Data Input/Outputs |
| 16 | GND | Ground |
| 22 | $\overline{CE1}$ | Chip Enable |
| 24 | $\overline{OE}$ | Output Enable |
| 29 | $\overline{WE}$ | Write Enable |
| 30 | CE2 | Chip Enable |
| 32 | VCC | Power Supply |

## Pin Description TSOP

| Pin No. | Symbol | Description |
|---|---|---|
| 1 - 4, 7, 11 - 20, 31 | A0 - A15 | Address Inputs |
| 5 | $\overline{WE}$ | Write Enable |
| 6 | CE2 | Chip Enable |
| 8 | VCC | Power Supply |
| 9, 10 | NC | No Connection |
| 21 - 23, 25 - 29 | $I/O_1$ - $I/O_8$ | Data Input/Outputs |
| 24 | GND | Ground |
| 30 | $\overline{CE1}$ | Chip Enable |
| 32 | $\overline{OE}$ | Output Enable |

### Recommended DC Operating Conditions ($T_A$ = 0°C to + 70°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VCC | Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| GND | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | 3.5 | VCC + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.3 | 0 | +0.8 | V |
| $C_L$ | Output Load | - | - | 30 | pF |
| TTL | Output Load | - | - | 1 | - |

### Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +7.0V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC +0.5V
Operating Temperature, Topr . . . . . 0 °C to +70°C
Storage Temperature, Tstg . . . . . -55 °C to +125°C
Temperature Under Bias, Tbias . . . . . -10 °C to +85°C
Power Dissipation, Pt . . . . . 1.0W
Soldering Temp. & Time . . . . . 260 °C, 10 sec

### *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### DC Electrical Characteristics ($T_A$ = 0°C to + 70°C, VCC = 5V ± 5%, GND = 0V)

| Symbol | Parameter | UM61512A-15/20/25 | | Unit | Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $\lvert I_{LI} \rvert$ | Input Leakage Current | - | 2 | µA | $V_{IN}$ = GND to VCC |
| $\lvert I_{LO} \rvert$ | Output Leakage Current | - | 2 | µA | $\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$ or $\overline{OE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ $V_{I/O}$ = GND to VCC |
| $I_{CC1}$ (1) | Dynamic Operating Current | - | 160 | mA | $\overline{CE1}$ = $V_{IL}$, CE2 = $V_{IH}$ $I_{I/O}$ = 0 mA |
| $I_{SB}$ | Standby Power Supply Current | - | 30 | mA | $\overline{CE1}$ = $V_{IH}$ or CE2 = $V_{IL}$ |
| $I_{SB1}$ | | - | 20 | mA | $\overline{CE1}$ ≥ VCC - 0.2V, CE2 ≥ VCC - 0.2V, $V_{IN}$ ≤ 0.2V or $V_{IN}$ ≥ VCC - 0.2V |
| $I_{SB2}$ | | - | 20 | mA | $\overline{CE1}$ ≤ 0.2V, CE2 ≤ 0.2V $V_{IN}$ ≤ 0.2V or $V_{IN}$ ≥ VCC - 0.2V |
| $V_{OL}$ | Output Low Voltage | - | 0.4 | V | $I_{OL}$ = 8 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | - | V | $I_{OH}$ = -4 mA |

Note: 1. $I_{CC1}$ is dependent on output loading, cycle rates, and Read/Write patterns.

### Truth Table

| Mode | $\overline{CE1}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | I/O Operation | Supply Current |
|---|---|---|---|---|---|---|
| Standby | H | X | X | X | High Z | $I_{SB}$, $I_{SB1}$ |
| | X | L | X | X | High Z | $I_{SB}$, $I_{SB2}$ |
| Output Disable | L | H | H | H | High Z | $I_{CC1}$ |
| Read | L | H | L | H | $D_{OUT}$ | $I_{CC1}$ |
| Write | L | H | X | L | $D_{IN}$ | $I_{CC1}$ |

Note: X = H or L

### Capacitance ($T_A$ = 25°C, f = 1.0 MHz)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ * | Input Capacitance | | 8 | pF | $V_{IN}$ = 0V |
| $C_{I/O}$ * | Input/Output Capacitance | | 10 | pF | $V_{I/O}$ = 0V |

* These parameters are sampled and not 100% tested.

### AC Characteristics ($T_A$ = 0°C to +70°C, VCC = 5V ± 10%)

| Symbol | Parameter | | UM61512A-15 | | UM61512A-20 | | UM61512A-25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | | 15 | - | 20 | - | 25 | - | ns |
| $t_{AA}$ | Address Access Time | | - | 15 | - | 20 | - | 25 | ns |
| $t_{ACE1}$ | Chip Enable Access Time | $\overline{CE1}$ | - | 15 | - | 20 | - | 25 | ns |
| $t_{ACE2}$ | | CE2 | - | 15 | - | 20 | - | 25 | ns |
| $t_{OE}$ | Output Enable to Output Valid | | - | 7 | - | 9 | - | 12 | ns |
| $t_{CLZ1}$ | Chip Enable to Output in Low Z | $\overline{CE1}$ | 5 | - | 5 | - | 5 | - | ns |
| $t_{CLZ2}$ | | CE2 | 5 | - | 5 | * | 5 | - | ns |
| $t_{OLZ}$ | Output Enable to Output in Low Z | | 2 | - | 2 | - | 2 | - | ns |
| $t_{CHZ1}$ | Chip Disable to Output in High Z | $\overline{CE1}$ | - | 10 | - | 10 | - | 15 | ns |
| $t_{CHZ2}$ | | CE2 | - | 10 | - | 10 | - | 15 | ns |
| $t_{OHZ}$ | Output Disable to Output in High Z | | 2 | 9 | 2 | 9 | 2 | 10 | ns |
| $t_{OH}$ | Output Hold from Address Change | | 3 | - | 5 | - | 5 | - | ns |

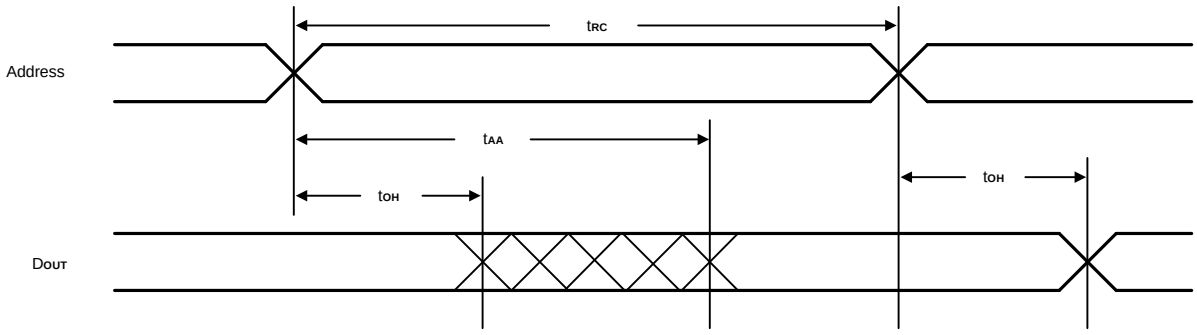
## AC Characteristics (continued)

| Symbol | Parameter | UM61512A-15 | | UM61512A-20 | | UM61512A-25 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write Cycle | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 15 | 20 | 20 | 25 | 25 | - | ns |
| $t_{CW}$ | Chip Enable to End of Write | 12 | 15 | 15 | 20 | 20 | - | ns |
| $t_{AS}$ | Address Setup Time of Write | 0 | 0 | 0 | 0 | 0 | - | ns |
| $t_{AW}$ | Address Valid to End of Write | 12 | 15 | 15 | 20 | 20 | - | ns |
| $t_{WP}$ | Write Pulse Width | 9 | - | 11 | - | - | - | ns |
| $t_{WR}$ | Write Recovery Time | 0 | - | 0 | - | - | - | ns |
| $t_{WHZ}$ | Write to Output in High Z | 0 | 8 | 0 | 13 | 13 | 13 | ns |
| $t_{DW}$ | Data to Write Time Overlap | 7 | - | 7 | - | - | - | ns |
| $t_{DH}$ | Data Hold from Write Time | 0 | - | 0 | - | - | - | ns |
| $t_{OW}$ | Output Active from End of Write | 5 | - | 5 | - | - | - | ns |

Notes: $t_{CHZ1}$, $t_{CHZ2}$, $t_{OHZ}$ and $t_{WHZ}$ are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

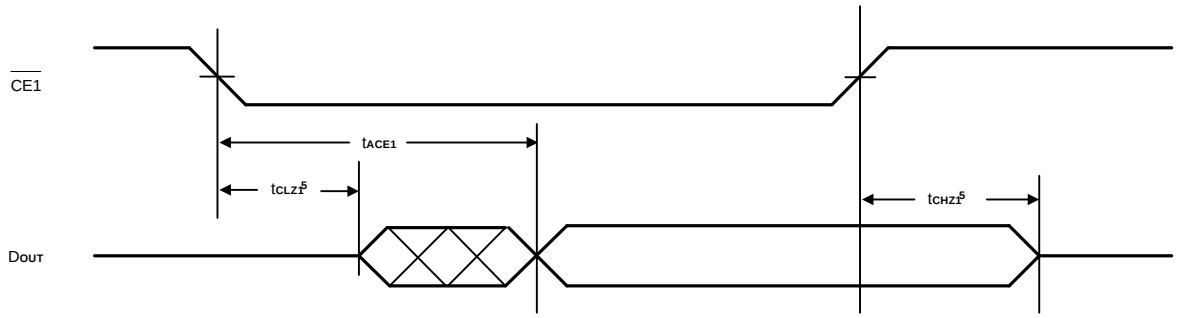
## Timing Waveforms

### Read Cycle 1 (1,2,4)

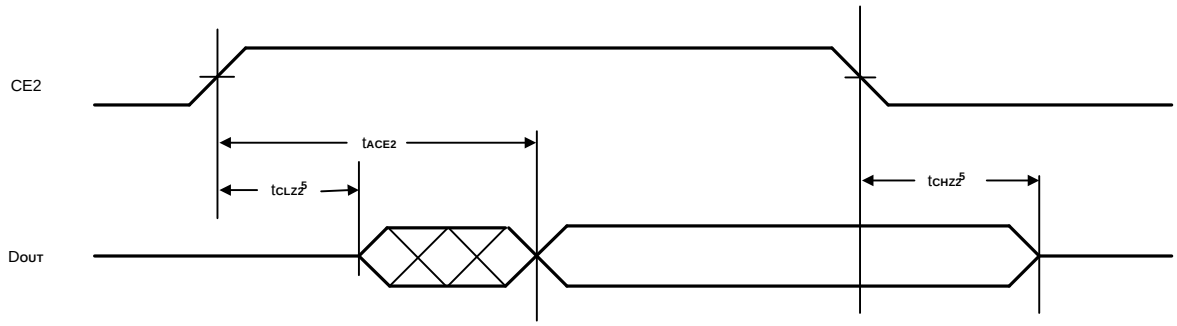


## Timing Waveforms (continued)

### Read Cycle 2 (1,3,4,6)

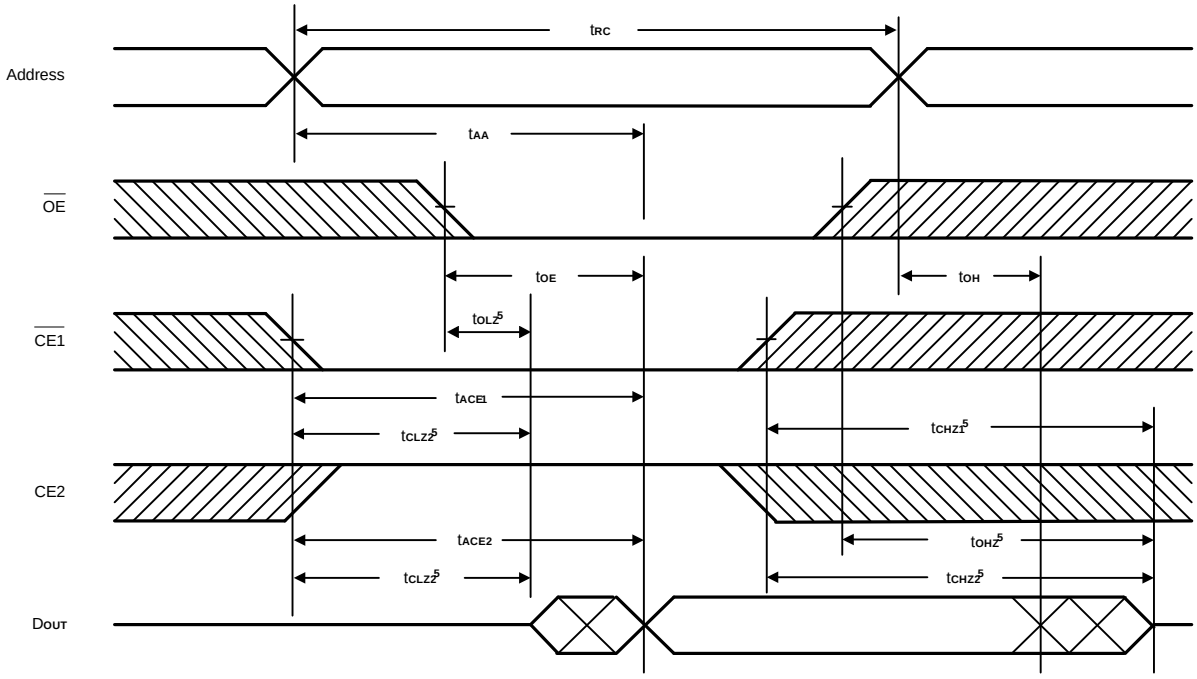



### Read Cycle 3 (1,4,7,8)



## Timing Waveforms (continued)

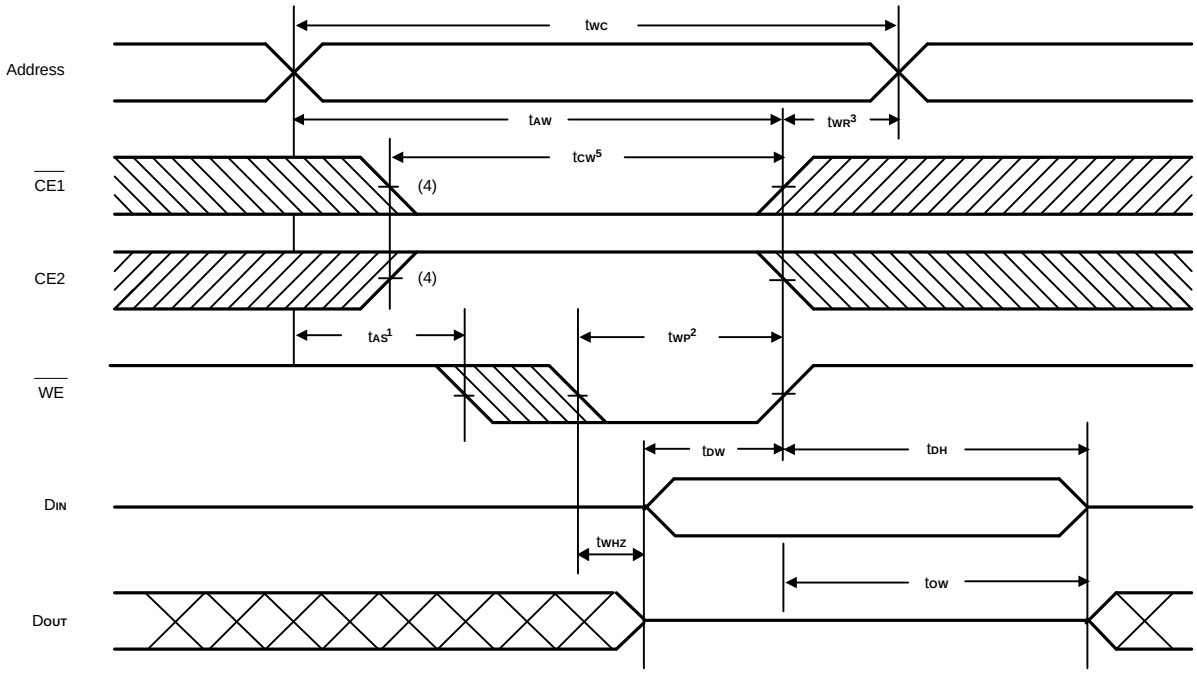
### Read Cycle 4[1)]




Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE1}$ = $V_{IL}$ and CE2 = $V_{IH}$.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
4. $\overline{OE}$ = $V_{IL}$.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high.
7. $\overline{CE1}$ is low.
8. Address valid prior to or coincident with CE2 transition high.

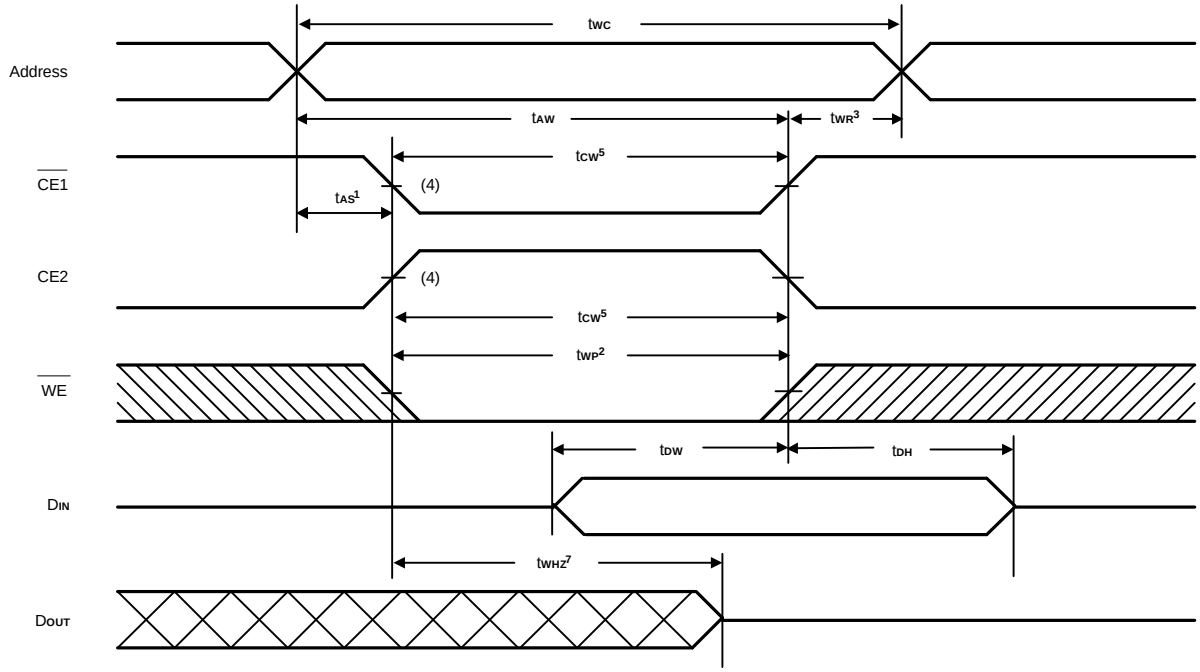
## Timing Waveforms (continued)

### Write Cycle 1[6]
### (Write Enable Controlled)



## Timing Waveforms (continued)

### Write Cycle 2
### (Chip Enable Controlled)




Notes: 1. $t_{AS}$ is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap ($t_{WP}$) of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. $t_{WR}$ is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low to the end of the Write cycle.
4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $t_{CW}$ is measured from the later of $\overline{CE}$ going low or CE2 going high to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = $V_{IL}$)
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

### AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Time | 5 ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Figures 1 and 2 |

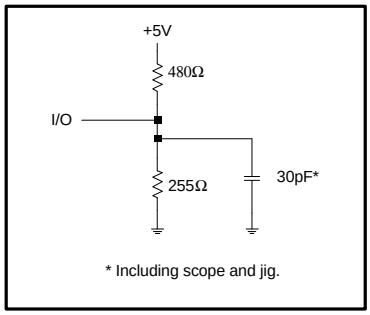



**Figure 1.Output Load**

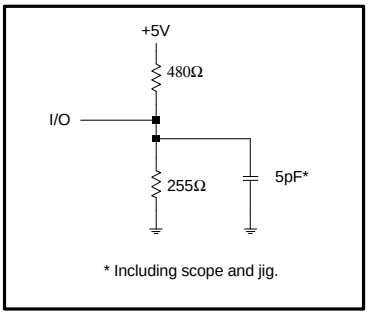
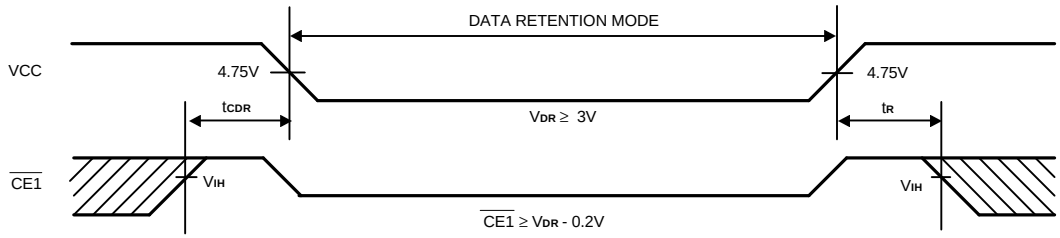



**Figure 2. Output Load for $t_{LZ1}$, $t_{CLZ2}$, $t_{OLZ}$, $t_{CHZ1}$, $t_{CHZ2}$, $t_{OHZ}$, $t_{WHZ}$, and $t_{OW}$**

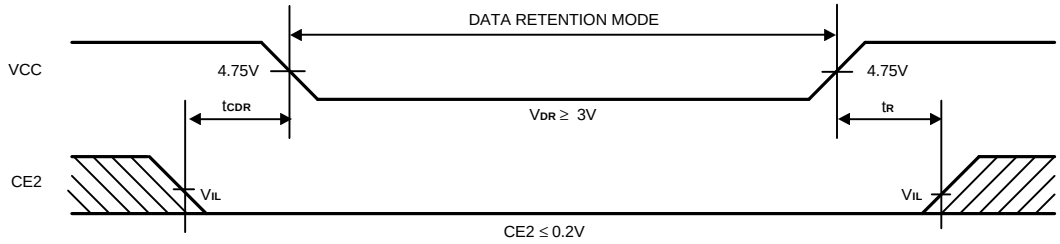
### Data Retention Characteristics ($T_A$ = 0°C to 70°C)

| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| $V_{DR1}$ | VCC for Data Retention | 3 | 5.25 | V | $\overline{CE1} \geq$ VCC - 0.2V<br>CE2 ≥ VCC - 0.2V or<br>CE2 ≤ 0.2V |
| $V_{DR2}$ | | 3 | 5.25 | V | CE2 ≤ 0.2V<br>$\overline{CE1} \geq$ VCC - 0.2V or<br>$\overline{CE1} \leq$ 0.2V |
| $I_{CCDR1}$ | Data Retention Current | - | 5 | mA | VCC = 3.0V<br>$\overline{CE1} \geq$ VCC - 0.2V<br>CE2 ≥ VCC - 0.2V<br>$V_{IN} \geq$ VCC - 0.2V or<br>$V_{IN} \leq$ 0.2V |
| $I_{CCDR2}$ | | - | 5 | mA | VCC = 3.0V<br>CE2 ≤ 0.2V<br>$\overline{CE1} \leq$ 0.2V<br>$V_{IN} \geq$ VCC - 0.2V or<br>$V_{IN} \leq$ 0.2V |
| $t_{CDR}$ | Chip Disable to Data Retention Time | 0 | - | ns | See Retention Waveform |
| $t_R$ | Operation Recovery Time | 5 | - | ms | |

### Low VCC Data Retention Waveform (1) ($\overline{CE1}$ Controlled)




### Low VCC Data Retention Waveform (2) (CE2 Controlled)



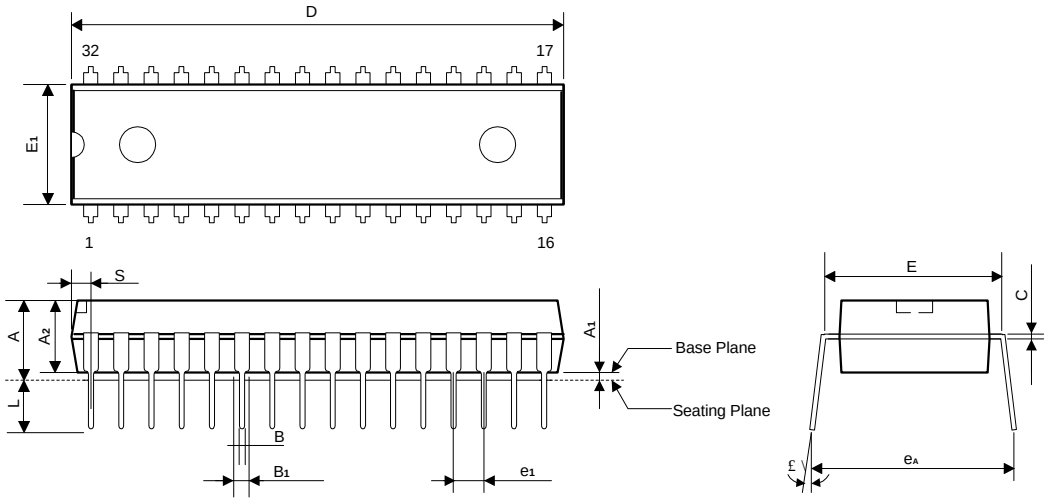

### Ordering Information

| Part No. | Access Time (ns) | Operating Current Max. (mA) | Standby Current Max. (mA) | Package |
|---|---|---|---|---|
| UM61512AK-15 | 15 | 160 | 10 | 32L SKINNY |
| UM61512AK-20 | 20 | 160 | 10 | 32L SKINNY |
| UM61512AS-15 | 15 | 160 | 10 | 32L SOJ (300 mil) |
| UM61512AS-20 | 20 | 160 | 10 | 32L SOJ (300 mil) |
| UM61512ASW-15 | 15 | 160 | 10 | 32L SOJ (400 mil) |
| UM61512ASW-20 | 20 | 160 | 10 | 32L SOJ (400 mil) |
| UM61512AM-25 | 25 | 160 | 10 | 32L SOP |
| UM61512AV-15 | 15 | 160 | 10 | 32L TSOP |

## Package Information

### SKINNY 32L Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | Dimensions in mm |
|---|---|---|
| A | 0.200 Max. | 5.08 Max. |
| $A_1$ | 0.015 Min. | 0.38 Min. |
| $A_2$ | 0.130 ¡ Ó.010 | 3.30 ¡ Ó.25 |
| B | 0.018 +0.004<br>-0.002 | 0.46 +0.10<br>-0.05 |
| $B_1$ | 0.050 +0.004<br>-0.002 | 1.27 +0.10<br>-0.05 |
| C | 0.010 +0.004<br>-0.002 | 0.25 +0.10<br>-0.05 |
| D | 1.600 Typ. (1.620 Max.) | 40.64 Typ. (41.15 Max.) |
| E | 0.310 ¡ Ó.010 | 7.87 ¡ Ó.25 |
| $E_1$ | 0.288 Typ. (0.300 Max.) | 7.32 Typ. (7.62 Max.) |
| $e_1$ | 0.100 ¡ Ó.007 | 2.54 ¡ Ó.18 |
| L | 0.130 ¡ Ó.010 | 3.30 ¡ Ó.25 |
| £ \ | 0° ~ 15° | 0° ~ 15° |
| $e_A$ | 0.355 ¡ Ó.035 | 9.02 ¡ Ó.89 |
| S | 0.059 Max. | 1.50 Max. |

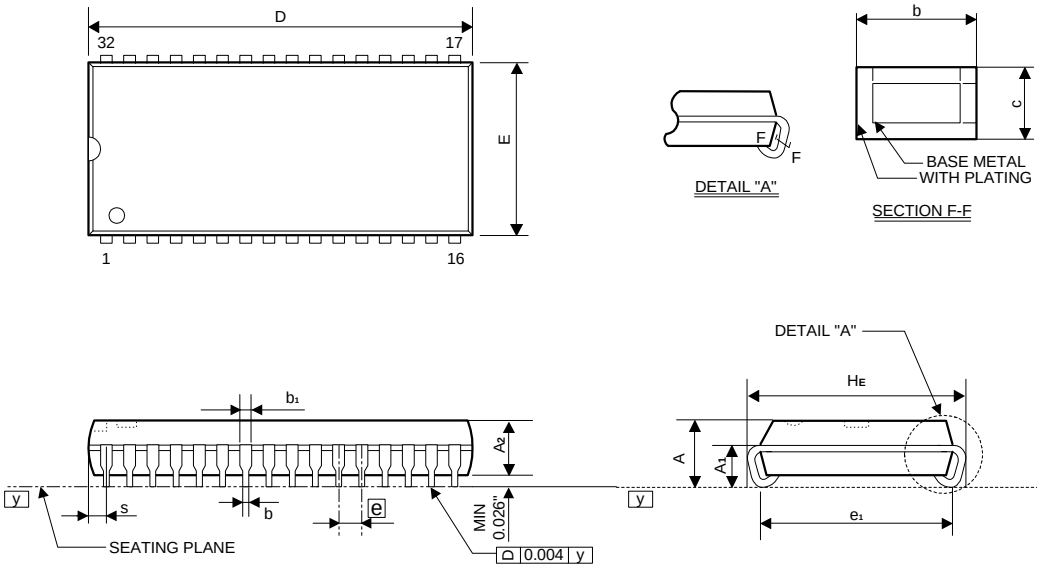
**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension $E_1$ does not include resin fins.
3. Dimension S includes end flash.

## Package Information

### SOJ 32/32LD (300mil BODY) Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | 0128 | 0.132 | 0.140 | 3.25 | 3.35 | 3.56 |
| $A_1$ | 0.052 | - | - | 2.08 | - | - |
| $A_2$ | 0.095 | 0.100 | 0.105 | 2.41 | 2.54 | 2.67 |
| b | 0.016 | 0.018 | 0.020 | 0.41 | 0.46 | 0.51 |
| $b_1$ | 0.026 | 0.028 | 0.032 | 0.66 | 0.71 | 0.81 |
| c | 0.006 | 0.008 | 0.012 | 0.15 | 0.20 | 0.30 |
| D | 0.820 | 0.825 | 0.830 | 20.83 | 20.96 | 21.08 |
| $H_E$ | 0.330 | 0.335 | 0.340 | 8.39 | 8.51 | 8.63 |
| E | 0.295 | 0.300 | 0.305 | 7.49 | 7.62 | 7.75 |
| $e_1$ | 0.260 | 0.267 | 0.274 | 6.61 | 6.78 | 6.96 |
| e | - | 0.050 | - | - | 1.27 | - |
| s | - | - | 0.048 | - | - | 1.22 |
| y | - | - | 0.004 | - | - | 0.10 |

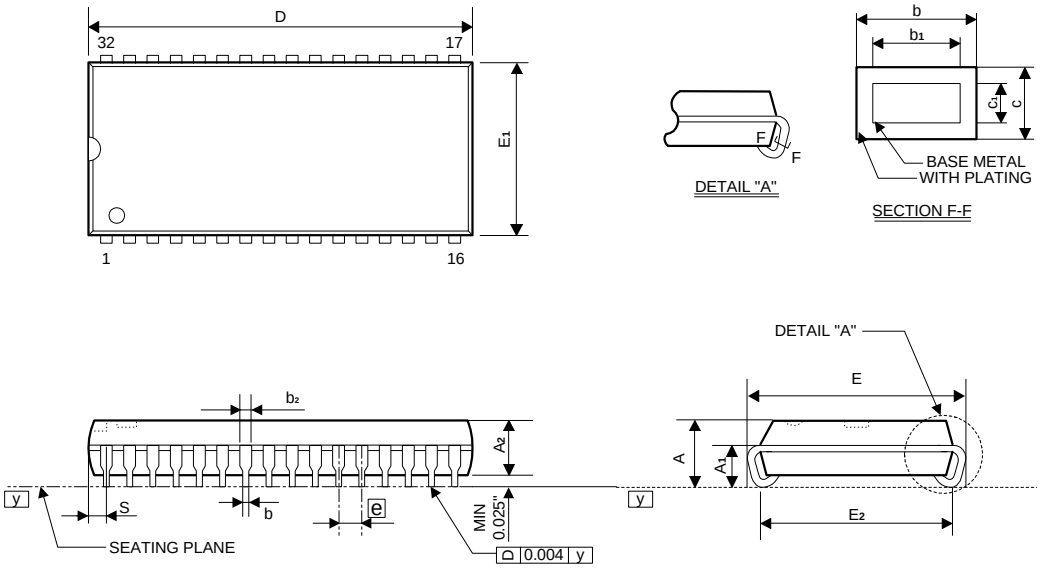
**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E doesn't include resin fins.
3. Dimension $e_1$ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

## Package Information

### SOJ 32/32LD (400mil BODY) Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | 0.131 | 0.138 | 0.145 | 3.35 | 3.51 | 3.68 |
| $A_1$ | 0.082 | - | - | 2.08 | - | - |
| $A_2$ | 0.105 | 0.110 | 0.115 | 2.67 | 2.79 | 2.91 |
| b | 0.016 | 0.018 | 0.020 | 0.41 | 0.46 | 0.51 |
| $b_2$ | 0.026 | 0.028 | 0.032 | 0.66 | 0.71 | 0.81 |
| c | 0.006 | 0.008 | 0.011 | 0.15 | 0.20 | 0.28 |
| D | 0.820 | 0.825 | 0.830 | 20.83 | 20.96 | 21.08 |
| E | 0.435 | 0.440 | 0.445 | 11.05 | 11.18` | 11.31 |
| $E_1$ | 0.395 | 0.400 | 0.405 | 10.03 | 10.16 | 10.29 |
| $E_2$ | 0.360 | 0.370 | 0.380 | 9.15 | 9.40 | 9.65 |
| e | - | 0.050 | - | - | 1.27 | - |
| S | - | - | 0.045 | - | - | 1.14 |
| y | - | - | 0.004 | - | - | 0.10 |

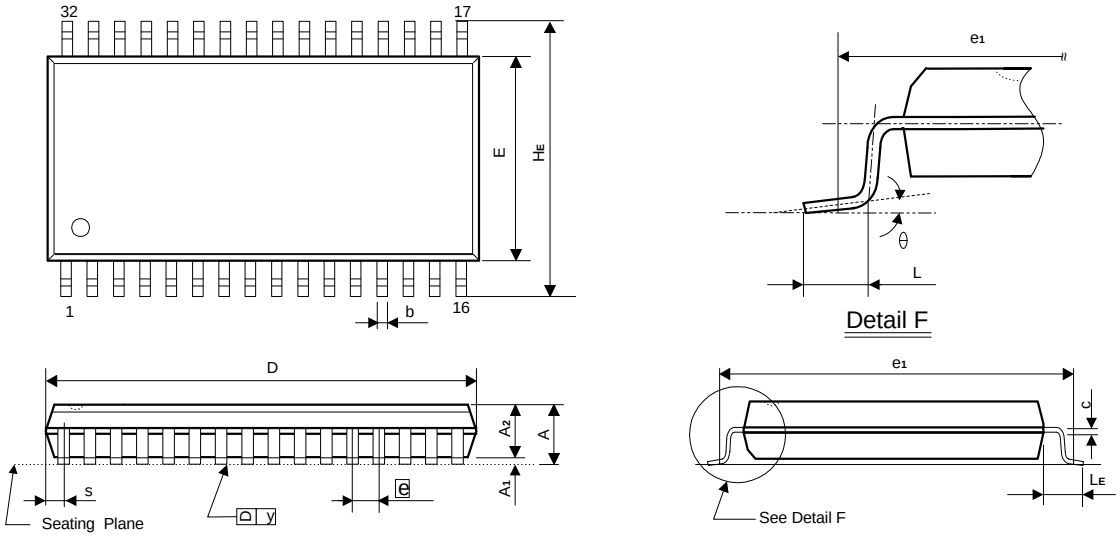
**Notes:**

1. Dimension D includes end flash.
2. Dimension E doesn't include resin fins.
3. Dimension $E_1$ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

## Package Information

### SOP (W.B.) 32L Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | Dimensions in mm |
|---|---|---|
| A | 0.118 Max. | 3.00 Max. |
| $A_1$ | 0.004 Min. | 0.10 Min. |
| $A_2$ | 0.106 ± 0.005 | 2.69 ± 0.13 |
| b | 0.016 +0.004 -0.002 | 0.41 +0.10 -0.05 |
| c | 0.008 +0.004 -0.002 | 0.20 +0.10 -0.05 |
| D | 0.805 Typ. (0.820 Max.) | 20.45 Typ. (20.83 Max.) |
| E | 0.445 ± 0.010 | 11.30 ± 0.25 |
| e | 0.050 ± 0.006 | 1.27 ± 0.15 |
| $e_1$ | 0.525 NOM. | 13.34 NOM. |
| $H_E$ | 0.556 ± 0.010 | 14.12 ± 0.25 |
| L | 0.031 ± 0.008 | 0.79 ± 0.20 |
| $L_E$ | 0.055 ± 0.008 | 1.40 ± 0.20 |
| S | 0.044 Max. | 1.12 Max. |
| y | 0.004 Max. | 0.10 Max. |
| θ | 0° ~ 10° | 0° ~ 10° |

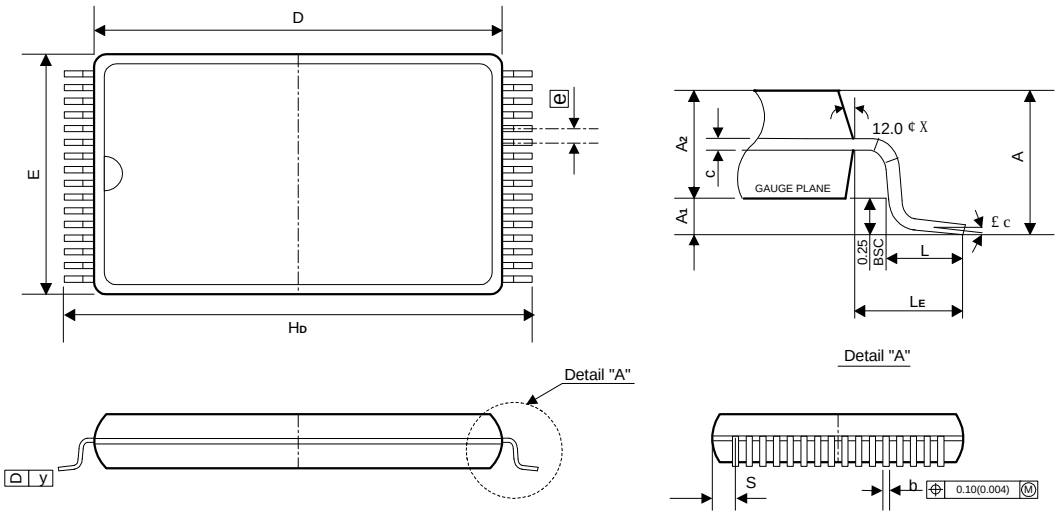
**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension $e_1$ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

## Package Information

### TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | Dimensions in mm |
|---|---|---|
| A | 0.047 Max. | 1.20 Max. |
| A1 | 0.004 ¡ Ó.002 | 0.10 ¡ Ó.05 |
| A2 | 0.039 ¡ Ó.002 | 1.00 ¡ Ó.05 |
| b | 0.008 ¡ Ó.001 | 0.20 ¡ Ó.03 |
| c | 0.006 ¡ Ó.001 | 0.15 ¡ Ó.02 |
| D | 0.724 ¡ Ó.004 | 18.40 ¡ Ó.10 |
| E | 0.315 ¡ Ó.004 | 8.00 ¡ Ó.10 |
| e | 0.020 TYP. | 0.50 TYP. |
| HD | 0.787 ¡ Ó.007 | 20.00 ¡ Ó.20 |
| L | 0.020 ¡ Ó.004 | 0.50 ¡ Ó.10 |
| LE | 0.031 TYP. | 0.80 TYP. |
| S | 0.0167 TYP. | 0.425 TYP. |
| Y | 0.004 Max. | 0.10 Max. |
| θ | 0° ~ 6° | 0° ~ 6° |

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension $e_1$ is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.