

TEMIC

Siliconix

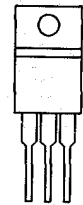
SMP40N10

N-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
100	0.040	40

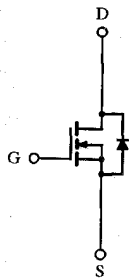
TO-220AB



G D S

Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings ( $T_C = 25^\circ\text{C}$  Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$T_C = 25^\circ\text{C}$	$I_D$	40	A
	$T_C = 100^\circ\text{C}$		25	
Pulsed Drain Current		$I_{DM}$	160	
Avalanche Current		$I_{AR}$	40	
Avalanche Energy		$E_A$	240	mJ
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	40	
Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	125	W
	$T_C = 100^\circ\text{C}$		60	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Lead Temperature ( $1/16''$ from case for 10 sec.)		$T_L$	300	

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N-/P-Channel  
MOSFETs

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	$R_{thJA}$		80	$^\circ\text{C/W}$
Junction-to-Case	$R_{thJC}$		1.0	
Case-to-Sink	$R_{thCS}$	1.0		

Notes:

a. Duty cycle  $\leq 1\%$

### Specifications ( $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0		4.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			25	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C			250	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	40			A
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A		0.030	0.040	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 125°C		0.055	0.072	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A	15	20		S
Dynamic						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		3000		pF
Output Capacitance	C <sub>oss</sub>			750		
Reverse Transfer Capacitance	C <sub>rss</sub>			150		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A		62	80	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			20	30	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			26	35	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 1.25 Ω I <sub>D</sub> = 40 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 5 Ω		17	30	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			80	120	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			40	60	
Fall Time <sup>c</sup>	t <sub>f</sub>			20	40	
Source-Drain Diode Ratings and Characteristics (T <sub>C</sub> = 25°C)						
Continuous Current	I <sub>S</sub>				40	A
Pulsed Current	I <sub>SM</sub>				180	
Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V			1.8	V
Reverse Recovery Time	t <sub>rr</sub>			120	250	ns
Reverse Recovery Charge	Q <sub>rr</sub>			0.3		μC

**Notes:**

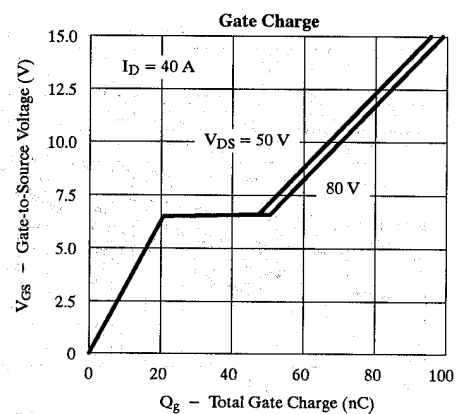
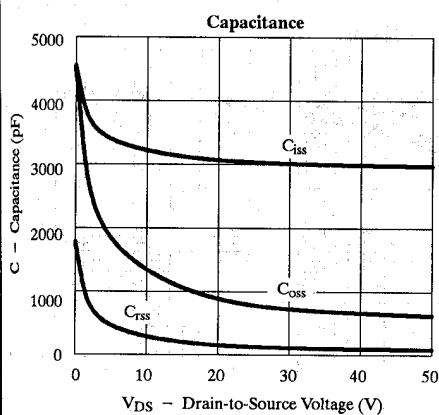
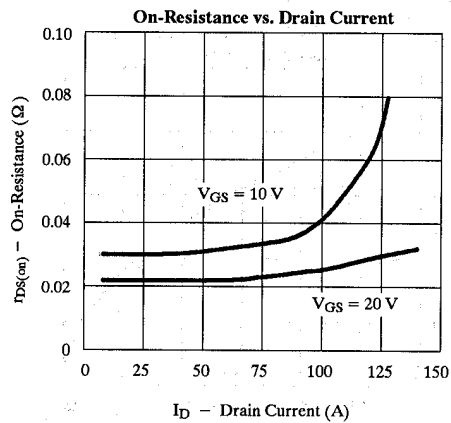
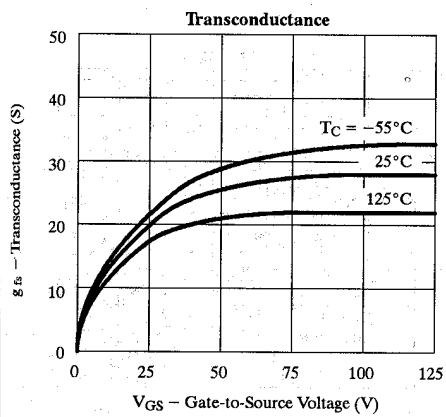
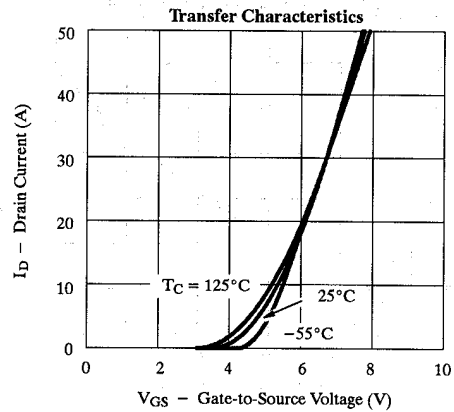
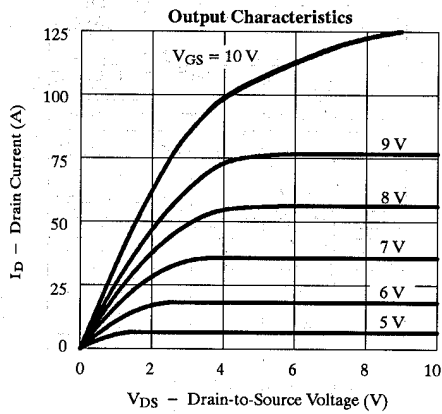
- For design aid only; not subject to production testing.
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Independent of operating temperature.

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## SMP40N10

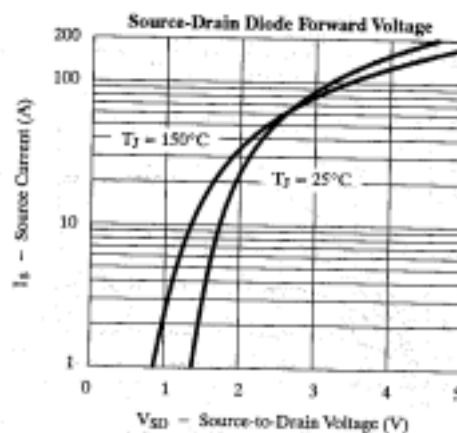
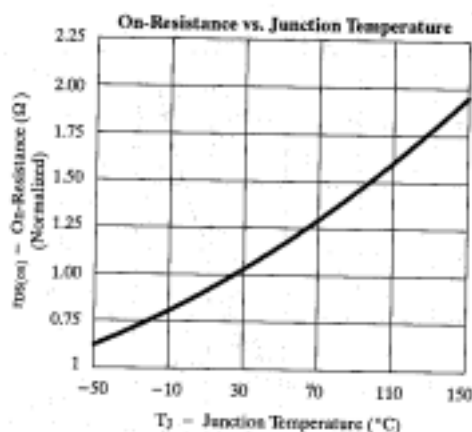
Typical Characteristics (25°C Unless Otherwise Noted)



## SMP40N10

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### Typical Characteristics (25°C Unless Otherwise Noted)



### Thermal Ratings

