

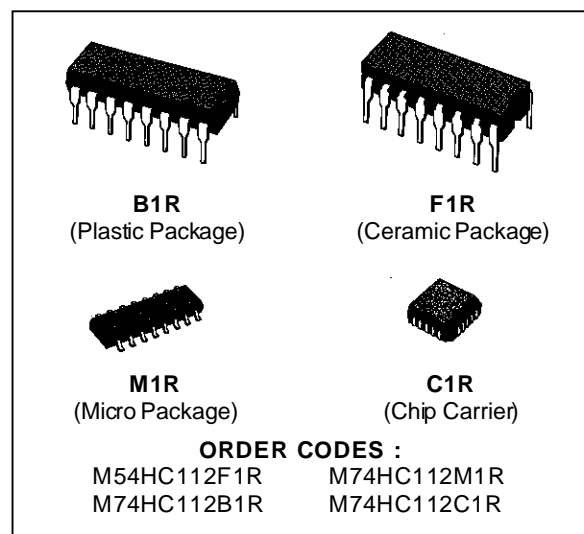
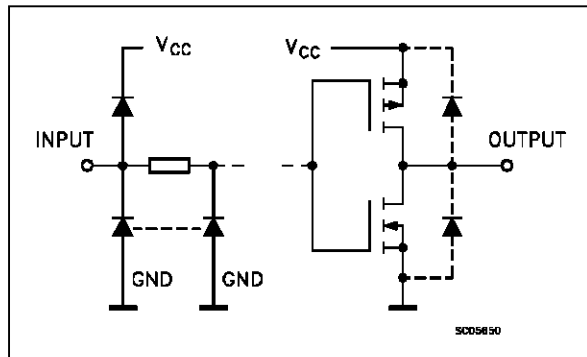
DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED
 $f_{MAX} = 67 \text{ MHz (TYP.) AT } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION
 $I_{CC} = 2 \mu\text{A AT } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- OUTPUT DRIVE CAPABILITY
10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = |I_{OL}| = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 $V_{CC} \text{ (OPR)} = 2 \text{ V TO } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE
WITH 54/74LS112

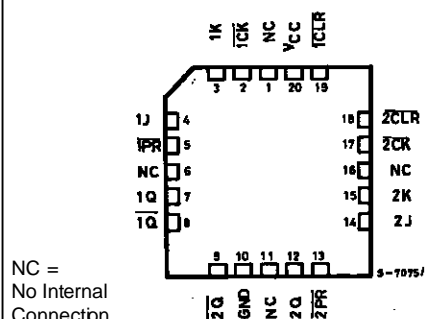
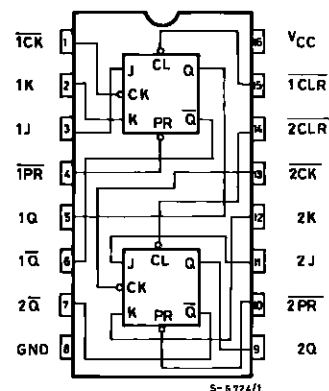
DESCRIPTION

The M54/74HC112 is a high speed CMOS DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54HC112/M74HC112 dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs for each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will function as shown in the truth table. Input data is transferred to the input on the negative going edge of the clock pulse. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN CONNECTIONS (top view)



NC =
No Internal
Connection

TRUTH TABLE

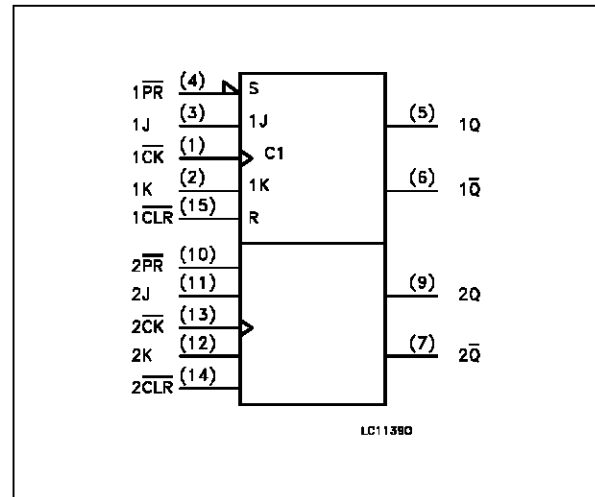
INPUTS					OUTPUTS		FUNCTION
CLR	PR	J	K	CK	Q	\bar{Q}	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	\downarrow	Q_n	\bar{Q}_n	NO CHANGE
H	H	H	L	\downarrow	H	L	
H	H	L	H	\downarrow	L	H	
H	H	H	H	\downarrow	\bar{Q}_n	Q_n	TOGGLE
H	H	X	X	\downarrow	Q_n	\bar{Q}_n	NO CHANGE

X: Don't Care

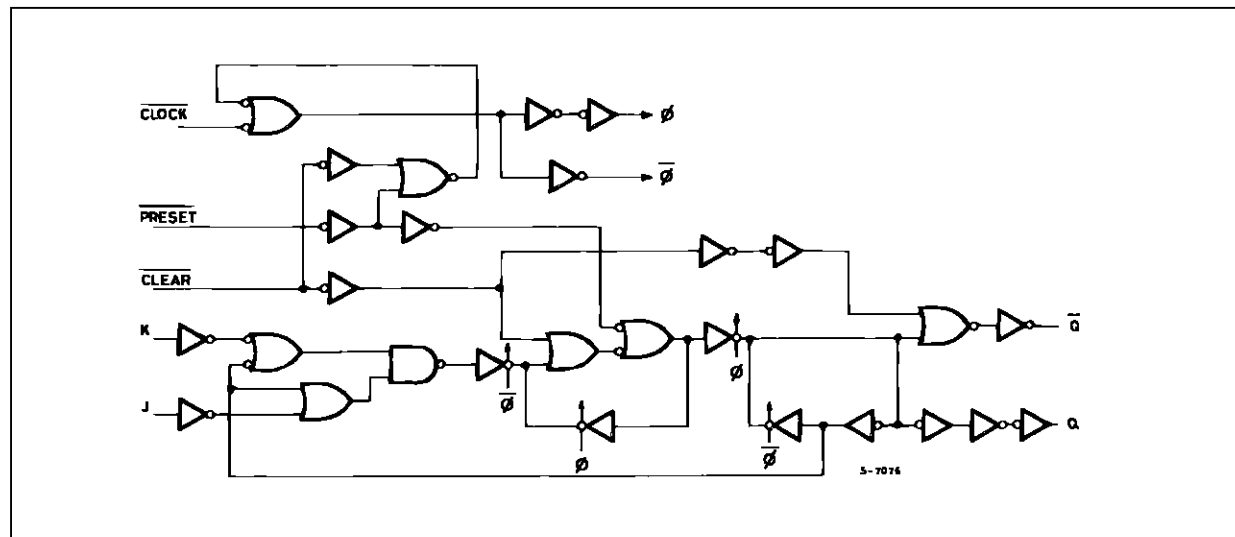
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{1CK}, \overline{2CK}$	Clock Input (HIGH to LOW edge triggered)
2, 12	1K, 2K	Data Inputs: Flip-Flop 1 and 2
3, 11	1J, 2J	Data Inputs: Flip-Flop 1 and 2
4, 10	$\overline{1PR}, \overline{2PR}$	Set Inputs
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 7	$\overline{1Q}, \overline{2Q}$	Complement Flip-Flop Outputs
15, 14	$\overline{1CLR}, \overline{2CLR}$	Reset inputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\equiv 65^\circ\text{C}$ derate to 300 mW by 10mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: M54HC Series M74HC Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6\text{ V}$	0 to 1000 0 to 500 0 to 400
			ns

DC SPECIFICATIONS

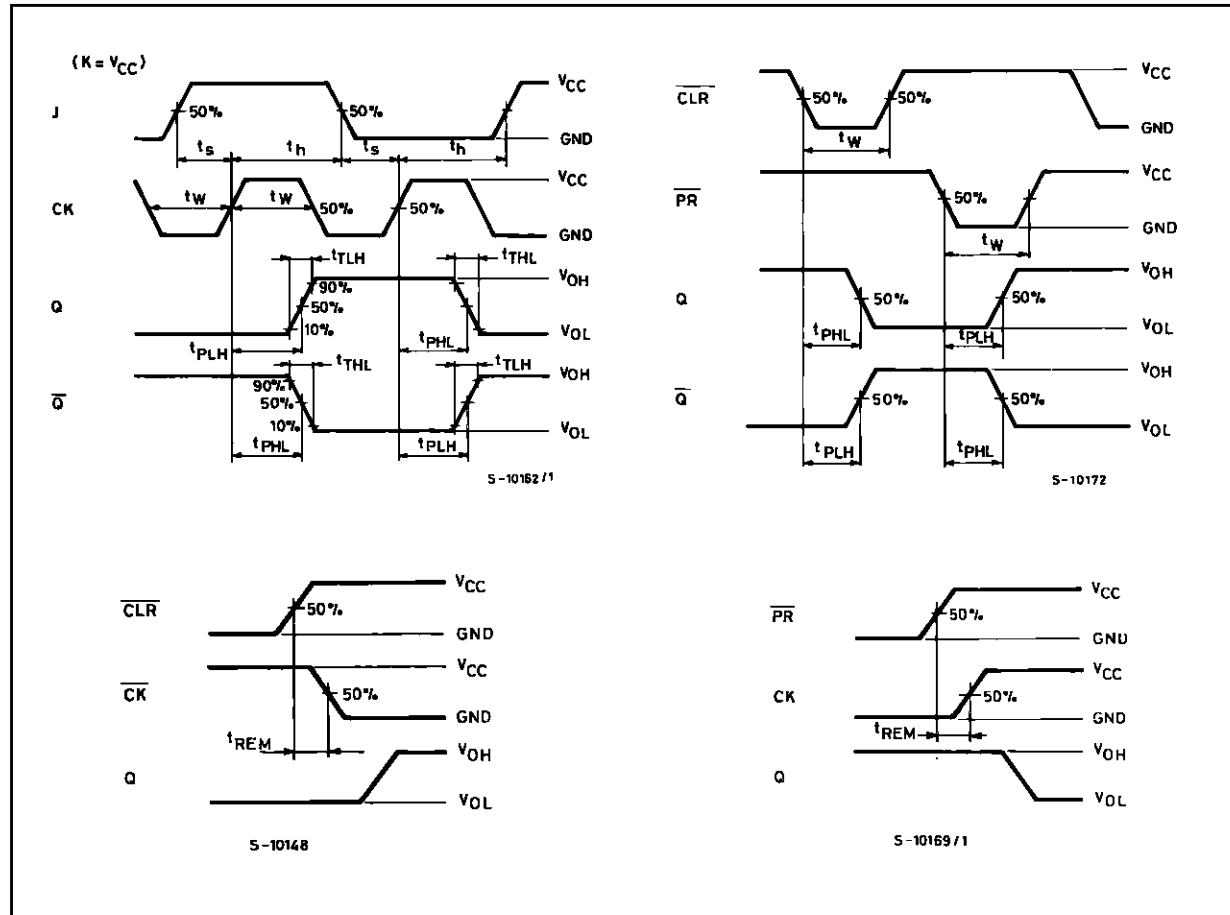
Symbol	Parameter	Test Conditions			Value						Unit	
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5					3.15		3.15			
		6.0					4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5		V
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O =-20 μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I _O =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0		I _O =-5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I _O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0		I _O = 5.2 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			2		20		40	μA	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

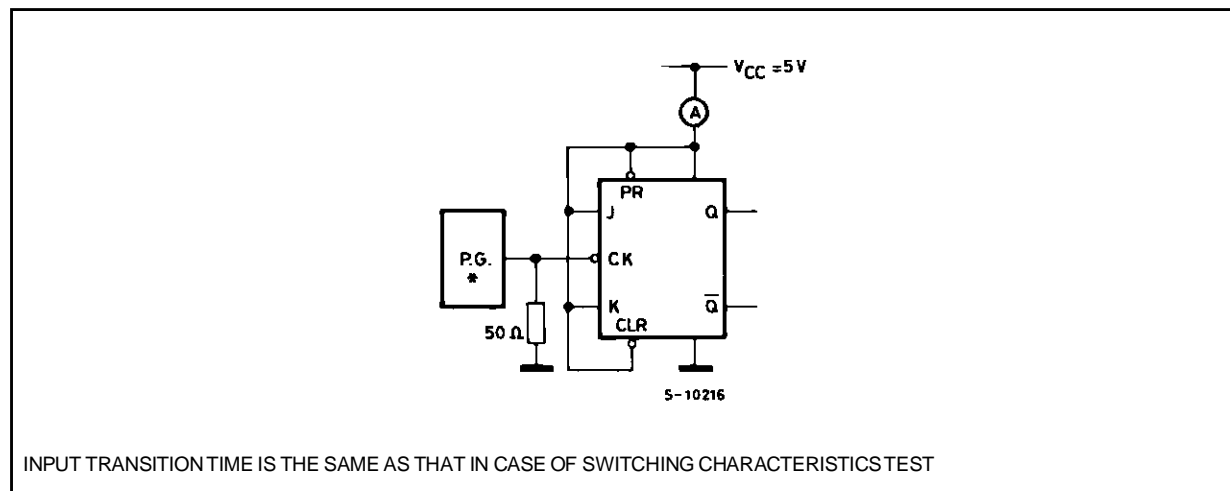
Symbol	Parameter	Test Conditions		Value						Unit	
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _{PLH} t _{PHL}	Propagation Delay Time (CK - Q, \overline{Q})	2.0			52	125		155		190	ns
		4.5			16	25		31		38	
		6.0			14	21		26		32	
t _{PLH} t _{PHL}	Propagation Delay Time (CLR, PR - Q, \overline{Q})	2.0			68	135		170		205	ns
		4.5			17	27		34		41	
		6.0			14	23		29		35	
f _{MAX}	Maximum Clock Frequency	2.0			8	16		6.4		5.4	MHz
		4.5			40	68		32		27	
		6.0			47	79		38		32	
t _{W(H)} t _{W(L)}	Minimum Pulse Width (CLOCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t _{W(L)}	Minimum Pulse Width (CLR, \overline{PR})	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t _s	Minimum Set-up Time	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t _h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t _{REM}	Minimum Removal Time (CLR, PR)	2.0			24	50		60		70	ns
		4.5			4	10		12		14	
		6.0			3	9		10		12	
C _{IN}	Input Capacitance				5	10		10		10	pF
C _{PD} (*)	Power Dissipation Capacitance				33						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM



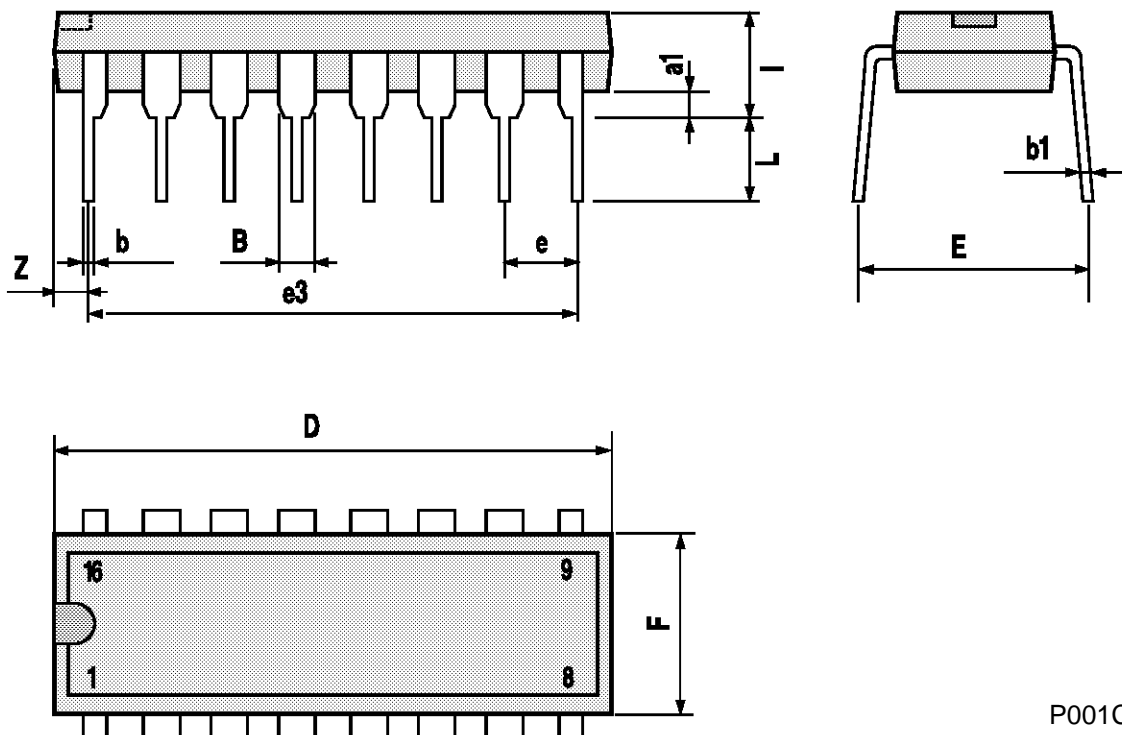
TEST CIRCUIT (Opr.)



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

Plastic DIP16 (0.25) MECHANICAL DATA

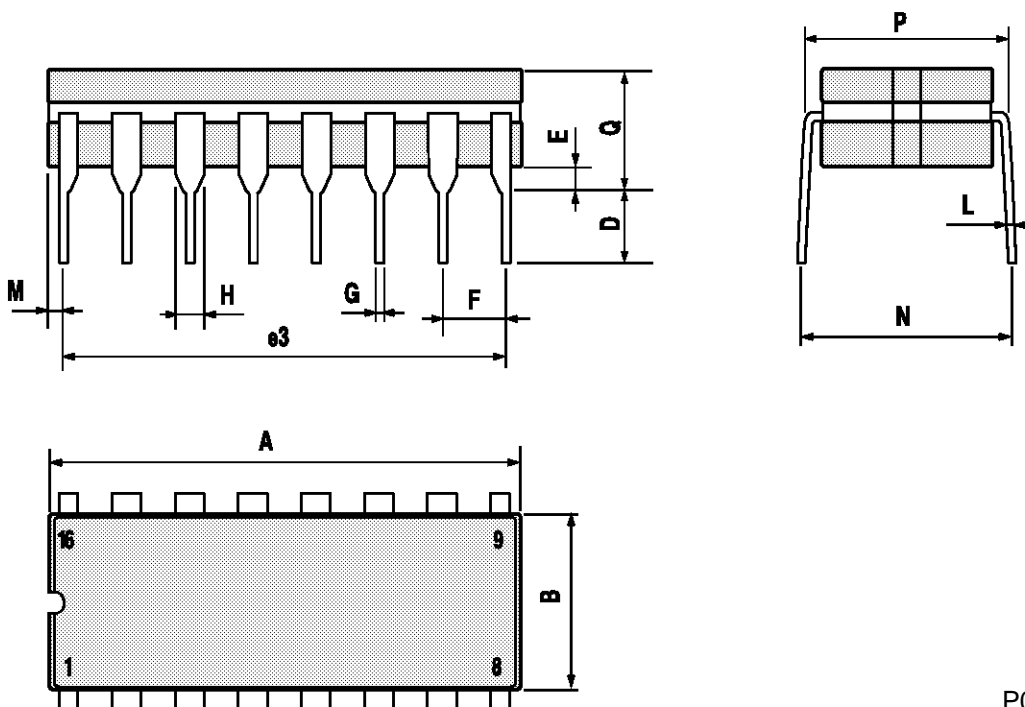
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

Ceramic DIP16/1 MECHANICAL DATA

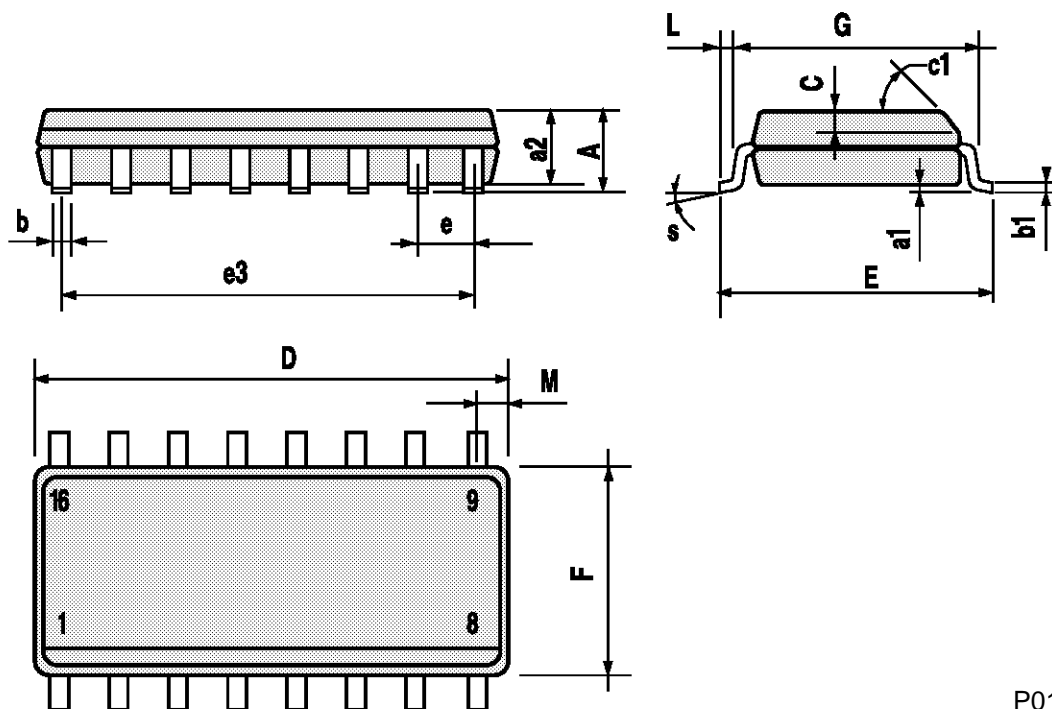
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



P053D

SO16 (Narrow) MECHANICAL DATA

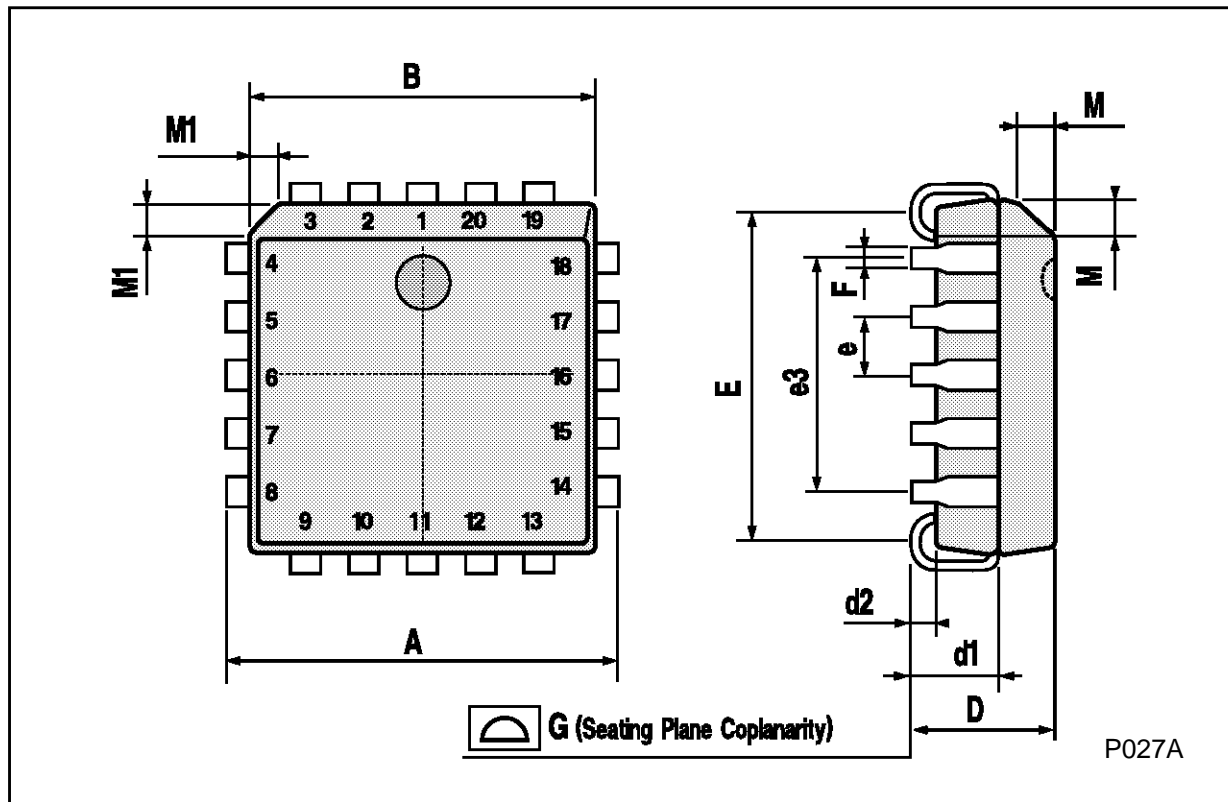
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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