

DUAL 4-INPUT NAND GATE

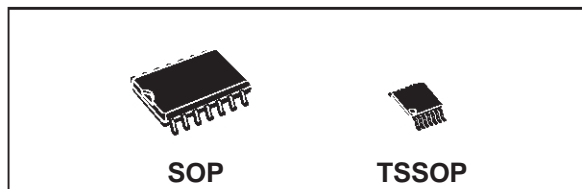
- HIGH SPEED: $t_{PD} = 5 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 2 \mu A$ (MAX.) at $T_A = 25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS:
 $V_{IH} = 2V$ (MIN), $V_{IL} = 0.8V$ (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 20
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74VHCT20A is an advanced high-speed CMOS DUAL 4-INPUT NAND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

The internal circuit is composed of 3 stages

PRELIMINARY DATA



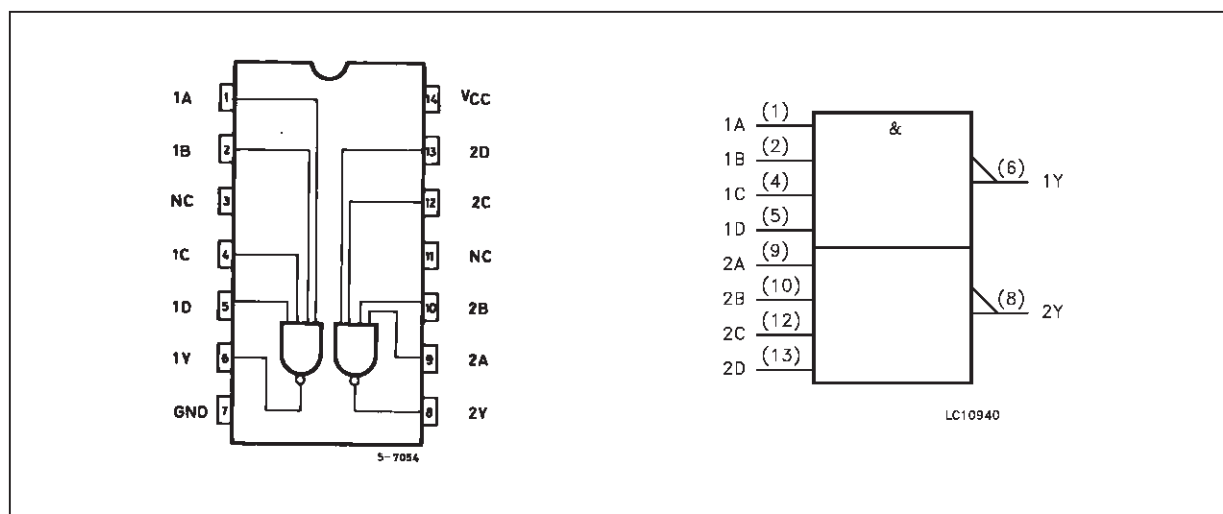
ORDER CODES		
PACKAGE	TUBE	T & R
SOP	74VHCT20AM	74VHCT20AMTR
TSSOP		74VHCT20ATTR

including buffer output, which provide high noise immunity and stable output.

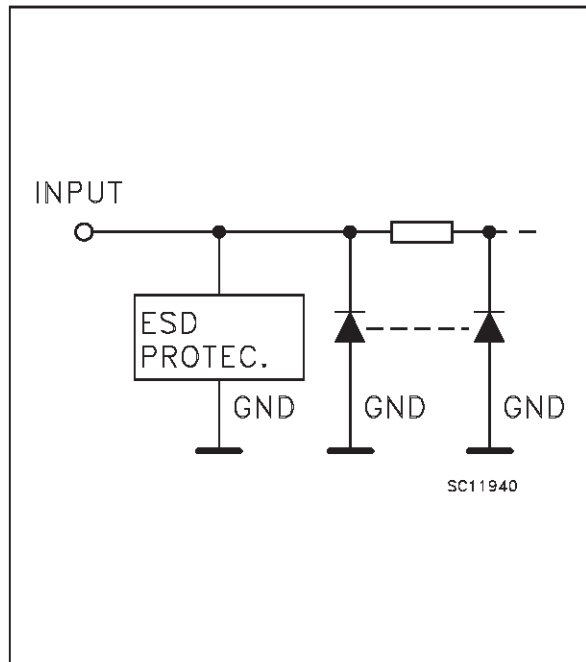
Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 9	1A to 2A	Data Inputs
2, 10	1B to 2B	Data Inputs
3, 11	N.C.	Not Connected
4, 12	1C to 2C	Data Inputs
5, 13	1D to 2D	Data Inputs
6, 8	1Y to 2Y	Data Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

TRUTH TABLE

A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

X: "H" or "L"

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage (see note 1)	-0.5 to +7.0	V
V _O	DC Output Voltage (see note 2)	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

1) V_{CC} = 0V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	4.5 to 5.5	V
V _I	Input Voltage	0 to 5.5	V
V _O	Output Voltage (see note 1)	0 to 5.5	V
V _O	Output Voltage (see note 2)	0 to V _{CC}	V
T _{op}	Operating Temperature	-40 to +85	°C
dt/dv	Input Rise and Fall Time (see note 3) (V _{CC} = 5.0 ± 0.5V)	0 to 20	ns/V

1) V_{CC} = 0V

2) High or Low State

3) V_{IN} from 0.8V to 2 V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	4.5 to 5.5		2			2		V
V _{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8	V
V _{OH}	High Level Output Voltage	4.5	I _O =-50 μA	4.4	4.5		4.4		V
		4.5	I _O =-8 mA	3.94			3.8		
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.0	0.1		0.1	V
		4.5	I _O =8 mA			0.36		0.44	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			2		20	μA
ΔI _{CC}	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V _{CC} or GND			1.35		1.5	mA
I _{OPD}	Output Leakage Current	0	V _{OUT} = 5.5V			0.5		5.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3 ns)

Symbol	Parameter	Test Condition			Value					Unit
		V _{CC} (*) (V)	C _L (pF)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay Time	5.0	15			5.0	7.0	1.0	8.0	ns
t _{PHL}		5.0	50			5.5	8.0	1.0	9.0	

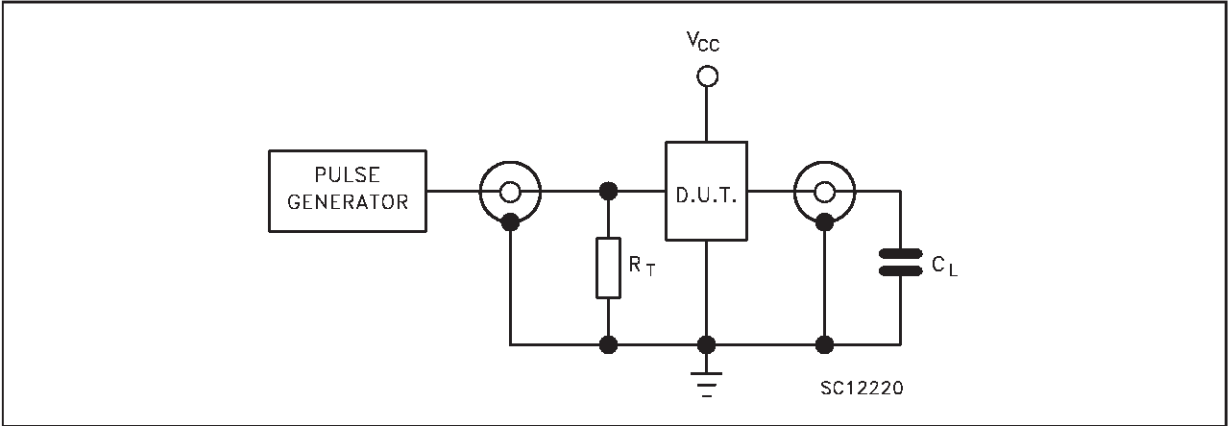
(*) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T _A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance			6	10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)			14				pF

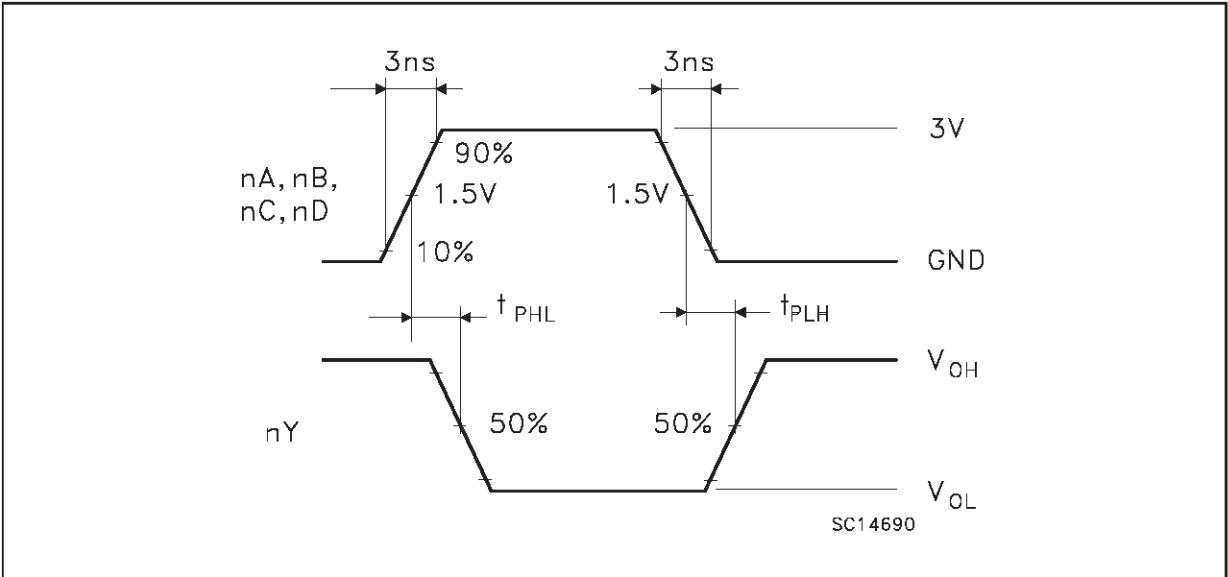
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(oper)} = C_{PD} • V_{CC} • f_{IN} + I_{CC}/2 (per Gate)

TEST CIRCUIT



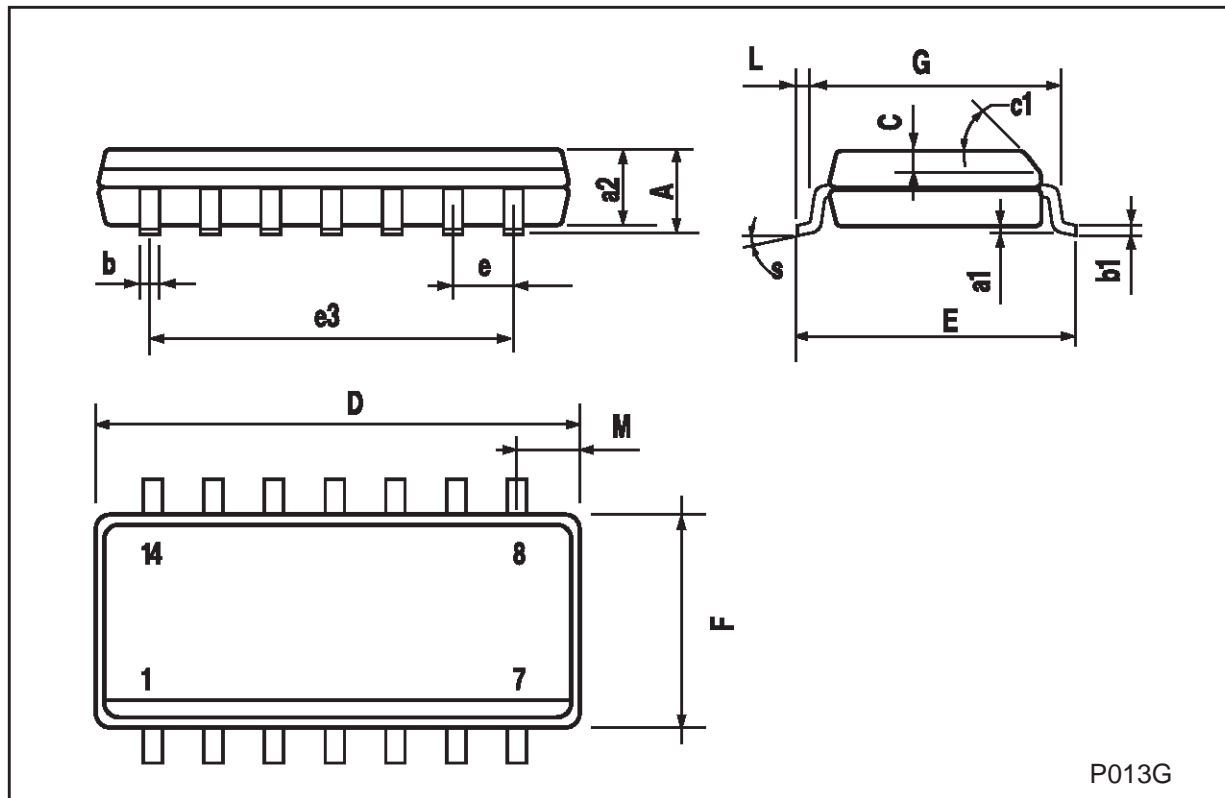
$C_L = 15/50$ pF or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)



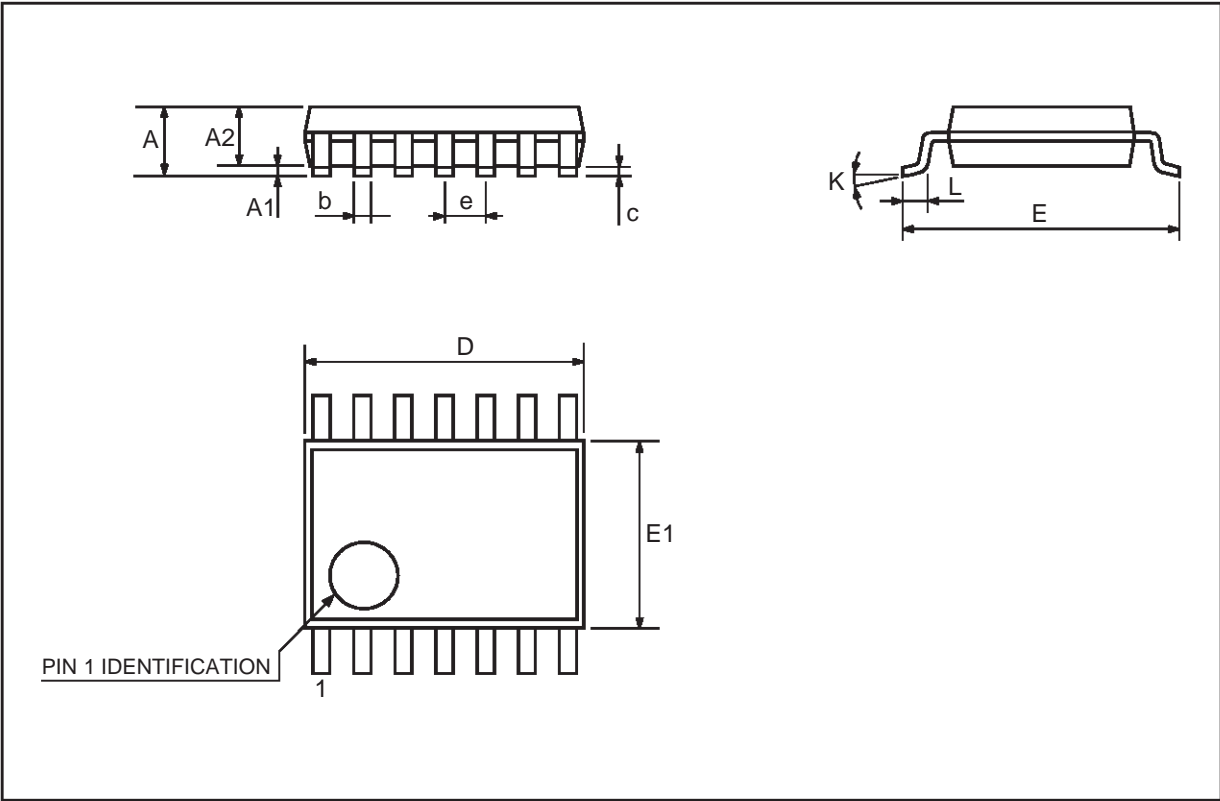
SO-14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



TSSOP14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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