4/30/98

SS8203

MICROCONTROLLER

External Specification

PRELIMINARY (V 1.1BA)

Siliconians, Inc.
4701 Patrick Henry Drive, Suite 501, Santa Clara, CA 95054
Tel: 408-748-8600 Fax: 408-748-8687
www.siliconians.com or info@siliconians.com

Table of Contents

Features

O CPU Industry standard 8051 code compatable
- Extensive boolean processing (single bit logic) capabilities
- Arithmetic 8 bit including multiply and divide
- Jumps, 8/16 bit address, conditional and unconditional
- Logical separation of program and data memory
- Six addressing modes

O Memory SS8203A
- 32K byte internal Flash electrically erasable eprom program memory
- 256 byte internal data memory (IRAM)
- 256 byte internal auxilliary data memory (XRAM)
- External Data RAM access allowed
- External Program ROM access allowed

O Timers
- Watch-Dog Timer: 1 CH x 8 bit, reset or interrupt
- Watch & Buzzer: 1K/2K/4KHz Buzzer output, 1Sec/1Min/1Hour interrupt
- Time Base Timer: 1 CH x 8 bit, Auto-Reload, 125mS/1Sec/1Min/1Hour input
- PWM Timer: 3 CH x 8 bit, Event Counter, PWM or 50% duty output
- Capture timer: 2 CH x 16 bit, Event Counter, Capture on input edge

O SIO
- SIO-1: 8-bit/16-bit transfer
- SIO-2: 8-bit transfer

O A/D Converter
- 8 bit resolution
- 10 channel analog input port

O Interrupt
- Six external interrupt input pins (IRQ0 to IRQ5)
- Eleven internal interrupt sources (Timer: 8, SIO: 2, ADC: 1)

O I/O Ports
- Standard I/O pins: 40
- Standard output pins: 4
- High current sink I/O pins for LED: 8

O Low Power Operation Modes
- StopAll Mode: CPU and peripherals halted. Register and RAM contents retained.
- SlowAll Mode: CPU and peripherals reduce clock rate from 12Mhz to 32khz.
- FastPeri Mode: CPU halts and peripherals continue to clock at 12Mhz.

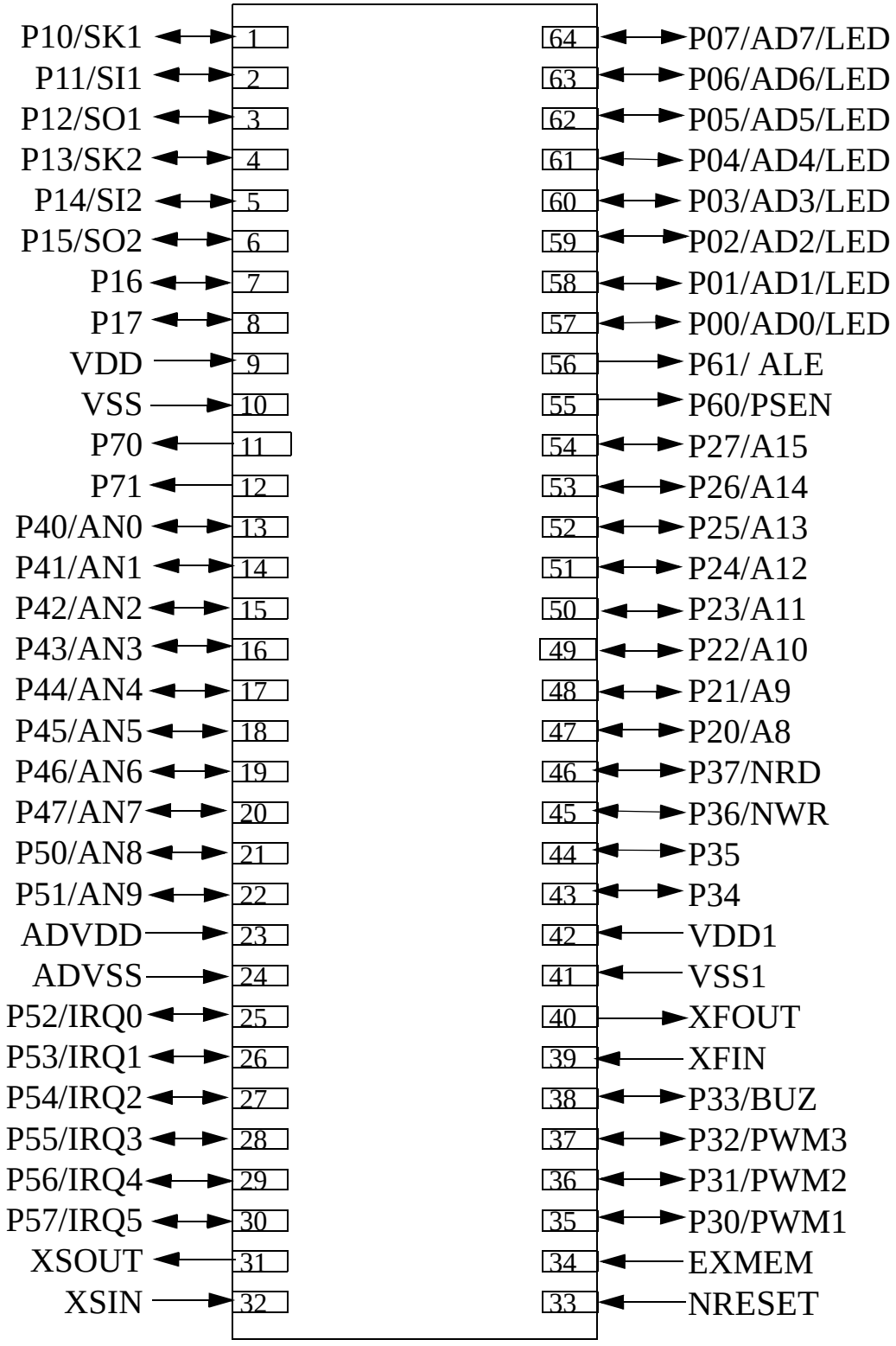
- SlowPeri Mode: CPU halts and peripherals reduce clock to 32khz.
- HIZ State: All pins except bus pins become high-impedance state.

Description

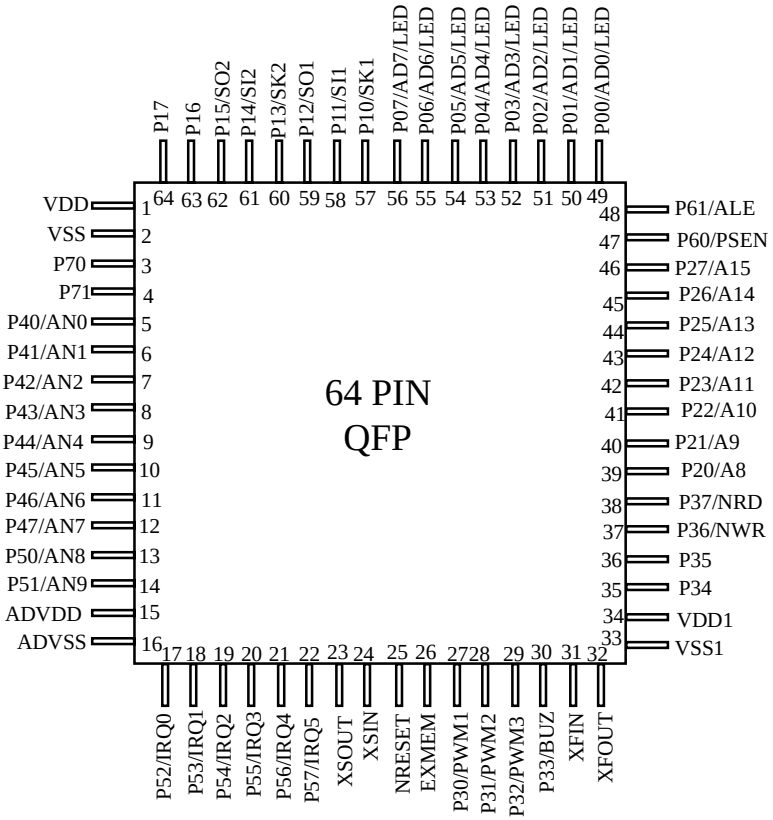
The SS8203A is a high performance CMOS 8-bit microcontroller with 32Kbytes of Flash programmable and erasable read only memory. The device uses the industry standard 8051 instruction set with an extensive set of peripherals to provide user with a powerful solution for consumer appliance applications. The Silconians SS8203A also provides the user with 256 bytes of additional onchip data memory accessible by the MOVX command(XRAM). This makes a total of 512 bytes of onchip data ram. The versatile design also allows the user to access additional external program rom or data ram up to 64Kbytes.

The extensive SS8203A peripheral set includes 32Kbyte Flash electrically erasable eprom, 512 bytes data RAM, 40 I/O lines, two serial I/O, two 16 bit timers and six 8 bit timers. In addition there is a 10 channel 8 bit A/D, and 17 two level vectored interrupts. The SS8203A is designed for low power with 5 power saving programmable modes using two on-chip oscillators at 12Mhz and 32Khz and the CPU halt mode.

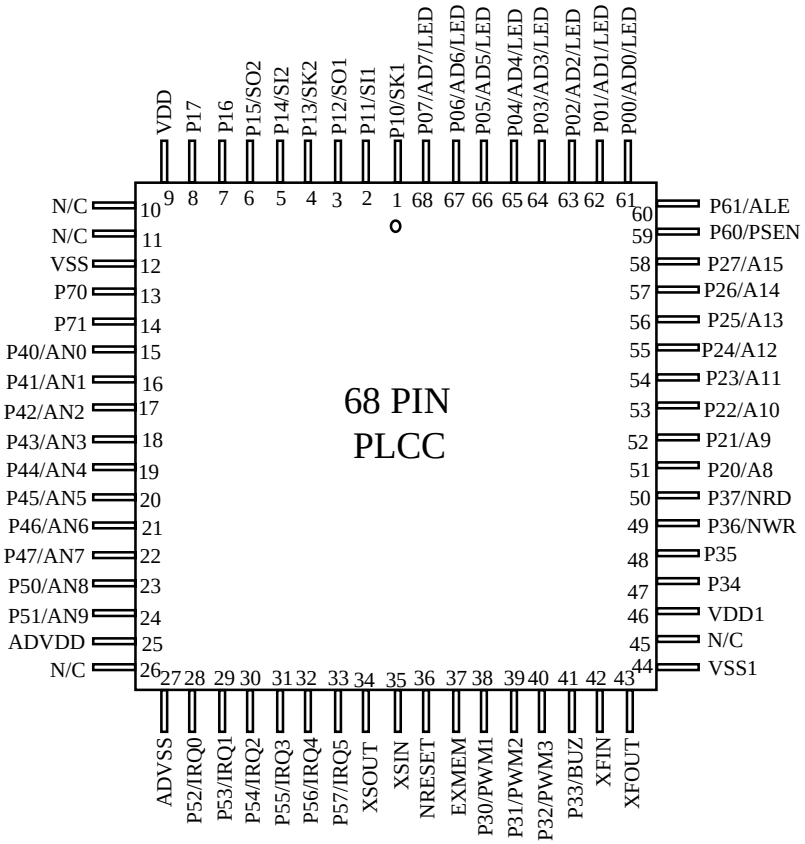
PIN CONFIGURATION



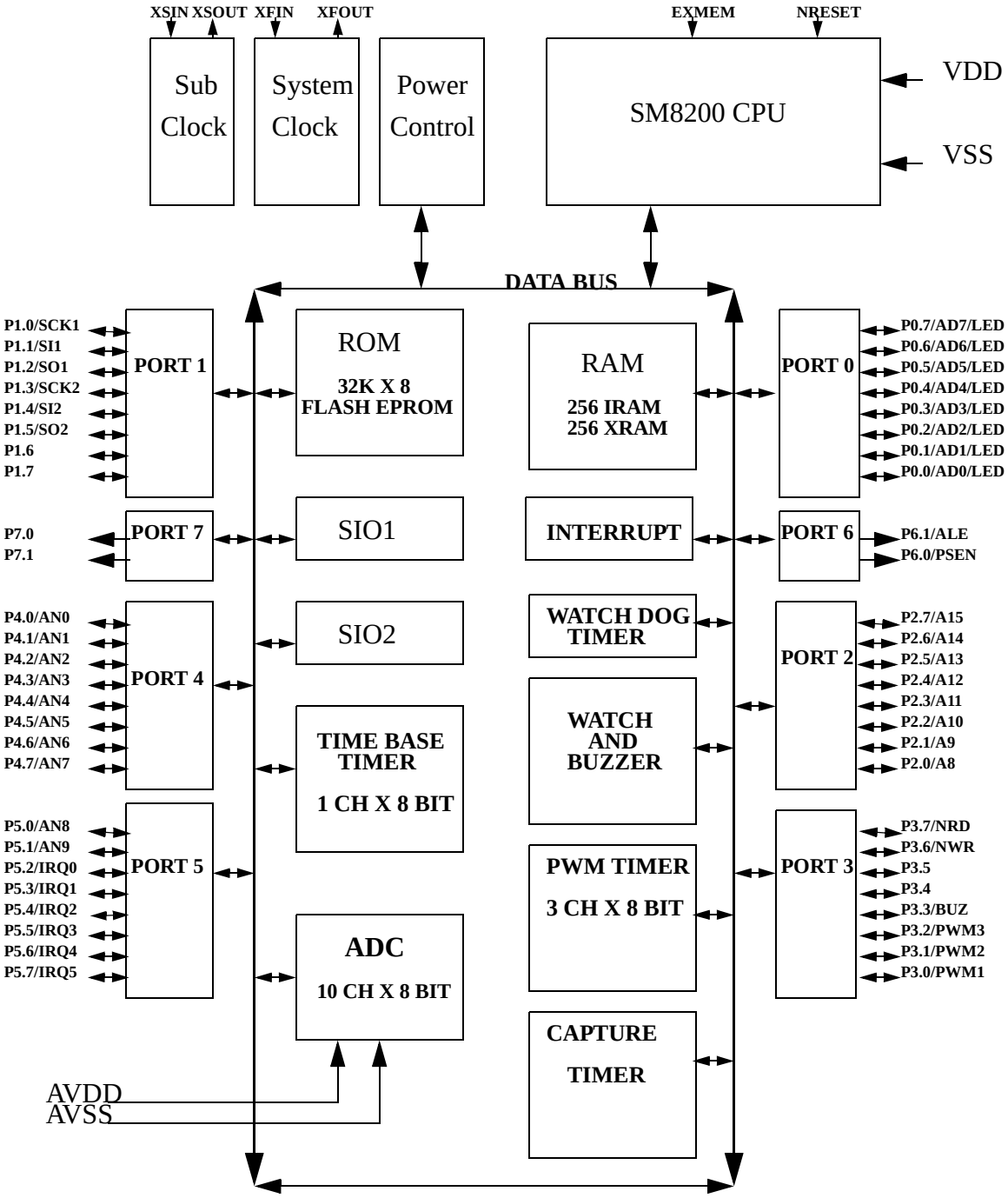
PIN CONFIGURATION



PIN CONFIGURATION



SS8203A Block Diagram



PIN DESCRIPTION

VDD, VDD1
Supply Voltage.
VSS, VSS1
Ground.
AVDD
Analog supply voltage.
AVSS
Analog ground.

Port 0
Port 0 is an 8-bit bidirectional I/O port. It is also used as low byte address and data lines for external memory and in addition has high sink current drive for LED applications. Port 0 is also used as the data lines for the Flash eprom programming.

Port 1
Port 1 is an 8-bit bidirectional I/O port. The alternate functions for port1 are for the serial I/O as listed in the table below. Port 1 is also used lower address byte for Flash eprom programming.

Port 2
Port 2 is an 8-bit bidirectional I/O port. It is also used as the upper address byte for external memory access. Port 2 is also used as the upper address byte for Flash eprom programming.

Port 3
Port 3 is an 8-bit bidirectional I/O port. The alternate functions for port 3 are PWM timers, buzzer timer, and external data memory read/write control as listed in the table below. Port 3 is also used for the programming control signals for Flash eprom programming.

Port 4
Port 4 is an 8-bit bidirectional I/O port. The alternate function for port 4 are for analog input channels as listed in the table below. Note that when analog inputs are used the digital input buffer should be disabled.

Port 5
Port 5 is an 8-bit bidirectional I/O port. The alternate function for port 5 are for analog input channels and external interrupts as listed in the table below. Note that when analog inputs are used the digital input buffer should be disabled.

Port 6
Port 6 is a 2-bit output port. The alternate function for port 6 is for external program memory read signal as listed in the table below.

Port 7
Port 7 is a 2-bit output port.

Table 1. Alternate port pin functions

PORT PIN	Alternate Function
P0.7-0	AD7-0 - Low byte address and data for external memory.
P0.7-0	LED - High current sink LED drivers.
P1.0	SCK1 - SIO1 clock input/output.
P1.1	SI1 - SIO1 data input.
P1.2	SO1 - SIO1 data output.
P1.3	SCK2 - SIO2 clock input/output.
P1.4	SI2 - SIO2 data input.
P1.5	SO2 - SIO2 data output.
P2.7-0	A15-8 - Upper address byte for external memory.
P3.0	PWM1 - PWM1 output.
P3.1	PWM2 - PWM2 output.
P3.2	PWM3 - PWM3 output.
P3.6	NWR - External data memory write control, active low.
P3.7	NRD - External data memory read control, active low.
P4.7-0	AN7-0 - Analog input channels 7 thru 0.
P5.1-0	AN9-8 - Analog input channels 9 and 8.
P5.7-2	IRQ5-0 - External interrupts 5 thru 0.
P6.0	PSEN - External program memory enable, active low.
P6.1	ALE - External memory address latch enable.

NRESET
Active low reset. The device resets when NRESET is set low and held low for two machine cycles while the oscillator is running and stable.

EXMEM
External memory access for program memory. When held high the device will switch to external program memory fetches.

XFIN
Input to the 12Mhz oscillator circuit.

XFOUT
Inverting output form the 12Mhz oscillator circuit.

XSIN
Input to the 32Khz oscillator circuit.

XSOUT
Inverting output for the 32Khz oscillator circuit.

MEMORY ORGANIZATION

DATA MEMORY

The SS8203A has separate address space for Program Memory and Data Memory.

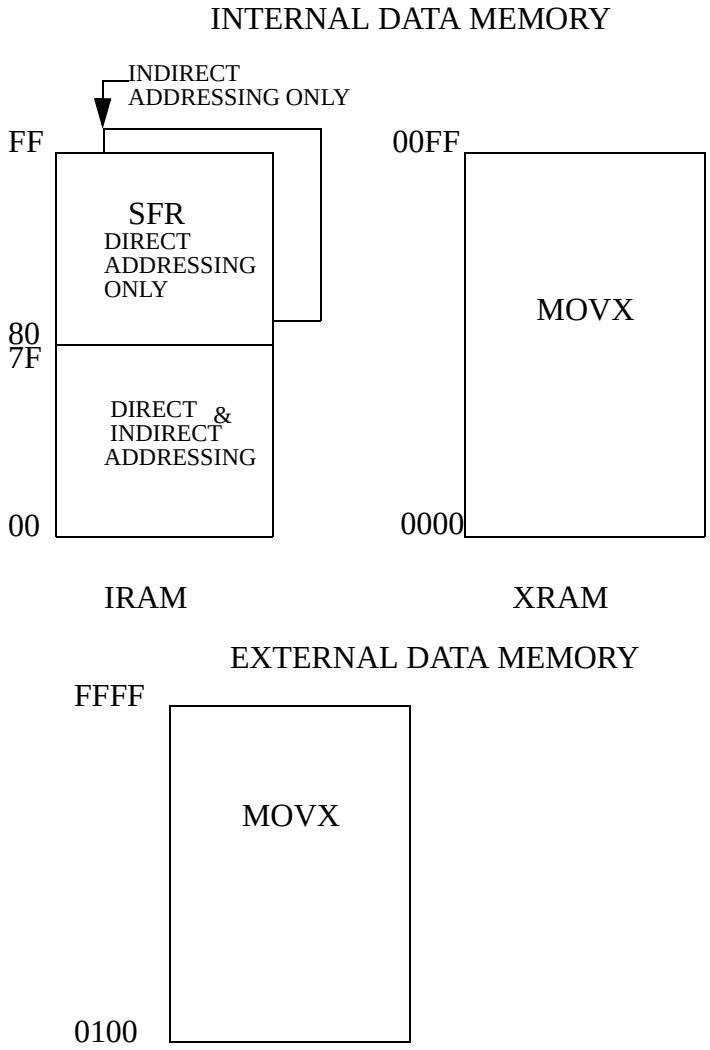
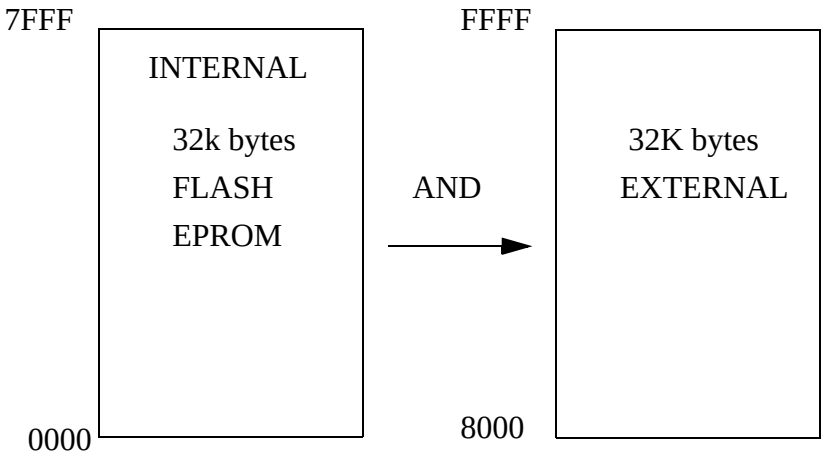


Figure X. The SS8203A Data Memory

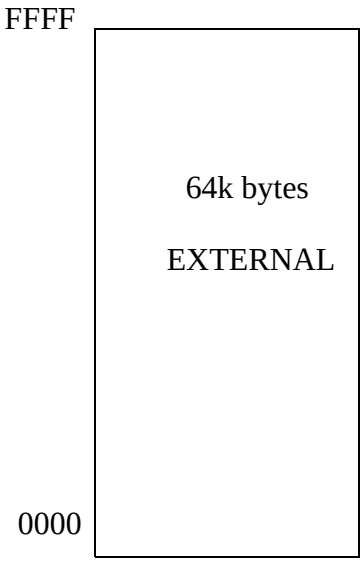
The SS8203A has 512 bytes of onchip data space and from 257 to 64K external. By direct and indirect addressing the lowest 128 bytes can be accessed. Then the next 128 bytes are accessed by indirect addressing while direct addressing in this area will access the SFR registers. With the MOVX command the first 256 bytes are onchip and the remaining up to 64K are external.

PROGRAM MEMORY

The SS8203A program memory will configure in two ways depending on the state of the EXMEM pin. With EXMEM low the first 32K bytes will be fetched from internal Flash eprom and the top 32K bytes from external memory. If the EXMEM pin is high all program fetches will be external from 0 to 64K bytes.



EXMEM - Low



EXMEM - High

Figure X. The SS8203A Program Memory

SPECIAL FUNCTION REGISTERS

The SS8203A special function registers (SFR) are accessed with direct memory addressing in the memory space from 80H to FFH. The table below shows the location of each register. The description of the register functions are in the respective peripheral block descriptions and the architectural overview section.

Lo \ Hi	8	9	A	B	C	D	E	F
0	P0	P1	P2	P3	P4	PSW	ACC	B
1	SP	ADCR	WDCR	TBCR	PT2CR	CT1CR	CT2CR	SIO1CR
2	DPL	ADAT	WDTR	TBCNT	PT2CNT	CT1CL	CT2CL	SIO1DH
3	DPH	ADENL	WBCR	TBDAT	PT2DAT	CT1CH	CT2CH	SIO1DL
4		ADENH	SECCNT	PT1CR	PT3CR	CT1DL	CT2DL	SIO2CR
5			MINCNT	PT1CNT	PT3CNT	CT1DH	CT2DH	SIO2D
6		SREL	XICR0	PT1DAT	PT3DAT			
7	-----	PSCR	XICR1	P6	P7	ISE0	ISE1	ISE2
8	-----	-----	IE	IP	P5	INT0	INT1	INT2
9	-----	-----						
A	-----	PCR	P0IO	P1IO	P2IO	P3IO	P4IO	P5IO
B	-----	ZCR	P0RD	P1RD	P2RD	P3RD	P4RD	P5RD
C	-----							
D	-----							
E								
F								MSIZ

The SFR register definitions are described within each peripheral block description and the general CPU registers SP, DPTR, PSW, ACC, B, and MSIZ are described below.

Stack Pointer (SP)

The SP register contains the stack pointer. The stack pointer is used to load the program counter into memory during LCALL and ACALL instructions, and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the stack pointer. The stack pointer points to the top location of the stack. On reset the stack pointer is set to 07 hex.

Data Pointer (DPTR)

The Data Pointer (DPTR) is 16 bits in size, and consists of two registers, the Data Pointer High byte (DPH), and the Data Pointer Low byte (DPL). Two 16 bit operations are possible on this register, they are load immediate and increment. This register is used for 16 bit address external memory accesses, for offset code byte fetches, and for offset program jumps. On reset the value of this register is 0000 hex.

Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operation. The bit definitions are given below:

PSW.7 CY. ALU carry flag.
PSW.6 AC. ALU auxiliary carry flag.
PSW.5 F0. General purpose user definable flag.
PSW.4 RS1. Register bank select bit 1.
PSW.3 RS0. Register bank select bit 0.
PSW.2 OV. ALU overflow flag.
PSW.1 F1. User definable flag.
PSW.0 P. Parity flag. Set each instruction cycle to indicate odd/even parity in the accumulator.

The register bank select bits operate as follows.

RS1	RS0	Register Bank Select
0	0	RB0. Registers from 00 - 07 hex.
0	1	RB1. Registers from 08 - 0F hex.
1	0	RB2. Registers from 10 - 17 hex.
1	1	RB3. Registers from 18 - 1F hex.

On reset this register returns 00 hex.

Accumulator (ACC)

This register provides one of the operands for most ALU operations. In the instruction table it is denoted as "A".

On reset this register returns 00 hex.

B Register (B)

This register provides the second operand for multiply or divide instructions. Otherwise it may be used as a scratch pad register.

On reset this register returns 00 hex.

Memory Size Register (MSIZ)

The purpose of this register is to define the amount of available internal program memory. The amount available is:

(MSIZ + 1) $\times$ 256.

On reset this register returns 7F hex.

It should be noted that the EXMEM pin overrides any value stored in this register, and that if the available internal memory is 0K in size, the EXMEM pin should be driven high. A value of FF hex in MSIZ enables the full 64K memory range as internal.

FLASH MEMORY PROGRAMMING

The SS8203A has 32Kbytes of electrically erasable flash eprom onchip. The memory when in the erased state the contents are all FFH. The memory is then programmed one byte at a time. The memory is reprogrammable a maximum of 10 times. The programming algorithm is as follows:

1. Set power on VDD and VSS.

2. Set NRESET to low and
   Set P7.0 to ‘L’
   Set P7.1 to ‘L’
   Set P2.7 to ‘L’
   Set P3.1 to ‘L’
   Set P3.2 to ‘L’
   Set P3.3 to ‘L’

3. Set EXMEM (VPP) to 12V.

4. Apply the appropriate combination of input levels ‘H’ or ‘L’ for inputs P3.0, P3.6, P3.7 according to the FLASH EPROM PROGRAMMING MODES table.

Program and verify

5. Apply the program address A14-A0 on port bits P2.6-P2.0 and P1.7-P1.0.

6. Apply the program data D7-0 on port P0.7-P0.0.

7. P3.7 (NOE) is set to ‘H’ and P3.6 (NCE) is pulsed low for TPWP. This programs the memory location.

8. Program data is then removed from P0.7-0 and then with P3.6 (NCE) set to “H’ and P3.7 (NOE) is set low and then the written data will appear on P0.7-0 after TDFP. This verifies that the data was written.

9. Steps 5 thru 8 are repeated until all the memory is programmed.

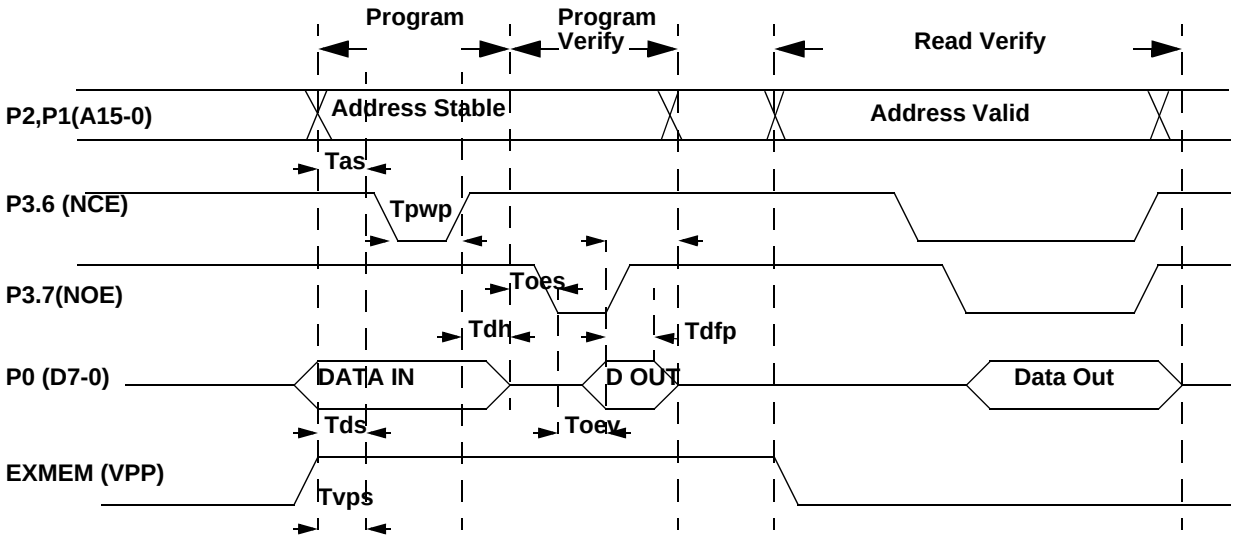
Flash memory erase

The entire flash memory 32K will be erased at one time. Steps 1 thru 4 as above, except that EXMEM should be 14V instead of 12V in step 3, with the controls at the proper ‘H’ and ‘L’ levels erasure occurs by holding P3.6 (NCE) low for TPWE with P1.0 (A0) at ‘L’.

FLASH MEMORY PROGRAMMING MODES

Mode	EXMEM (VPP)	P3.6 (NCE)	P3.7 (NOE)	P3.0	P3.1	P3.2	P3.3
Program Data	12V	_/	H	L	L	L	L
Program Verify	12V	H	_/	L	L	L	L
Erase Data	14V	_/	H	H	L	L	L
Erase Verify	14V	H	_/	H	L	L	L
Read Data	H	L	L	L	L	L	L

FLASH MEMORY PROGRAM OPERATION



FLASH MEMORY ERASE OPERATION

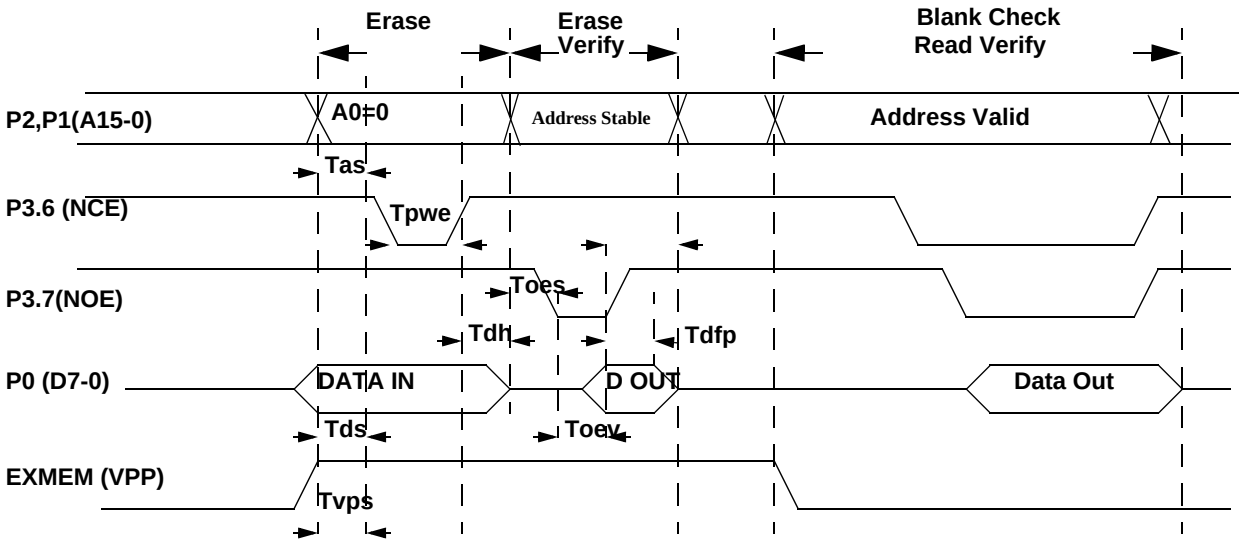


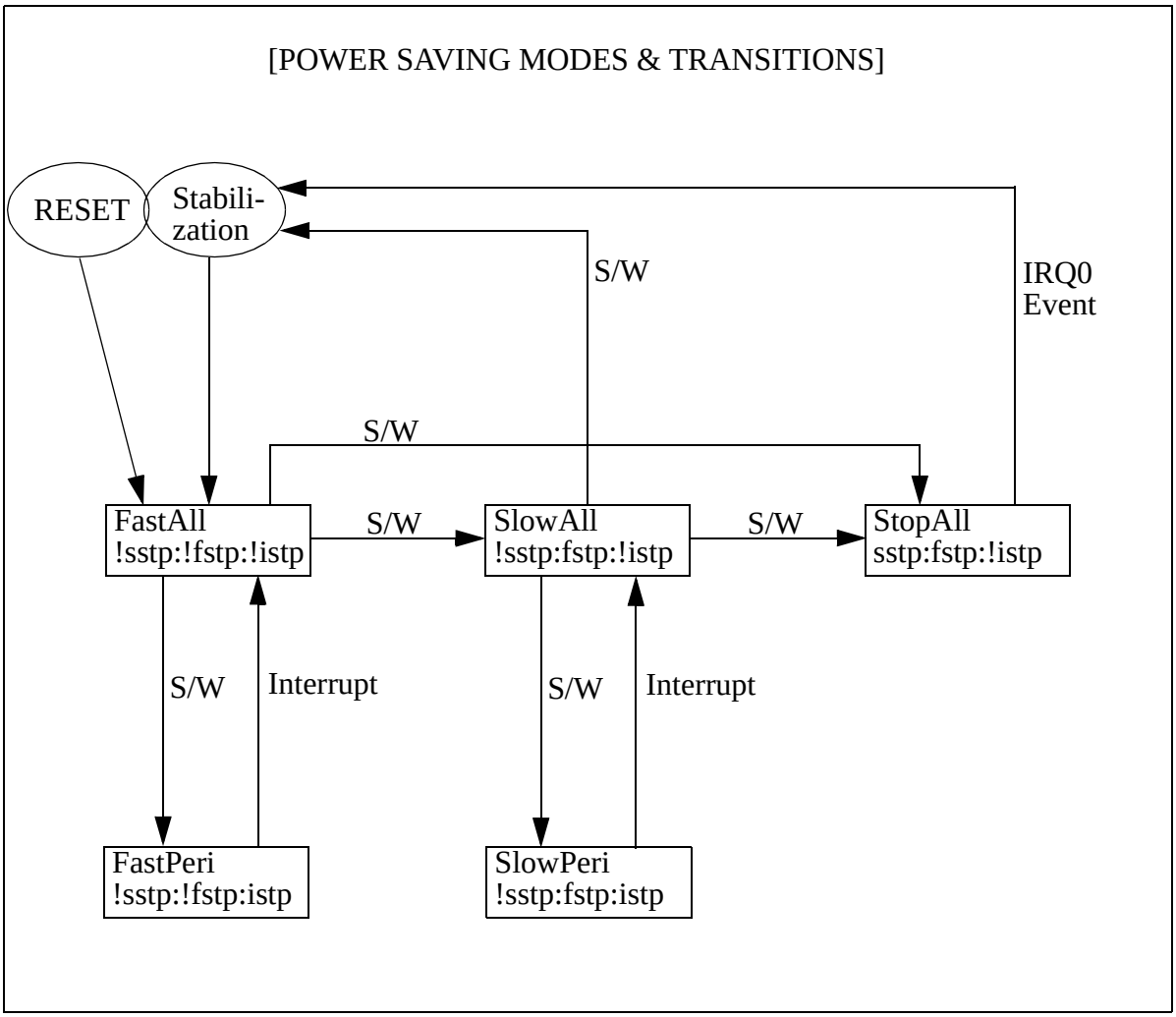
Table 1:

PARAMETER	SYM	MIN	TYP	MAX	UNIT
VPP Setup Time	**Tvps**	**2.0**	**-**	**-**	**uS**
Adress Setup Time	**Tas**	**2.0**	**-**	**-**	**uS**
Data Setup Time	**Tds**	**2.0**	**-**	**-**	**uS**
NCE Program Pulse Width	**Tpwp**	**95**	**100**	**105**	**uS**
NCE Erase Pulse Width	**Tpwe**	**95**	**100**	**105**	**mS**
Data Hold Time	**Tdh**	**2.0**	**-**	**-**	**uS**
NOE Setup Time	**Toes**	**2.0**	**-**	**-**	**uS**
Data Valid from NOE	**Toev**	**-**	**-**	**150**	**nS**
NOE high to Output High Z	**Tdfp**	**0**	**-**	**130**	**nS**
Address Hold Time	**Tah**	**0**	**-**	**-**	**uS**
Address Hold Time after NCE	**Tahc**	**2.0**	**-**	**-**	**uS**

Power-Saving Modes

1. Overview

The MCU(Micro-Controller Unit) provides two kinds of methods to save power consumption. The first method is to stop clock operations partially or wholly. The result is to reduce switching current of CMOS. The other is to make pin status High-Z(impedance). This feature will remove static current through resistors on board. Two methods(clock control scheme and pin control scheme) can be combined together. The Power-Saving Modes are controlled by the PSCR(Power-Saving Control Register) that is an SFR(Special Function Register) mapped on memory address map. Any kind of instruction, whose destination is the PSCR, can change the PSCR content. Thus, the transitions of modes among normal and Power-Saving modes can be controlled by software. In some cases, when CPU stops, hardware signals such like interrupts, an IRQ0 Pin Event, and reset make the device change modes.



2. Mode Definition and Transition

There are five Clocking Modes, i.e. FastAll, SlowAll, StopAll, FastPeri, and SlowPeri modes. These are controlled by PSCR[2:0] (Power Saving Register bit 2 downto 0). According to these bits, it is decided for the Fast Oscillator(upto 12MHz), Slow Oscillator(32.768KHz), and CPU operation or Instruction execution to run or stop.
There are two Pin State Modes, i.e. NorPin(Normal Pin operation mode) and HIZ(High-Z mode). The bit-4 of PSCR(HIZ) selects a mode between them.
In any mode of Clocking Modes, any Pin State Mode can be selected.

It is conceptually possible to make a new clocking power-saving mode because three bits of PSCR are assigned to select it. But, the other cases except listed five modes are never proved. If user need a new clocking Power-Saving mode other than listed five, to test and prove it is user's responsibility. We also recommend that only listed mode transition is used. For other transition than recommended transition, user must carefully test it. When Clocking Power-Saving Mode is chaged by Software, next two instructions should be NOP(No Operation).

[Table: Clocking Power-Saving Mode Definition and PSCR]

PSCR bit	**bit-2**	**bit-1**	**bit-0**
Bit Name	**SSTP**	**FSTP**	**ISTP**
FastAll mode	**0**	**0**	**0**
SlowAll mode	**0**	**1**	**0**
StopAll mode	**1**	**1**	**0**
FastPeri mode	**0**	**0**	**1**
SlowPeri mode	**0**	**1**	**1**
Another Cases	**Not Proved**		

[Table: Clocking Power-Saving Mode Definition and PSCR]

PSCR bit	**bit-4**
Bit Name	**HIZ**
NorPin mode	**0**
HIZ mode	**1**

FastAll mode (a Clocking Mode)

This is a normal operation mode. All of MCU may operate normally. Both Fast(upto 12MHz) and Slow(32.768KHz) oscillators generate clock signals. The Fast Clock is used as a System Clock to control the CPU and Peripherals.
In the FastAll mode, the content of the PSCR is xxxxx000B (x: don't care, B:binary). After Reset from any mode, the MCU goes into the FastAll mode.

Next available Clocking Modes are the SlowAll mode(PSCR[2:0] = 010B), FastPeri mode(PSCR[2:0] = 001B), and StopAll mode(PSCR[2:0] = 110B). All three mode transitions from FastAll mode are performed by software.

SlowAll mode (a Clocking Mode)

This is a slow operation mode. All of MCU may operate with low speed(32.768KHz). Fast(upto 12MHz) clock generator is halted. Slow(32.768KHz) oscillators generate clock signals. The Slow Clock is used as a System Clock to control the CPU and Peripherals.
In the SlowAll mode, the content of the PSCR is xxxxx010B (x: don't care, B:binary). After Reset from this mode, the MCU goes into the FastAll mode.

Next available Clocking Modes are the FastAll mode, StopAll mode, and SlowPeri mode. All three mode transitions from SlowAll mode are performed by software.

StopAll mode (a Clocking Mode)

This is a perfect stop mode. All of MCU stop to operate. Both Fast and Slow clock generators are halted.
In the StopAll mode, the content of the PSCR is xxxxx110B (x: don't care, B:binary). After Reset from this mode the MCU goes into the FastAll mode. In this transition case, most SFR data will be initialized. By an External Event signal(IRQ0), the MCU goes into FastAll mode. In this transition case, all SFR and RAM data will be retained.

FastPeri mode (a Clocking Mode)

This is a fast Peripheral operation mode. The CPU is halted. All of Peripheral may operate with fast speed. Fast and Slow oscillators generate clock signals. The Fast Clock is used as a System Clock to control the Peripherals.
In the FastPeri mode, the content of the PSCR is xxxxx001B (x: don't care, B:binary). After Reset from this mode, the MCU goes into the FastAll mode.

Next available Clocking Modes is the FastAll mode only. The mode transition from FastPeri mode is performed by an interrupt. In this mode CPU SFRs(Special Function Registers such like PSW, ACC, and etc.) and RAM data will be retained.

SlowPeri mode (a Clocking Mode)

This is a slow Peripheral operation mode. The CPU is halted. All of Peripheral may operate with slow speed(32.768KHz). Fast oscillator is halted. Slow oscillators generate clock signals. The Slow Clock is used as a System Clock to control the Peripherals.
In the SlowPeri mode, the content of the PSCR is xxxxx011B (x: don't care, B:binary). After Reset from this mode, the MCU goes into the FastAll mode.

Next available Clocking Modes is the SlowAll mode. The mode transition from SlowPeri mode is performed by an interrupt. In this mode CPU SFRs(Special Function Registers such like PSW, ACC, and etc.) and RAM data will be retained.

NorPin mode (a Pin State Mode)

This is a normal operation mode. All of pin state can be controlled by software or hardware. This is an initial state after Reset. In the NorPin mode, the content of the PSCR is xxx0xxxxB (x: don't care, B:binary). The mode transition from NorPin mode to HIZ mode is performed by software. The NorPin mode can be combined with any kinds of Clocking Power-Saving modes.

HIZ mode (a Pin State Mode)

This is a Pin State Power-Saving mode. All of normal port pin state become high-impedance state to remove static current. Thus, port pin state can not be controlled by software or other hardware. In the HIZ mode, the content of the PSCR is xxx1xxxxB (x: don't care, B:binary). The mode transition from HIZ mode to NorPin mode is performed by software and reset. The HIZ mode can be combined with any kinds of Clocking Power-Saving modes. In the HIZ mode, the port register content will be retained if software or hardware don't change them. For PORT-0 to 3, each port will be controlled by ZCR register. But, HIZ bit directly control PORT-4 to 5. Please, refer PORT block specification.

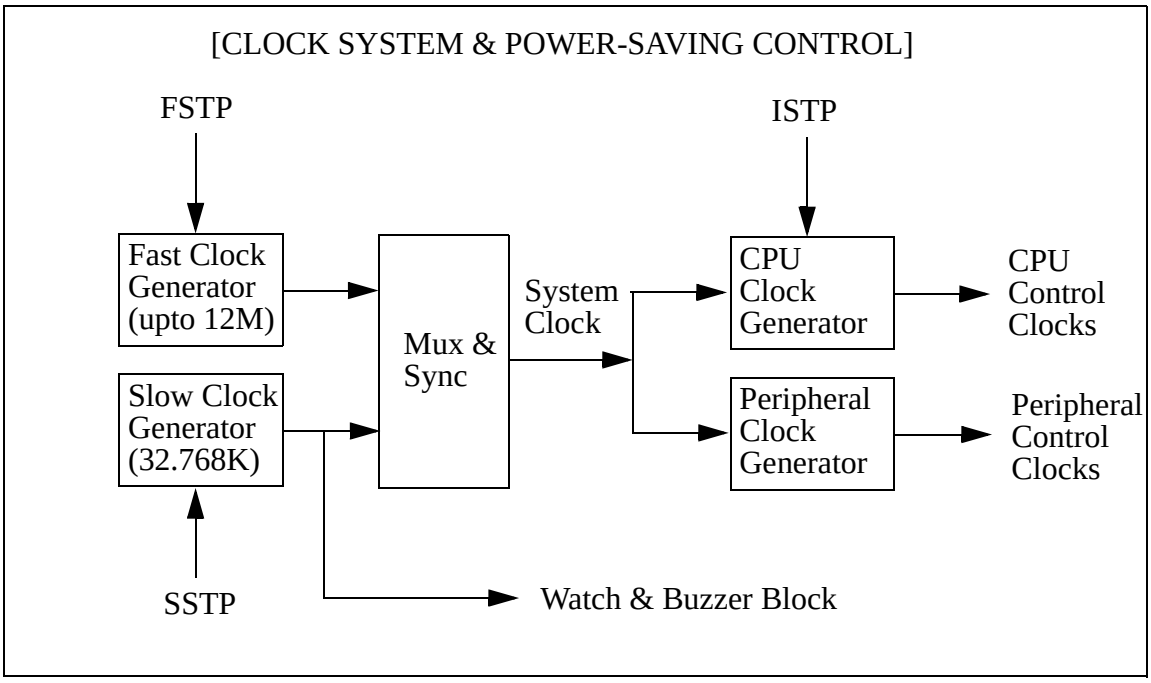
[Table: Device States in Power-Saving Modes]

Block	FastAll	SlowAll	StopAll	FastPeri	SlowPeri
Fast Oscillator	Run	**Stop**	**Stop**	Run	**Stop**
Slow Oscillator	Run	Run	**Stop**	Run	Run
System Clock	from Fast OSC	from **Slow** OSC	**Stop**	from Fast OSC	from **Slow** OSC
CPU Clock	from Fast OSC	from **Slow** OSC	**Stop**	**Stop**	**Stop**
Peripheral Clock	from Fast OSC	from **Slow** OSC	**Stop**	from Fast OSC	from **Slow** OSC
Instruction	Run(fast)	Run(slow)	**Stop**	**Stop**	**Stop**
CPU SFR	Run(fast)	Run(slow)	**Retained**	**Retained**	**Retained**
RAM	Run(fast)	Run(slow)	**Retained**	**Retained**	**Retained**
Peripheral	Run(fast)	Run(slow)	**Stop**	Run(fast)	Run(slow)
Peri SFR	Run(fast)	Run(slow)	**Retained**	Run(fast)	Run(slow)

3. Power-Saving Control Register (PSCR)

[Table: Summary of PSCR]

Address	97H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	PSCR7	PSCR6	FTST	HIZ	NOTS	SSTP	FSTP	ISTP
Definition	Power Saving Register bit-7	Power Saving Register bit-6	Fast Stabilization Time for Test	High Impedance	Not Use Slow Clock	Slow clock SToP	Fast clock SToP	CPU clock SToP
Reset Value	0	0	0	0	0	0	0	0
Read/ Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware						0 by An IRQ0 Event	0 by An IRQ0 Event	0 by Interrupt



[Table: The Definition of Each PSCR bit]

Name	Bit	Definition
PSCR[7:6]	7 to 6	**General purpose bits** These bits may be used to indicate during which mode an interrupt took place. For example, an instruction that activates an Power-Saving mode can also set a PSCR[7:6]. When the Power-Saving mode is terminated by an interrupt, the interrupt service routine can examine the bit of PSCR[7:6].
FTST	5	**Fast Stabilization Time for Test** [Bit Status: 0] When the StopAll mode is released by an IRQ0 Event, fast oscillator stabilization time will be 10.9 mSec (1/12MHz x 2^{18-1}). [Bit Status: 1] When the StopAll mode is released by an IRQ0 Event, fast oscillator stabilization time will be 1.33 uSec (1/12MHz x 2^{5-1}).
HIZ	4	**PIN State control bit** [Bit Status: 0] Normal Pin state. [Bit Status: 1] All normal I/O pins become High-Z(impedance) state.
NOTS	3	**Not Use Slow Oscillator bit** [Bit Status: 0] Slow oscillator (32.768KHz) is used. [Bit Status: 1] Slow oscillator is not used. The pin XSIN is connected to ground.
SSTP	2	**Slow clock SToP bit** [Bit Status: 0] Slow oscillator (32.768KHz) operates. [Bit Status: 1] Slow oscillator stops.
FSTP	1	**Fast clock SToP bit** [Bit Status: 0] Fast oscillator (upto 12MHz) operates and drives all CPU and peripherals. [Bit Status: 1] Fast oscillator stops. Slow oscillator (32.768KHz) may or may not drive all CPU and peripherals.
ISTP	0	**Instruction SToP bit** [Bit Status: 0] CPU control clocks drive CPU. Thus, instructions may be executed its operations normally. [Bit Status: 1] CPU control clocks stop. Thus, CPU stops to execute instructions.

4. Stop Release Register (SREL)

[Table: Summary of SREL]

Address	**96H**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**SREL2**	**SREL1**	**SREL0**
Definition						**Stop Release bit-2**	**Stop Release bit-1**	**Stop Release bit-0**
Reset Value	**Unknown**	**Unknown**	**Unknown**	**Unknown**	**Unknown**	**0**	**0**	**0**
Read/Write by Software						**R/W**	**R/W**	**R/W**
Write by Hardware								

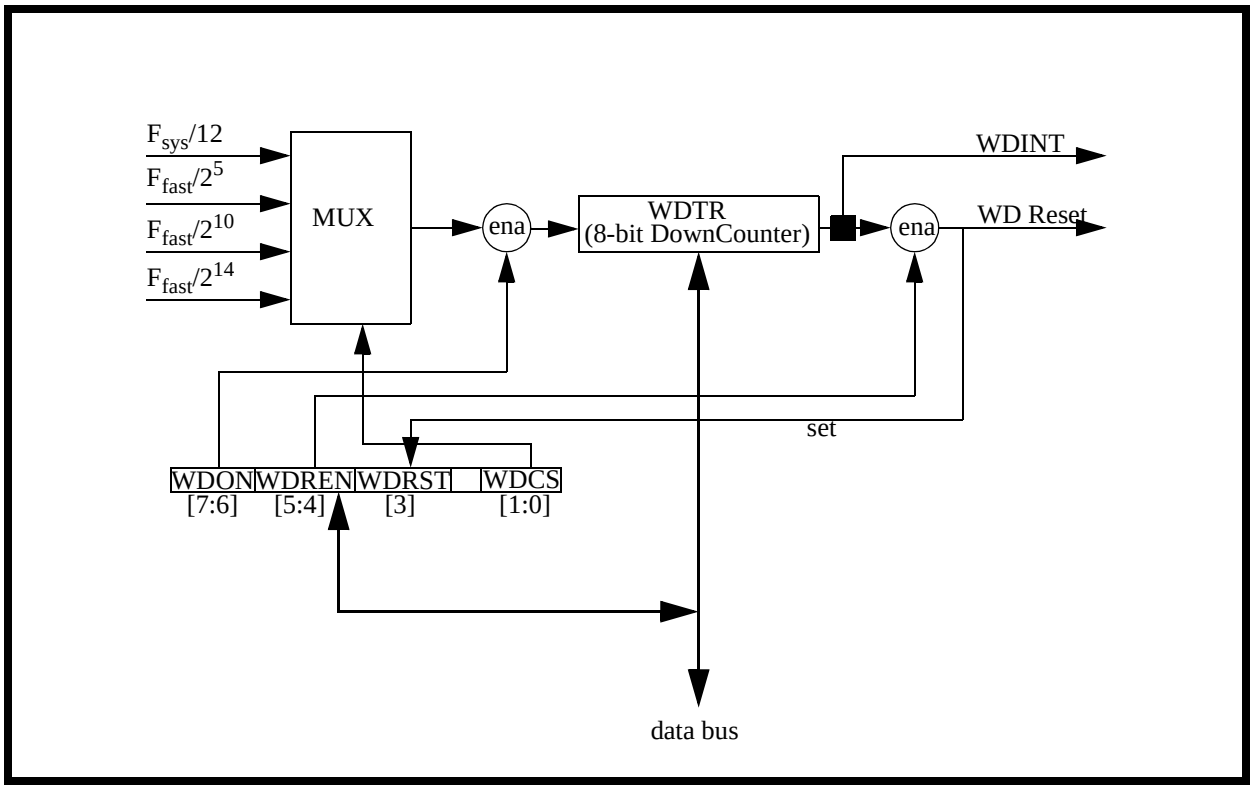
[Table: The Definition of Each SREL bit]

Name	Bit	Definition
SREL[2:0]	2 to 0	**Stop Release Bit-2 to 0** [Bit Status: 001] IRQ0 Negative Edge enabled [Bit Status: 010] IRQ0 Positive Edge enabled [Bit Status: 011] IRQ0 Any (Negative or Positive) Edge enabled [Bit Status: 101] IRQ0 Low Level enabled [Bit Status: 110] IRQ0 High Level enabled [Other Cases] StopAll Mode can not be released by IRQ0 pin event, can be released by only Reset. Stop Release by IRQ0 should be enabled just before going into the StopAll mode. If it is enabled in other mode, unexpected mode transition will be happened.

[WD-Timer]

1. Overview

The WD-Timer (WatchDog Timer) can be used as a watch-dog timer or a basic interval timer. The main purpose of the WD-Timer is to initialize the MCU again from an unexpected device upset state. For instance, if a program falls into an infinite loop by noise, the WD-Timer will make the CPU wake up. By enabling the WatchDog Reset, this feature will be taken. By disabling the WatchDog Reset and enabling the WatchDog Interrupt, the WD-Timer can be used as a basic interval timer. Only Fsys/12 is supported when under SlowAll or SlowPeri modes.



2. WatchDog Timer Control Register (WDCR)

[Table: Definition of WDCR]

Address	A1							
Bit Addr.								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**WDON1**	**WDON0**	**WDREN1**	**WDREN0**	**WDRST**		**WDCS1**	**WDCS0**
Definition	**WD-timer turn ON bit-1**	**WD-timer turn ON bit-0**	**WD-timer Reset gen-eration ENable bit-1**	**WD-timer Reset gen-eration ENable bit-0**	**WD-timer Reset STatus**	**Reserved**	**WD-timer counting Clock Select bit-1**	**WD-timer counting Clock Select bit-0**
Reset Value	**0**	**1**	**0**	**1**	**0: Pin Reset 1: WD Reset**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W**	**R/W**	**R/W**	**R**	**R**	**R/W**	**R/W**
Write by Hard-ware					**0 by Exter-nal Pin Reset 1 by WD-Tim-er Reset**			

[Table: The Description of WDCR bit-7 to 4]

Name	Bit	Description
WDON[1:0]	7 to 6	**WD-Timer turn ON bits** [Bit Status: 01 (Initial Value)] In this status, the WD-Timer turns off. This bit status makes a selected counting clock frozen. Thus, the 8-bit WD-Timer Register keeps previous value without down-counting. [Bit Status: 10] In this status, the WD-Timer turns on. This bit status makes a selected counting clock run. Thus, the 8-bit WD-Timer Register operates as a down-counter. [Bit Status: 00 or 11] Do **NOT** write these values on these two bits. In these status, the WD-Timer turns on just like status-10. The purpose of these two redundant status is to prevent unexpected WD-Timer stop by device upset. While the WD-Timer is running by setting 10 to the WDON[1:0], unexpected electrical shock can make a WDON bit toggle. If another WDON bit retains its value, the WD-Timer will be continuously running without stop.
WDREN[1:0]	5 to 4	**WD-Timer Reset generation ENable bits** [Bit Status: 01 (Initial Value)] In this status, the WD-Timer can not generate a Reset signal even though the underflow of the WD-Timer takes place. This allows the WD-Timer to be used as a simple Interval Timer. [Bit Status: 10] In this status, the WD-Timer will generate a Reset signal if the underflow of the WD-Timer takes place. After WD-Timer Reset, the program will begin at the ROM address 0000H. All registers will be initialized. [Bit Status: 00 or 11] Do **NOT** write these values on these two bits. In these status, the WD-Timer will generate a Reset signal just like status-10 if the underflow of the WD-Timer takes place. The purpose of these two redundant status is to prevent unexpected WD-Timer behavior by device upset. While the WD-Timer is running with setting 10 to the WDREN[1:0], unexpected electrical shock can make a WDREN bit toggle. If another WDREN bit retain its value, the WD-Timer can generate a Reset signal.

[Table: The Description of WDCR bit-3 to 0]

Name	Bit	Description
WDRST	3	**WD-Timer Reset Status bit** [Bit Status: 0] The chip was initialized by the external pin reset signal. [Bit Status: 1] The chip was initialized by the WD-Timer underflow reset signal.
	2	**Reserved bit**
WDCS[1:0]	1 to 0	**WD-Timer counting Clock Select bit** [Bit Status: 00] $F_{sys}/12$ [Bit Status: 01] $F_{fast}/2^5 = F_{fast}/32$ [Bit Status: 10] $F_{fast}/2^{10} = F_{fast}/1024$ [Bit Status: 11] $F_{fast}/2^{14} = F_{fast}/16384$

3. WatchDog Timer Register (WDTR)

[Table: Definition of WDTR]

Address	A2							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**WDTR[7:0]**							
Definition	**WatchDog Timer Register (8-bit down-counter)**							
Reset Value	**FFH**							
Read/ Write by Soft-ware	**R/W**							
Write by Hard-ware	**Written with a new count value.**							

4. Operation

STEP-1:
First of all, timer interval period should be decided. Then, a WDTR value can be decided. Any instruction, whose destination is the WDTR, can be used to write a value to the WDTR. If the content of the WDTR is FFH, that is the initial value after any Reset, and the FFH is the proper value, you do not have to perform a write instruction to the WDTR.
The interval period is as follows.

WD-Timer interval time = $(1 / F_{selected\text{-}clock})$ X (WDTR + 1) - Deviation period
0 <=Deviation period < $(1 / F_{selected\text{-}clock})$

STEP-2:
You should perform a write instruction to the WDCR with proper content. To turn the WD-Timer on, you must set the WDON[1:0] to 10. While the WD-Timer is running, if you change the content of the WDON[1:0] to 01 the WDTR will retain its last count value. If the WD-Timer Reset is needed, the WDREN[1:0] should be set to 10. If the WDREN[1:0] is 01, the WD-Timer can be used as a basic interval timer. You can choose a counting clock among four clock sources.

STEP-3:
While the WD-Timer is running, software must repeatedly re-initialize the WDTR before the WD Reset is generated. This write operation can be performed without halting the WD-Timer.

STEP-Underflow:
If the WD Reset is enabled and a WD underflow happens, the MCU goes into Reset state and all registers are initialized again. The Program Counter will point to the address 0000H. Initialization routine of software can check the WDRST bit to distinguish the reset source.
In any case, the WDINT bit is set to high when the underflow happens. If the WD-Timer interrupt is enabled by the Interrupt Control Block, the interrupt service routine for the WD-Timer will be served. At this time the WDINT bit will be cleared by hardware.

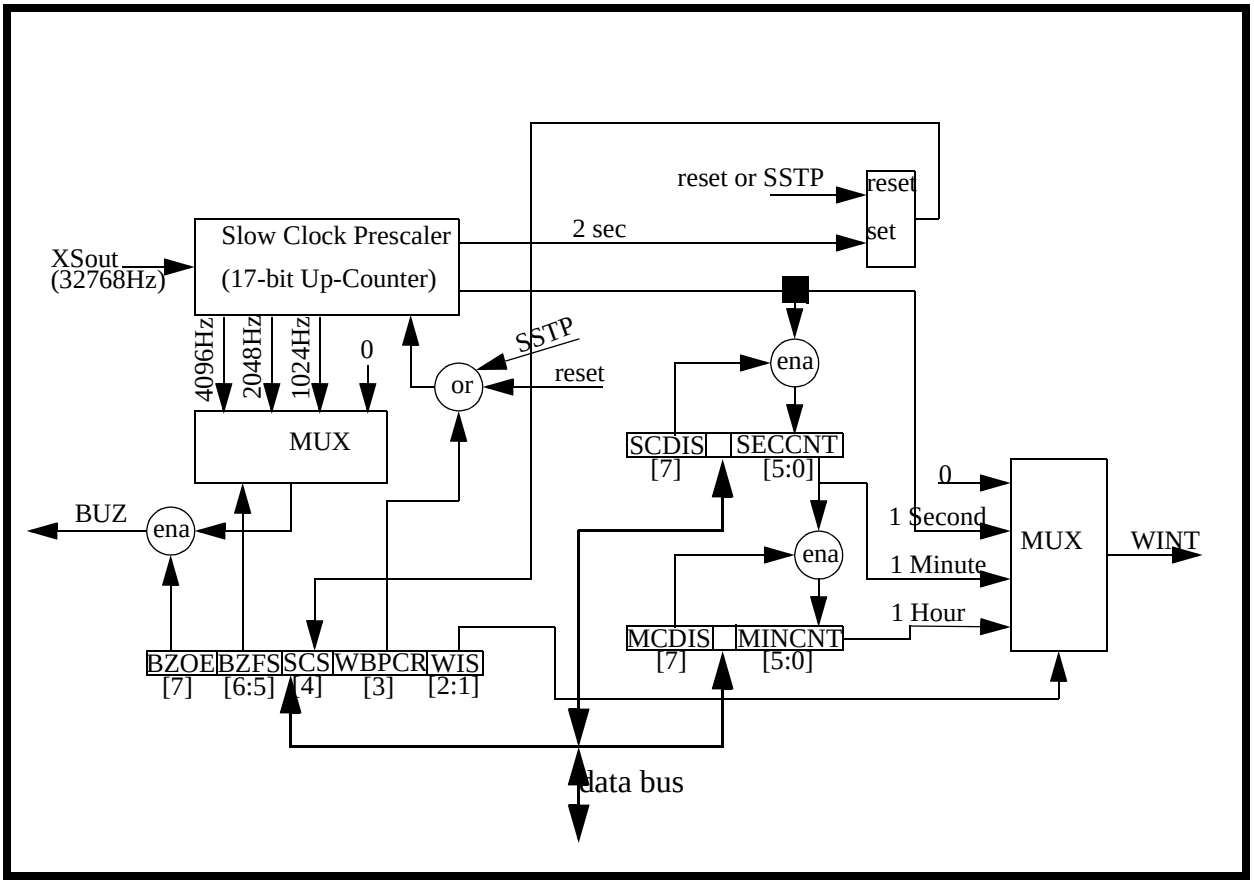
Note: Writing “FFh” to the down counter register while it is in the “00h” state, might cause the “Underflow”. Writing anything other than “FFh” will not cause the “Underflow”.

[Watch & Buzzer]

1. Overview

The functions of the Watch & Buzzer block are to generate a 50% duty buzzer out signal(BUZ), to generate a time interval interrupt request among 1 second, 1 minute, and 1 hour (WINT), to notify the slow oscillator(32.768KHz) stable, and to supply clock signals to the TB-Timer. The Watch & Buzzer block is composed of a Slow Clock Prescaler, a Buzzer Output select portion, a Second Counter, a Minute Counter, an Interrupt select portion, and a Control register.

The Slow Clock Prescaler is a 17-bit up-counter whose clock input is the XSout signal (32.768KHz). This counter will be cleared to low when the Reset, SSTP(PSCR), or WCLR(WBCR) become active high. This prescaler generate the buzzer output signals, the TB-Timer input clocks, 1 second signal, 2 second overflow signal. A multiplexer for buzzer output select a 50% duty clock signal among 1.024KHz, 2.048KHz, or 4.096KHz. The SCS bit (Slow Clock Stable bit) will be cleared to low after the Reset or SSTP. But, the bit will be set to high two second after the Slow Clock Oscillator starts. A 6-bit second counter counts the one second signal from 00 to 59(3BH) and generates a 1 minute overflow signal. A 6-bit minute counter counts the one minute signal from 00 to 59(3BH) and generates a 1 hour overflow signal. A multiplexer is provided to select a watch interrupt request(WINT) among the 1 second, 1 minute, and 1 hour.



2. Watch & Buzzer Control Register (WBCR)

[Table: Definition of WBCR]

Address	A3							
Bit Addr.								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**BZOE**	**BZFS1**	**BZFS0**	**SCS**	**WBPCR**	**WIS1**	**WIS0**	
Definition	**BuZzer Output Enable**	**BuZzer Frequency Select bit-1**	**BuZzer Frequency Select bit-0**	**Slow Clock Stable**	**Watch & Buzzer Prescaler CleaR**	**Watch Interrupt Select bit-1**	**Watch Interrupt Select bit-0**	**Reserved**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W**	**R/W**	**R**	**R/W Always 0 read.**	**R/W**	**R/W**	**R**
Write by Hard-ware				**0 by SSTP (Slowclock SToP in PSCR) or Reset 1 by 2 Second overflow from the Slow clock prescaler**				

[Table: The Description of WBCR]

Name	Bit	Description
BZOE	7	**BuZzer Output Enable bit** [Bit Status: 0 (Initial Value)] The Buzzer output and a bit of general port share a pin. In this status, the pin is used as a general port pin. [Bit Status: 1] In this status, the pin is used as a buzzer output pin(BUZ).
BZFS[1:0]	6 to 5	**BuZzer Frequency Select bits** [Bit Status: 00 (Initial Value)] Output low(0v). [Bit Status: 01] Output a 50% duty 1.024KHz signal. [Bit Status: 10] Output a 50% duty 2.048KHz signal. [Bit Status: 11] Output a 50% duty 4.096KHz signal.
SCS	4	**Slow Clock Stable bit** [Bit Status: 0 (Initial Value)] This state means that the slow oscillator and its dividend clocks may be still unstable or halted. [Bit Status: 1] The slow oscillator and its dividend clocks may be stable.
WBPCR	3	**Watch & Buzzer Prescaler CleaR bit** If this bit is written high, the 17-bit Slow Clock Prescaler and the SCS bit will be cleared to zero. Writing low will not affect anything. When read, low(0) is always read.
WIS[1:0]	2 to 1	**Watch Interrupt Select bits** [Bit Status: 00 (Initial Value)] Nothing selected. [Bit Status: 01] One Second signal from the Slow Clock Prescaler is selected. [Bit Status: 10] One Minute signal from the Second Counter is selected. [Bit Status: 11] One Hour signal from the Minute Counter is selected.
	0	**Reserved bit**

3. Second Counter Register (SECCNT)

[Table: Definition of SECCNT]

Address	A4							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**SCDIS**	**STST**	**SECCNT[5:0]**					
Definition	**Second Counter Disable**	**Second counter TeST**	**SECond CouNTer register bit 5 to 0 (Modulo 60 Up-counter: 00 to 59)**					
Reset Value	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hard-ware			**Written with new count value**					

[Table: The Description of SECCNT]

Name	Bit	Description
SCDIS	7	**Second Counter DISable bit** [Bit Status: 1 (Initial Value)] The Second Counter is halted. [Bit Status: 0] The Second Counter is run.
STST	6	**Second counter TeST bit** [Bit Status: 0 (Initial Value)] A normal counting mode by the 1 second signal. [Bit Status: 1] A test counting mode by the XSout (32.768KHz). Note: The bit can only be set either under FastAll or FastPeri modes.
SECCNT[5:0]	5 to 0	**SECond CouNTer bits** A Modulo-60 (00 to 3BH) up-counter using the 1 second signal. This counter generate the 1 minute signal. Note: Whenever WBCR[2:1] is set at “01” and SECCNT[5] goes from “1” to “0” either by H/W counting or memory_mapped writing, an interrupt will be generated.

4. MINute Counter Register (MINCNT)

[Table: Definition of MINCNT]

Address	A5							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**MCDIS**	**MTST**	**MINCNT[5:0]**					
Definition	**Minute Counter Disable**	**Minute counter TeST**	**MINute CouNTer register bit 5 to 0 (Modulo 60 Up-counter: 00 to 59)**					
Reset Value	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hard-ware			**Written with new count value**					

[Table: The Description of MINCNT]

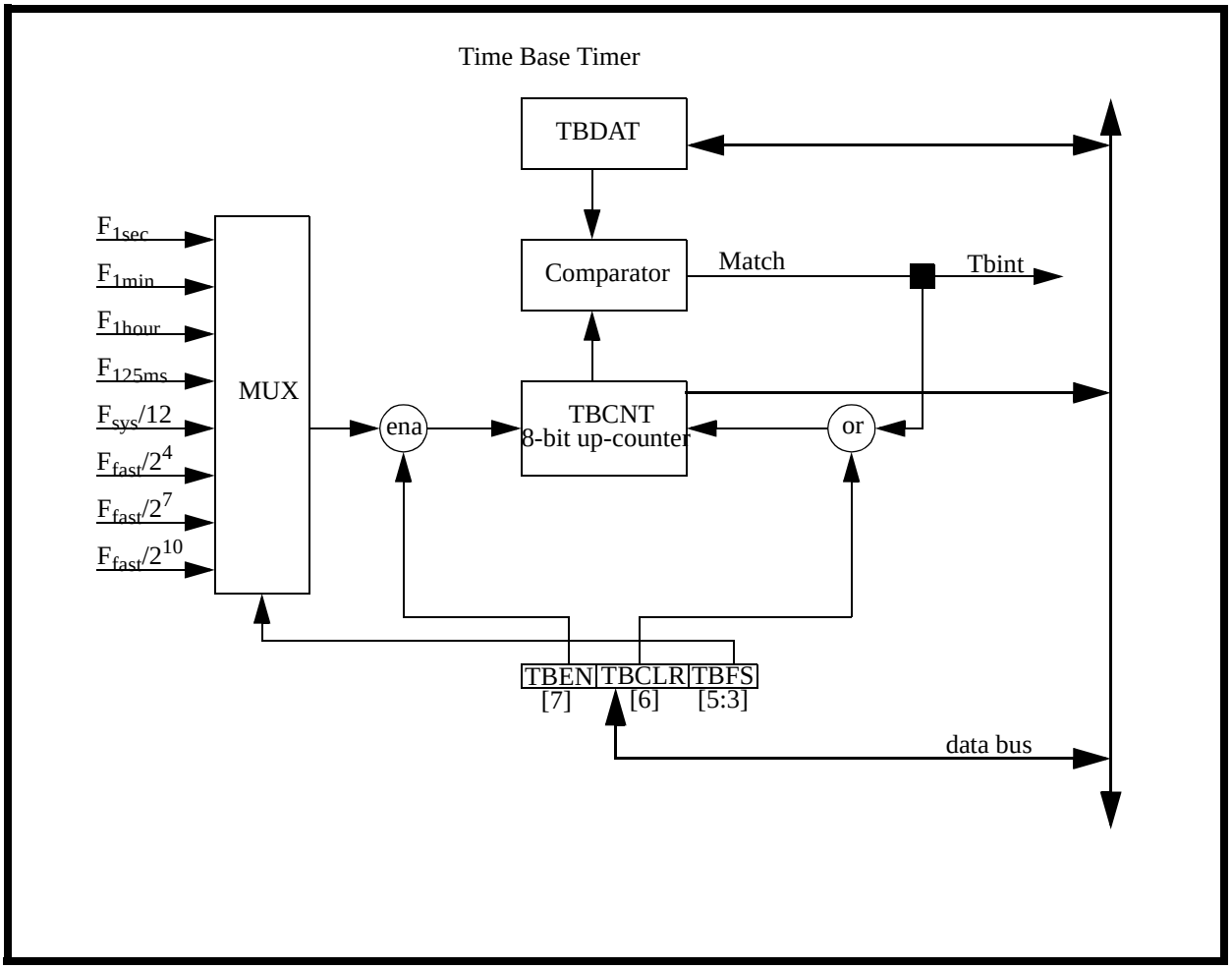
Name	Bit	Description
MCDIS	7	**Minute Counter DISable bit** [Bit Status: 1 (Initial Value)] The Minute Counter is halted. [Bit Status: 0] The Minute Counter is run.
MTST	6	**Minute counter TeST bit** [Bit Status: 0 (Initial Value)] A normal counting mode by the 1 minute signal. [Bit Status: 1] A test counting mode by the XSout (32.768KHz). Note: The bit can only be set either under FastAll or FastPeri modes.
MINCNT[5:0]	5 to 0	**MINute CouNTer bits** A Modulo-60 (00 to 3BH) up-counter using the 1 minute signal. This counter generate the 1 hour signal. Note: Whenever WBCR[2:1] is set at “10” and MINCNT[5] goes from “1” to “0” either by H/W counting or memory_mapped writing, an interrupt will be generated.

[Time Base Timer]

1. Overview

The Time Base Timer (TB-Timer) is an 8-bit auto-reload timer. The TB-Timer is composed of a input frequency select MUX, an 8-bit up-counter(TBCNT), a Comparator, an 8-bit data register(TBDAT), and a control register(TBCR).

The TB-Timer has the 8 counting clocks that can be selected by TBFS[2:0]. Four of the clocks come from the Watch & Buzzer block, i.e. F_{1SEC}, F_{1MIN}, F_{1HOUR}, and F_{125mS}. If the slow oscillator is stop, these four clocks will be stop, too. These four clocks will be very useful to generate a real time interval and to minimize the number of CPU wake-up. The period of the $F_{sys}/12$ clock is one machine cycle or one fastest instruction cycle. This clock will be run during any power-saving mode except the StopAll mode. During the FastAll or FastPeri mode, the $F_{sys}/12$ clock is equal to $F_{fast}/12$. During the SlowAll or SlowPeri mode, the $F_{sys}/12$ clock is equal to $F_{slow}/12$. The $F_{fast}/2^4$, $F_{fast}/2^7$, and $F_{fast}/2^{10}$ can be used during the FastAll or FastPeri mode only.
After the TBEN bit is set to high, the TBCNT will start to count the negative edge of an input clock. When the TBEN bit is low, the Match signal is never generated even though the contents of the TBDAT and TBCNT are the same. The TBCNT is the 8-bit up-counter that can be cleared by the TBCLR bit or the Match signal. The TBCNT is a modulo-N counter (from 0 to N-1), N is the content of the TBDAT. The match signal will always set the TBINT bit to high. The TBINT bit can be cleared by the TB-Timer Interrupt Acknowledge or software.



2. Time Base Timer Control Register (TBCR)

[Table: Definition of TBCR]

Address	B1							
Bit Addr.								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**TBEN**	**TBCLR**	**TBFS2**	**TBFS1**	**TBFS0**			
Definition	**TB timer ENable**	**TB counter CLeaR**	**TB timer input Frequency Select bit-2**	**TB timer input Frequency Select bit-1**	**TB timer input Frequency Select bit-0**	**Reserved**	**Reserved**	**Reserved**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W Always 0 read.**	**R/W**	**R/W**	**R/W**	**R**	**R**	**R**
Write by Hard-ware								

[Table: The Description of TBCR]

Name	Bit	Description
TBEN	7	**TB timer ENable bit** [Bit Status: 0 (Initial Value)] A selected input clock is halted. The TBCNT keeps the counter value. [Bit Status: 1] A selected input clock is run. The TBCNT counts up the negative edge of the selected clock.
TBCLR	6	**TB counter CLeaR bit** If this bit is written with high, the TBCNT (8-bit up-counter) of the TB Timer will be cleared to 00H. Writing low will not affect anything. When read, a low(0) will be always read.
TBFS[2:0]	5 to 3	**TB timer input clock Frequency Select bits** [Bit Status: 000 (Initial Value)] F_{1SEC} [Bit Status: 001] F_{1MIN} [Bit Status: 010] F_{1HOUR} [Bit Status: 011] F_{125mS} [Bit Status: 100] $F_{sys}/12$ [Bit Status: 101] $F_{fast}/2^4$ [Bit Status: 110] $F_{fast}/2^7$ [Bit Status: 111] $F_{fast}/2^{10}$
TBINT	2 to 0	**Reserved bits**

3. TB-Timer Counter Register (TBCNT)

[Table: Definition of TBCNT]

Address	B2							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**TBCNT[7:0]**							
Definition	**TB-timer CouNTer register bit 7 to 0 (Modulo N Up-counter: 00 to N-1, N is the content of TBDAT)**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Write by Hard-ware	**Written with a new count val-ue 0 or 1. 0 by TBCLR.**	**Written with a new count val-ue 0 or 1. 0 by TBCLR.**	**Written with a new count val-ue 0 or 1. 0 by TBCLR.**	**Written with a new count val-ue 0 or 1. 0 by TBCLR.**	**Written with a new count val-ue 0 or 1. 0 by TBCLR.**	**Written with a new count val-ue 0 or 1. 0 by TBCLR.**	**Written with a new count val-ue 0 or 1. 0 by TBCLR.**	**Written with a new count val-ue 0 or 1. 0 by TBCLR.**

[Table: The Description of TBCNT]

Name	Bit	Description
TBCNT[7:0]	7 to 0	**TB-timer CouNTer bits** A Modulo-N (00 to N-1) up-counter. N is the content of TBDAT. This counter counts up from 00H to N-1. Then, the counter will go back to 00H and the comparator will generate match signal. The counter will not stop after the Match. Thus, the TB-Timer will generate continuous Match signals with a fixed period. The TB-Timer is an auto-reload timer.

4. TB-Timer Data Register (TBDAT)

[Table: Definition of TBDAT]

Address	B3							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**TBDAT[7:0]**							
Definition	**TB-timer DATa register bit 7 to 0**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hard-ware	**none**	**none**	**none**	**none**	**none**	**none**	**none**	**none**

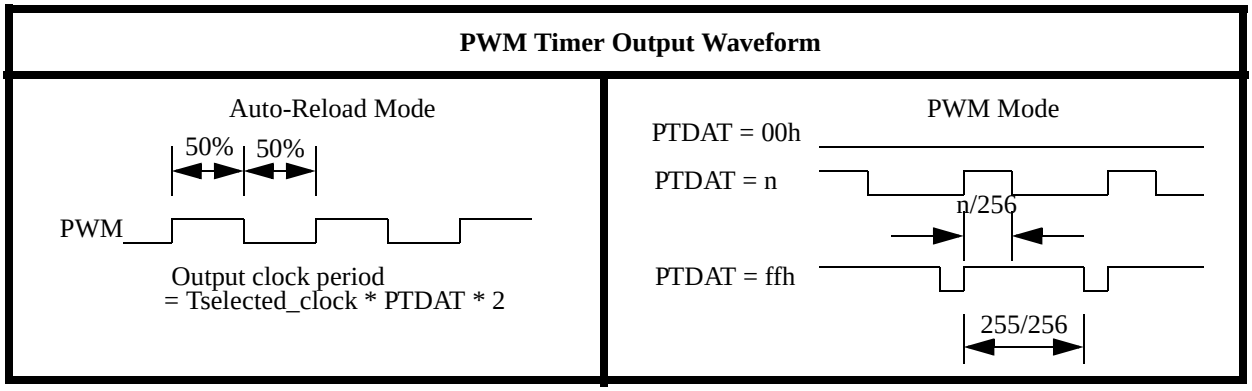
[Table: The Description of TBDAT]

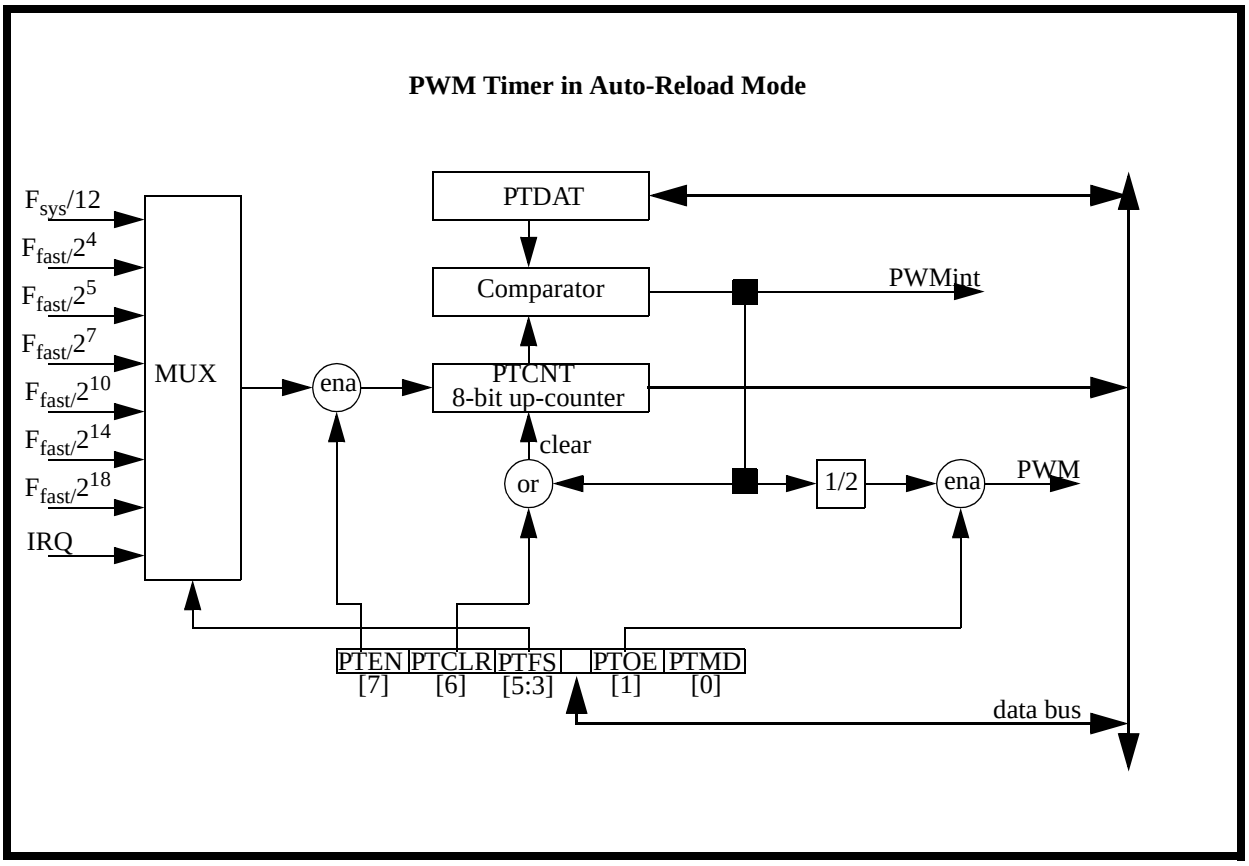
Name	Bit	Description
TBDAT[7:0]	7 to 0	**TB-timer DATa bits** [The first Match period] TB-Timer Match signal period = (1 / $F_{selected\text{-}clock}$) X (TBDAT + 1) - Deviation period 0 <= Deviation period < (1 / $F_{selected\text{-}clock}$) If any clock, which are divided from XSout(32.768KHz), is selected, the Deviation period can be minimized because the Slow Clock prescaler can be cleared by software. [The second or later Match period] TB-Timer Match signal period = (1 / $F_{selected\text{-}clock}$) X TBDAT (No Deviation period)

[PWM Timer1/2/3]

1. Overview

There are three 8-bit PWM Timer in the MCU, P-Timer1, P-Timer2, and P-Timer3. A PWM Timer (or P-Timer) can be used as an Auto-Reload Timer, an Event Counter, a Square Wave Generator or a Pulse Width Modulator(PWM). A P-Timer is composed of a input frequency select MUX, an 8-bit up-counter(PT1CNT, PT2CNT, PT3CNT), a Comparator, an 8-bit data register(PT1DAT, PT2DAT, PT3DAT), a square wave generator, a PWM output generator, and a control register(PT1CR, PT2CR, PT3CR). There are two operation modes in the P-Timers. These are Auto-Reload Mode and PWM mode that is selected by the PT1MD bit (or PT2MD or PT3MD) in the PT1CR (or PT2CR or PT3CR). In the Auto-Reload Mode, the P-Timer can be used as an Auto-Reload Timer, an Auto-Reload Event Counter, or a Square Wave Generator. In the PWM mode, the P-Timer can be used as a Pulse Width Modulator.





2. Auto-Reload Mode

If the PT1MD bit (or PT2MD or PT3MD) in the PT1CR (or PT2CR or PT3CR) is low, the P-Timer1 (or P-Timer2 or P-Timer3) will operate in the Auto-Reload Mode.

A P-Timer has the 8 counting clocks that can be selected by PT1FS[2:0] (or PT2FS[2:0] or PT3FS[2:0]). The period of the $F_{sys}/12$ clock is one machine cycle or one fastest instruction cycle. This clock will be run during any power-saving mode except the StopAll mode. During the FastAll or FastPeri mode, the $F_{sys}/12$ clock is equal to $F_{fast}/12$. During the SlowAll or SlowPeri mode, the $F_{sys}/12$ clock is equal to $F_{slow}/12$. The $F_{fast}/2^4$, $F_{fast}/2^5$, $F_{fast}/2^7$, $F_{fast}/2^{10}$, $F_{fast}/2^{14}$, and $F_{fast}/2^{18}$ can be used during the FastAll or FastPeri mode only. Three external interrupt pins(IRQ1, IRQ2, and IRQ3) are connected to the P-Timer1, 2, and 3. Thus, the timers can be used as the Event Counters.

After the PT1EN(or PT2EN or PT3EN) bit is set to high, the PT1CNT(or PT2CNT or PT3CNT) will start to count the negative edge of a selected input clock. When the PT1EN(or PT2EN or PT3EN) bit is low, the Match signal is never generated even though the contents of the PT1DAT(or PT2DAT or PT3DAT) and PT1CNT(or PT2CNT or PT3CNT) are the same. The PT1CNT(or PT2CNT or PT3CNT) is the 8-bit up-counter that can be cleared by the PT1CLR(or PT2CLR or PT3CLR) bit or the Match signal. The PT1CNT(or PT2CNT or PT3CNT) is a modulo-N counter (from 0 to N-1), N is the content of the PT1DAT(or PT2DAT or PT3DAT). The match signal will always set the PT1INT(or PT2INT or PT3INT) bit to high. The PT1INT(or PT2INT or PT3INT) bit can be cleared by a P-Timer Interrupt Acknowledge or software.

In the Auto-Reload mode, a 50% duty square wave can be out through a pin, PWM1 (or PWM2 or PWM3). If the PT1OE (or PT2OE or PT3OE) in the control register is set to high, a pin will be assigned as the PWM1 (or PWM2 or PWM3) output pin that output a 50% duty square wave.

Duty Cycle = 50%
Output Clock Period = $T_{selected\_clock}$ X PTnDAT X 2
n = 1, 2, or 3

Note: Whenever we disable the PTCNT (clear the PTCR[7]). the PWM output will be frozen at it present state.

3. PWM Mode

If the PT1MD bit (or PT2MD or PT3MD) in the PT1CR (or PT2CR or PT3CR) is high, the P-Timer1 (or P-Timer2 or P-Timer3) will operate in the PWM Mode. Counting clock selection feature is the same with the Auto-Reload Mode.

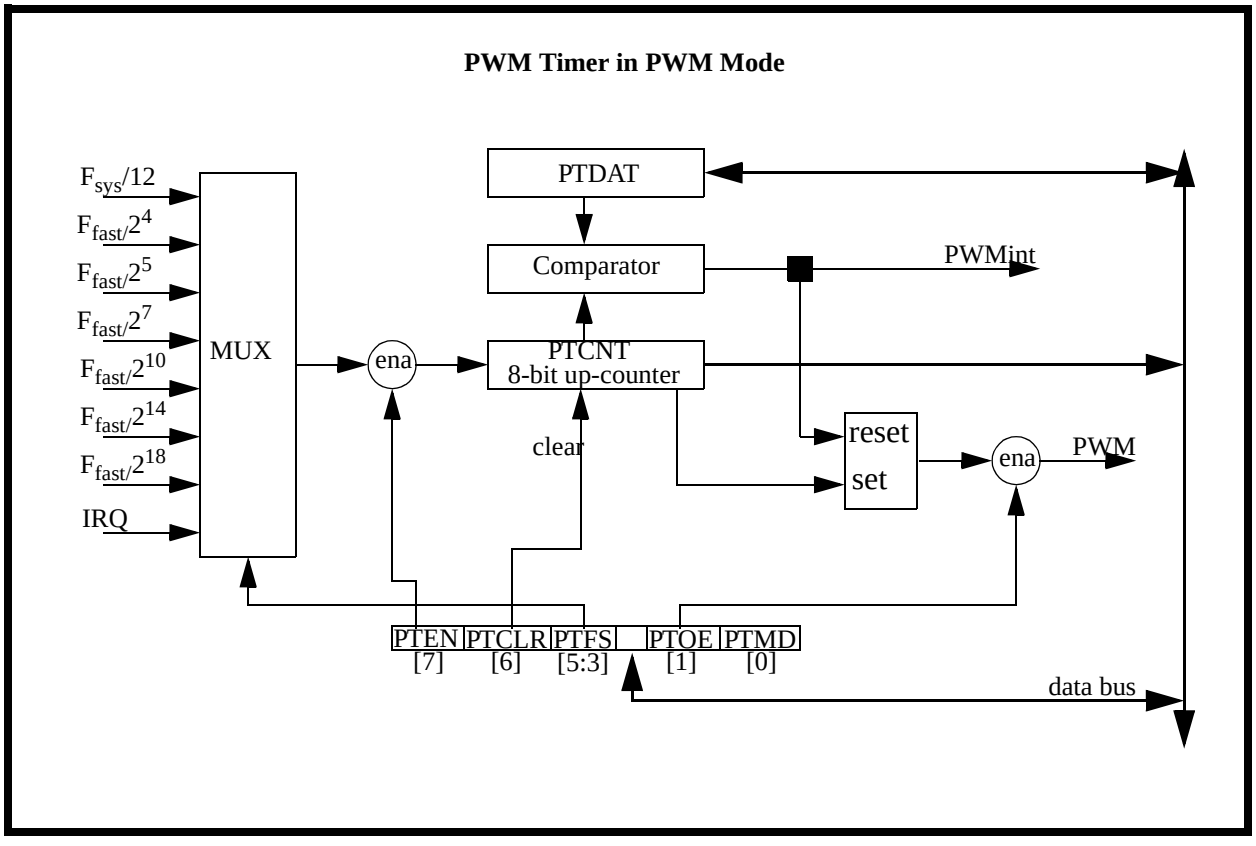
After the PT1EN(or PT2EN or PT3EN) bit is set to high, the PT1CNT(or PT2CNT or PT3CNT) will start to count the negative edge of a selected input clock. When the PT1CNT(or PT2CNT or PT3CNT) is 00H, the PWM output will become high. When the PT1CNT(or PT2CNT or PT3CNT) matches with the PT1DAT(or PT2DAT or PT3DAT), the PWM output will become low. The PT1CNT(or PT2CNT or PT3CNT) is the 8-bit up-counter that can be cleared by the PT1CLR(or PT2CLR or PT3CLR) bit. The PT1CNT(or PT2CNT or PT3CNT) is a modulo-256 counter (from 0 to 255). The match signal will always set the PT1INT(or PT2INT or PT3INT) bit to high. The PT1INT(or PT2INT or PT3INT) bit can be cleared by a PT-Timer Interrupt Acknowledge or software. If these timer interrupts are not needed, those can be disabled in the interrupt control block.

The PWM output can be out through a pin, PWM1 (or PWM2 or PWM3). If the PT1OE (or PT2OE or PT3OE) in the control register is set to high, a pin will be assigned as the PWM1 (or PWM2 or PWM3) output pin.

Duty Cycle = n/256(0 (n (255)
Output Clock Period = $T_{selected\_clock}$ X 256

Note1: Whenever we disable the PTCNT (clear the PTCR[7]). the PWM output will be frozen at it present state.
Note2: PWM output only changes state at either PTCNT = 00h or (PTCNT = PTDAT), if enabled

PWM Timer in PWM Mode



4. PWM Timer Control Registers (PT1CR/PT2CR/PT3CR)

[Table: Definition of PT1CR/PT2CR/PT3CR]

Address	B4/C1/C4							
Bit Addr.								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**PT1EN PT2EN PT3EN**	**PT1CLR PT2CLR PT3CLR**	**PT1FS2 PT2FS2 PT3FS2**	**PT1FS1 PT2FS1 PT3FS1**	**PT1FS0 PT2FS0 PT3FS0**		**PT1OE PT2OE PT3OE**	**PT1MD PT2MD PT3MD**
Definition	**P-Timer ENable**	**P-Timer counter CLeaR**	**P-Timer input Frequency Select bit-2**	**P-Timer input Frequency Select bit-1**	**P-Timer input Frequency Select bit-0**	**Reserved**	**P-Timer Output Enable**	**P-Timer operation MoDe**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W Always 0 read.**	**R/W**	**R/W**	**R/W**	**R**	**R/W**	**R/W**

[Table: The Description of PT1CR/PT2CR/PT3CR]

Name	Bit	Description (Note: n = 1, 2, or 3)
PT1EN PT2EN PT3EN	7	**P-Timer ENable bit** [Bit Status: 0 (Initial Value)] A selected input clock is halted. The PTnCNT keeps counting data. [Bit Status: 1] A selected input clock is run. The PTnCNT counts up the negative edge of the selected clock.
PT1CLR PT2CLR PT3CLR	6	**PTn counter CLeaR bit** If this bit is written with high, the PTnCNT (8-bit up-counter) of the P-Timer will be cleared to 00H. Writing low will not affect anything. When read, a low(0) will be always read.
PT1FS[2:0] PT2FS[2:0] PT3FS[2:0]	5 to 3	**P-Timer input clock Frequency Select bits** [Bit Status: 000 (Initial Value)] $F_{sys}/12$ [Bit Status: 001] $F_{fast}/2^4$ [Bit Status: 010] $F_{fast}/2^5$ [Bit Status: 011] $F_{fast}/2^7$ [Bit Status: 100] $F_{fast}/2^{10}$ [Bit Status: 101] $F_{fast}/2^{14}$ [Bit Status: 110] $F_{fast}/2^{18}$ [Bit Status: 111] IRQn To use the IRQn pin as an Event Input, the pin should be assigned to input mode by a port control register.
PT1INT PT2INT PT3INT	2	**Reserved bit**
PT1OE PT2OE PT3OE	1	**P-Timer Output Enable bit (PWMn pin)** [Bit Status: 0 (Initial Value)] The PWMn output and a bit of general port share a pin. In this status, the pin is used as a general port pin. [Bit Status: 1] In this status, the pin is used as a PWMn pin.
PT1MD PT2MD PT3MD	0	**P-Timer MoDe select bit** [Bit Status: 0 (Initial Value)] Auto-Reload Mode [Bit Status: 1] PWM Mode

5. P-Timer Counter Register (PT1CNT/PT2CNT/PT3CNT)

[Table: Definition of PTnCNT (n = 1, 2, or 3)]

Address	B5/C2/C5							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**PTnCNT[7:0]**							
Definition	**P-Timer-n CouNTer register bit 7 to 0 (Auto-Reload Mode: Modulo N Up-counter: 00 to N-1, N is the content of PTnDAT) (PWM Mode: Modulo 256 Up-counter: 00 to 255)**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Write by Hard-ware	**Written with a new count val-ue 0 or 1. 0 by PTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by PTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by PTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by PTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by PTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by PTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by PTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by PTnCLR.**

[Table: The Description of PTnCNT]

Name	Bit	Description
PTnCNT[7:0]	7 to 0	**P-Timer-n CouNTer bits** [Auto-Reload Mode] A Modulo-N (00 to N-1) up-counter. N is the content of PTnDAT. This counter counts up from 00H to N-1. Then, the counter will go back to 00H and the comparator will generate match signal. The Match signal will issue an interrupt request. The counter will not stop after the Match. Thus, any P-Timer will generate continuous Match signals with a fixed period. [PWM Mode] A Modulo-256 (00 to 255) up-counter. This counter counts up from 00H to 255. Then, the counter will go back to 00H and the PWM output will be set to high. The counter will not stop after the Match or overflow. Thus, any P-Timer will generate continuous PWM output signals with a selected duty and period.

6. P-Timer Data Register (PT1DAT/PT2DAT/PT3DAT)

[Table: Definition of PTnDAT (n = 1, 2, or 3)]

Address	B6/C3/C6							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**PTnDAT[7:0]**							
Definition	**P-Timer-n DATa register bit 7 to 0**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hard-ware	**none**	**none**	**none**	**none**	**none**	**none**	**none**	**none**

[Table: The Description of PTnDAT]

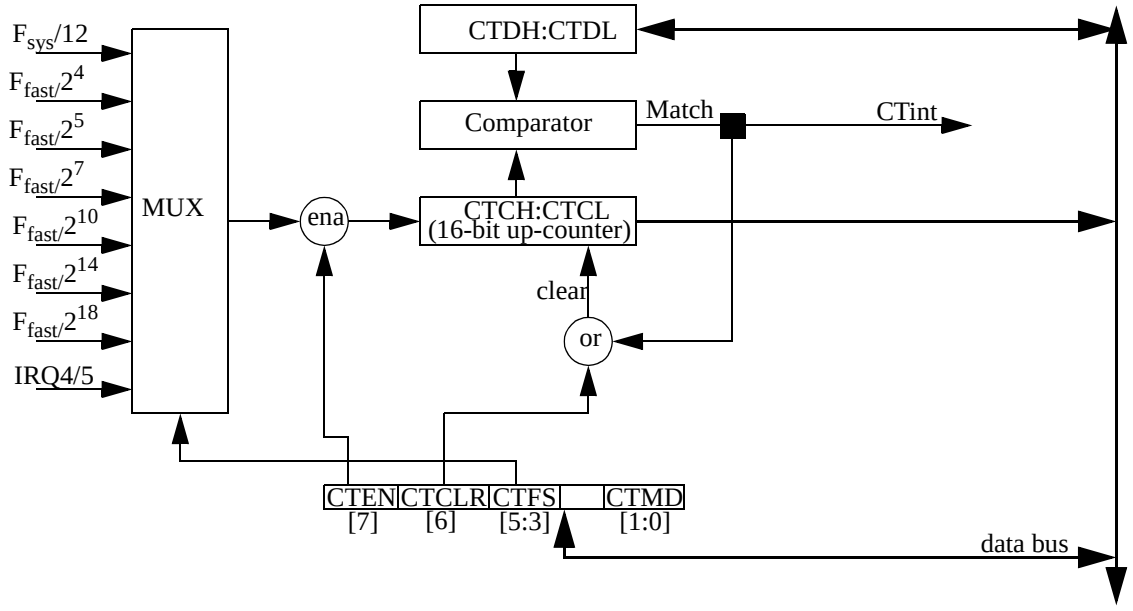
Name	Bit	Description
PTnDAT[7:0]	7 to 0	**P-Timer-n DATa bits** [The first Match period in Auto-Reload Mode] P-Timer Match signal period = (1 / $F_{selected\text{-}clock}$) X (PTnDAT + 1) - Deviation period 0 <= Deviation period < (1 / $F_{selected\text{-}clock}$) [The second or later Match period in Auto-Reload Mode] P-Timer Match signal period = (1 / $F_{selected\text{-}clock}$) X PTnDAT (No Deviation period) [In PWM Mode] Duty Cycle = PTnDAT/256 0 (PTnDAT (255

[Capture Timer1/2]

1. Overview

There are two 16-bit Capture Timer in the MCU, C-Timer1 and C-Timer2. A Capture Timer (or C-Timer) can be used as an Auto-Reload Timer, an Event Counter, or a Capture Timer. A C-Timer is composed of a input frequency select MUX, an 16-bit up-counter(CT1CH-CT1CL, CT2CH-CT2CL), a Comparator, an 16-bit data register(CT1DH-CT1DL, CT2DH-CT2DL), an Edge Detector for Capture, and a control register(CT1CR, CT2CR). There are two operation modes in the C-Timers. These are Auto-Reload Mode and Capture modes that are selected by the CT1MD[1:0] bits (or CT2MD[1:0]) in the CT1CR (or CT2CR). In the Auto-Reload Mode, the C-Timers can be used as an Auto-Reload Timer, an Auto-Reload Event Counter. In the Capture mode, the C-Timer can be used as a Capture Timer.

Capture Timer in Auto-Reload Mode



2. Auto-Reload Mode

If the CT1MD[1:0] bits (or CT2MD[1:0]) in the CT1CR (or CT2CR) are 00B, the C-Timer1 (or C-Timer2) will operate in the Auto-Reload Mode.

A C-Timer has the 8 counting clocks that can be selected by CT1FS[2:0] (or CT2FS[2:0]). The period of the $F_{sys}/12$ clock is one machine cycle or one fastest instruction cycle. This clock will be run during any power-saving mode except the StopAll mode. During the FastAll or FastPeri mode, the $F_{sys}/12$ clock is equal to $F_{fast}/12$. During the SlowAll or SlowPeri mode, the $F_{sys}/12$ clock is equal to $F_{slow}/12$. The $F_{fast}/2^4$, $F_{fast}/2^5$, $F_{fast}/2^7$, $F_{fast}/2^{10}$, $F_{fast}/2^{14}$, and $F_{fast}/2^{18}$ can be used during the FastAll or FastPeri mode only. Two external interrupt pins(IRQ4 and IRQ5) are connected to the C-Timer1 and 2. Thus, the timers can be used as the Event Counters. To use this timer as an Event Counter, the IRQ4 (or IRQ5) should be assigned as an input port by the port control register.

After the CT1EN(or CT2EN) bit is set to high, the CT1CH & CT1CL (or CT2CH & CT2CL) will start to count the negative edge of a selected input clock. When the CT1EN (or CT2EN) bit is low, the Match signal is never generated even though the contents of the CT1DH & CT1DL (or CT2DH & CT2DL) and CT1CH & CT1CL (or CT2CH & CT2CL) are the same. The CT1CH & CT1CL (or CT2CH & CT2CL) is the 16-bit up-counter that can be cleared by the CT1CLR (or CT2CLR) bit or the Match signal. The CT1CH & CT1CL (or CT2CH & CT2CL) is a modulo-N counter (from 0 to N-1), N is the content of the CT1DH & CT1DL (or CT2DH & CT2DL). The match signal will always set the CT1INT (or CT2INT) bit to high. The CT1INT (or CT2INT) bit can be cleared by a C-Timer Interrupt Acknowledge or software.

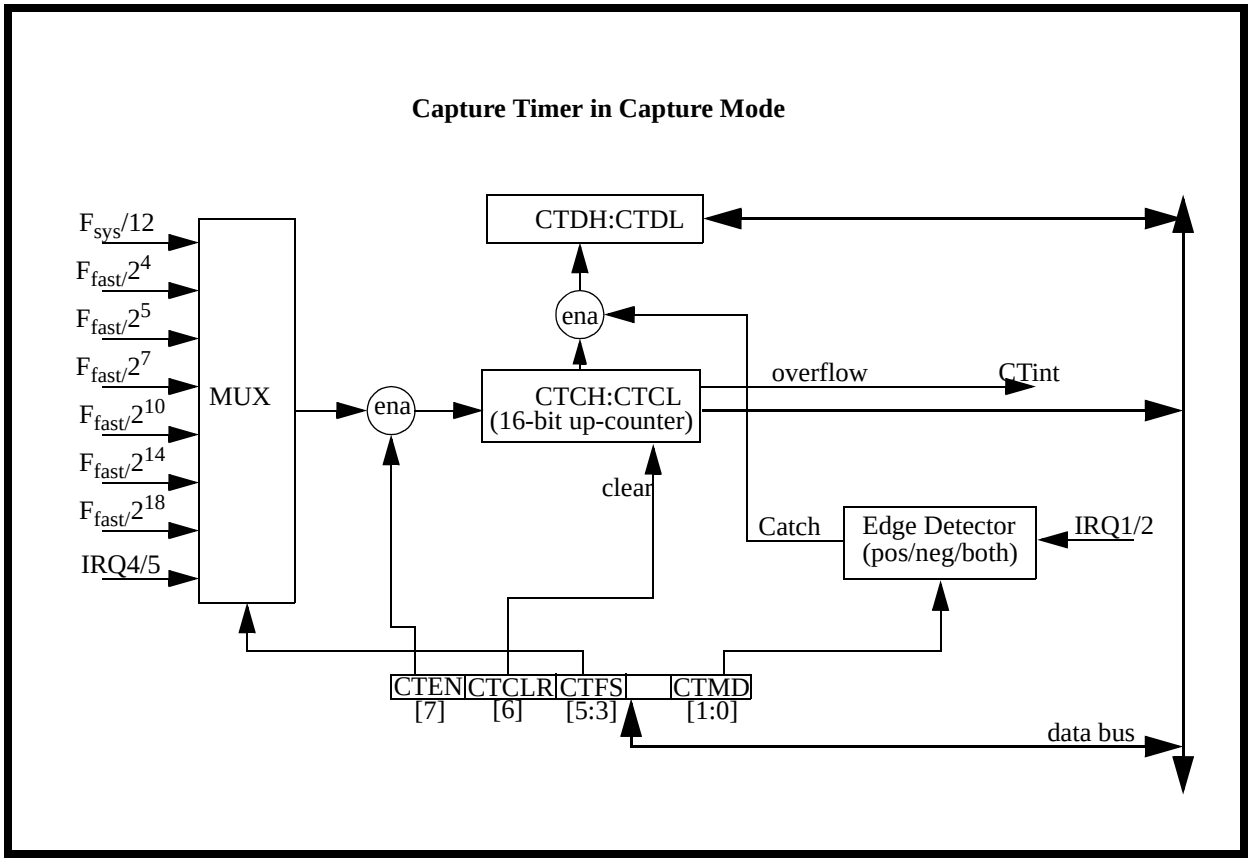
3. Capture Mode

If the CT1MD[1:0] bits (or CT2MD[1:0]) in the CT1CR (or CT2CR) are 01, 10, or 11, the C-Timer1 (or C-Timer2) will operate in the Capture Mode. Counting clock selection feature is the same with the Auto-Reload Mode.

After the CT1EN (or CT2EN) bit is set to high, the 16-bit up-counter (CT1CH & CT1CL or CT2CH & CT2CL) will start to count the negative edge of a selected input clock. The CT1CH & CT1CL (or CT2CH & CT2CL) is the 16-bit up-counter that can be cleared by the CT1CLR (or CT2CLR) bit. The CT1CH & CT1CL (or CT2CH & CT2CL) is a modulo-65536 counter (from 0 to 65535). The overflow signal will always set the CT1INT (or CT2INT) bit to high. The CT1INT (or CT2INT) bit can be cleared by a C-Timer Interrupt Acknowledge or software.

During up-counting, the content of 16-bit counter (CT1CH & CT1CL or CT2CH & CT2CL) will be capture into the 16-bit latch (CT1DH & CT1DL or CT2DH & CT2DL) when an event of IRQ1 (or IRQ2) is detected. One of three event (positive edge, negative edge, or any edge) can be selected by the CT1MD[1:0] bits (or CT2MD[1:0]) in the CT1CR (or CT2CR). To use this feature, the IRQ1 pin (or IRQ2 pin) should be assigned an input port by the port control register. Using the Capture Mode, external clock period or pulse width (high width or low width) can be measured.

Note: While in Capture mode, the CTDH and CTDL are still writable by S/W.



4. Capture Timer Control Registers (CT1CR/CT2CR)

[Table: Definition of CT1CR/CT2CR]

Address	D1/E1							
Bit Addr.								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**CT1EN CT2EN**	**CT1CLR CT2CLR**	**CT1FS2 CT2FS2**	**CT1FS1 CT2FS1**	**CT1FS0 CT2FS0**		**CT1MD1 CT2MD1**	**CT1MD0 CT2MD0**
Definition	**C-Timer ENable**	**C-Timer counter CLeaR**	**C-Timer input Frequency Select bit-2**	**C-Timer input Frequency Select bit-1**	**C-Timer input Frequency Select bit-0**	**Reserved**	**C-Timer operation MoDe bit-1**	**C-Timer operation MoDe bit-0**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W Always 0 read.**	**R/W**	**R/W**	**R/W**	**R**	**R/W**	**R/W**

[Table: The Description of CT1CR/CT2CR]

Name	Bit	Description (Note: n = 1 or 2)
CT1EN CT2EN	7	**C-Timer ENable bit** [Bit Status: 0 (Initial Value)] A selected input clock is halted. The CTnCH & CTnCL keeps counting value. [Bit Status: 1] A selected input clock is run. The CTnCH & CTnCL counts up the negative edge of the selected clock.
CT1CLR CT2CLR	6	**CTn counter CLeaR bit** If this bit is written with high, the CTnCH & CTnCL (16-bit up-counter) of the C-Timer will be cleared to 0000H. Writing low will not affect anything. When read, a low(0) will be always read.
CT1FS[2:0] CT2FS[2:0]	5 to 3	**C-Timer input clock Frequency Select bits** [Bit Status: 000 (Initial Value)] $F_{sys}/12$ [Bit Status: 001] $F_{fast}/2^4$ [Bit Status: 010] $F_{fast}/2^5$ [Bit Status: 011] $F_{fast}/2^7$ [Bit Status: 100] $F_{fast}/2^{10}$ [Bit Status: 101] $F_{fast}/2^{14}$ [Bit Status: 110] $F_{fast}/2^{18}$ [Bit Status: 111] IRQ4 or IRQ5 To use the IRQ4 or IRQ5 pin as an Event Input, the pin should be assigned to input mode by a port control register.
CT1INT CT2INT	2	**Reserved bit**
CT1MD[1:0] CT2MD[1:0]	1 to 0	**C-Timer MoDe select bits** [Bit Status: 00 (Initial Value)] Auto-Reload Mode [Bit Status: 01] Positive Edge Detect Capture Mode [Bit Status: 10] Negative Edge Detect Capture Mode [Bit Status: 11] Any Edge (Positive or Negative) Detect Capture Mode

5. C-Timer Counter Registers (CT1CH & CT1CL / CT2CH & CT2CL)

[Table: Definition of CTnCH (n = 1 or 2)]

Address	D3/E3							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**CTnCH[7:0]**							
Definition	**C-Timer-n CouNTer register bit 15 to 8 (Auto-Reload Mode: High 8-bit of the Modulo N Up-counter: 0000H to N-1, N is the content of CTnDH & CTnDL) (Capture Mode: High 8-bit of the Modulo 65536 Up-counter: 00 to 65535)**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Write by Hard-ware	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**

[Table: Definition of CTnCL (n = 1 or 2)]

Address	D2/E2							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**CTnCL[7:0]**							
Definition	**C-Timer-n CouNTer register bit 7 to 0 (Auto-Reload Mode: Low 8-bit of the Modulo N Up-counter: 0000H to N-1, N is the content of CTnDH & CTnDL) (Capture Mode: Low 8-bit of the Modulo 65536 Up-counter: 00 to 65535)**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
Write by Hard-ware	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**	**Written with a new count val-ue 0 or 1. 0 by CTnCLR.**

[Table: The Description of CTnCH & CTnCL]

Name	Bit	Description
CTnCH[7:0] & CTnCL[7:0]	15 to 0	**C-Timer-n CouNTer bits** [Auto-Reload Mode] A Modulo-N (0000H to N-1) up-counter. N is the content of CTnDH & CT-nDL. This counter counts up from 0000H to N-1. Then, the counter will go back to 0000H and the comparator will generate match signal. The Match signal will issue an interrupt request. The counter will not stop after the Match. Thus, any C-Timer will generate continuous Match signals with a fixed period. [Capture Mode] A Modulo-65536 (0000H to 65535) up-counter. This counter counts up from 0000H to 65535. Then, the counter will go back to 0000H and the CTnINT will be set to high. The counter will not stop after the overflow. Thus, any C-Timer will generate continuous interrupt request with a fixed period.

6. C-Timer Data Register (CT1DH & CT1DL / CT2DH & CT2DL)

[Table: Definition of CTnDH (n = 1 or 2)]

Address	D5/E5							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**CTnDH[7:0]**							
Definition	**C-Timer-n DATa register bit 15 to 8**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hard-ware	**[A-Reload] none [Capture] Written with CT-nDH when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDH when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDH when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDH when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDH when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDH when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDH when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDH when IRQ4/5 edge**

[Table: Definition of CTnDL (n = 1 or 2)]

Address	D4/E4							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**CTnDL[7:0]**							
Definition	**C-Timer-n DATa register bit 7 to 0**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Soft-ware	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hard-ware	**[A-Reload] none [Capture] Written with CT-nDL when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDL when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDL when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDL when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDL when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDL when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDL when IRQ4/5 edge**	**[A-Reload] none [Capture] Written with CT-nDL when IRQ4/5 edge**

[Table: The Description of CTnDATH & CTnDL]

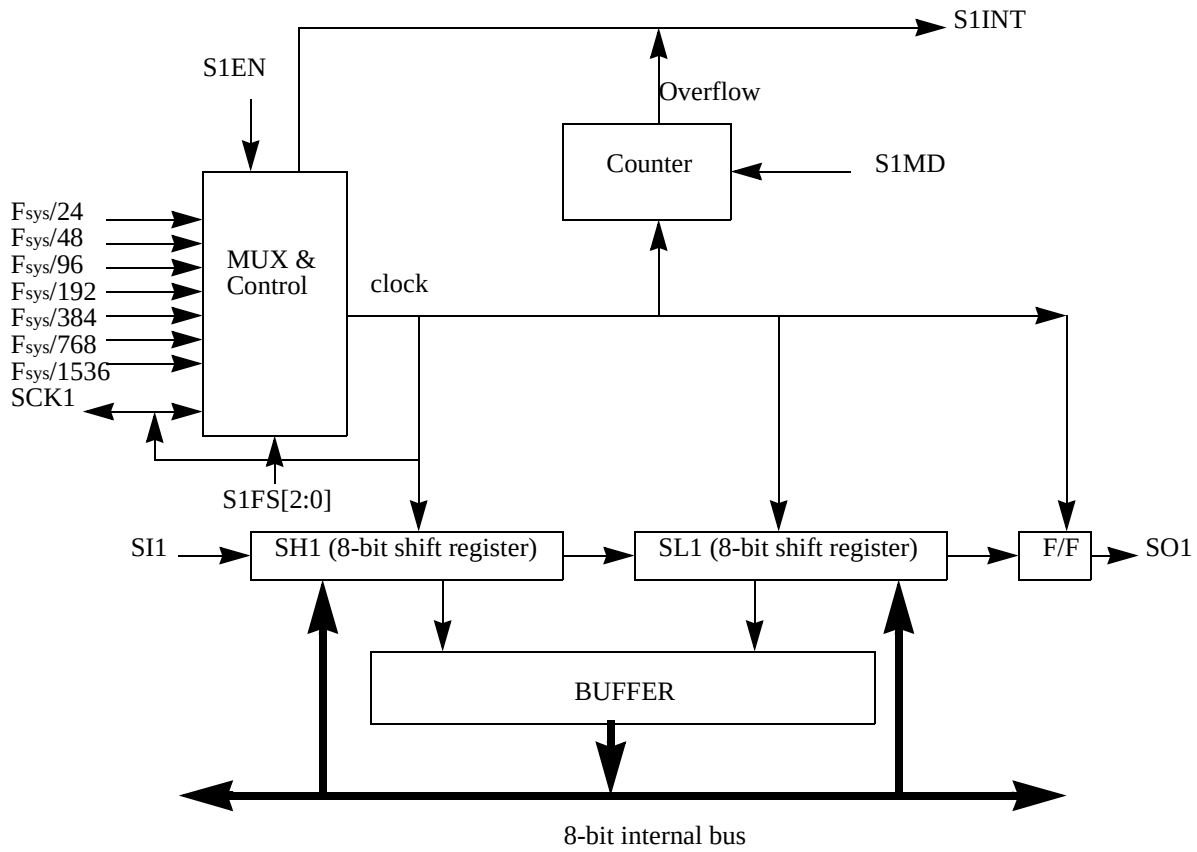
Name	Bit	Description
CTnDH[7:0] & CTnDL[7:0]	15 to 0	**C-Timer-n DATa bits** [The first Match period in Auto-Reload Mode] C-Timer Match signal period = $(1 / F_{selected\text{-}clock})$ X ({CTnDH,CTnDL} + 1) - Deviation period 0 <= Deviation period < $(1 / F_{selected\text{-}clock})$ [The second or later Match period in Auto-Reload Mode] C-Timer Match signal period = $(1 / F_{selected\text{-}clock})$ X CTnDH&CTnDL (No Deviation period) [In Capture Mode] The CTnDH & CTnDL is updated by the content of the CTnCH & CTnCL when a selected edge of IRQ4 or IRQ5 is happened.

SIO-1(16/8-Bit Serial In-Out)

1. Overview

There is an 16/8-bit SIO (Serial In-Out) in the MCU, SIO-1. The SIO-1 can be used as a 16-bit serial-in, 16-bit serial-out, 16-bit serial-I/O, 8-bit serial-in, 8-bit serial-out, and 8-bit serial-I/O. SIO-1 is receive buffered, meaning it can commence reception before a previously received data has been read from the register. (However, if the data still hasn't been read by the time reception of the next data is complete, one of the data will be lost). The SIO-1 is composed of a input frequency select MUX and control, a clock divider, an up-counter, a 16-bit shift register (SH1 and SL1), a 1-bit flip-flop for serial output synchronization, a control register(SIO1CR) and a 16-bit buffer. Note SH1 is SIO1DH and SL1 is SIO1DL in SFR table.

[SIO -1(16/8-bit) Block Diagram]



2. 8-bit Serial-Output Mode

[Table: Control Bits of SIO1CR for 8-bit Serial-Output Mode]

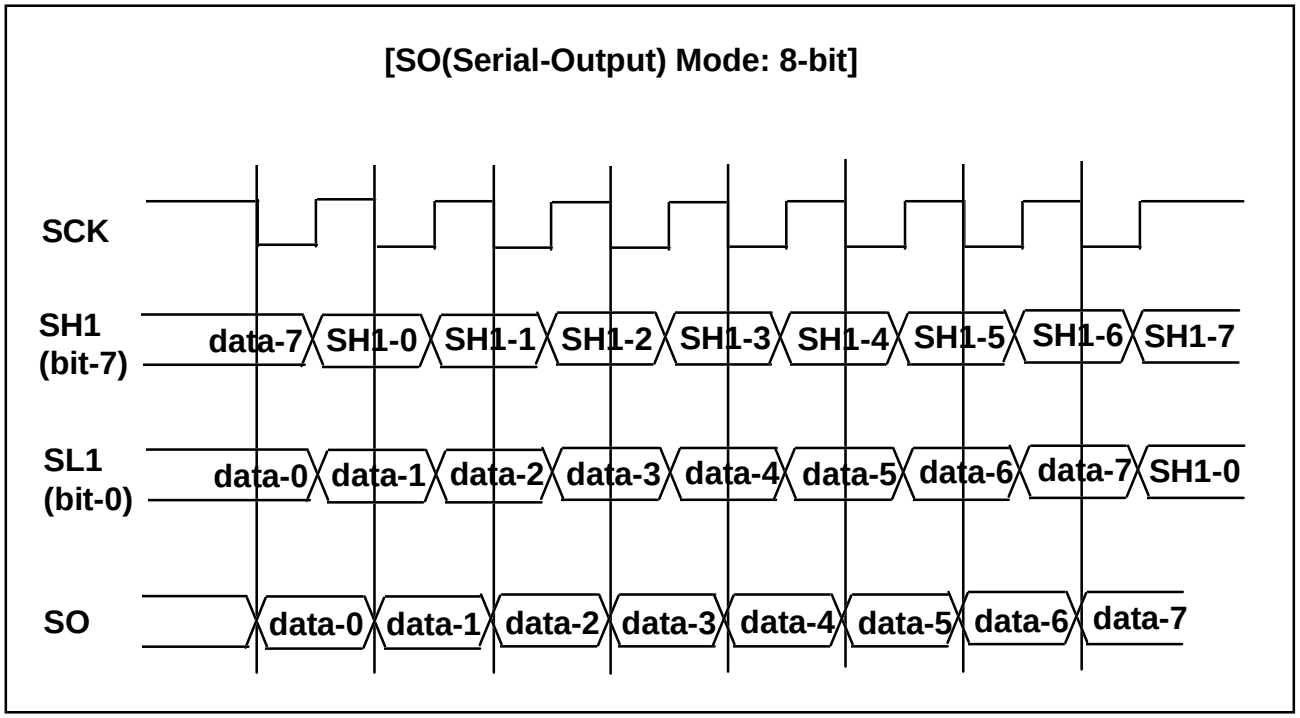
Control Bit	SO1OE (bit-1)	S1MD (bit-0)
Content	1	0

[Table: Pin Configuration of SIO-1 for 8-bit Serial-Output Mode]

Pin	In/Out Mode	Note
SI1	Normal Port Input or Output	The pin SI1 may be used for a normal port pin not for serial input. The I/O mode of the pin is decided by a port control register.
SO1	SO1 output	SO1OE = 1
SCK1 (S1FS[2:0] = ‘000’)	SCK1 input mode	The pin SCK1 should be assigned as input mode by the port control register.
SCK1 (S1FS[2:0] = ‘1 or 1 or 1’)	SCK1 output mode	The pin SCK1 is assigned as the SCK1 output pin automatically by the S1FS[2:0].

[Table: Shift Registers of SIO-1 for 8-bit Serial-Output Mode]

Shift Register	SH1 (SFR SIO1DH Address F2)	SL1 (SFR SIO1DL address F3)
Operation	(Not Used) The MSB (bit-7) is connected to SI1. SI1 should be synchronized to negative edge of the SCK1 if it needed. The shift operation is performed on positive edge of the SCK1.	The SL1 should be loaded 8-bit data to be serial output before operation. The LSB(bit-0) is connected to the output flip-flop. The flip-flop is connected to the SO1 pin. The shift operation is performed on positive edge of the SCK1. The SO1 output synchronized to the just next negative edge of the SCK1. After 8-bit shift, SL1 will have previous SH1 content.



3. 16-bit Serial-Output Mode

[Table: Control Bits of SIO1CR for 16-bit Serial-Output Mode]

Control Bit	SO1OE (bit-1)	S1MD (bit-0)
Content	1	1

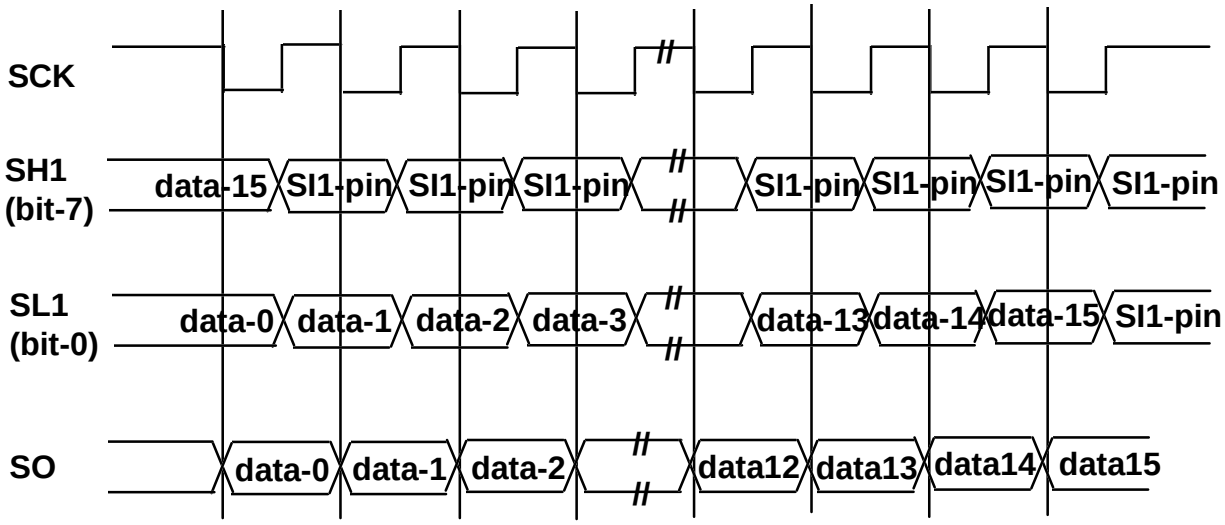
[Table: Pin Configuration of SIO-1 for 16-bit Serial-Output Mode]

Pin	In/Out Mode	Note
SI1	Normal Port Input or Output	The pin SI1 may be used for a normal port pin not for serial input. The I/O mode of the pin is decided by a port control register.
SO1	SO1 output	SO1OE = 1
SCK1 (S1FS[2:0] = ‘000’)	SCK1 input mode	The pin SCK1 should be assigned as input mode by the port control register.
SCK1 (S1FS[2:0] = ‘1 or 1 or 1’)	SCK1 output mode	The pin SCK1 is assigned as the SCK1 output pin automatically by the S1FS[2:0].

[Table: Shift Registers of SIO-1 for 16-bit Serial-Output Mode]

Shift Register	SH1 (SFR SIODH Address F2)	SL1 (SFR SIO1DL Address F3)
Operation	The SH1 should be loaded high 8-bit data to be serial output before operation. The MSB (bit-7) is connected to SI1. SI1 should be synchronized to negative edge of the SCK1 if it needed. The shift operation is performed on positive edge of the SCK1.	The SL1 should be loaded low 8-bit data to be serial output before operation. The LSB(bit-0) is connected to the output flip-flop. The flip-flop is connected to the SO1 pin. The shift operation is performed on positive edge of the SCK1. The SO1 output synchronized to the just next negative edge of the SCK1. After 16-bit shift, SL1 will have the content from SI1 pin.

[SO(Serial-Output) Mode: 16-bit]



4. 8-bit Serial-Input Mode

[Table: Control Bits of SIO1CR for 8-bit Serial-Input Mode]

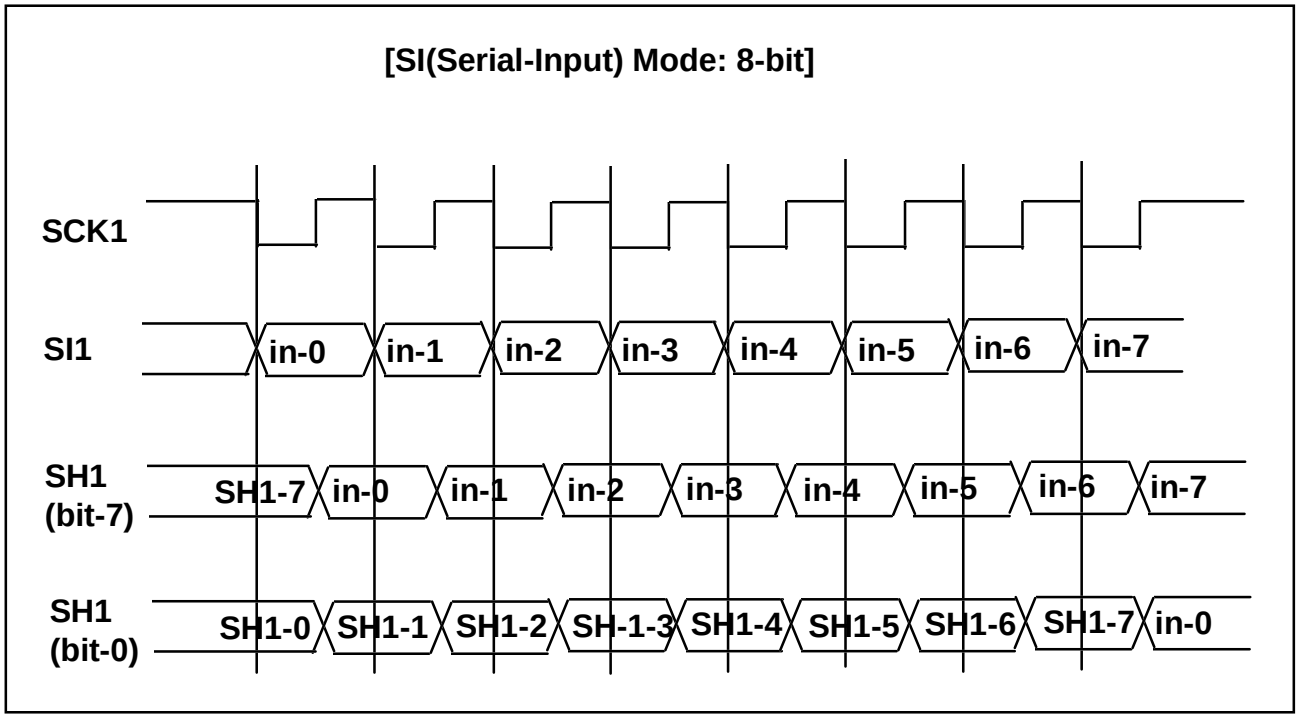
Control Bit	SO1OE (bit-1)	S1MD (bit-0)
Content	0	0

[Table: Pin Configuration of SIO-1 for 8-bit Serial-Input Mode]

Pin	In/Out Mode	Note
SI1	Input Mode	The pin SI1 must be assigned to input mode by a port control register.
SO1	Normal Port	SO1OE = 0. This pin can be used as a normal input or output port.
SCK1 (S1FS[2:0] = ‘000’)	SCK1 input mode	The pin SCK1 should be assigned as input mode by the port control register.
SCK1 (S1FS[2:0] = ‘1 or 1 or 1’)	SCK1 output mode	The pin SCK1 is assigned as the SCK1 output pin automatically by the S1FS[2:0].

[Table: Shift Registers of SIO-1 for 8-bit Serial-Input Mode]

Shift Register	SH1 (SFR SIO1DH Adress F2)	SL1 (SFR SIO1DL Address F3)
Operation	The MSB (bit-7) is connected to SI1. SI1 should be synchronized to negative edge of the SCK1. The shift operation is performed on positive edge of the SCK1. After 8-bit shift, SH1 will have 8-bit serial input data.	(Not Used) The LSB(bit-0) is connected to the output flip-flop. The flip-flop is disconnected to the SO1 pin. The shift operation is performed on positive edge of the SCK. After 8-bit shift, SL1 will have previous SH1 content.



5. 16-bit Serial-Input Mode

[Table: Control Bits of SIO1CR for 16-bit Serial-Input Mode]

Control Bit	SO1OE (bit-1)	S1MD (bit-0)
Content	0	1

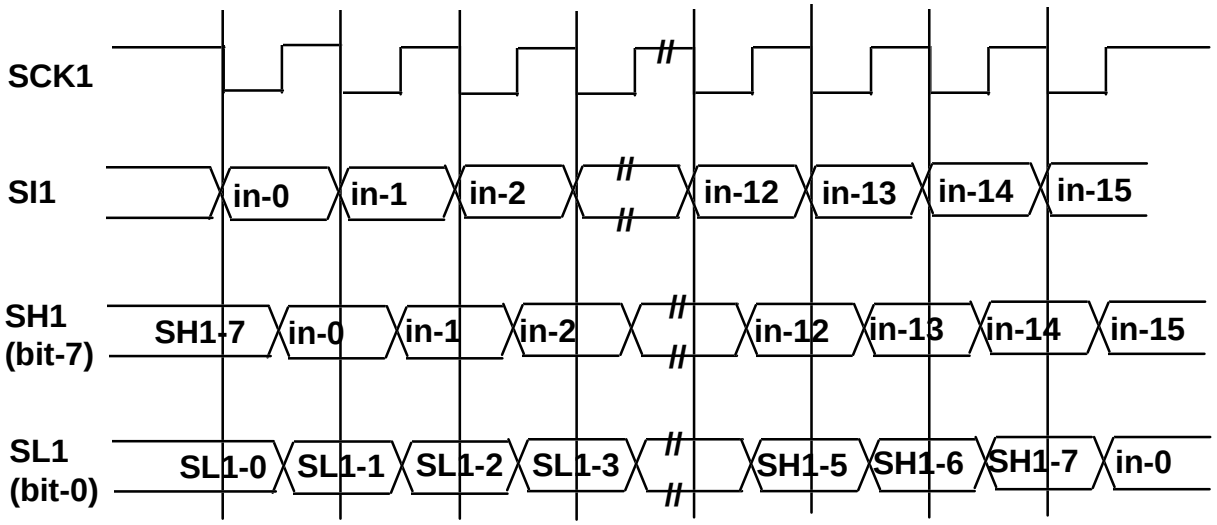
[Table: Pin Configuration of SIO-1 for 16-bit Serial-Input Mode]

Pin	In/Out Mode	Note
SI1	Input Mode	The pin SI1 must be assigned to input mode by a port control register.
SO1	Normal Port	SO1OE = 0. This pin can be used as a normal input or output port.
SCK1 (S1FS[2:0] = ‘000’)	SCK1 input mode	The pin SCK1 should be assigned as input mode by the port control register.
SCK1 (S1FS[2:0] = ‘1 or 1 or 1’)	SCK1 output mode	The pin SCK1 is assigned as the SCK1 output pin automatically by the S1FS[2:0].

[Table: Shift Registers of SIO-1 for 16-bit Serial-Input Mode]

Shift Register	SH1 (SFR SIO1DH address F2)	SL1 (SFR SIO1DL address F3)
Operation	The MSB (bit-7) is connected to SI1. The SI1 input signal should be synchronized to negative edge of the SCK1. The shift operation is performed on positive edge of the SCK1. After 16-bit shift, SH1 will have upper 8-bit serial input data.	The LSB(bit-0) is connected to the output flip-flop. The flip-flop is disconnected to the SO1 pin. The shift operation is performed on positive edge of the SCK. After 16-bit shift, SL1 will have lower 8-bit serial input data.

[SI(Serial-Input) Mode: 16-bit]



6. 8-bit Serial-I/O Mode

[Table: Control Bits of SIO1CR for 8-bit Serial-I/O Mode]

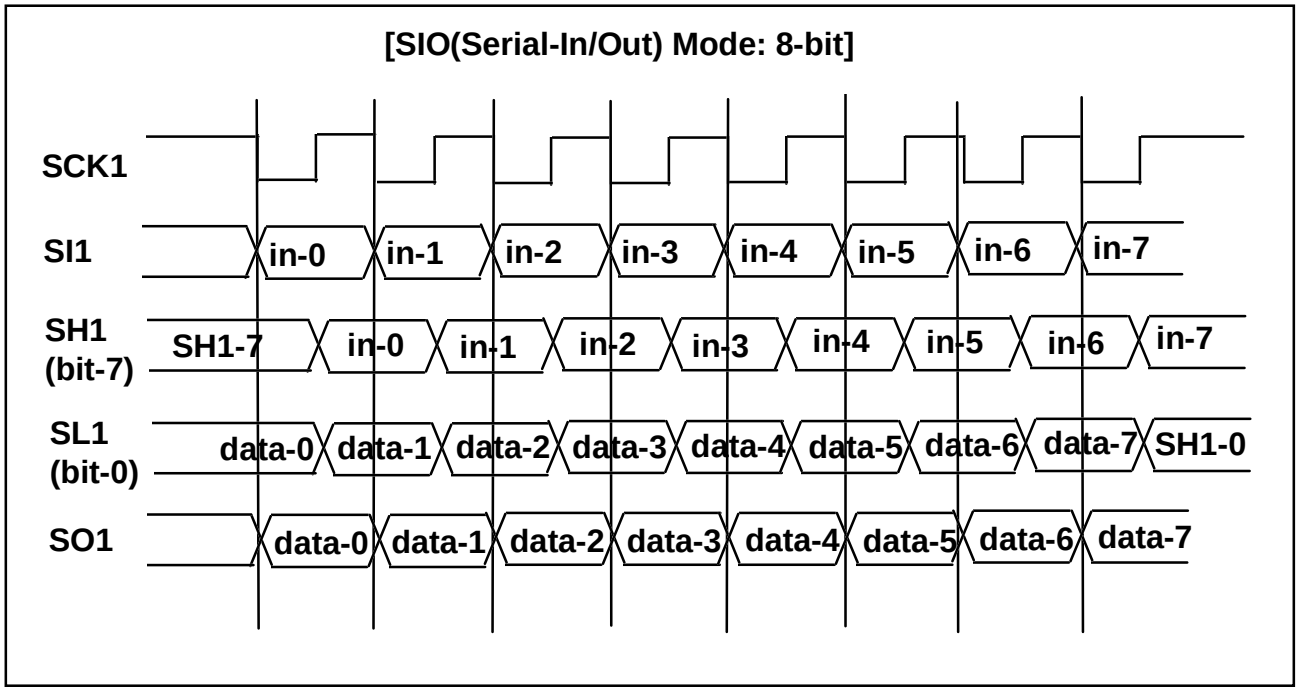
Control Bit	SO1OE (bit-1)	S1MD (bit-0)
Content	1	0

[Table: Pin Configuration of SIO-1 for 8-bit Serial-I/O Mode]

Pin	In/Out Mode	Note
SI1	Input Mode	The pin SI1 must be assigned to input mode by a port control register.
SO1	SO1 output	SO1OE = 1
SCK1 (S1FS[2:0] = ‘000’)	SCK1 input mode	The pin SCK1 should be assigned as input mode by the port control register.
SCK1 (S1FS[2:0] = ‘1 or 1 or 1’)	SCK1 output mode	The pin SCK1 is assigned as the SCK1 output pin automatically by the S1FS[2:0].

[Table: Shift Registers of SIO-1 for 8-bit Serial-I/O Mode]

Shift Register	SH1 (SFR SIO1DH Address F2)	SL1 (SFR SIO1DL Address F3)
Operation	(For Serial Input) The MSB (bit-7) is connected to SI1. The SI1 input signal should be synchronized to negative edge of the SCK1. The shift operation is performed on positive edge of the SCK1. After 8-bit shift, SH1 will have 8-bit serial input data.	(For Serial Output) The SL1 should be loaded 8-bit data to be serial output before operation. The LSB(bit-0) is connected to the output flip-flop. The flip-flop is connected to the SO1 pin. The shift operation is performed on positive edge of the SCK1. The SO1 output synchronized to the just next negative edge of the SCK1. After 8-bit shift, SL1 will have previous SH1 content.



7. 16-bit Serial-I/O Mode

[Table: Control Bits of SIO1CR for 16-bit Serial-I/O Mode]

Control Bit	SO1OE (bit-1)	S1MD (bit-0)
Content	1	1

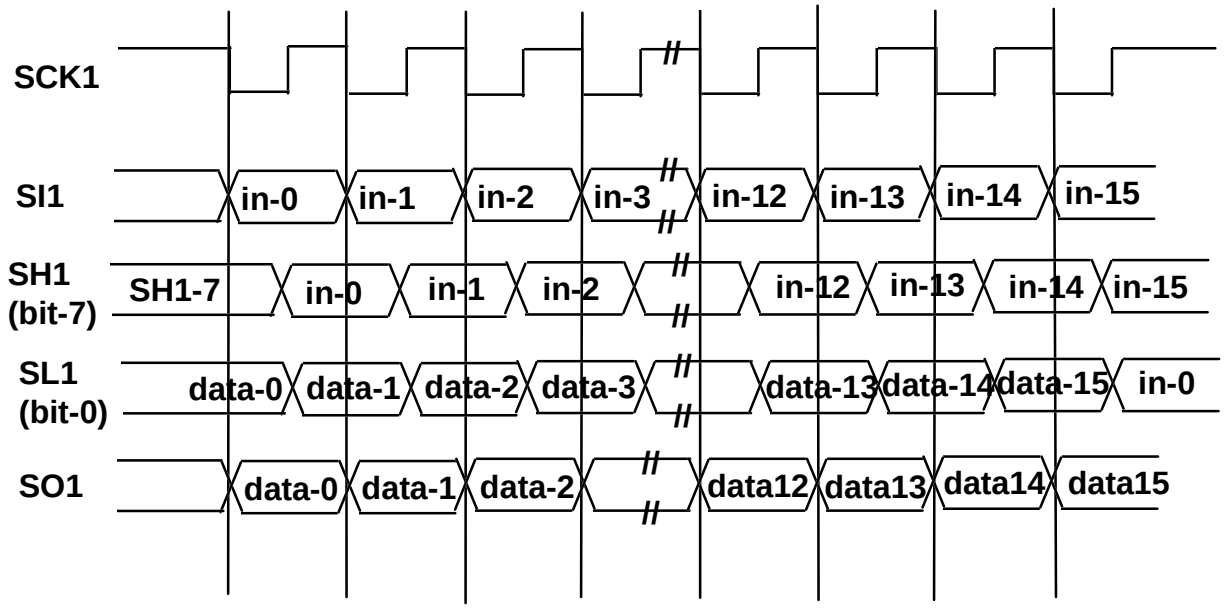
[Table: Pin Configuration of SIO-1 for 16-bit Serial-I/O Mode]

Pin	In/Out Mode	Note
SI1	Input Mode	The pin SI1 must be assigned to input mode by a port control register.
SO1	SO1 output	SO1OE = 1
SCK1 (S1FS[2:0] = ‘000’)	SCK1 input mode	The pin SCK1 should be assigned as input mode by the port control register.
SCK1 (S1FS[2:0] = ‘1 or 1 or 1’)	SCK1 output mode	The pin SCK1 is assigned as the SCK1 output pin automatically by the S1FS[2:0].

[Table: Shift Registers of SIO-1 for 16-bit Serial-I/O Mode]

Shift Register	SH1 (SFR SIO1DH Address F2)	SL1 (SFR SIO1DL Address F3)
Operation	The SH1 should be loaded upper 8-bit data to be serial output before operation. The MSB (bit-7) is connected to SI1. The SI1 input signal should be synchronized to negative edge of the SCK1. The shift operation is performed on positive edge of the SCK1. After 16-bit shift, the SH1 will have upper 8-bit serial input data.	The SL1 should be loaded lower 8-bit data to be serial output before operation. The LSB(bit-0) is connected to the output flip-flop. The flip-flop is connected to the SO1 pin. The shift operation is performed on positive edge of the SCK1. The SO1 output synchronized to the just next negative edge of the SCK1. After 16-bit shift, SL1 will have lower 8-bit serial input data.

[SIO(Serial-In/Out) Mode: 16-bit]



8. SIO-1 Control Register (SIO1CR)

[Table: Definition of SIO1CR]

Address	F1H							
Bit Addr.								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**S1EN**		**S1FS2**	**S1FS1**	**S1FS0**		**SO1OE**	**S1MD**
Definition	**SIO-1 ENable**	**Reserved bit**	**SIO-1 input Frequency Select bit-2**	**SIO-1 input Frequency Select bit-1**	**SIO-1 input Frequency Select bit-0**	**Reserved bit**	**SIO-1 SO1 Output Enable**	**SIO-1 operation MoDe**
Reset Value	**0**	**unknown**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Software	**R/W**		**R/W**	**R/W**	**R/W**	**User MUST write a '0' to this bit. This bit is readable and writ-able.**	**R/W**	**R/W**
Write by Hardware	**0 by SIO-1 over-flow or S/W**							

[Table: The Description of SIO1CR]

Name	Bit	Description
S1EN	7	**SIO-1 ENable bit** [Bit Status: 0 (Initial Value)] A selected input clock is halted to high. The SIO-1 counter is cleared to 0. [Bit Status: 1] A selected input clock is run. The SIO-1 counter counts up the negative edge of the select-ed clock.
Reserved	6	

S1FS[2:0]	5 to 3	**SIO-1 input clock Frequency Select bits** [Bit Status: 000 (Initial Value)] SCK1 (from external input) [Bit Status: 001] F_{sys}/24 [Bit Status: 010] F_{sys}/48 [Bit Status: 011] F_{sys}/96 [Bit Status: 100] F_{sys}/192 [Bit Status: 101] F_{sys}/384 [Bit Status: 110] F_{sys}/768 [Bit Status: 111] F_{sys}/1536 To use the SCK1 pin as an external clock input, the SCK1 pin should be assigned to input mode by a port control register.
Reserved	2	User **MUST** write a '0' to this bit. **NEVER** write a '1' to this bit.
SO1OE	1	**SO1 Output Enable** [Bit Status: 0 (Initial Value)] The pin SO1 can be used as a normal I/O port. [Bit Status: 1] The pin SO1 is used as the serial output pin.
S1MD	0	**SIO-1 MoDe select bits** [Bit Status: 0 (Initial Value)] 8-bit Mode [Bit Status: 1] 16-bit Mode

9. SIO-1 Shift Registers (SIO1DH & SIO1DL)

[Table: Definition of SIO1DH]

Address	F2H							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**SIO1DH[7:0]**							
Definition	**Shift register High byte** **8-bit SO Mode: Not Used** **16-bit SO Mode: Upper 8-bit output buffer** **8-bit SI Mode: 8-bit input buffer** **16-bit SI Mode: Upper 8-bit input buffer** **8-bit SIO Mode: 8-bit input buffer** **16-bit SIO Mode: Upper 8-bit output buffer & Upper 8-bit input buffer**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**

[Table: Definition of SIO1DL]

Address	F3H							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**SIO1DL[7:0]**							
Definition	**Shift register Low byte** **8-bit SO Mode: 8-bit output buffer** **16-bit SO Mode: Lower 8-bit output buffer** **8-bit SI Mode: Not Used** **16-bit SI Mode: Lower 8-bit input buffer** **8-bit SIO Mode: 8-bit output buffer** **16-bit SIO Mode: Lower 8-bit output buffer & Lower 8-bit input buffer**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**undefined**
Read/ Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**

10. Serial In

STEP-1:
Before the SIO-1 clock signal get transmitted through SCK1 pin, SCK1 pin should set to high. This is necessary only when internal clock is used (SIO1CR[5:3] not equal to 000).

STEP-2:
Then, user should enable the SIO-1. This is done by writing the SIO1CR with proper value.

STEP-3:
If internal clock is used, SIO-1 will generate the appropriate clock signal for interfacing with the external chip.

If external clock is used, user will need to signal the external chip that SIO-1 is ready to take data and clock signal.

STEP-4:
After receiving the data, S1INT(interrupt signal) will set to high. At that time, SIO-1 waits for the CPU to read the received data.

11. Serial Out

STEP-1:
Before the SIO-1 clock signal get transmitted through SCK1 pin, SCK1 pin should set to high. This is necessary only when internal clock is used (SIO1CR[5:3] not equal to 000).

STEP-2:
Then, user should write the data to appropriate data register, SIO1DL for eight bit serial out and both SIO1DL & SIO1DH for sixteen bit serial out.

STEP-3:
Next, user should enable the SIO-1. This is done by writing the SIO1CR with proper value.

STEP-4:
If internal clock is used, SIO-1 will generate the appropriate clock signal for interfacing with the external chip.

If external clock is used, user will need to signal the external chip that SIO-1 is ready to transmit the data and is waiting for their clock signal.

STEP-5:
After transmitting the data, S1INT will set to high.

12. Serial-I/O:

Before the SIO-1 clock signal get transmitted through SCK1 pin, SCK1 pin should set to high. This is necessary only when internal clock is used (SIO1CR[5:3] not equal to 000).

STEP-2:
Then, user should write the data to appropriate data register, SIO1DL for eight bit serial I/O and both SIO1DL & SIO1DH for serial I/O.

STEP-3:
Next, user should enable the SIO-1. This is done by writing the SIO1CR with proper value.

STEP-4:
If internal clock is used, SIO-1 will generate the appropriate clock signal for interfacing with the external chip.

If external clock is used, user will need to signal the external chip that SIO-1 is ready to do transmission and reception, and is waiting for their clock signal.

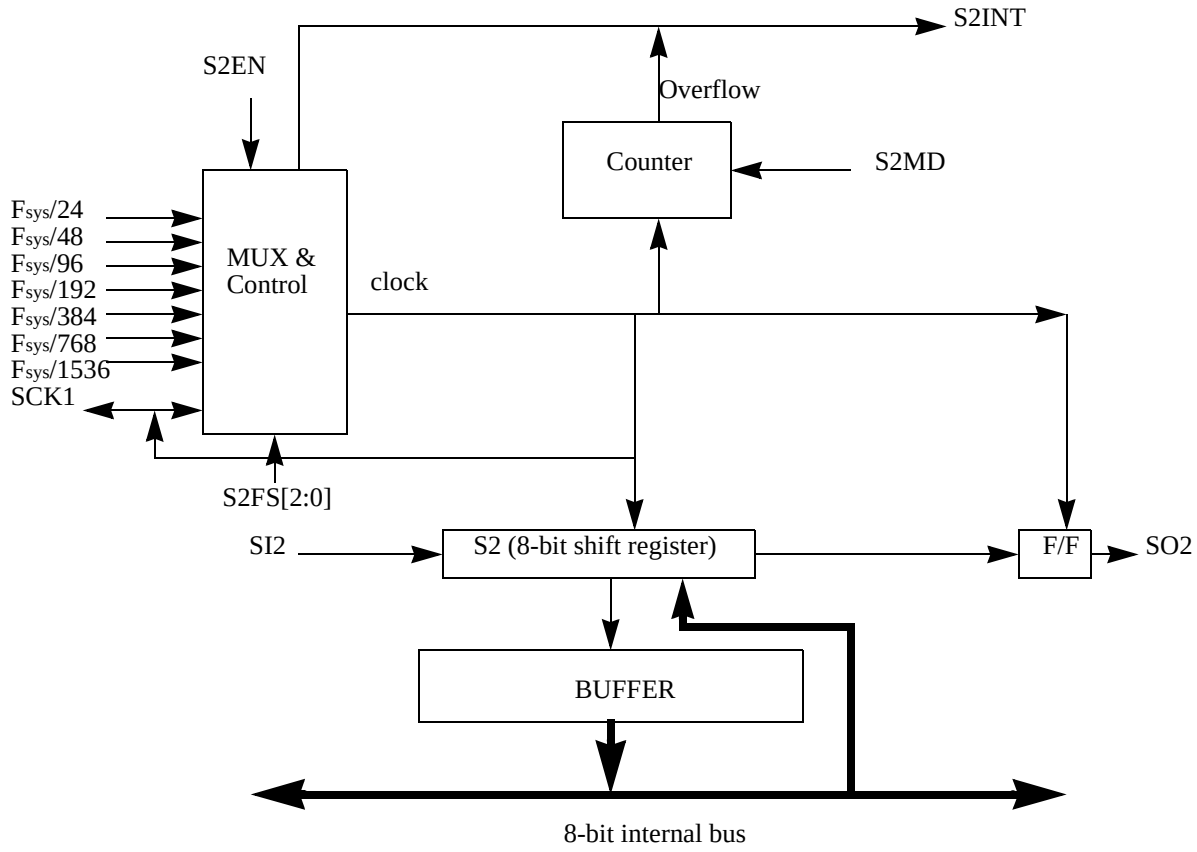
STEP-5:
After the operation, S1INT will set to high. At this time, SIO1 waits for CPU to read the received data.

[SIO-2 (8-Bit Serial In-Out)]

1. Overview

There is an 8-bit SIO (Serial In-Out) in the MCU, SIO-2. The SIO-2 can be used as a 8-bit serial-in, 8-bit serial-out, and 8-bit serial-I/O. SIO-2 is receive buffered, meaning it can commence reception before a previously received data has been read from the register. (However, if the data still hasn't been read by the time reception of the next data is complete, one of the data will be lost). The SIO-2 is composed of a input frequency select MUX and control, an up-counter, a 8-bit shift register (S2), a 1-bit flip-flop for serial output synchronization, a control register (SIO2CR), and a buffer. Note S2 is SIO2D in the SFR table.

[SIO-2 (8-bit) Block Diagram]



2. 8-bit Serial-Output Mode

[Table: Control Bits of SIO2CR for 8-bit Serial-Output Mode]

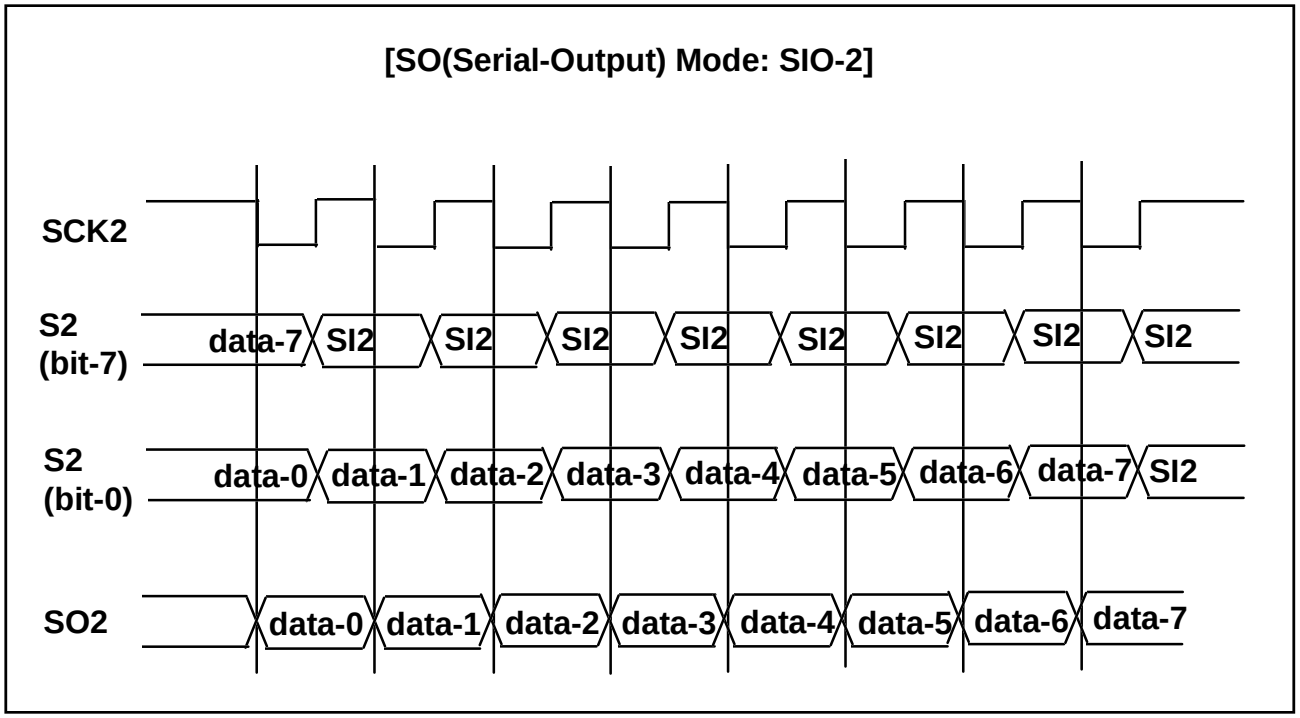
Control Bit	SO2OE (bit-1)
Content	1

[Table: Pin Configuration of SIO-2 for 8-bit Serial-Output Mode]

Pin	In/Out Mode	Note
SI2	Normal Port Input or Output	The pin SI2 may be used for a normal port pin not for serial input. The I/O mode of the pin is decided by a port control register.
SO2	SO2 output	SO2OE = 1
SCK2 (S2FS[2:0] = ‘000’)	SCK2 input mode	The pin SCK2 should be assigned as input mode by the port control register.
SCK2 (S2FS[2:0] = ‘1 or 1 or 1’)	SCK2 output mode	The pin SCK2 is assigned as the SCK2 output pin automatically by the S2FS[2:0].

[Table: Shift Registers of SIO-2 for 8-bit Serial-Output Mode]

Shift Register	S2 (SFR SIO2D Address F4)
Operation	The MSB (bit-7) is connected to SI2. The SI2 input signal should be synchronized to negative edge of the SCK2 if it needed. The S2 should be loaded with 8-bit data to be serial output before operation. The LSB(bit-0) is connected to the output flip-flop. The flip-flop is connected to the SO2 pin. The shift operation is performed on positive edge of the SCK2. The SO2 output synchronized to the just next negative edge of the SCK2. After 8-bit shift, S2 will have new content from SI2 pin.



3. 8-bit Serial-Input Mode

[Table: Control Bits of SIO2CR for 8-bit Serial-Input Mode]

Control Bit	SO2OE (bit-1)
Content	0

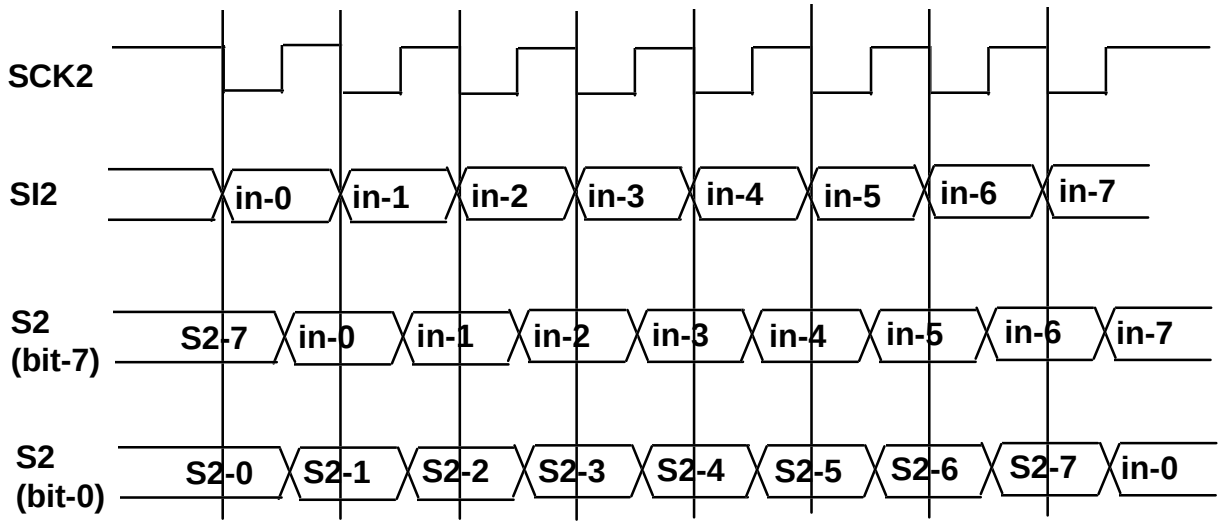
[Table: Pin Configuration of SIO-2 for 8-bit Serial-Input Mode]

Pin	In/Out Mode	Note
SI2	Input Mode	The pin SI2 must be assigned to input mode by a port control register.
SO2	Normal Port	SO2OE = 0. This pin can be used as a normal input or output port.
SCK2 (S2FS[2:0] = '000')	SCK2 input mode	The pin SCK2 should be assigned as input mode by the port control register.
SCK1 (S2FS[2:0] = '1 or 1 or 1')	SCK2 output mode	The pin SCK2 is assigned as the SCK2 output pin automatically by the S2FS[2:0].

[Table: Shift Registers of SIO-2 for 8-bit Serial-Input Mode]

Shift Register	S2 (SFR SIO2D Address F4)
Operation	The MSB (bit-7) is connected to SI2. The SI2 input signal should be synchronized to negative edge of the SCK2. The shift operation is performed on positive edge of the SCK2. After 8-bit shift, the S2 will have 8-bit serial input data.

[SI(Serial-Input) Mode: SIO-2]



4. 8-bit Serial-I/O Mode

[Table: Control Bits of SIO2CR for 8-bit Serial-I/O Mode]

Control Bit	SO2OE (bit-1)
Content	1

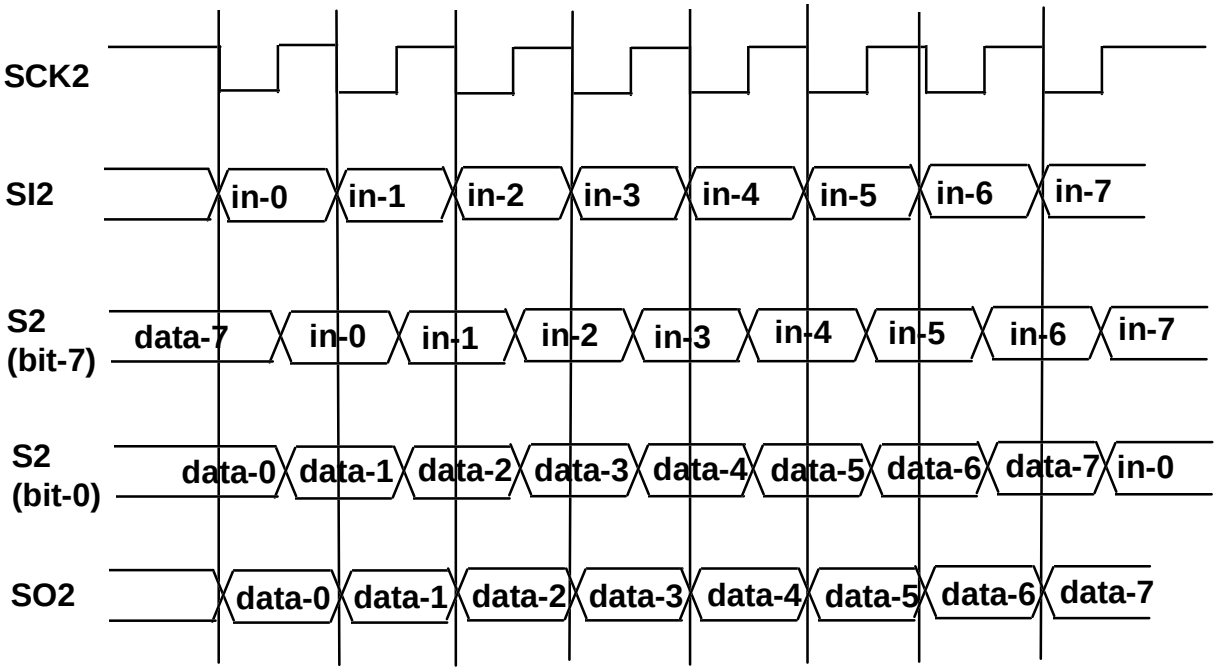
[Table: Pin Configuration of SIO-2 for 8-bit Serial-I/O Mode]

Pin	In/Out Mode	Note
SI2	Input Mode	The pin SI2 must be assigned to input mode by a port control register.
SO2	SO2 output	SO2OE = 1
SCK2 (S2FS[2:0] = ‘000’)	SCK2 input mode	The pin SCK2 should be assigned as input mode by the port control register.
SCK2 (S2FS[2:0] = ‘1 or 1 or 1’)	SCK2 output mode	The pin SCK2 is assigned as the SCK2 output pin automatically by the S2FS[2:0].

[Table: Shift Registers of SIO-2 for 8-bit Serial-I/O Mode]

Shift Register	S2 (SFR SIO2D Address F4)
Operation	The MSB (bit-7) is connected to SI2. The SI2 input signal should be synchronized to negative edge of the SCK2. The S2 should be loaded 8-bit data to be serial output before operation. The LSB(bit-0) is connected to the output flip-flop. The flip-flop is connected to the SO2 pin. The shift operation is performed on positive edge of the SCK2. The SO2 output synchronized to the just next negative edge of the SCK2. After 8-bit shift, the S2 will have 8-bit serial input data.

[SIO(Serial-In/Out) Mode: SIO-2]



5. SIO-2 Control Register (SIO2CR)

[Table: Definition of SIO2CR]

Address	F4H							
Bit Addr.								
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**S2EN**		**S2FS2**	**S2FS1**	**S2FS0**		**SO2OE**	
Definition	**SIO-2 ENable**	**Reserved bit**	**SIO-2 input Frequency Select bit-2**	**SIO-2 input Frequency Select bit-1**	**SIO-2 input Frequency Select bit-0**	**Reserved bit**	**SIO-2 SO2 Output En-able**	**Reserved bit**
Reset Value	**0**	**unknown**	**0**	**0**	**0**	**0**	**0**	**unknown**
Read/ Write by Software	**R/W**		**R/W**	**R/W**	**R/W**	**User MUST write a '0' to this bit. This bit is readable and writ-able.**	**R/W**	
Write by Hardware	**0 by SIO-2 over-flow or S/W**							

[Table: The Description of SIO2CR]

Name	Bit	Description
S2EN	7	**SIO-2 ENable bit** [Bit Status: 0 (Initial Value)] A selected input clock is halted to high. The SIO-2 counter is cleared to 0. [Bit Status: 1] A selected input clock is run. The SIO-2 counter counts up the negative edge of the select-ed clock.
Reserved	6	

S2FS[2:0]	5 to 3	**SIO-2 input clock Frequency Select bits** [Bit Status: 000 (Initial Value)] SCK2 (from external input) [Bit Status: 001] F_{sys}/24 [Bit Status: 010] F_{sys}/48 [Bit Status: 011] F_{sys}/96 [Bit Status: 100] F_{sys}/192 [Bit Status: 101] F_{sys}/384 [Bit Status: 110] F_{sys}/768 [Bit Status: 111] F_{sys}/1536 To use the SCK2 pin as an external clock input, the SCK2 pin should be assigned to input mode by a port control register.
Reserved	2	User **MUST** write a '0' to this bit. **NEVER** write a '1' to this bit.
SO2OE	1	**SO2 Output Enable** [Bit Status: 0 (Initial Value)] The pin SO2 can be used as a normal I/O port. [Bit Status: 1] The pin SO2 is used as the serial output pin.
Reserved	0	

6. SIO-2 Shift Register (SIO2D)

[Table: Definition of SIO2D]

Address	F5H							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**SIO2D[7:0]**							
Definition	**Shift register** **8-bit SO Mode: 8-bit output buffer** **8-bit SI Mode: 8-bit input buffer** **16-bit SIO Mode: 8-bit output buffer & 8-bit input buffer**							
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/ Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**	**Written with a new shift value 0 or 1.**

7. Serial In

STEP-1:
Before the SIO-2 clock signal get transmitted through SCK2 pin, SCK2 pin should set to high. This is necessary only when internal clock is used (SIO1CR[5:3] not equal to 000).

STEP-2:
Then, user should enable the SIO-2. This is done by writing the SIO2CR with proper value.

STEP-3:
If internal clock is used, SIO-2 will generate the appropriate clock signal for interfacing with the external chip.

If external clock is used, user will need to signal the external chip that SIO-2 is ready to take data and clock signal.

STEP-4:
After receiving the data, S2INT(interrupt signal) will set to high. At that time, SIO-2 waits for the CPU to read the received data.

8. Serial Out

STEP-1:
Before the SIO-2 clock signal get transmitted through SCK2 pin, SCK2 pin should set to high. This is necessary only when internal clock is used (SIO2CR[5:3] not equal to 000).

STEP-2:
Then, user should write the data to SIO2D..

STEP-3:
Next, user should enable the SIO-2. This is done by writing the SIO2CR with proper value.

STEP-4:
If internal clock is used, SIO-2 will generate the appropriate clock signal for interfacing with the external chip.

If external clock is used, user will need to signal the external chip that SIO-2 is ready to transmit the data and is waiting for their clock signal.

STEP-5:
After transmitting the data, S2INT will set to high.

9. Serial-I/O:

Before the SIO-2 clock signal get transmitted through SCK2 pin, SCK2 pin should set to high. This is necessary only when internal clock is used (SIO2CR[5:3] not equal to 000).

STEP-2:
Then, user should write the data to SIO2D.

STEP-3:
Next, user should enable the SIO-2. This is done by writing the SIO2CR with proper value.

STEP-4:
If internal clock is used, SIO-2 will generate the appropriate clock signal for interfacing with the external chip.

If external clock is used, user will need to signal the external chip that SIO-2 is ready to do transmission and reception, and is waiting for their clock signal.

STEP-5:
After the operation, S2INT will set to high. At this time, SIO2 waits for CPU to read the received data.

1. Overview:

The SS8203 includes an analog-to-digital converter module with 10 (ten) input channels. The A/D conversion is performed by the successive approximation method with 8-bit resolution.

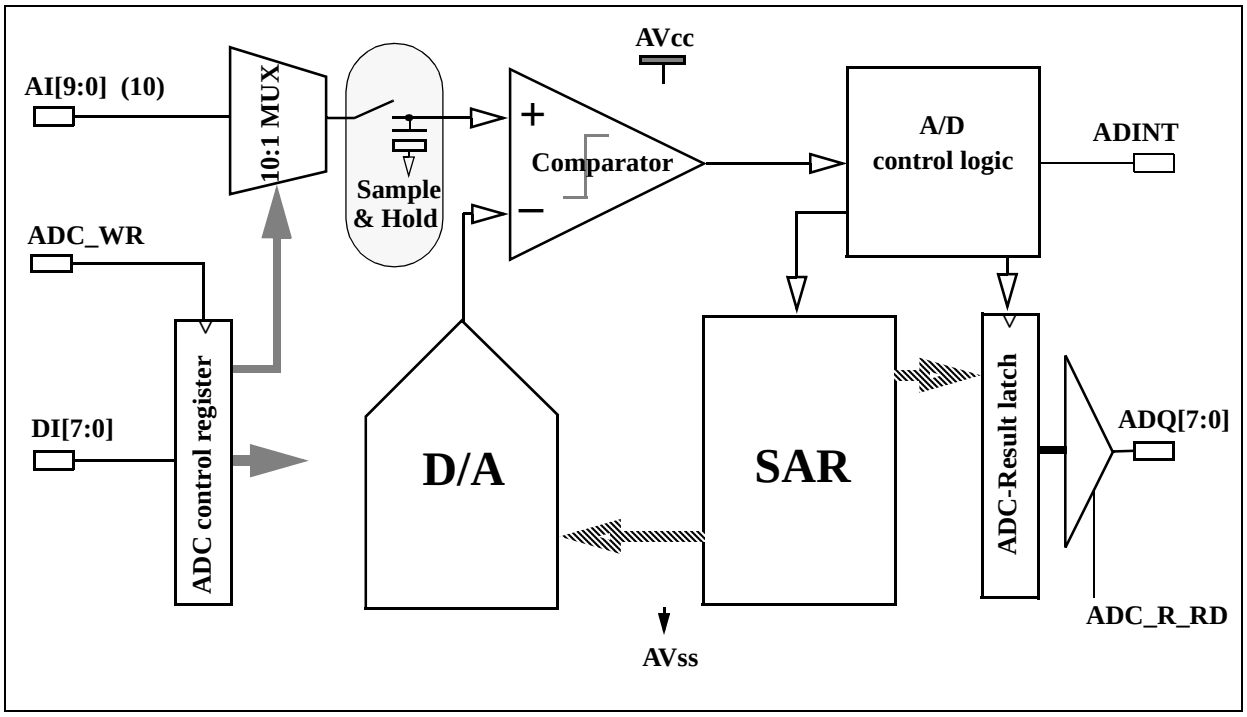
2. Features:

- 8-bit resolution.
- Ten analog input channels.
- Rapid conversion.
  Conversion time is 16 micro seconds with a 12MHz system clock.
- One 8-bit ADC Control Register.
  This register controls the ADC-module: Enable ADC, Start ADC and Input Channel Selection.
- One 8-bit ADC-Result Latch.
  This latch stores A/D conversion result.
- Sample and Hold function.
- A CPU interrupt (ADINT) can be requested at the completion of each A/D conversion.

3. Block diagram of A/D converter:

The A/D converter on SS8203 consists of:

- 10:1 analog input channel Mux.
- 8-bit digital-to-analog converter (DAC).
- CPU-to-ADC and ADC-to-CPU Interface Block.
- A comparator.
- Sample-and-Hold capacitor.
- Successive approximation registers.
- A/D result latch.
- A/D timing control block.



4. A/D converter characteristics:

Table 2: A/D-characteristics

	8 bits ADC
Resolution	8-bits
Power supply (AVcc/AVss)	5V +(-) 10%
Temperature	0 degree C to 85 degree C
Analog input Capacitance	6 pF (Max)
LSB	AVcc/2^8 (AVcc analog power supply for ADC)
Nonlinearity error	LSB (max)
Offset error	LSB (max)
Full-scale error (gain error)	LSB (max)
Quantization error	0.5 x LSB (max)
Absolute accuracy	1.5 x LSB (max)
Conversion time	16 micro second

5. A/D Input/Output Pins:

The Inputs and Outputs pins for ADC. Analog inputs are through port 4 and the 2 (two) least significant bits of port 5 and digital input buffers must be disabled when using the analog inputs.

Table 3: Inputs/Outputs

Name	***Abbreviation***	***I/O***	***Function***
Analog Input [9:0]	AI[9:0]	Inputs	Analog input pins.
ADC_Write	ADC_WR	Input	ADC control register write-signal.
ADC_Data bus[7:0]	DI[7:0]	Input/Output	Write-Data to ADC control register.
ADC_Result Read	ADC_R_RD	Input	ADC result read-signal.
ADC_Result data [7:0]	ADQ[7:0]	Input/Output	ADC result data-bus.
ADC_Reset (active low)	RES_N	Input	ADC reset signal (asynchronuos).
ADC_Interrupt request	ADINT	Output	ADC interrupt request to CPU, when the A/D conversion completed.

6. ADC-Control Register Description:

The ADC-Control Register enables the ADC-megacell, starts the analog-to-digital conversion, selects the analog input channel. The ADC-Control Register is reset asynchronuosly to “0X000”.

Table 4: ADC-Control Register contents

Address	***91H***							
Bit	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***
Name	ADC_EN	ADC_STR	“reserved”	“reserved”	SELECT3	SELECT2	SELECT1	SELECT0
Description	ADC enable (active “H”)	ADC-conversion start. (active “H”) *(This bit is automatically cleared to “0” after the conversion is started).* a)	“Unused”	“Unused”	Analog input channel select (active “H”)	Analog input channel select (active “H”)	Analog input channel select (active “H”)	Analog input channel select (active “H”)
Initial value	X	X	X	X	X	X	X	X
Reset	0	0	0	0	0	0	0	0
Read/ Write	Write	Write	Write	Write	Write	Write	Write	Write

a) *ADC-STR is only active when ADC-EN is “H”.*

Assignment of ADC-Control Register data to Analog Input Channels:

Table 5: Analog Input Channel Select

Select3	***Select2***	***Select1***	***Select0***	***Analog Input Channel***
0	**0**	**0**	**0**	Analog Input Channel 0 [AI0]
0	**0**	**0**	**1**	Analog Input Channel 1 [AI1]
0	**0**	**1**	**0**	Analog Input Channel 2 [AI2]
0	**0**	**1**	**1**	Analog Input Channel 3 [AI3]
0	**1**	**0**	**0**	Analog Input Channel 4 [AI4]

Table 5: Analog Input Channel Select

Select3	***Select2***	***Select1***	***Select0***	***Analog Input Channel***
0	**1**	**0**	**1**	Analog Input Channel 5 [AI5]
0	**1**	**1**	**0**	Analog Input Channel 6 [AI6]
0	**1**	**1**	**1**	Analog Input Channel 7 [AI7]
1	**0**	**0**	**0**	Analog Input Channel 8 [AI8]
1	**0**	**0**	**1**	Analog Input Channel 9 [AI9]
1	**0**	**1**	**0**	***Analog Input Channel 0 [AI0]***
1	**0**	**1**	**1**	***Analog Input Channel 0 [AI0]***
1	**1**	**X**	**X**	***Analog Input Channel 0 [AI0]***

7. ADC-Result Latch:

After the analog-to-digital conversion is completed the result data are latched into the ADC result data latch. During the conversion the previous conversion result data are held in those latches and can be read in anytime.

Table 6: ADC Result Data Latch

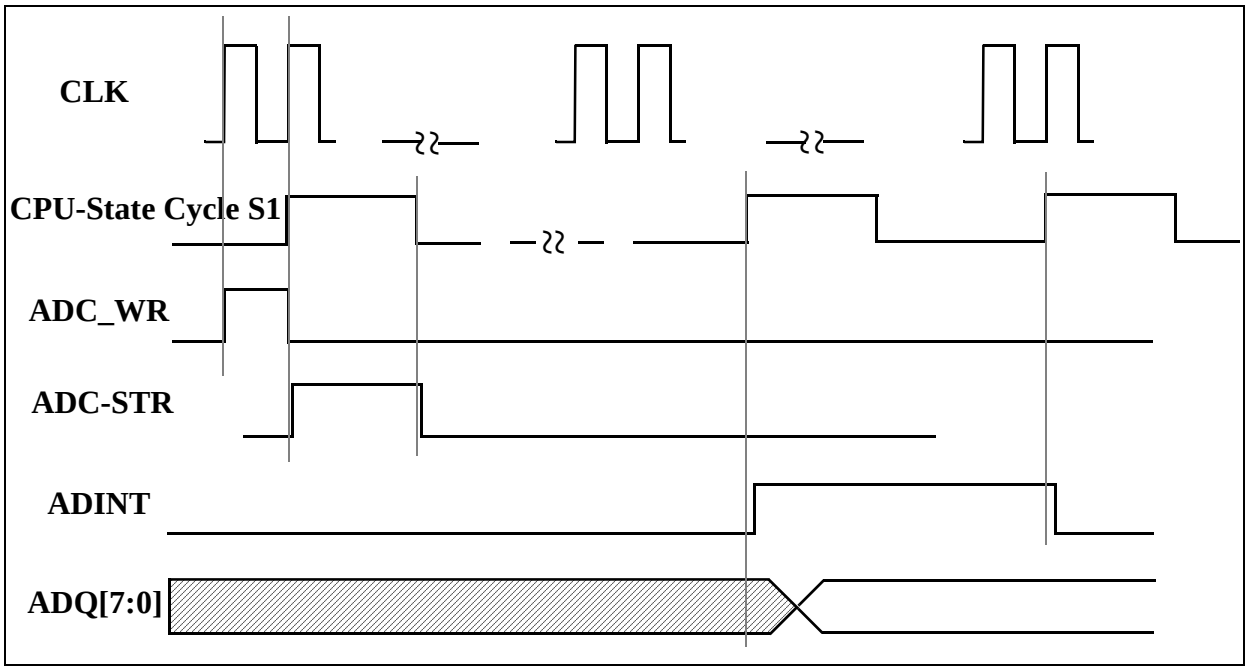
Address	***92H***							
Bit	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***
A-to-D a)								
Initial value	X	X	X	X	X	X	X	X
Reset (RES_N) b)	X	X	X	X	X	X	X	X
Read/ Write c)	Read	Read	Read	Read	Read	Read	Read	Read

a) A-to-D : Analog-to-digital conversion result data.
b) Reset-signal doesn't affect the latch-data.
c) ADC-result latch data only can be read.

8. A/D Conversion Timing Diagram

Analog-to-digital conversion is started from the signal ADC-STR of ADC Control Register. When the conversion has been started, it cleares ADC-STR to "L" after S1. And when the conversion is completed it signals the interrupt

request ADINT to CPU by the rising edge of S1, writes the conversion result data to ADC-Result Latch and resets the interrupt request to “L” by the next S1.



[External Interrupts]

1. Overview

There are 6 external interrupts, IRQ0 to IRQ5. The external interrupts share pins with the Port-0.0 to Port-0.5. To use an IRQi (i = 0 to 5) pin as an external interrupt pin, the pin must be assigned to input mode by the Port-0 Control Register. The external interrupt sources can be programmed to be negative edge activated, low level activated, positive edge activated, or both edge activated by setting or clearing bit IRQi1 and IRQi0 in Register XICRn (External Interrupt Control Register). If IRQiA = 0 and IRQiB = 0, IRQi is negative edge triggered. In this mode if successive samples of the IRQi pin show a high in one sample and a low in the next cycle, interrupt request flag, IRQiF, will be set. Flag bit IRQiF then requests the interrupt. This bit must be cleared by software in the interrupt service routine. The IRQiF bit can be also set or cleared by software. If IRQiA = 1 and IRQiB = 0, IRQi is positive edge triggered. In this mode if successive samples of the IRQi pin show a low in one sample and a high in the next cycle, interrupt request flag IRQiF will be set. Flag bit IRQiF then requests the interrupt. If IRQiA = 1 and IRQiB = 1, IRQi is both (positive or negative) edge triggered. In this mode if successive samples of the IRQi pin show difference between one sample and the next sample, interrupt request flag IRQiF will be set. Flag bit IRQiF then requests the interrupt. If IRQiA = 0 and IRQiB = 1, IRQi is low level activated. If IRQi is low, interrupt request flag IRQiF will be set. In this case, software can not clear IRQiF if the pin IRQi is still low. Thus, make sure the pin IRQi becoming high level (inactivate state) in the interrupt service routine.

[Table: IRQi (i = 0 to 5) Mode Selection]

IRQiA:IRQiB	Active Edge or Level
[IRQiA:IRQiB] = 00	Negative Edge
[IRQiA:IRQiB] = 01	Low Level
[IRQiA:IRQiB] = 10	Positive Edge
[IRQiA:IRQiB] = 11	Both (Positive or Negative) Edge

2. External Interrupt Control Register (XICR0, XICR1)

[Table: Definition of XICR0]

Address	A6H							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME			**IRQ2A**	**IRQ2B**	**IRQ1A**	**IRQ1B**	**IRQ0A**	**IRQ0B**
Definition	**Reserved bit**	**Reserved bit**	**IRQ2 Mode Select Bit-A**	**IRQ2 Mode Select Bit-B**	**IRQ1 Mode Select Bit-A**	**IRQ1 Mode Select Bit-B**	**IRQ0 Mode Select Bit-A**	**IRQ0 Mode Select Bit-B**
Reset Value	**unknown**	**unknown**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software			**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

[Table: Definition of XICR1]

Address	A7H							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME			**IRQ5A**	**IRQ5B**	**IRQ4A**	**IRQ4B**	**IRQ3A**	**IRQ3B**
Definition	**Reserved bit**	**Reserved bit**	**IRQ5 Mode Select Bit-A**	**IRQ5 Mode Select Bit-B**	**IRQ4 Mode Select Bit-A**	**IRQ4 Mode Select Bit-B**	**IRQ3 Mode Select Bit-A**	**IRQ3 Mode Select Bit-B**
Reset Value	**unknown**	**unknown**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software			**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

[Interrupt Control Block]

1. Overview

The SS8203 provides 17 interrupt sources (6 external interrupt and 11 internal interrupt). There are six external interrupt pins, IRQ0 to IRQ5. Following peripheral blocks may generate interrupt request, Watch-Dog Timer, Watch Timer, Time Base Timer, PWM Timer-1 to 3, Capture Timer-1 to 2, SIO-1 to 2, and A/D converter. These interrupt sources are divided into 5 group.

When an interrupt is generated, the interrupt request flag that generated it should be cleared by the software when the service routine is vectored. All of the interrupt request flag can be set or cleared by software, with the same result as though it had been set or cleared by hardware. That is, interrupt can be generated or pending interrupts can be canceled in software. Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Registers ISE0 to ISE2. And, each of interrupt group can be enabled or disabled by setting or clearing a bit in Special Function Register IE. The bit EA in IE contains also a global disable bit (0: disable, 1: Enable), which disables all interrupts at once.

3. Interrupt Source Enable Registers (ISE0, ISE1, ISE2)

[Table: Definition of ISE0]

Address	D7H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME			EIRQ5F	EIRQ4F	EIRQ3F	EIRQ2F	EIRQ1F	EIRQ0F
Definition	Reserved bit	Reserved bit	Enable IRQ5F 1: Enable 0: Disable	Enable IRQ4F 1: Enable 0: Disable	Enable IRQ3F 1: Enable 0: Disable	Enable IRQ2F 1: Enable 0: Disable	Enable IRQ1F 1: Enable 0: Disable	Enable IRQ0F 1: Enable 0: Disable
Reset Value	unknown	unknown	0	0	0	0	0	0
Read/Write by Software			R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of ISE1]

Address	E7H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	ECT2INT	ECT1INT	EPT3INT	EPT2INT	EPT1INT	ETBINT	EWINT	EWDINT
Definition	Enable Capture Timer-2 Interrupt 1: Enable 0: Disable	Enable Capture Timer-1 Interrupt 1: Enable 0: Disable	Enable PWM Timer-3 Interrupt 1: Enable 0: Disable	Enable PWM Timer-2 Interrupt 1: Enable 0: Disable	Enable PWM Timer-1 Interrupt 1: Enable 0: Disable	Enable Time-Base Timer Interrupt 1: Enable 0: Disable	Enable Watch Timer In-terrupt 1: Enable 0: Disable	Enable Watch-Dog Timer Interrupt 1: Enable 0: Disable
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of ISE2]

Address	F7H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME						ES2INT	ES1INT	EADINT
Definition	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Reserved bit	Enable SIO-2 Interrupt 1: Enable 0: Disable	Enable SIO-1 Interrupt 1: Enable 0: Disable	Enable ADC Interrupt 1: Enable 0: Disable
Reset Value	unknown	unknown	unknown	unknown	unknown	0	0	0
Read/Write by Software						R/W	R/W	R/W
Write by Hardware								

4. Interrupt Group Enable Register (IE)

[Table: Definition of IE]

Address	A8H							
Bit Addr.	AFH	AEH	ADH	ACH	ABH	AAH	A9H	A8H
BIT	7	6	5	4	3	2	1	0
NAME	EA			EGE	EGD	EGC	EGB	EGA
Definition	Enable All Interrupt 1: Enable 0: Disable	Reserved bit	Reserved bit	Enable Group-E 1: Enable 0: Disable	Enable Group-D 1: Enable 0: Disable	Enable Group-C 1: Enable 0: Disable	Enable Group-B 1: Enable 0: Disable	Enable Group-A 1: Enable 0: Disable
Reset Value	0	unknown	unknown	0	0	0	0	0
Read/Write by Software	R/W			R/W	R/W	R/W	R/W	R/W
Write by Hardware								

5. Interrupt Priority Register (IP)

Each interrupt group (Group-A, B, C, D, and E) can also be individually programmed to one of two priority levels by setting or clearing a bit in Special Function Register IP. A low priority interrupt can be interrupted by a high priority interrupt, but not by another low priority interrupt. A high priority interrupt can not be interrupted by another interrupt group. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If request of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence, as follows.

[Table: Internal Priority and Vector Address]

Number	Group	Request Flags	Vector Addr.	Priority Within Level
1	Group-A	IRQ0/1/2F	0003H	Highest
2	Group-B	IRQ3/4/5F	000BH	
3	Group-C	WDINT,WINT,TBINT	0013H	
4	Group-D	S1/2INT,ADINT	001BH	
5	Group-E	PT1/2/3INT,CT1/2INT	0023H	Lowest

[Table: Definition of IP]

Address	**B8H**							
Bit Addr.	**BFH**	**BEH**	**BDH**	**BCH**	**BBH**	**BAH**	**B9H**	**B8H**
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME				**PGE**	**PGD**	**PGC**	**PGB**	**PGA**
Definition	**Reserved bit**	**Reserved bit**	**Reserved bit**	**Priority of Group-E 1: High Priority 0: Low Priority**	**Priority of Group-D 1: High Priority 0: Low Priority**	**Priority of Group-C 1: High Priority 0: Low Priority**	**Priority of Group-B 1: High Priority 0: Low Priority**	**Priority of Group-A 1: High Priority 0: Low Priority**
Reset Value	**unknown**	**unknown**	**unknown**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software				**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

6. Interrupt Processing

The interrupt request flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware generated LCALL is blocked by any of the following conditions:

1. An interrupt of equal or higher priority level is already in progress
2. The current polling cycle is not the final cycle in the execution of the instruction in progress
3. The instruction in progress is RETI.
4. The instruction in progress is any access to the IE or IP registers.

Any of these four conditions will block the generation of the LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring to any service routine. Condition 3 & 4 ensures that if the instruction in progress is RETI or any access to IE or IP, then at least one more instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note then that if an interrupt flag is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag once active but not serviced is not remembered. Every polling cycle is new.

The processor acknowledges an interrupt request by executing a hardware generated LCALL to the appropriate service routine. It also clears the flag that generated the interrupt. The hardware generated LCALL pushes the contents of the Program Counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to.

Executing proceeds from that location until the RETI instructions is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off. Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress.

[Port-0 to 3]

1. Overview

In the SS8203, there are three groups of ports, Port-0 to 3, Port-4 to 5, and Port-6 to 7. Each port group has diferent configuration. Thus, user should carefully read port specification.

The output drivers of Port-0 and 2, and the input buffer of Port-0 are used in accesses to external memory. In this application, Port-0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port-2 outputs the high byte of the external memory address when the address is 16-bits wide. Otherwise the Port-2 pins continue to emit the P2 SFR content.

The Port-1 pins and Port-3 pins are multifunctional. They are not only port pins, but also serve the functions of various special features as listed below:

PORT BIT	ALTERNATE FUNCTION
P1.0	SCK1 (SIO-1 Clock Input/Output)
P1.1	SI1 (SIO-1 Serial Data Input)
P1.2	SO1 (SIO-1 Serial Data Output)
P1.3	SCK2 (SIO-2 Clock Input/Output)
P1.4	SI2 (SIO-2 Serial Data Input)
P1.5	SO2 (SIO-2 Serial Data Output)
P3.0	PWM1 (P-Timer 1 Output)
P3.1	PWM2 (P-Timer 2 Output)
P3.2	PWM3 (P-Timer 3 Output)
P3.3	BUZ (Buzzer Output)
P3.6	NWR (External Data Memory Write Strobe)
P3.7	NRD (External Data Memory Read Strobe)

The alternate functions for NWR, NRD can only be activated if the corresponding port bit latch (P3.6, P3.7) in the port SFR contains a 1 (high, initial value). Otherwise the port pin is stuck at 0 (low).

2. Read-Modify-Write Feature

Some instructions, that read a port (Port-0 to 3 only), read the latch and others read pin. The instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called “read-modify-write” instructions. The instructions listed below are read-modify-write instructions. When the destination operand is a port, or a port bit, these instructions read the latch than the pin:

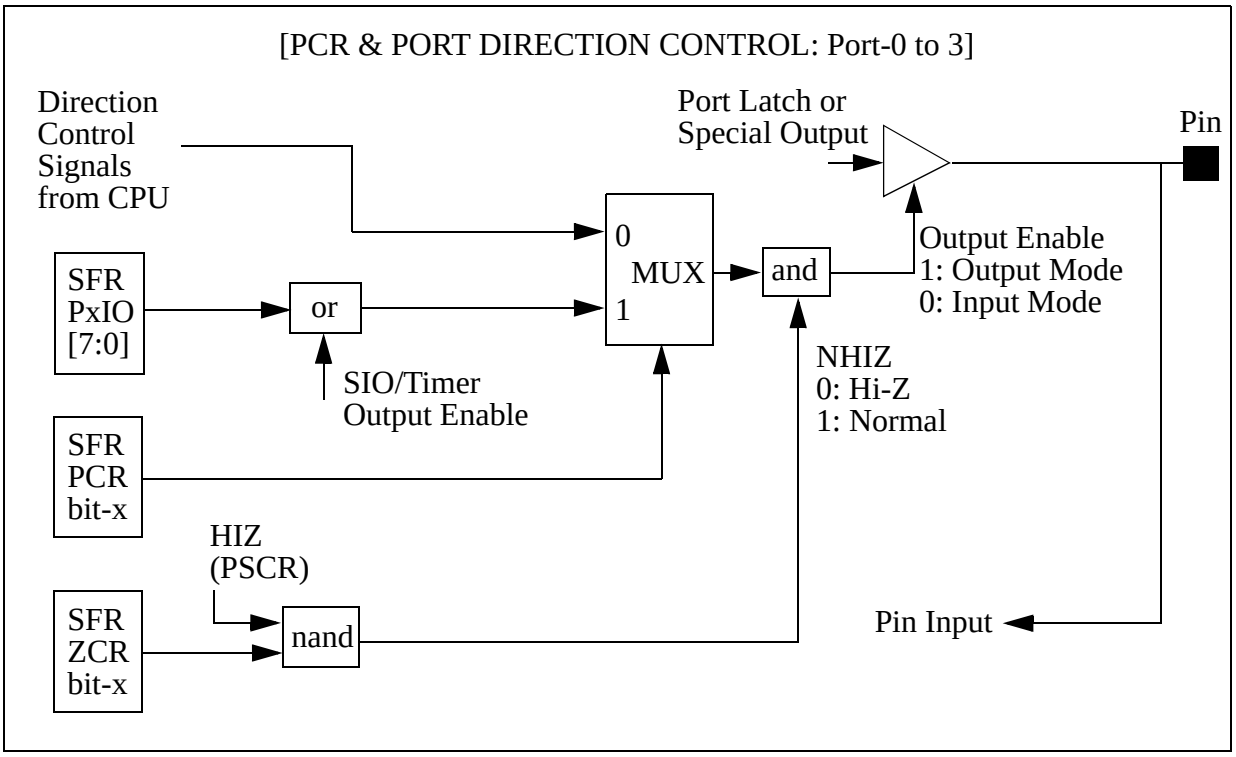
INSTRUCTIONS	DESCRIPTION
ANL	logical AND, e.g. ANL P0, A
ORL	logical OR, e.g. ORL P1, A
XRL	logical EX-OR, e.g. XRL P2, A
JBC	jump if bit = 1 and clear bit, e.g. JBC P3.0, LABEL
CPL	complement bit, e.g. CPL P3.1
INC	increment, e.g. INC P0
DEC	decrement, e.g. DEC P1
DJNZ	decrment and jump if not zero, e.g. DJNZ P0, LABEL
MOV PX.Y, C	move carry bit to bit Y of Port-X
CLR PX.Y	clear bit Y of Port-X
SET PX.Y	set bit Y of Port-X

It is not obvious that the last three instructions in this list are read-modify-instructions, but they are. They read the port byte, all 8 bits, modify the addressed bit, then write the new byte back to the latch. The reason that read-modify-write instructions are directed to the latch than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of the transistor. When a 1 is written to the bit, the transistor is turn on. If the CPU then reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of 1.

3. PCR (Port Control Register)

[Table: Definition of PCR]

Address	9AH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME				PCR4	PCR3	PCR2	PCR1	PCR0
Definition	Reserved bit	Reserved bit	Reserved bit	Port-3.6 to 3.7 I/O Control bit 0: CPU Control 1: P3IO Control	Port-3.0 to 3.5 I/O Control bit 0: CPU Control 1: P3IO Control	Port-2 I/O Control bit 0: CPU Control 1: P2IO Control	Port-1 I/O Control bit 0: CPU Control 1: P1IO Control	Port-0 I/O Control bit 0: CPU Control 1: P0IO Control
Reset Value	unknown	unknown	unknown	0	0	0	0	0
Read/Write by Software				R/W	R/W	R/W	R/W	R/W
Write by Hardware								



4. ZCR (Hi-Z Control Register)

[Table: Definition of ZCR]

Address	**9BH**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME				**ZCR4**	**ZCR3**	**ZCR2**	**ZCR1**	**ZCR0**
Definition	**Reserved bit**	**Reserved bit**	**Reserved bit**	**Port-3.6 to 3.7 Hi-Z Control bit 0: Disable 1: Hi-Z Enable**	**Port-3.0 to 3.5 Hi-Z Control bit 0: Disable 1: Hi-Z Enable**	**Port-2 Hi-Z Control bit 0: Disable 1: Hi-Z Enable**	**Port-1 Hi-Z Control bit 0: Disable 1: Hi-Z Enable**	**Port-0 Hi-Z Control bit 0: Disable 1: Hi-Z Enable**
Reset Value	**unknown**	**unknown**	**unknown**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software				**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

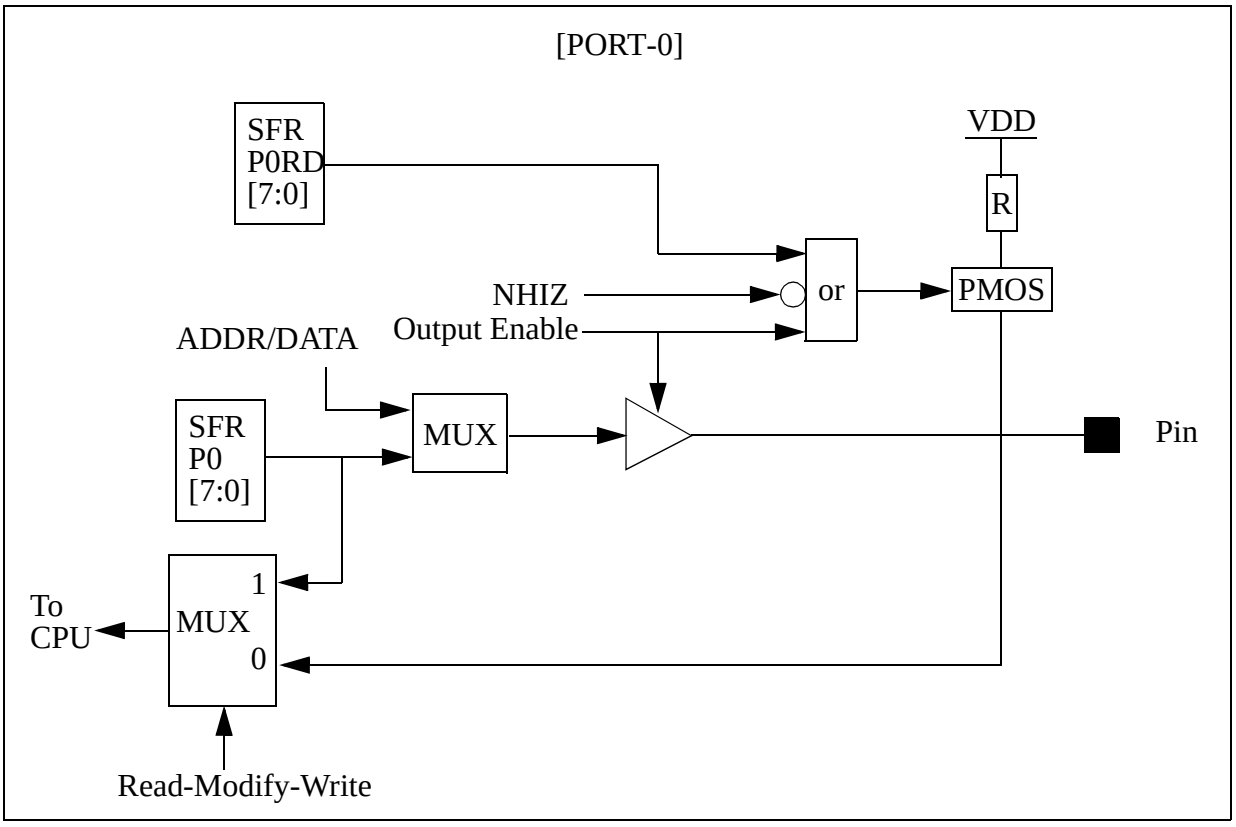
5. P0 (Port-0)

The Pin-0.0 to 0.7 have two functional modes, A/D Mode (Low Address/Data Mode) and Port Mode (High Current Sink Bi-directional Port Mode). Initial Staus is A/D Mode because PCR0 (Port Control Register Bit-0) is 0 (low). In Port Mode, the direction of Port-0 can be decided bit-by-bit. In A/D Mode, writing to Port-0 is prohibited. The read policy in Port Mode follows that described before. Read-Modify-Write instructions read the port latch than the pin.

To use Pin-0.0 to 0.7 as a normal input port, PCR0 should be high. If PCR0 is high, the direction of each Port-0 pin is decided by each P0IO bit. If the P0IO bit-x is high, Port-0.x is output mode. If low, Port-0.x is input mode. Initial status is input mode because P0IO (Port-0 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P0RD (Port-0 Resistor Disable Register). If the P0RD bit-x is high, Port-0.x pull-up resistor is disconnected. If low, Port-0.x pull-up resistor is connected. Initial status of P0RD is 11111111B, thus pull-up resistor is disconnected. If ZCR0 (High-Z Control Register Bit-0) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence.

To use Pin-0.0 to 0.7 as a normal output port, PCR0 should be high. If the P0IO bit-x is high, Port-0.x is output mode. In output mode, pull-up resistor is automatically disconnected regardless P0RD bit-x. If ZCR0 (High-Z Control Register Bit-0) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence. Port-0 can be used as an LED current sink port.

To use Pin-0.0 to 0.7 as an A/D input/output port, PCR0 should be low (reset value). If PCR0 is low, the direction of each Port-0 pin is controlled by CPU. In input mode, pull-up resistor can be connected by P0RD (Port-0 Resistor Disable Register). In output mode, pull-up resistor is automatically disconnected regardless P0RD bit-x. For the A/D Mode, the ZCR0 must be low (reset value) not to support Hi-Z state.



[Table: Definition of P0]

Address	80H							
Bit Addr.	87H	86H	85H	84H	83H	82H	81H	80H
BIT	7	6	5	4	3	2	1	0
NAME	P07	P06	P05	P04	P03	P02	P01	P00
Definition	Port-0 Pin or Latch bit-7	Port-0 Pin or Latch bit-6	Port-0 Pin or Latch bit-5	Port-0 Pin or Latch bit-4	Port-0 Pin or Latch bit-3	Port-0 Pin or Latch bit-2	Port-0 Pin or Latch bit-1	Port-0 Pin or Latch bit-0
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W RMW Ins: P07 Latch Read Other Ins: P0.7 Pin Read	R/W RMW Ins: P06 Latch Read Other Ins: P0.6 Pin Read	R/W RMW Ins: P05 Latch Read Other Ins: P0.5 Pin Read	R/W RMW Ins: P04 Latch Read Other Ins: P0.4 Pin Read	R/W RMW Ins: P03 Latch Read Other Ins: P0.3 Pin Read	R/W RMW Ins: P02 Latch Read Other Ins: P0.2 Pin Read	R/W RMW Ins: P01 Latch Read Other Ins: P0.1 Pin Read	R/W RMW Ins: P00 Latch Read Other Ins: P0.0 Pin Read
Write by Hardware								

[Table: Definition of P0IO]

Address	AAH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P0IO7	P0IO6	P0IO5	P0IO4	P0IO3	P0IO2	P0IO1	P0IO0
Definition	Port-0 I/O Control Register bit-7 0: Input Mode 1: Output Mode	Port-0 I/O Control Register bit-6 0: Input Mode 1: Output Mode	Port-0 I/O Control Register bit-5 0: Input Mode 1: Output Mode	Port-0 I/O Control Register bit-4 0: Input Mode 1: Output Mode	Port-0 I/O Control Register bit-3 0: Input Mode 1: Output Mode	Port-0 I/O Control Register bit-2 0: Input Mode 1: Output Mode	Port-0 I/O Control Register bit-1 0: Input Mode 1: Output Mode	Port-0 I/O Control Register bit-0 0: Input Mode 1: Output Mode
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P0RD]

Address	ABH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P0RD7	P0RD6	P0RD5	P0RD4	P0RD3	P0RD2	P0RD1	P0RD0
Definition	Port-0 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-0 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

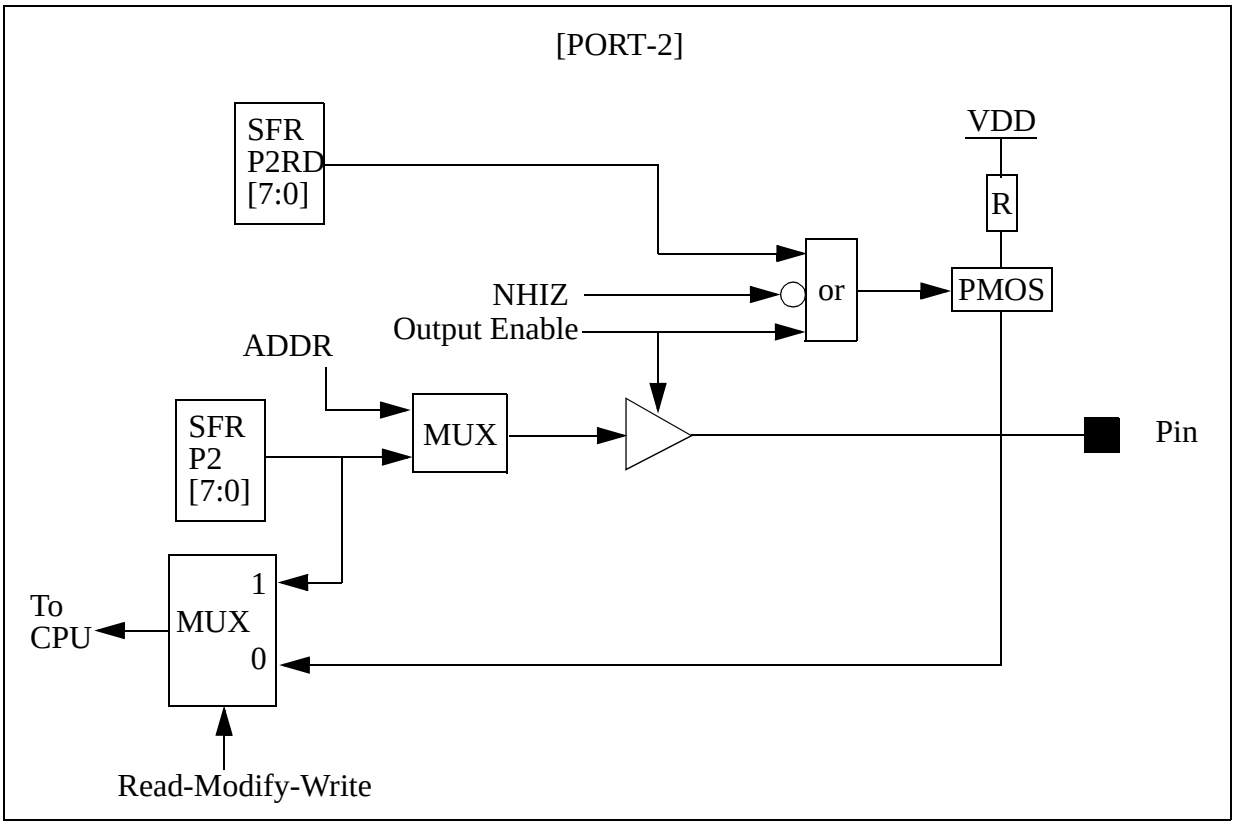
6. P2 (Port-2)

The Pin-2.0 to 2.7 have two functional modes, ADDR Mode (High Address Mode) and Port Mode (Bi-directional Port Mode). Initial Staus is ADDR Mode because PCR2 (Port Control Register Bit-2) is 0 (low). In Port Mode, the direction of Port-2 can be decided bit-by-bit. The read policy in Port Mode follows that described before. Read-Modify-Write instructions read the port latch than the pin.

To use Pin-2.0 to 2.7 as a normal input port, PCR2 should be high. If PCR2 is high, the direction of each Port-2 pin is decided by each P2IO bit. If the P2IO bit-x is high, Port-2.x is output mode. If low, Port-2.x is input mode. Initial status is input mode because P2IO (Port-2 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P2RD (Port-2 Resistor Disable Register). If the P2RD bit-x is high, Port-2.x pull-up resistor is disconnected. If low, Port-2.x pull-up resistor is connected. Initial status of P2RD is 11111111B, thus pull-up resistor is disconnected. If ZCR2 (High-Z Control Register Bit-2) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence.

To use Pin-2.0 to 2.7 as a normal output port, PCR2 should be high. If the P2IO bit-x is high, Port-2.x is output mode. In output mode, pull-up resistor is automatically disconnected regardless P2RD bit-x. If ZCR2 (High-Z Control Register Bit-2) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use Pin-2.0 to 2.7 as an ADDR output port, PCR2 should be low (reset value). If PCR2 is low, the direction of each Port-2 pin is controlled by CPU. In output mode, pull-up resistor is automatically disconnected regardless P2RD bit-x. For the ADDR Mode, the ZCR2 must be low (reset value) not to support Hi-Z state.



[Table: Definition of P2]

Address	A0H							
Bit Addr.	A7H	A6H	A5H	A4H	A3H	A2H	A1H	A0H
BIT	7	6	5	4	3	2	1	0
NAME	P27	P26	P25	P24	P23	P22	P21	P20
Definition	Port-2 Pin or Latch bit-7	Port-2 Pin or Latch bit-6	Port-2 Pin or Latch bit-5	Port-2 Pin or Latch bit-4	Port-2 Pin or Latch bit-3	Port-2 Pin or Latch bit-2	Port-2 Pin or Latch bit-1	Port-2 Pin or Latch bit-0
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W RMW Ins: P27 Latch Read Other Ins: P2.7 Pin Read	R/W RMW Ins: P26 Latch Read Other Ins: P2.6 Pin Read	R/W RMW Ins: P25 Latch Read Other Ins: P2.5 Pin Read	R/W RMW Ins: P24 Latch Read Other Ins: P2.4 Pin Read	R/W RMW Ins: P23 Latch Read Other Ins: P2.3 Pin Read	R/W RMW Ins: P22 Latch Read Other Ins: P2.2 Pin Read	R/W RMW Ins: P21 Latch Read Other Ins: P2.1 Pin Read	R/W RMW Ins: P20 Latch Read Other Ins: P2.0 Pin Read
Write by Hardware								

[Table: Definition of P2IO]

Address	CAH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P2IO7	P2IO6	P2IO5	P2IO4	P2IO3	P2IO2	P2IO1	P2IO0
Definition	Port-2 I/O Control Register bit-7 0: Input Mode 1: Output Mode	Port-2 I/O Control Register bit-6 0: Input Mode 1: Output Mode	Port-2 I/O Control Register bit-5 0: Input Mode 1: Output Mode	Port-2 I/O Control Register bit-4 0: Input Mode 1: Output Mode	Port-2 I/O Control Register bit-3 0: Input Mode 1: Output Mode	Port-2 I/O Control Register bit-2 0: Input Mode 1: Output Mode	Port-2 I/O Control Register bit-1 0: Input Mode 1: Output Mode	Port-2 I/O Control Register bit-0 0: Input Mode 1: Output Mode
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P2RD]

Address	CBH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P2RD7	P2RD6	P2RD5	P2RD4	P2RD3	P2RD2	P2RD1	P2RD0
Definition	Port-2 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-2 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

7. P1 (Port-1)

The Pin-1.0 to 1.7 have two functional modes, SIO output Mode (SCK1/2, SO1/2) and Port Mode (Bi-directional Port Mode). Initial Staus of PCR1 (Port Control Register Bit-1) is 0 (low). The PCR1 must be set to high for any case. In Port Mode, the direction of Port-1 can be decided bit-by-bit. The read policy in Port Mode follows that described before. Read-Modify-Write instructions read the port latch than the pin.

To use Pin-1.0 to 1.7 as a normal input port, PCR1 should be high. If PCR1 is high, the direction of each Port-1 pin is decided by each P1IO bit. If the P1IO bit-x is high, Port-1.x is output mode. If low, Port-1.x is input mode. Initial status is input mode because P1IO (Port-1 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P1RD (Port-1 Resistor Disable Register). If the P1RD bit-x is high, Port-1.x pull-up resistor is disconnected. If low, Port-1.x pull-up resistor is connected. Initial status of P1RD is 11111111B, thus pull-up resistor is disconnected. If ZCR1 (High-Z Control Register Bit-1) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence. In input mode, P1.0/SCK1, P1.1/SI1, P1.3/SCK2, and P1.4/SI2 can be used SIO input pins.

To use Pin-1.0 to 1.7 as a normal output port, PCR1 should be high. If the P1IO bit-x is high, Port-1.x is output mode. In output mode, pull-up resistor is automatically disconnected regardless P1RD bit-x. If ZCR1 (High-Z Control Register Bit-1) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use P1.0/SCK1, P1.2/SO1, P1.3/SCK2, and P1.5/SO2 as an SIO output port, PCR1 should be high. And, an SIO output should be enabled in the SIO block.

[Table: P1.0/SCK1 & P1.3/SCK2 Pin Configuration]

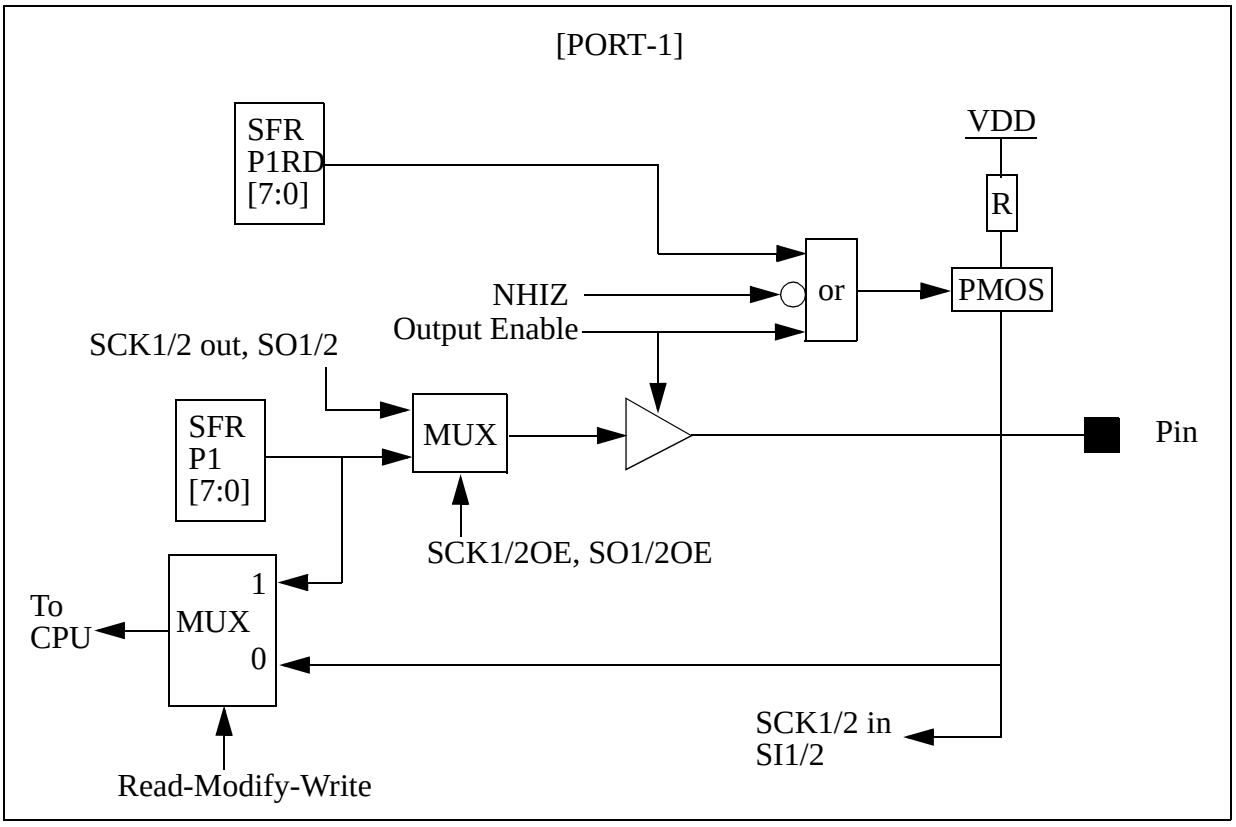
Pin	SxFS[2:0] = not(000) (x = 1 or 2)	SxFS=000 & P1IOi=0 (i = 0 or 3)	SxFS=000 & P1IOi=1 (i = 0 or 3)
P1.0/SCK1	SCK1 Output Mode	P1.0 Input Mode & SCK1 Input Mode	P1.0 Output Mode
P1.3/SCK2	SCK2 Output Mode	P1.3 Input Mode & SCK2 Input Mode	P1.3 Output Mode

[Table: P1.1/SI1 & P1.4/SI2 Pin Configuration]

Pin	P1IOi=0 (i = 1 or 4)	P1IOi=1 (i = 1 or 4)
P1.1/SI1	P1.1 Input Mode & SI1 Input Mode	P1.1 Output Mode
P1.4/SI2	P1.4 Input Mode & SI2 Input Mode	P1.4 Output Mode

[Table: P1.2/SO1 & P1.5/SO2 Pin Configuration]

Pin	SOxOE = 1 (x = 1 or 2)	SOxOE=0 & P1IOi=0 (i = 2 or 5)	SOxOE=0 & P1IOi=1 (i = 2 or 5)
P1.2/SO1	SO1 Output Mode	P1.2 Input Mode	P1.2 Output Mode
P1.5/SO2	SO2 Output Mode	P1.5 Input Mode	P1.5 Output Mode



[Table: Definition of P1]

Address	90H							
Bit Addr.	97H	96H	95H	94H	93H	92H	91H	90H
BIT	7	6	5	4	3	2	1	0
NAME	P17	P16	P15	P14	P13	P12	P11	P10
Definition	Port-1 Pin or Latch bit-7	Port-1 Pin or Latch bit-6	Port-1 Pin or Latch bit-5	Port-1 Pin or Latch bit-4	Port-1 Pin or Latch bit-3	Port-1 Pin or Latch bit-2	Port-1 Pin or Latch bit-1	Port-1 Pin or Latch bit-0
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W RMW Ins: P17 Latch Read Other Ins: P1.7 Pin Read	R/W RMW Ins: P16 Latch Read Other Ins: P1.6 Pin Read	R/W RMW Ins: P15 Latch Read Other Ins: P1.5 Pin Read	R/W RMW Ins: P14 Latch Read Other Ins: P1.4 Pin Read	R/W RMW Ins: P13 Latch Read Other Ins: P1.3 Pin Read	R/W RMW Ins: P12 Latch Read Other Ins: P1.2 Pin Read	R/W RMW Ins: P11 Latch Read Other Ins: P1.1 Pin Read	R/W RMW Ins: P10 Latch Read Other Ins: P1.0 Pin Read
Write by Hardware								

[Table: Definition of P1IO]

Address	BAH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P1IO7	P1IO6	P1IO5	P1IO4	P1IO3	P1IO2	P1IO1	P1IO0
Definition	Port-1 I/O Control Register bit-7 0: Input Mode 1: Output Mode	Port-1 I/O Control Register bit-6 0: Input Mode 1: Output Mode	Port-1 I/O Control Register bit-5 0: Input Mode 1: Output Mode	Port-1 I/O Control Register bit-4 0: Input Mode 1: Output Mode	Port-1 I/O Control Register bit-3 0: Input Mode 1: Output Mode	Port-1 I/O Control Register bit-2 0: Input Mode 1: Output Mode	Port-1 I/O Control Register bit-1 0: Input Mode 1: Output Mode	Port-1 I/O Control Register bit-0 0: Input Mode 1: Output Mode
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P1RD]

Address	BBH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P1RD7	P1RD6	P1RD5	P1RD4	P1RD3	P1RD2	P1RD1	P1RD0
Definition	Port-1 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-1 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

8. P3 (Port-3)

The Pin-3.0 to 3.7 have two functional modes, Timer output Mode (BUZ, PWM1/2/3) and Port Mode (Bi-directional Port Mode). Initial Staus of PCR3 (Port Control Register Bit-3) is 0 (low). The PCR3 must be set to high for any case. The direction of Port-3 can be decided bit-by-bit. The read policy in Port Mode follows that described before. Read-Modify-Write instructions read the port latch than the pin.

To use Pin-3.0 to 3.7 as a normal input port, PCR3 should be high. If PCR3 is high, the direction of each Port-3 pin is decided by each P3IO bit. If the P3IO bit-x is high, Port-3.x is output mode. If low, Port-3.x is input mode. Initial status is input mode because P3IO (Port-3 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P3RD (Port-3 Resistor Disable Register). If the P3RD bit-x is high, Port-3.x pull-up resistor is disconnected. If low, Port-3.x pull-up resistor is connected. Initial status of P3RD is 00111111B, thus pull-up resistor of bit-7 and 6 is connected. But, pull-up resistor bit-0 to 5 is disconnected. If ZCR3 (High-Z Control Register Bit-3) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence.

To use Pin-3.0 to 3.7 as a normal output port, PCR3 should be high. If the P3IO bit-x is high, Port-3.x is output mode. In output mode, pull-up resistor is automatically disconnected regardless P3RD bit-x. If ZCR3 (High-Z Control Register Bit-3) is high, High-Z control is enabled. At this time, if HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use P1.0/PWM1, P1.1/PWM2, P1.2/PWM3, and P1.3/BUZ as a Timer output port, PCR3 should be high. And, a Timer output should be enabled in the Timer block.

To use P3.6/NWR and P3.7/NRD as External Memory Read and Write Pins, PCR3 should be high. And, P3IO.6, P3IO.7, P3.6, and P3.7 latch should be high. To use P3.6/NWR and P3.7/NRD as normal Port Pins, don’t use MOVX instructions that access External Data Memory.

[Table: P3.3/BUZ Pin Configuration]

Pin	NHIZ = 0	NHIZ = 1 & BZOE = 1	NHIZ = 1 & BZOE = 0 & P3IO3 = 0	NHIZ = 1 & BZOE = 0 & P3IO3 = 1
P3.3/BUZ	High Impedance	BUZ (output)	P3.3 input mode	P3.3 out mode

[Table: P3.0/PWM1 to P3.2/PWM3 Pin Configuration]

Pin (x = 1 to 3) (i = 0 to 2)	NHIZ = 0	NHIZ = 1 & PTxOE = 1	NHIZ = 1 & PTxOE = 0 & P3IOi = 0	NHIZ = 1 & PTxOE = 0 & P3IOi = 1
P3.0/PWM1	High Impedance	PWM1 (output)	P3.0 input mode	P3.0 out mode
P3.1/PWM2	High Impedance	PWM2 (output)	P3.1 input mode	P3.1 out mode
P3.2/PWM3	High Impedance	PWM3 (output)	P3.2 input mode	P3.2 out mode

[Table: Definition of P3]

Address	B0H							
Bit Addr.	B7H	B6H	B5H	B4H	B3H	B2H	B1H	B0H
BIT	7	6	5	4	3	2	1	0
NAME	P37	P36	P35	P34	P33	P32	P31	P30
Definition	Port-3 Pin or Latch bit-7	Port-3 Pin or Latch bit-6	Port-3 Pin or Latch bit-5	Port-3 Pin or Latch bit-4	Port-3 Pin or Latch bit-3	Port-3 Pin or Latch bit-2	Port-3 Pin or Latch bit-1	Port-3 Pin or Latch bit-0
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W RMW Ins: P37 Latch Read Other Ins: P3.7 Pin Read	R/W RMW Ins: P36 Latch Read Other Ins: P3.6 Pin Read	R/W RMW Ins: P35 Latch Read Other Ins: P3.5 Pin Read	R/W RMW Ins: P34 Latch Read Other Ins: P3.4 Pin Read	R/W RMW Ins: P33 Latch Read Other Ins: P3.3 Pin Read	R/W RMW Ins: P32 Latch Read Other Ins: P3.2 Pin Read	R/W RMW Ins: P31 Latch Read Other Ins: P3.1 Pin Read	R/W RMW Ins: P30 Latch Read Other Ins: P3.0 Pin Read
Write by Hardware								

[Table: Definition of P3IO]

Address	DAH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P3IO7	P3IO6	P3IO5	P3IO4	P3IO3	P3IO2	P3IO1	P3IO0
Definition	Port-3 I/O Control Register bit-7 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-6 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-5 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-4 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-3 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-2 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-1 0: Input Mode 1: Output Mode	Port-3 I/O Control Register bit-0 0: Input Mode 1: Output Mode
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P3RD]

Address	**DBH**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**P3RD7**	**P3RD6**	**P3RD5**	**P3RD4**	**P3RD3**	**P3RD2**	**P3RD1**	**P3RD0**
Definition	**Port-3 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable**	**Port-3 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable**	**Port-3 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable**	**Port-3 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable**	**Port-3 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable**	**Port-3 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable**	**Port-3 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable**	**Port-3 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable**
Reset Value	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**
Read/Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

[Port-4]

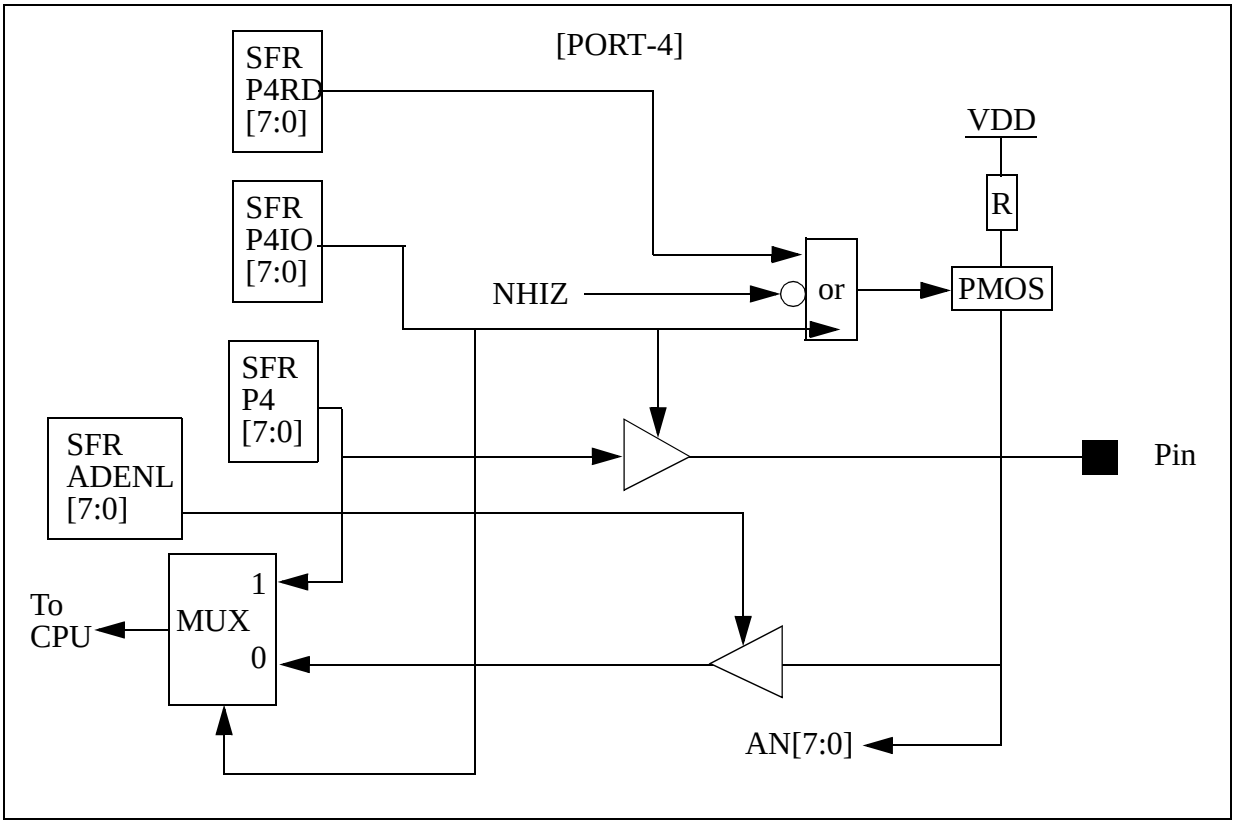
1. Overview

The Port-4(P4) is a 8-bit bidirectional port that can be used as ADC input pins (AN0 to AN7). The direction of Port-4 can be decided bit-by-bit. In the input mode, CPU reads pin status. In the output mode, CPU reads port latch rather than pin.

To use Pin-4.x as a normal input port, P4IOx should be low. The direction of each Port-4 pin is decided by each P4IO bit. If the P4IO bit-x is high, Port-4.x is output mode. If low, Port-4.x is input mode. Initial status is input mode because P4IO (Port-4 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P4RD (Port-4 Resistor Disable Register). If the P4RD bit-x is high, Port-4.x pull-up resistor is disconnected. If low, Port-4.x pull-up resistor is connected. Initial status of P4RD is 11111111B, thus pull-up resistor is disconnected. If HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence.

To use Pin-4.x as a normal output port, P4IOx should be high. If the P4IO bit-x is high, Port-4.x is output mode. In output mode, pull-up resistor is automatically disconnected regardless P4RD bit-x. If HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use P4.x/ANx as an analog input port, P4IOx should be low and P4RDx should be high. In addition ADENLx should be high to disable the input buffer. This will prevent current flow due to an analog input applied to the buffer.



[Table: Definition of P4]

Address	C0H							
Bit Addr.	C7H	C6H	C5H	C4H	C3H	C2H	C1H	C0H
BIT	7	6	5	4	3	2	1	0
NAME	P47	P46	P45	P44	P43	P42	P41	P40
Definition	Port-4 Pin or Latch bit-7	Port-4 Pin or Latch bit-6	Port-4 Pin or Latch bit-5	Port-4 Pin or Latch bit-4	Port-4 Pin or Latch bit-3	Port-4 Pin or Latch bit-2	Port-4 Pin or Latch bit-1	Port-4 Pin or Latch bit-0
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W Out Mode: P47 Latch Read In Mode: P4.7 Pin Read	R/W Out Mode: P46 Latch Read In Mode: P4.6 Pin Read	R/W Out Mode: P45 Latch Read In Mode: P4.5 Pin Read	R/W Out Mode: P44 Latch Read In Mode: P4.4 Pin Read	R/W Out Mode: P43 Latch Read In Mode: P4.3 Pin Read	R/W Out Mode: P42 Latch Read In Mode: P4.2 Pin Read	R/W Out Mode: P41 Latch Read In Mode: P4.1 Pin Read	R/W Out Mode: P40 Latch Read In Mode: P4.0 Pin Read
Write by Hardware								

[Table: Definition of P4IO]

Address	EAH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P4IO7	P4IO6	P4IO5	P4IO4	P4IO3	P4IO2	P4IO1	P4IO0
Definition	Port-4 I/O Control Register bit-7 0: Input Mode 1: Output Mode	Port-4 I/O Control Register bit-6 0: Input Mode 1: Output Mode	Port-4 I/O Control Register bit-5 0: Input Mode 1: Output Mode	Port-4 I/O Control Register bit-4 0: Input Mode 1: Output Mode	Port-4 I/O Control Register bit-3 0: Input Mode 1: Output Mode	Port-4 I/O Control Register bit-2 0: Input Mode 1: Output Mode	Port-4 I/O Control Register bit-1 0: Input Mode 1: Output Mode	Port-4 I/O Control Register bit-0 0: Input Mode 1: Output Mode
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P4RD]

Address	EBH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P4RD7	P4RD6	P4RD5	P4RD4	P4RD3	P4RD2	P4RD1	P4RD0
Definition	Port-4 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-4 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of ADENL]

Address	**93H**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**ADENL7**	**ADENL6**	**ADENL5**	**ADENL4**	**ADENL3**	**ADENL2**	**ADENL1**	**ADENL0**
Definition	**Port-4 Input Disable Register bit-7 0: Input Enable 1: Disable**	**Port-4 Input Disable Register bit-6 0: Input Enable 1: Disable**	**Port-4 Input Disable Register bit-5 0: Input Enable 1: Disable**	**Port-4 Input Disable Register bit-4 0: Input Enable 1: Disable**	**Port-4 Input Disable Register bit-3 0: Input Enable 1: Disable**	**Port-4 Input Disable Register bit-2 0: Input Enable 1: Disable**	**Port-4 Input Disable Register bit-1 0: Input Enable 1: Disable**	**Port-4 Input Disable Register bit-0 0: Input Enable 1: Disable**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Write by Hardware								

[Port-5]

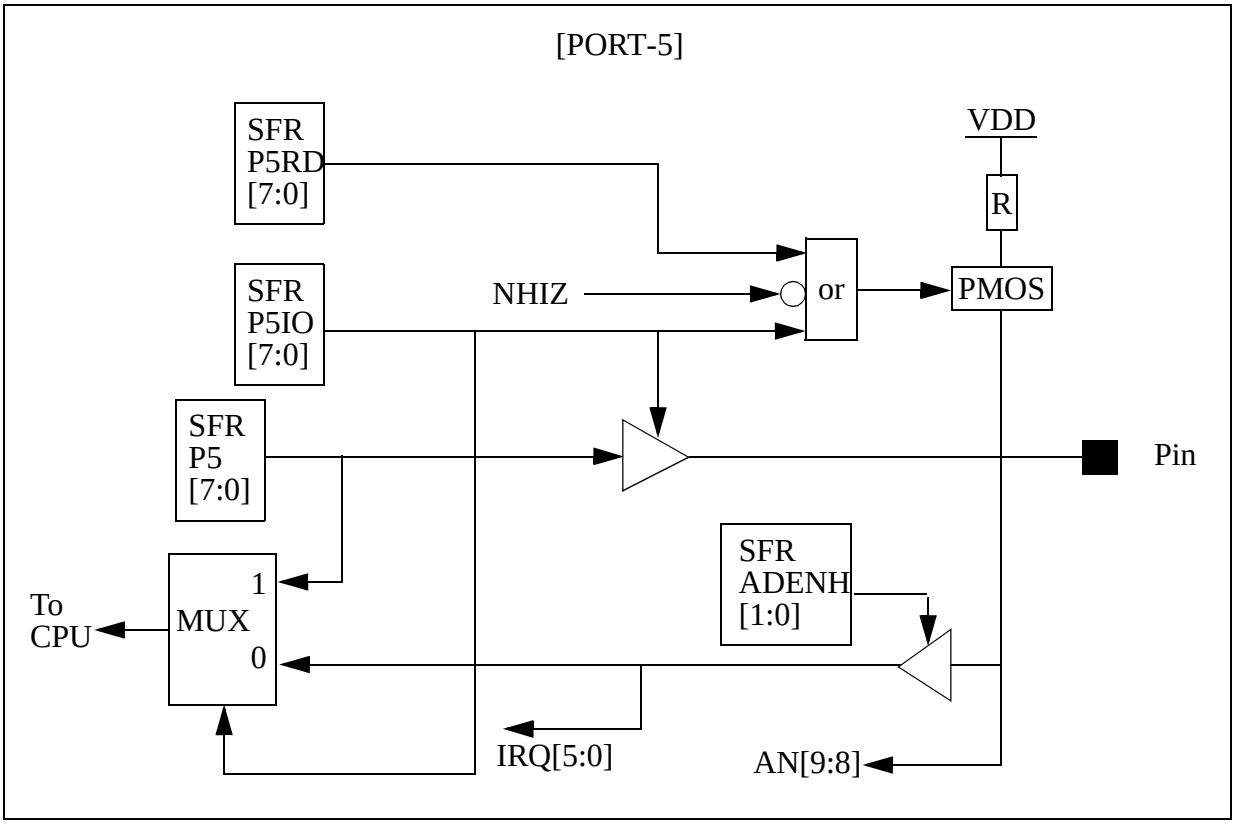
1. Overview

The Port-5(P5) is a 8-bit bidirectional port that can be used as ADC input pins (AN8 to AN9) or External Interrupt Pins (IRQ0 to IRQ5). The direction of Port-5 can be decided bit-by-bit. In the input mode, CPU reads pin status. In the output mode, CPU reads port latch rather than pin.

To use Pin-5.x as a normal input port, P5IOx should be low. The direction of each Port-5 pin is decided by each P5IO bit. If the P5IO bit-x is high, Port-5.x is output mode. If low, Port-5.x is input mode. Initial status is input mode because P5IO (Port-5 I/O Direction Register) is reset to 00000000B. In input mode, pull-up resistor can be connected by P5RD (Port-5 Resistor Disable Register). If the P5RD bit-x is high, Port-5.x pull-up resistor is disconnected. If low, Port-5.x pull-up resistor is connected. Initial status of P5RD is 11111111B, thus pull-up resistor is disconnected. If HIZ bit in the PSCR (Power Saving Control Register) becomes high, pull-up resistor is disconnected and pin status becomes high impedence. In input mode, P5.2/IRQ0 to P5.7/IRQ5 can be used as external interrupt pins.

To use Pin-5.x as a normal output port, P5IOx should be high. If the P5IO bit-x is high, Port-5.x is output mode. In output mode, pull-up resistor is automatically disconnected regardless P5RD bit-x. If HIZ bit in the PSCR (Power Saving Control Register) becomes high, pin status becomes high impedence.

To use P5.x/ANx as an analog input port, P5IOx should be low and P5RDx should be high. In addition ADENLx should be high to disable the input buffer. This will prevent current flow due to an analog input applied to the buffer.



[Table: Definition of P5]

Address	C8H							
Bit Addr.	CFH	CEH	CDH	CCH	CBH	CAH	C9H	C8H
BIT	7	6	5	4	3	2	1	0
NAME	P57	P56	P55	P54	P53	P52	P51	P50
Definition	Port-5 Pin or Latch bit-7	Port-5 Pin or Latch bit-6	Port-5 Pin or Latch bit-5	Port-5 Pin or Latch bit-4	Port-5 Pin or Latch bit-3	Port-5 Pin or Latch bit-2	Port-5 Pin or Latch bit-1	Port-5 Pin or Latch bit-0
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W Out Mode: P57 Latch Read In Mode: P5.7 Pin Read	R/W Out Mode: P56 Latch Read In Mode: P5.6 Pin Read	R/W Out Mode: P55 Latch Read In Mode: P5.5 Pin Read	R/W Out Mode: P54 Latch Read In Mode: P5.4 Pin Read	R/W Out Mode: P53 Latch Read In Mode: P5.3 Pin Read	R/W Out Mode: P52 Latch Read In Mode: P5.2 Pin Read	R/W Out Mode: P51 Latch Read In Mode: P5.1 Pin Read	R/W Out Mode: P50 Latch Read In Mode: P5.0 Pin Read
Write by Hardware								

[Table: Definition of P5IO]

Address	FAH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P5IO7	P5IO6	P5IO5	P5IO4	P5IO3	P5IO2	P5IO1	P5IO0
Definition	Port-5 I/O Control Register bit-7 0: Input Mode 1: Output Mode	Port-5 I/O Control Register bit-6 0: Input Mode 1: Output Mode	Port-5 I/O Control Register bit-5 0: Input Mode 1: Output Mode	Port-5 I/O Control Register bit-4 0: Input Mode 1: Output Mode	Port-5 I/O Control Register bit-3 0: Input Mode 1: Output Mode	Port-5 I/O Control Register bit-2 0: Input Mode 1: Output Mode	Port-5 I/O Control Register bit-1 0: Input Mode 1: Output Mode	Port-5 I/O Control Register bit-0 0: Input Mode 1: Output Mode
Reset Value	0	0	0	0	0	0	0	0
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of P5RD]

Address	FBH							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	P5RD7	P5RD6	P5RD5	P5RD4	P5RD3	P5RD2	P5RD1	P5RD0
Definition	Port-5 Resistor Disable Register bit-7 0: Resistor Enable 1: Disable	Port-5 Resistor Disable Register bit-6 0: Resistor Enable 1: Disable	Port-5 Resistor Disable Register bit-5 0: Resistor Enable 1: Disable	Port-5 Resistor Disable Register bit-4 0: Resistor Enable 1: Disable	Port-5 Resistor Disable Register bit-3 0: Resistor Enable 1: Disable	Port-5 Resistor Disable Register bit-2 0: Resistor Enable 1: Disable	Port-5 Resistor Disable Register bit-1 0: Resistor Enable 1: Disable	Port-5 Resistor Disable Register bit-0 0: Resistor Enable 1: Disable
Reset Value	1	1	1	1	1	1	1	1
Read/Write by Software	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Write by Hardware								

[Table: Definition of ADENH]

Address	**94H**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**ADENH7**	**ADENH6**	**ADENH5**	**ADENH4**	**ADENH3**	**ADENH2**	**ADENH1**	**ADENH0**
Definition	**Unused Read 0**	**Unused Read 0**	**Unused Read 0**	**Unused Read 0**	**Unused Read 0**	**Unused Read 0**	**Port-5 Input Disable Register bit-1 0: Input Enable 1: Disable**	**Port-5 Input Disable Register bit-0 0: Input Enable 1: Disable**
Reset Value	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Read/Write by Software	**R**	**R**	**R**	**R**	**R**	**R**	**R/W**	**R/W**
Write by Hardware								

[Port-6]

1. Overview

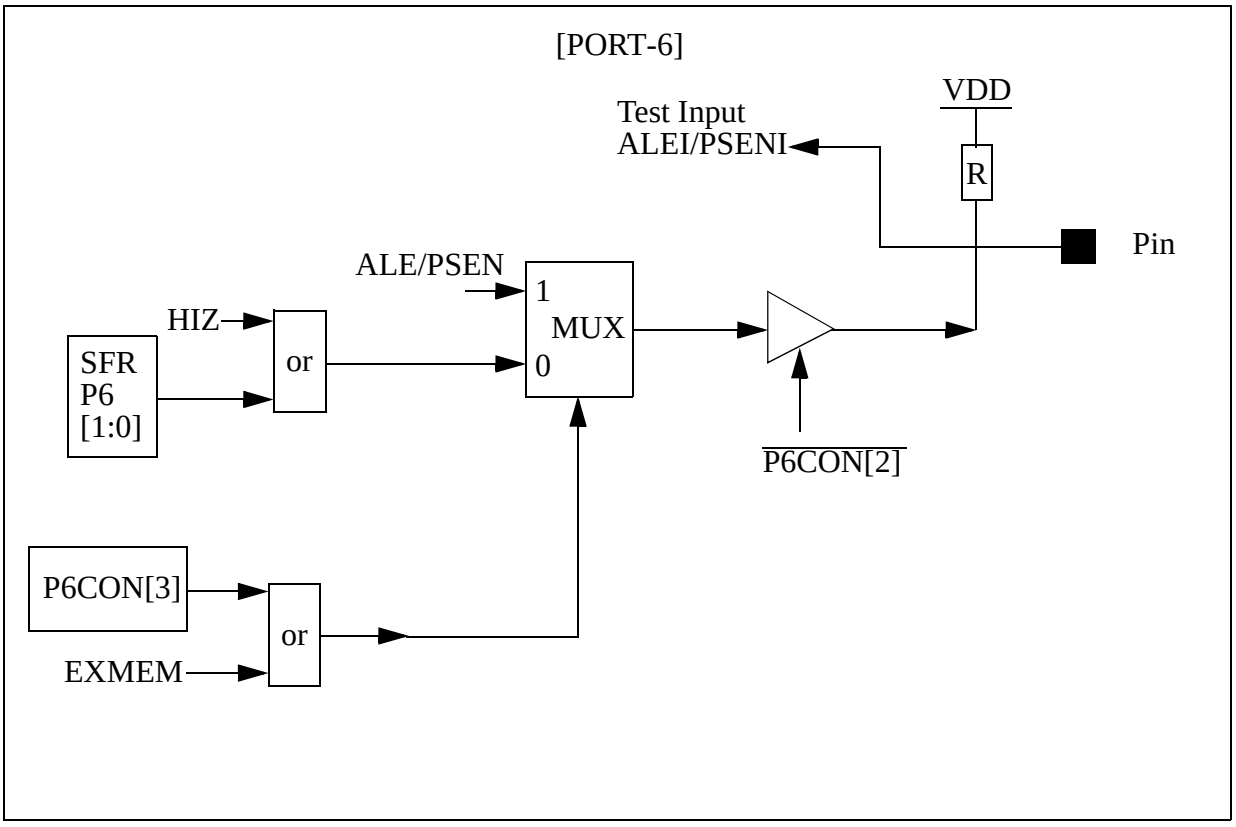
The Port-6 is a two bit CMOS Push-pull output port with pull-up resistor. To use this port as a normal output port, EXMEM pin should be low and P6CON[3:2] should be 00B. In this normal port mode, if HIZ bit of SFR PSCR becomes high, output CMOS becomes off and pin status becomes high-impedance.

In the initial state, P6.0/PSEN and P6.1/ALE are test input port with pull-up resistor. If P6CON[3:2](bit-[3:2] of SFR P6) is 10B or EXMEM pin is high, these two pins are used as external bus interface pins, PSEN, ALE.

The bit-4 of Port-6 (EXMEM Bit) indicates the EXMEM pin status.

Table 7: P6 Control

EXMEM	P6CON[3:2]	Description
1	[xx]	Bidirectional ALE/PSEN Mode (CPU control)
0	[11]	Initial State, ALEI/PSENI Input Mode
0	[10]	ALE/PSEN Output Mode
0	[00]	General Port-6 Output Mode
0	[01]	Never Use



[Table: Definition of P6]

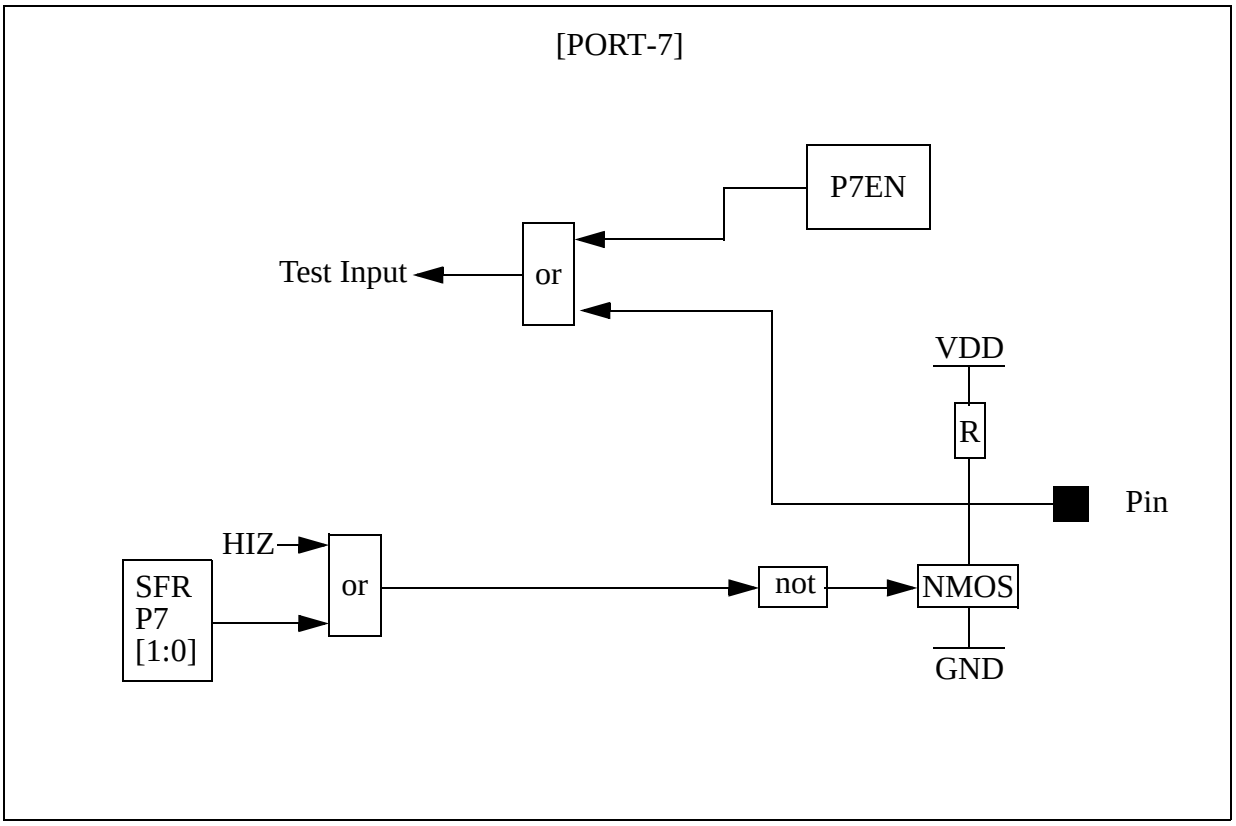
Address	B7H							
Bit Addr.	None							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	EXMEM	P6CON3	P6CON2	P61	P60
Definition				Exmem Pin Input Status	0: Port Mode 1: ALE Mode	0: Output Mode 1: Test In-put Mode	Port-6 Latch bit-1	Port-6 Latch bit-0
Reset Value	unknown	unknown	unknown	unknown	1	1	1	1
Read/Write by Software				R	R/W	R/W	R/W Nor Mode: P61 Latch Read Tst Mode: P6.1 Pin Read	R/W Nor Mode: P60 Latch Read Tst Mode: P6.0 Pin Read
Write by Hardware								

[Port-7]

1. Overview

The Port-7 is a two bit N-channel open drain output port with pull-up resistor. To use this port as a normal output port, P7EN(bit-2 of SFR P7) should be high. In this normal port mode, if HIZ bit of SFR PSCR becomes high, output NMOS becomes off and pin status becomes weakly high.

In the initial state, P7.0 and P7.1 are test input port with pull-up resistor. If P7.0 and P7.1 latches are high and P7EN(bit-2 of SFR P7) is low, these two pins are used as active low test input pins



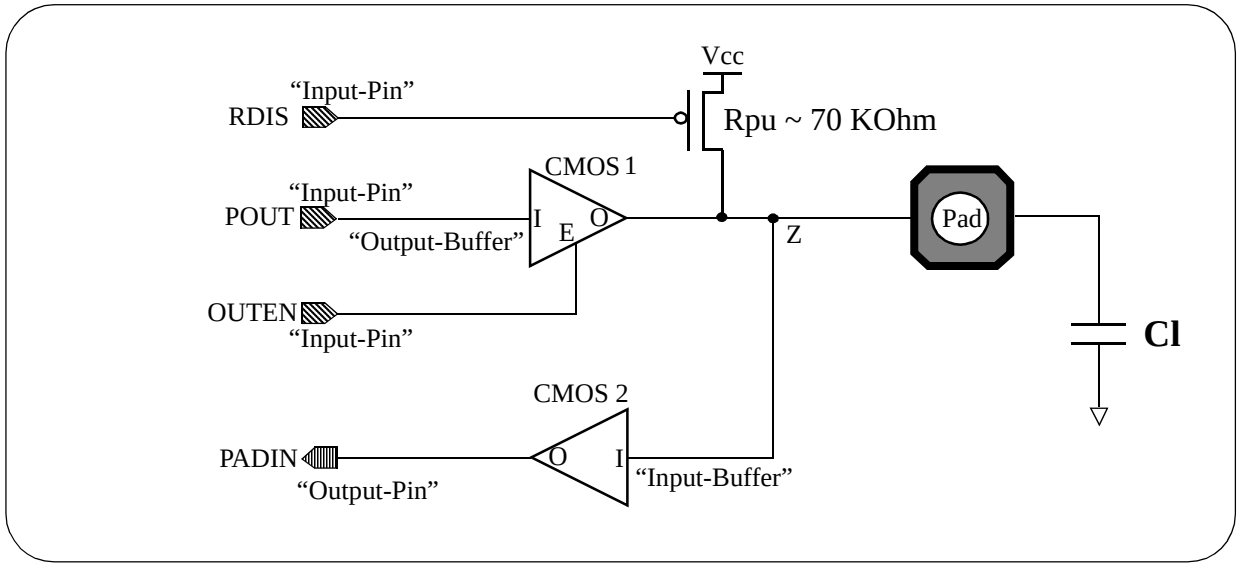
[Table: Definition of P7]

Address	**B7H**							
Bit Addr.	**None**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**P7EN**	**P71**	**P70**
Definition						**0: Test In 1: Output Port**	**Port-7 Latch bit-1**	**Port-7 Latch bit-0**
Reset Value	**unknown**	**unknown**	**unknown**	**unknown**	**unknown**	**0**	**1**	**1**
Read/Write by Software						**R/W**	**R/W Nor Mode: P71 Latch Read Tst Mode: P7.1 Pin Read**	**R/W Nor Mode: P70 Latch Read Tst Mode: P7.0 Pin Read**
Write by Hardware								

Input/Output-Pads Specification for SS8203

1.Bidirection CMOS I/O with active “High” Enable and Pullup-Enable Type-A:

1.1) Schematic:



1.2) Specification:

OUTEN is active “High” and RDIS is active “Low”. Logical Z=POUT when OUTEN=”H” and logical PADIN=Z. Z is tristate when OUTEN=”L” . Input voltage varies rail-to-rail. The resistance Rpu is active when RDIS=”L”, otherwise is disable.

Table 8: I/O-Type A Specification

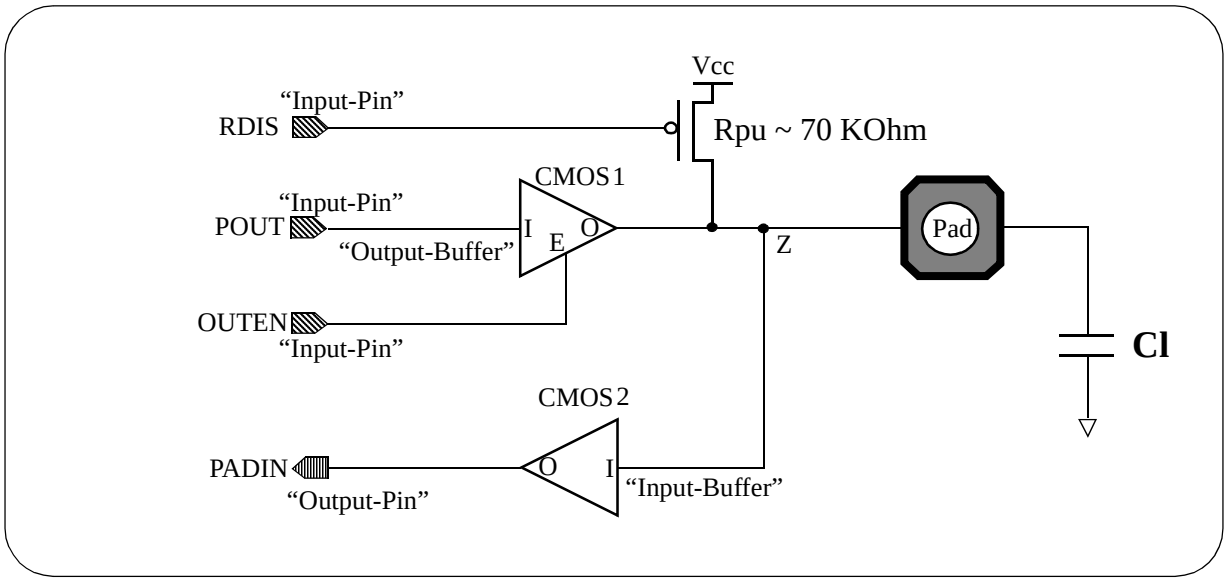
ITEMS	***Symbol***	***Min***	***Typ***	***Max***	***Units***
Supply Voltage	Vcc	5 - 10%	5	5 + 10%	V
Ground	Vss		0		V
Temperature	T	-20	25	+85	degree C
POUT-to-PAD (OUTEN-to-PAD) (Output Drive: 2 mA) @ Cl=50pF	toPLH		6.5		nS
	toPHL		10.6		nS
	TR		12.6		nS
	TF		16.8		nS
PAD-to-PADIN	tiPLH		2		nS
	tiPHL		2		nS
Transistor-pullup	Rpu	50	70	100	KOhm

Table 8: I/O-Type A Specification

ITEMS	***Symbol***	***Min***	***Typ***	***Max***	***Units***
Output High @ IOH=200 uA	VOH	Vcc - 0.4			V
Output Low @ IOL=200 uA	VOL			Vss + 0.4	V
Leakage Current	Ileakage			1	micro A
Output Current Sink	IOL @ VOL=Vss + 0.4V	2.96			mA
Output Current Sink	IOH @ VOH=Vcc - 0.4V	3.1			mA

2.Bidirection CMOS I/O with active “High” Enable and Pullup-Enable Type-B:

2.1) Schematic:



2.2) Specification:

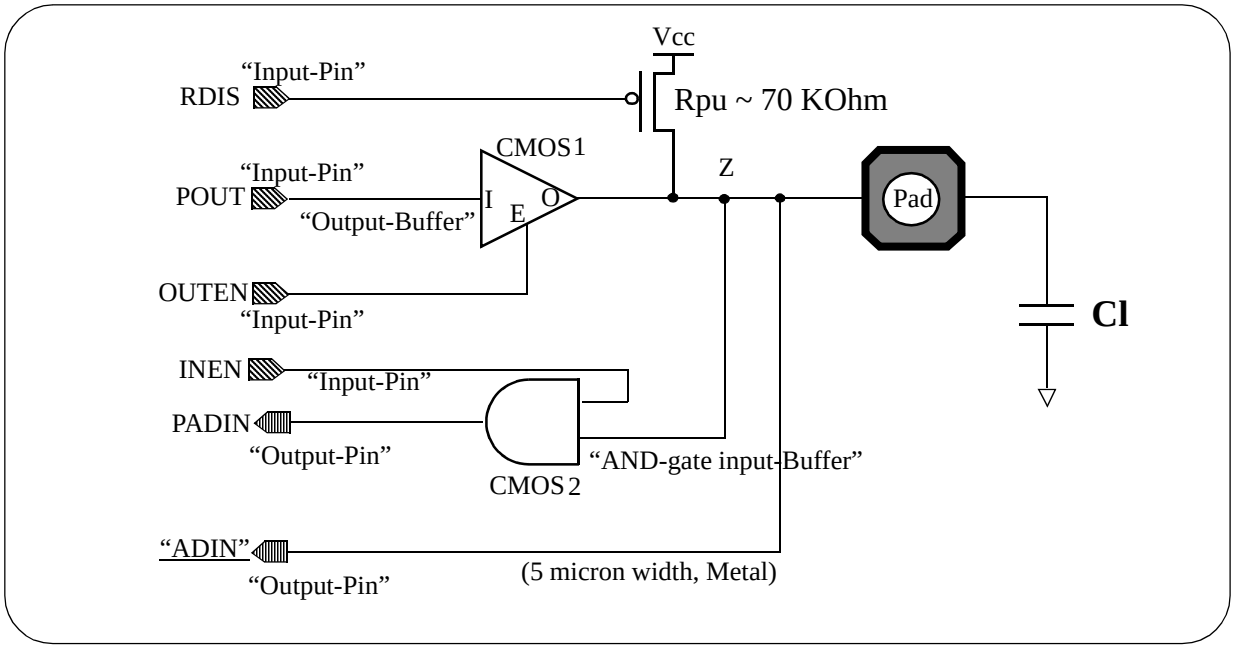
I/O-Type B has DC-Current Sink inside CMOS1. OUTEN is active “High” and RDIS is active “Low”. Logical Z=POUT when OUTEN=”H” and logical PADIN=Z. Z is tristate when OUTEN=”L”. Input voltage varies rail-to-rail. The resistance Rpu is active when RDIS=”L”, otherwise is disable.

Table 9: I/O-Type B Specification

ITEMS	***Symbol***	***Min***	***Typ***	***Max***	***Unit***
Supply Voltage	Vcc	5 - 10%	5	5 + 10%	V
Ground	Vss		0		V
Temperature	T	-20	25	+85	degree C
POUT-to-PAD (OUTEN-to-PAD) @ Cl=50pF	toPLH		6.7		nS
	toPHL		4.3		nS
	TR		12.6		nS
	TF		3.5		nS
PAD-to-PADIN	tiPLH		2		nS
	tiPHL		2		nS
Transistor-pullup	Rpu	50	70	100	KOhm
Output High @ IOH=200 uA	VOH	Vcc - 0.4			V
Output Low @ IOL=200 uA	VOL			Vss + 0.4	V
Leakage Current	Ileakage			1	micro A
Output Current Sink (Two types)	IOL @ VOL=Vss + 0.4V	20.12 20.12			mA
Output Current Sink	IOH @ VOL=Vcc - 0.4V	3.1			mA

3.Bidirection CMOS I/O with active “High” Enable and Pullup-Enable Type-C:

3.1) Schematic:



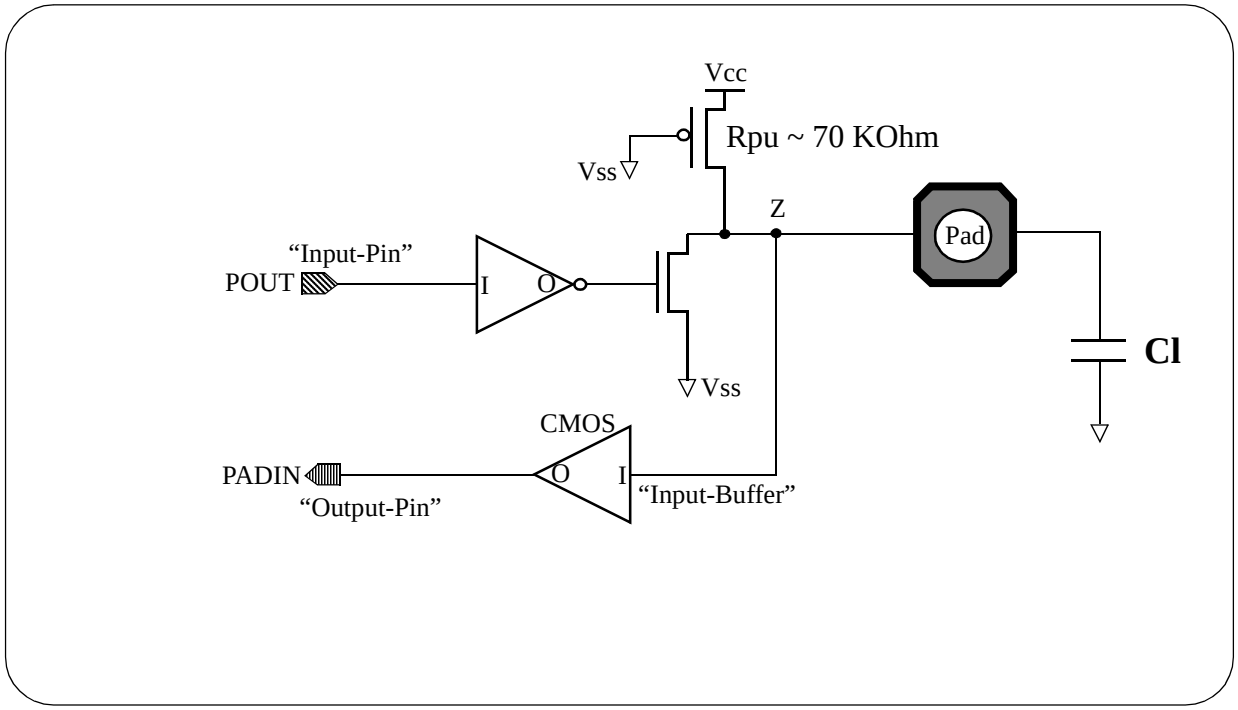
3.2) Specification:

I/O-Type C is the same as I/O-Type A except that Metal-wire from Pad to internal Pin “ADIN” directly. OUTEN is active “High” and RDIS is active “Low”. Logical Z=POUT when OUTEN=”H” and logical PADIN=Z. The delay path "INEN-to-PADIN" is equal to the delay path "PAD-to-PADIN".Z is tristate when OUTEN=”L” Input voltage varies rail-to-rail. The resistance Rpu is active when RDIS=”L”, otherwise is disable.

I/O-Type C Specification is same I/O-Type A Specification.(The same as Table 1)

4. Open Drain I/O with static Pullup Type-D:

4.1) Schematic:



4.2) Specification:

I/O-Type D is Open Drain I/O with static Pullup equivalent 70 KOhm. Logical Z=POUT and logical PADIN=Z.

Table 10: I/O-Type D Specification

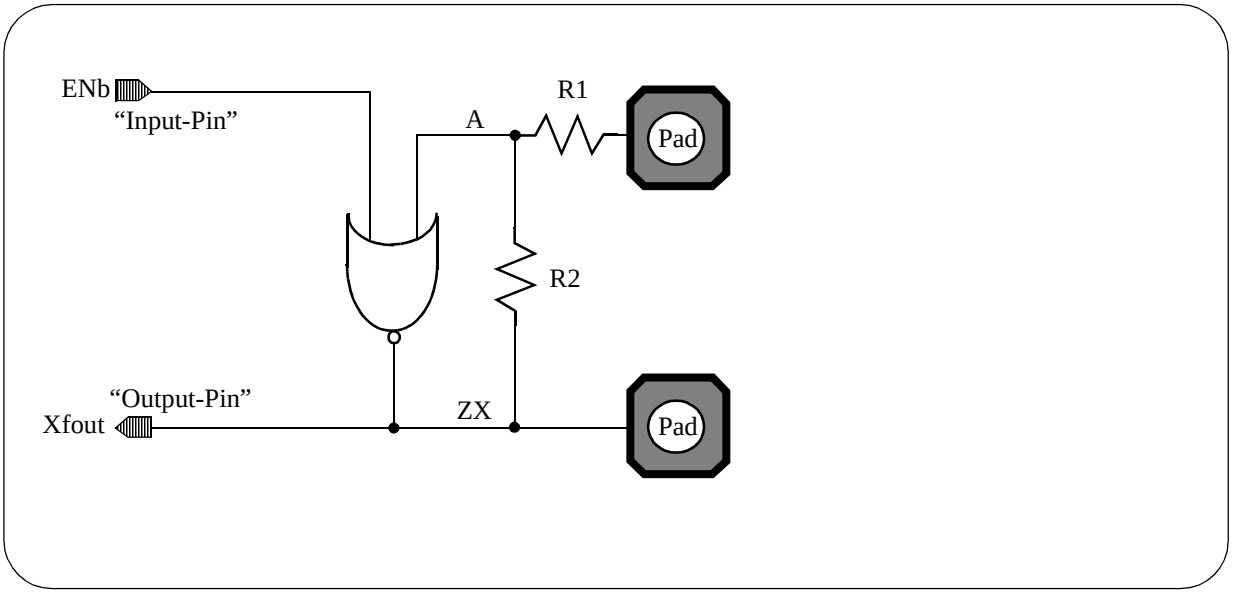
ITEMS	***Symbol***	***Min***	***Typ***	***Max***	***Unit***
Supply Voltage	Vcc	5 - 10%	5	5 + 10%	V
Ground	Vss		0		V
Temperature	T	-20	25	+85	degree C
POUT-to-PAD @ Cl=50pF	toPHL		10.2		nS
	TF		16.8		nS
PAD-to-PADIN	tiPLH		2		nS
	tiPHL		2		nS

Table 10: I/O-Type D Specification

ITEMS	***Symbol***	***Min***	***Typ***	***Max***	***Unit***
Transistor-pullup	Rpu	50	70	100	KOhm
Output Low @ IOL=200 uA	VOL			Vss + 0.4	V
Leakage Current	Ileakage			1	micro A
Output Current Sink	IOL @ VOL=Vss + 0.4V	2.96			mA

5. Oscillator-Pads with Enable-signal:

5.1) Schematic:



5.2) Specification:

ENb is active "Low".

Table 11: Oscillator Pads Specification

ITEMS	***Symbol***	***Min***	***Typ***	***Max***	***Unit***
Supply Voltage	Vcc	5 - 10%	5	5 + 10%	V
Ground	Vss		0		V
Temperature	T	-20	25	+85	degree C
Frequency (*cell 1*)	f	1	12	30	MHz

Table 11: Oscillator Pads Specification

ITEMS	***Symbol***	***Min***	***Typ***	***Max***	***Unit***
Frequency (*cell 2*)	f	1	32.768	60	KHz
Peak-to-Peak Voltage	Vpp			5	V
Duty cycle of Xfout		50 -1%	50%	50 +1%	

6. DC-Parametrics:

Table 12: I/O-DC Characteristics

I/O-Types	**VOL**	**VOH**	**IOL**	**IOH**	**Vcc**	**Vss**	**Temperature**
Type-A	Vss	Vcc	2.96 mA @VOL=Vss + 0.4V	3.10 mA @VOH=Vcc - 0.4V	5V+(-)10%	0V	-20 C degree to +85 C degree
Type-B	Vss	Vcc	20.12 mA @VOL=Vss + 0.4V	3.10 mA @VOH=Vcc - 0.4V	5V+(-)10%	0V	-20 C degree to +85 C degree
Type-C	Vss	Vcc	2.96 mA @VOL=Vss + 0.4V	3.10 mA @VOH=Vcc - 0.4V	5V+(-)10%	0V	-20 C degree to +85 C degree
Type-D (Open Drain)	Vss	Vcc	2.96 mA @VOL=Vss + 0.4V	**None**	5V+(-)10%	0V	-20 C degree to +85 C degree

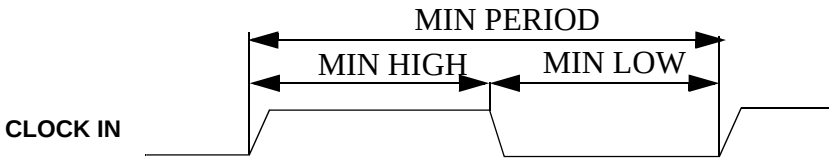
SS8203A AC Specifications

SPEC	Description	Min	Max	Unit	Condition
TCYC	XFIN oscillator period	83.3		ns	
TCYCH	XFIN high	30		ns	
TCYCL	XFIN low	30		ns	
TCYCR	XFIN rise time	10		ns	
TCYCF	XFIN fall time	10		ns	
TCYS	XSIN oscillator period	31.3		us	
TCYSH	XSIN high	12		us	
TCYSL	XSIN low	12		us	
TCYSR	XSIN rise time	25		ns	
TCYSF	XSIN fall time	25		ns	
TOD	XFIN to output delay		41	ns	Prog pull-up off
TODRPU	XFIN to output rise delay		2.0	us	Prog pull-up on
TDPSENR	XFIN to PSEN rise delay		90	ns	external 3K pull-up
TDALER	XFIN to ALE rise delay		90	ns	external 3K pull-up
TCYCS	External Serial Clock period	167		ns	
TCYCSH	External Serial Clock High	60		ns	
TCYCSL	External Serial Clock Low	60		ns	
TSUSI	Serial data in to SK rise set up	35		ns	
THLDSI	Serial data in to SK rise hold	10		ns	
TDSO	SK fall to serial data out delay		35	ns	
TIRQL	minimum interrupt low		12	mc	Note: 1
TRSTL	minimum reset low		12	mc	Note: 1

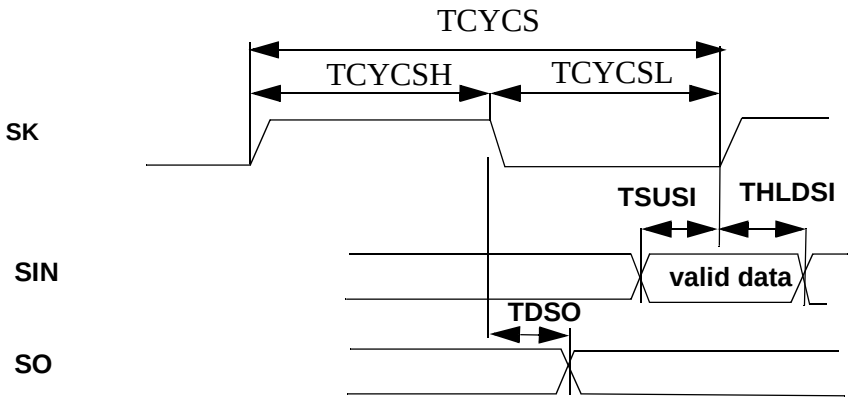
Note 1: MC is machine cycle and 1 machine cycle is 12 cpu clock cycles which is either XFIN or XSIN.

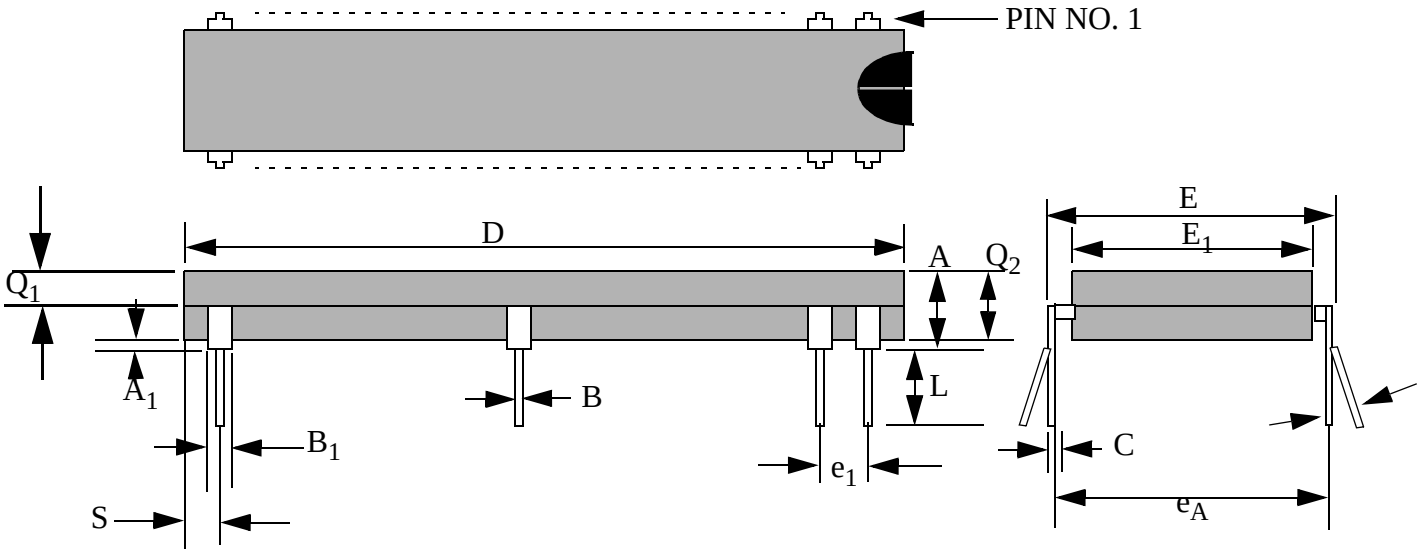
TIMING WAVEFORMS

CLOCK INPUT WAVEFORMS XFIN, XSIN

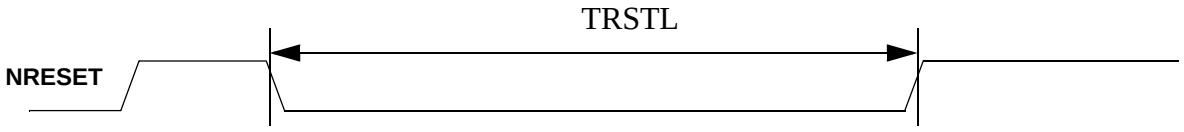


SIO WAVEFORMS

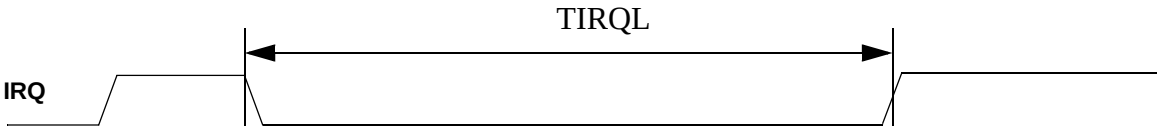




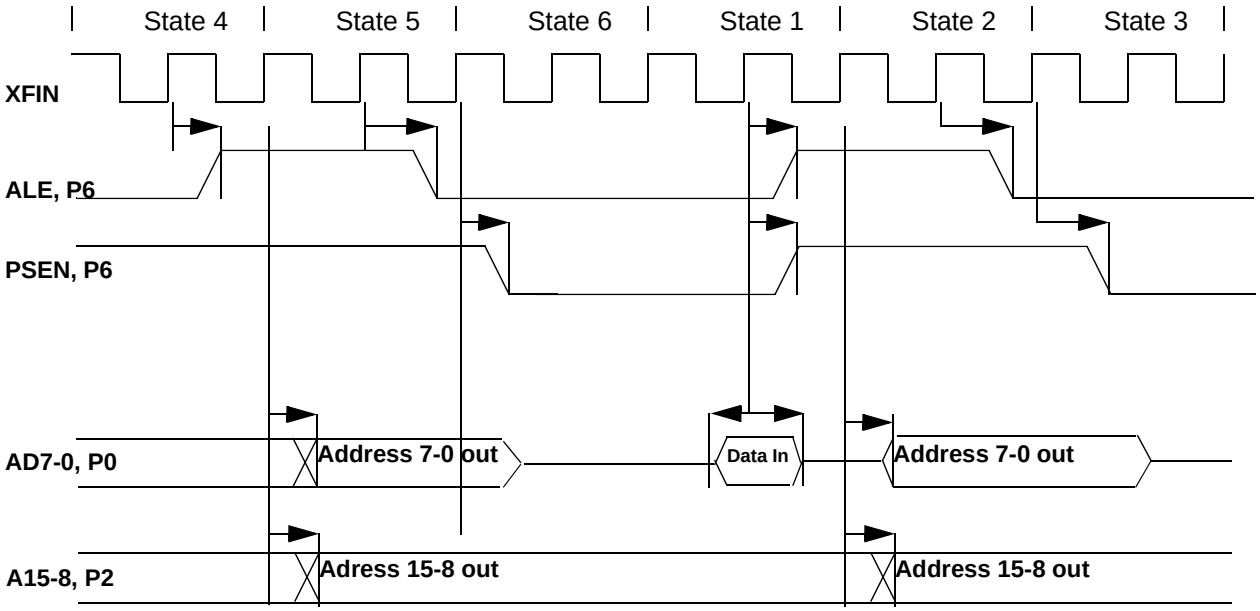
RESET TIMING



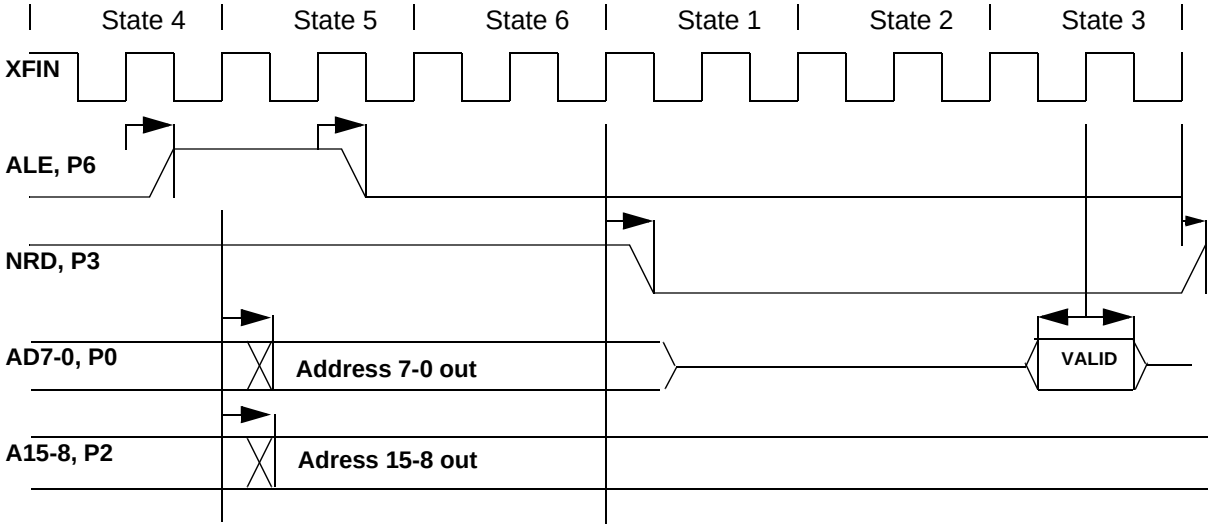
INTERRUPT TIMING



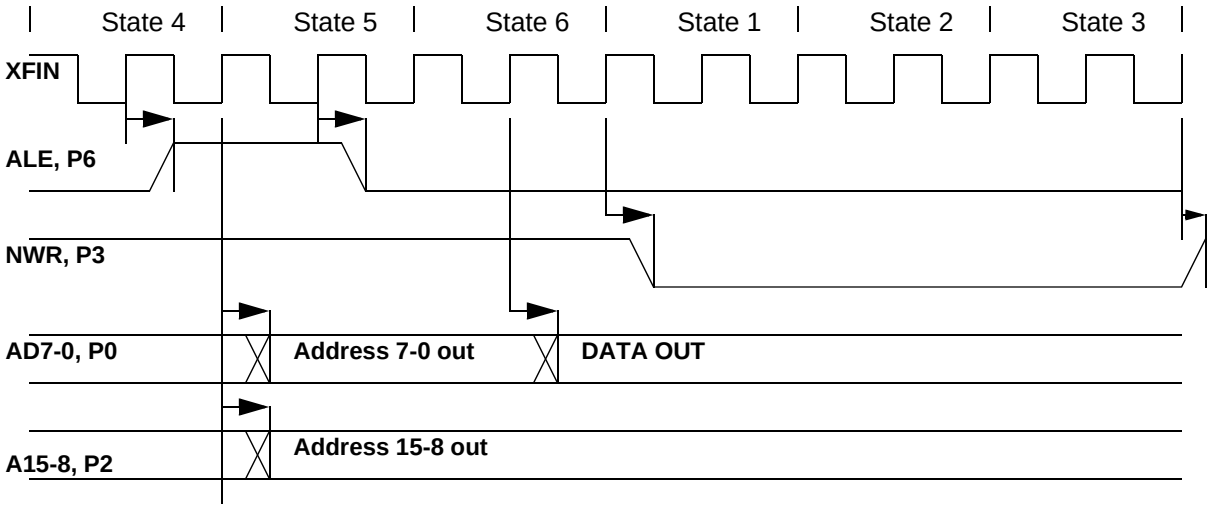
INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



EXTERNAL DATA MEMORY READ



EXTERNAL DATA MEMORY WRITE



SS8203 PACKAGE DATA SHEET

		MIN,mm	NOM,	MAX	MIN,in	NOM	MAX
Overall Height	A			0.200			5.08
Board Standoff	A_1	0.020			0.51		
	B	0.015	0.018	0.022	0.38	0.46	0.56
	B_1	0.030	0.040	0.050	0.076	1.02	1.27
	C	0.008	0.010	0.012	0.20	0.25	0.30
Body Length	D	2.260	2.273	2.280	57.40	57.73	57.91
	E	0.750		0.775	19.05		19.69
Body Width	E_1	0.660	0.670	0.680	16.76	17.02	17.27
Lead Pitch	e_1		0.070			1.78	
	e_A		0.750			19.05	
	L	0.120		0.135	3.05		3.43
	α	0^0		15^0	0^0		15^0
	N		64			64	
	Q_1	0.065	0.070	0.075	1.65	1.78	1.91
Body Thickness	Q_2		0.150			3.81	
	S	0.047	0.052	0.057	1.19	1.32	1.45