

## General Description

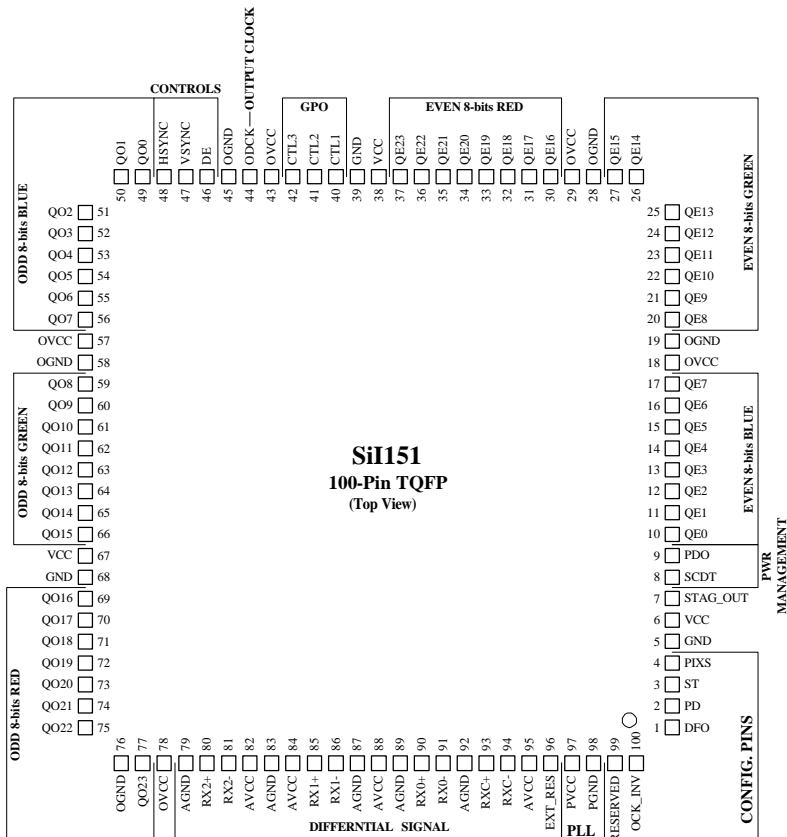
The SiI151 uses PanelLink Digital technology to support displays ranging from VGA to SXGA (25-112 MHz) which is ideal for desktop and specialty applications. The SiI151 receiver supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 or 2 pixels/clock mode, and also features an inter-pair skew tolerance up to 1 full input clock cycle. In addition, the receiver data output is time staggered to reduce ground bounce which affects EMI. Since all PanelLink products are designed on scaleable CMOS architecture to support future performance requirements while maintaining the same logical interface, system designers can be assured that the interface will be fixed through a number of technology and performance generations.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed digital design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

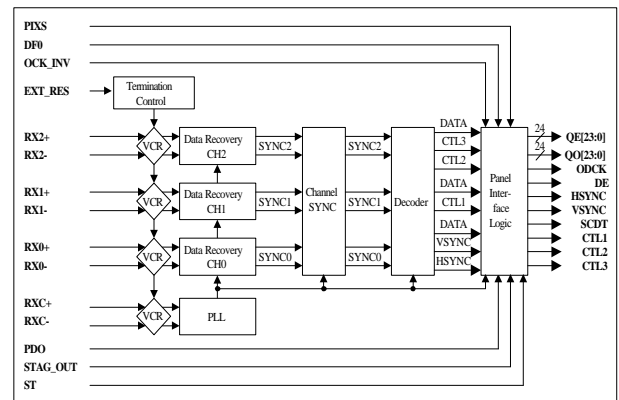
## Features

- Scalable Bandwidth: 25-112 MHz (VGA to SXGA)
- Low Power: 3.3V core operation & power-down mode
- High Skew Tolerance: 1 full input clock cycle (9ns at 108 MHz)
- Time staggered data output for reduced ground bounce
- Sync Detect: for Plug & Display "Hot Plugging"
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)

## SiI151 Pin Diagram



## Functional Block Diagram



## Absolute Maximum Conditions

Note: Permanent device damage may occur if absolute maximum conditions are exceeded.

Functional operation should be restricted to the conditions described under Normal Operating Conditions.

| Symbol    | Parameter                                | Min  | Typ | Max            | Units |
|-----------|--|------|-----|----------------|-------|
| $V_{CC}$  | Supply Voltage 3.3V                      | -0.3 |     | 4.0            | V     |
| $V_I$     | Input Voltage                            | -0.3 |     | $V_{CC} + 0.3$ | V     |
| $V_O$     | Output Voltage                           | -0.3 |     | $V_{CC} + 0.3$ | V     |
| $T_A$     | Ambient Temperature (with power applied) | -25  |     | 105            | °C    |
| $T_{STG}$ | Storage Temperature                      | -40  |     | 125            | °C    |
| $P_{PD}$  | Package Power Dissipation                |      |     | 1              | W     |

## Normal Operating Conditions

| Symbol    | Parameter                                | Min  | Typ | Max | Units             |
|-----------|--|------|-----|-----|-------------------|
| $V_{CC}$  | Supply Voltage                           | 3.00 | 3.3 | 3.6 | V                 |
| $V_{CCN}$ | Supply Voltage Noise <sup>1</sup>        |      |     | 100 | mV <sub>P-P</sub> |
| $T_A$     | Ambient Temperature (with power applied) | 0    | 25  | 70  | °C                |

Note: <sup>1</sup> Guaranteed by design.

## DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

| Symbol     | Parameter                         | Conditions       | Min | Typ | Max        | Units |
|------------|-----------------------------------|------------------|-----|-----|------------|-------|
| $V_{IH}$   | High-level Input Voltage          |                  | 2   |     |            | V     |
| $V_{IL}$   | Low-level Input Voltage           |                  |     |     | 0.8        | V     |
| $V_{OH}$   | High-level Output Voltage         |                  | 2.4 |     |            | V     |
| $V_{OL}$   | Low-level Output Voltage          |                  |     |     | 0.4        | V     |
| $V_{CINL}$ | Input Clamp Voltage <sup>1</sup>  | $I_{CL} = -18mA$ |     |     | GND -0.8   | V     |
| $V_{CIPL}$ | Input Clamp Voltage <sup>1</sup>  | $I_{CL} = 18mA$  |     |     | IVCC + 0.8 | V     |
| $V_{CONL}$ | Output Clamp Voltage <sup>1</sup> | $I_{CL} = -18mA$ |     |     | GND -0.8   | V     |
| $V_{COPL}$ | Output Clamp Voltage <sup>1</sup> | $I_{CL} = 18mA$  |     |     | OVCC + 0.8 | V     |
| $I_{OL}$   | Output Leakage Current            | High Impedance   | -10 |     | 10         | μA    |

Note: <sup>1</sup> Guaranteed by design.

## DC Specifications

Under normal operating conditions unless otherwise specified.

| Symbol    | Parameter  | Conditions  | Min         | Typ         | Max       | Units |
|-----------|--|---|-------------|-------------|-----------|-------|
| $I_{OHD}$ | Output High Drive<br>Data and Controls                     | $V_{OUT} = V_{OH};$<br>ST = 1<br>ST = 0   | 4.2<br>2.1  | 8<br>4      | 18<br>9   | mA    |
| $I_{OLD}$ | Output Low Drive<br>Data and Controls                      | $V_{OUT} = V_{OL};$<br>ST = 1<br>ST = 0   | 5.2<br>2.6  | 5.5<br>2.75 | 11<br>5.5 | mA    |
| $I_{OHC}$ | ODCK High Drive  | $V_{OUT} = V_{OH};$<br>ST = 1<br>ST = 0   | 8.5<br>4.2  | 17<br>9     | 37<br>18  | mA    |
| $I_{OLC}$ | ODCK Low Drive   | $V_{OUT} = V_{OL};$<br>ST = 1<br>ST = 0   | 10.4<br>5.2 | 16<br>8     | 23<br>11  | mA    |
| $V_{ID}$  | Differential Input Voltage<br>Single Ended Amplitude       |   | 75          |             | 1000      | mV    |
| $I_{PD}$  | Power-down Current <sup>2</sup>                            |   |             |             | 10        | mA    |
| $I_{CCR}$ | Receiver Supply Current<br>DCLK=112MHz, 1-pixel/clock mode | $C_{LOAD} = 10pF$<br>$R_{EXT\_SWING} = 680 \Omega$<br>Typical Pattern <sup>3</sup>    |             | 215         | 235       | mA    |
|           | DCLK=112MHz, 1-pixel/clock mode                            | $C_{LOAD} = 10pF$<br>$R_{EXT\_SWING} = 680 \Omega$<br>Worse Case Pattern <sup>4</sup> |             | 240         | 265       | mA    |

Note: <sup>1</sup> Guaranteed by design.

<sup>2</sup> The transmitter must be in power-down mode, powered off, or disconnected for the current to be under this maximum.

<sup>3</sup> The Typical Pattern contains a gray scale area, checkerboard area, and text.

<sup>4</sup> Black and white checkerboard pattern, each checker is two pixel wide.

**AC Specifications**

Under normal operating conditions unless otherwise specified. Low drive strength values, when ST=0, are given below.

| Symbol            | Parameter   | Conditions  | Min      | Typ  | Max        | Units            |
|-------------------|---|---|----------|------|------------|------------------|
| T <sub>DPS</sub>  | Intra-Pair (+ to -) Differential Input Skew <sup>1</sup>  | 112 MHz<br>One Pixel / Clock                                  |          |      | 360        | ps               |
| T <sub>CCS</sub>  | Channel to Channel Differential Input Skew <sup>1</sup>   | 112 MHz<br>One Pixel / Clock                                  |          |      | 6          | ns               |
| T <sub>IJIT</sub> | Worst Case Differential Input Clock Jitter tolerance <sup>2,3</sup><br>65 MHz, One Pixel / Clock          |   |          |      | 465        | ps               |
|                   | 112 MHz, One Pixel / Clock  |   |          |      | 270        |                  |
| D <sub>LHT</sub>  | Low-to-High Transition Time<br>Data and Controls  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 |          |      | 5.5<br>3.1 | ns               |
|                   | ODCK  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 |          |      | 2.75       |                  |
| D <sub>HLT</sub>  | High-to-Low Transition Time<br>Data and Controls  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 |          |      | 3<br>2.5   | ns               |
|                   | ODCK  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 |          |      | 2          |                  |
| T <sub>SOF</sub>  | Data/Control Setup Time to ODCK falling edge <sup>4</sup> (OCK_INV = 0)<br>65MHz, 1-pixel/clock, PIXS = 0 | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 | 3<br>3   |      |            | ns               |
|                   | 56MHz, 2-pixel/clock, PIXS = 1  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 | 5<br>3.5 |      |            |                  |
| T <sub>HOFF</sub> | Data/Control Hold Time to ODCK falling edge <sup>4</sup> (OCK_INV = 0)<br>65MHz, 1-pixel/clock, PIXS = 0  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 | 8<br>8   |      |            | ns               |
|                   | 56MHz, 2-pixel/clock, PIXS = 1  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 | 8<br>7   |      |            |                  |
| R <sub>CIP</sub>  | ODCK Cycle Time <sup>1</sup> (1-pixels/clock)   |   | 8.9      |      | 50         | ns               |
| F <sub>CIP</sub>  | ODCK Frequency <sup>1</sup> (1-pixel/clock)   |   | 20       |      | 112        | MHz              |
| R <sub>CIP</sub>  | ODCK Cycle Time <sup>1</sup> (2-pixels/clock)   |   | 17.8     |      | 100        | ns               |
| F <sub>CIP</sub>  | ODCK Frequency <sup>1</sup> (2-pixel/clock)   |   | 10       |      | 56         | MHz              |
| R <sub>CIH</sub>  | ODCK High Time <sup>1,5</sup> 65MHz, 1-pixel/clock, PIXS = 0  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 | 3        |      |            | ns               |
|                   | 56MHz, 1-pixel/clock, PIXS = 1  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 |          |      |            |                  |
| R <sub>CIL</sub>  | ODCK Low Time <sup>1,5</sup> 65MHz, 1-pixel/clock, PIXS = 0   | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 | 3        |      |            | ns               |
|                   | 56MHz, 1-pixel/clock, PIXS = 1  | C <sub>L</sub> = 10pF; ST = 1<br>C <sub>L</sub> = 5pF; ST = 0 |          |      |            |                  |
| T <sub>PDL</sub>  | Delay from PD Low to high impedance outputs <sup>1</sup>  |   |          |      | 10         | ns               |
| T <sub>HSC</sub>  | Link disabled (DE inactive) to SCDT low <sup>1</sup>  |   |          | 100  |            | ms               |
|                   | Link disabled (Tx power down) to SCDT low <sup>6</sup>  |   |          |      | 250        |                  |
| T <sub>FSC</sub>  | Link enabled (DE active) to SCDT high <sup>1</sup>  |   |          | 25   |            | DE edges         |
| T <sub>ST</sub>   | ODCK high to even data output <sup>1</sup>  |   |          | 0.25 |            | R <sub>CIP</sub> |

- Notes:
- <sup>1</sup> Guaranteed by design.
  - <sup>2</sup> Jitter defined as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
  - <sup>3</sup> Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electrical Measurement Procedures*.
  - <sup>4</sup> The setup and hold timing for the data and controls relative to the ODCK rising edge (OCK\_INV=1) is by design the same as the falling edge timing.
  - <sup>5</sup> Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
  - <sup>6</sup> Measured when transmitter was powered down (see SiI/AN-0005 "PanelLink Basic Design/Application Guide," Section 2.4).

## Timing Diagrams

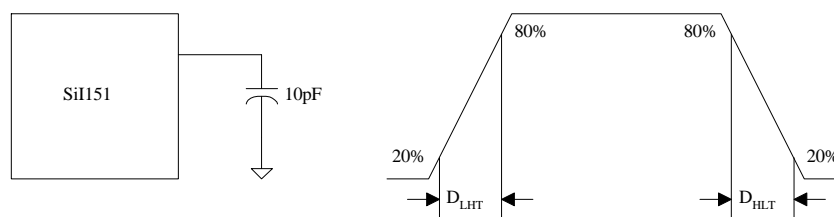


Figure 1. Digital Output Transition Times

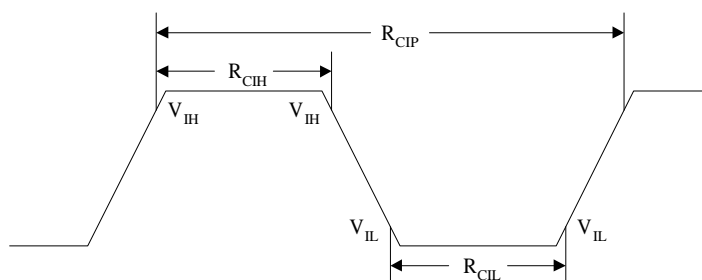


Figure 2. Receiver Clock Cycle/High/Low Times

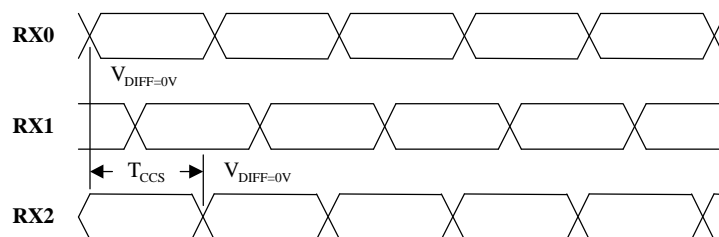


Figure 3. Channel-to-Channel Skew Timing

## Output Timing

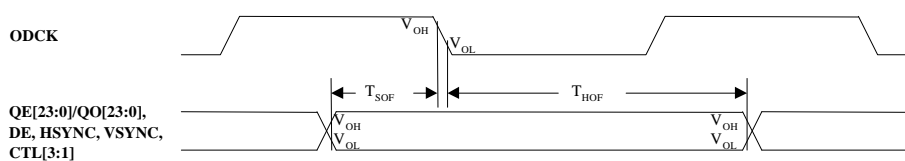


Figure 4. Output Data, DE, and Control Signals Setup/Hold Times to ODCCK Falling Edge

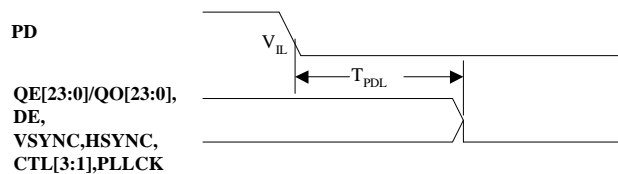


Figure 5. Output Signals Disabled Timing from PD Active

## Output Timing (continued)

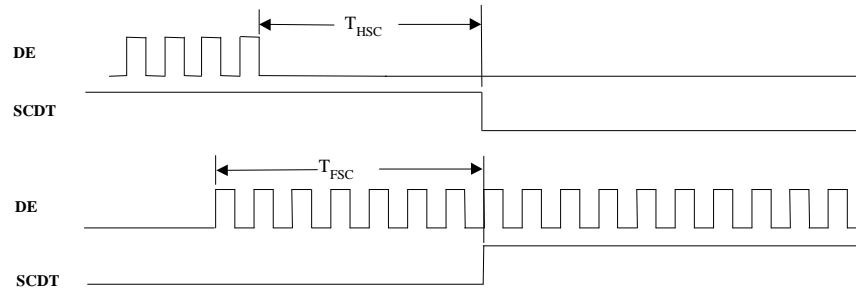


Figure 6. SCDT Timing from DE Inactive/Active

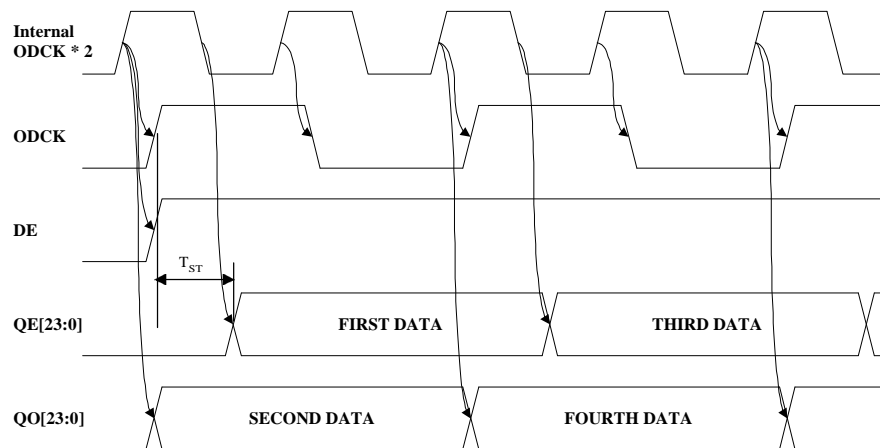


Figure 7. TFT 2-Pixels/Clock Staggered Output Timing Diagram

## Output Pin Description

| Pin Name | Pin #                  | Type | Description  |
|----------|------------------------|------|--|
| QE23-QE0 | See SiI151 Pin Diagram | Out  | Output Even Data[23:0] corresponds to 24-bit pixel data for 1-pixel/clock input mode and to the first 24-bit pixel data for 2-pixels/clock mode.<br>Output data is synchronized with output data clock (ODCK).<br>Refer to the TFT and DSTN Signal Mapping application notes (SiI/AN-0007-A and SiI/AN-0008-A) which tabulates the relationship between the input data to the transmitter and output data from the receiver.<br>A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.    |
| QO23-QO0 | See SiI151 Pin Diagram | Out  | Output Odd Data[23:0] corresponds to the second 24-bit pixel data for 2-pixels/clock mode. During 1-pixel/clock mode, these outputs are driven low.<br>Output data is synchronized with output data clock (ODCK).<br>Refer to the TFT and DSTN Signal Mapping application notes (SiI/AN-0007-A and SiI/AN-0008-A) which tabulates the relationship between the input data to the transmitter and output data from the receiver.<br>A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. |
| ODCK     | 44                     | Out  | Output Data Clock. A low level on PD or PDO will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground.   |
| DE       | 46                     | Out  | Output Data Enable. This signal qualifies the active data area. A low level on PD or PDO will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground.  |
| HSYNC    | 48                     | Out  | Horizontal Sync input control signal.  |
| VSYNC    | 47                     | Out  | Vertical Sync input control signal.  |
| CTL1     | 40                     | Out  | General output control signal 1. This output is <b>not</b> powered down by PDO.  |
| CTL2     | 41                     | Out  | General output control signal 2.   |
| CTL3     | 42                     | Out  | General output control signal 3.<br>A low level on PD or PDO will put the output drivers (except CTL1 by PDO) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.   |

**Configuration Pin Description**

| Pin Name | Pin # | Type | Description  |
|----------|-------|------|--|
| OCK_INV  | 100   | In   | ODCK Polarity. A low level selects normal ODCK output. A high level (3.3V) selects inverted ODCK output. All other outputs signals are not affected by this pin. They will maintain the same timing no matter the setting of OCK_INV pin.  |
| PIXS     | 4     | In   | Pixel Select. A low level indicates one pixel (up to 24-bits) per clock mode using QE[23:0]. A high level (3.3V) indicates two pixels (up to 48-bits) per clock mode using QE[23:0] for first pixel and QO[23:0] for second pixel.   |
| DFO      | 1     | In   | Output Data Format. This pin controls clock output format. A low level indicates that ODCK runs continuously for TFT panel support. A high level indicates that ODCK is stopped (LOW) when DE is low for DSTN panel support. Refer to the TFT and/or DSTN Signal Mapping application notes (SiI/AN-0007-A and SiI/AN-0008-A) for a table on TFT or DSTN panel support. |
| STAG_OUT | 7     | In   | A high level selects normal simultaneous outputs on all odd and even data lines. A low level selects staggered output drive. This function is only available in 2-pixels per clock mode.   |
| ST       | 3     | In   | Output Drive. A high level selects HIGH output drive strength. A low level selects LOW output drive strength.  |

**Power Management Pin Description**

| Pin Name | Pin # | Type | Description   |
|----------|-------|------|---|
| SCDT     | 8     | Out  | Sync Detect. A high level is outputted when DE is actively toggling indicating that the link is alive. A low level is outputted when DE is inactive, indicating the link is down. Can be connected to PDO to power down the outputs when DE is not detected. The SCDT output itself, however, remains in the active mode at all times.  |
| PDO      | 9     | In   | Output Driver Power Down (active low). A high level indicates normal operation. A low level puts all the output drivers only (except SCDT and CTL1) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. PDO is a sub-set of the PD description. The chip is not in power-down mode with this pin.<br>There is an internal pull-up resistor that defaults the chip to normal operation if left unconnected. SCDT and CTL1 are not tri-stated by this pin. |
| PD       | 2     | In   | Power Down (active low). A high level (3.3V) indicates normal operation and a low level indicates power down mode. During power down mode, all output buffers are disabled and brought low, all analog logic is powered down, and all inputs are disabled.  |

**Differential Signal Data Pin Description**

| Pin Name | Pin # | Type   | Description   |
|----------|-------|--------|---|
| RX0+     | 90    | Analog | TMDS Low Voltage Differential Signal input data pairs.  |
| RX0-     | 91    | Analog |   |
| RX1+     | 85    | Analog |   |
| RX1-     | 86    | Analog |   |
| RX2+     | 80    | Analog |   |
| RX2-     | 81    | Analog | TMDS Low Voltage Differential Signal input data pairs.  |
| RXC+     | 93    | Analog |   |
| RXC-     | 94    | Analog | Impedance Matching Control. Resistor value should be ten times the characteristic impedance of the cable. In the common case of 50Ω transmission line, an external 500Ω resistor must be connected between AVCC and this pin. |
| EXT_RES  | 96    | Analog |   |

**Reserved Pin Description**

| Pin Name | Pin # | Type | Description                             |
|----------|-------|------|---|
| RESERVED | 99    | In   | Must be tied high for normal operation. |

**Power and Ground Pin Description**

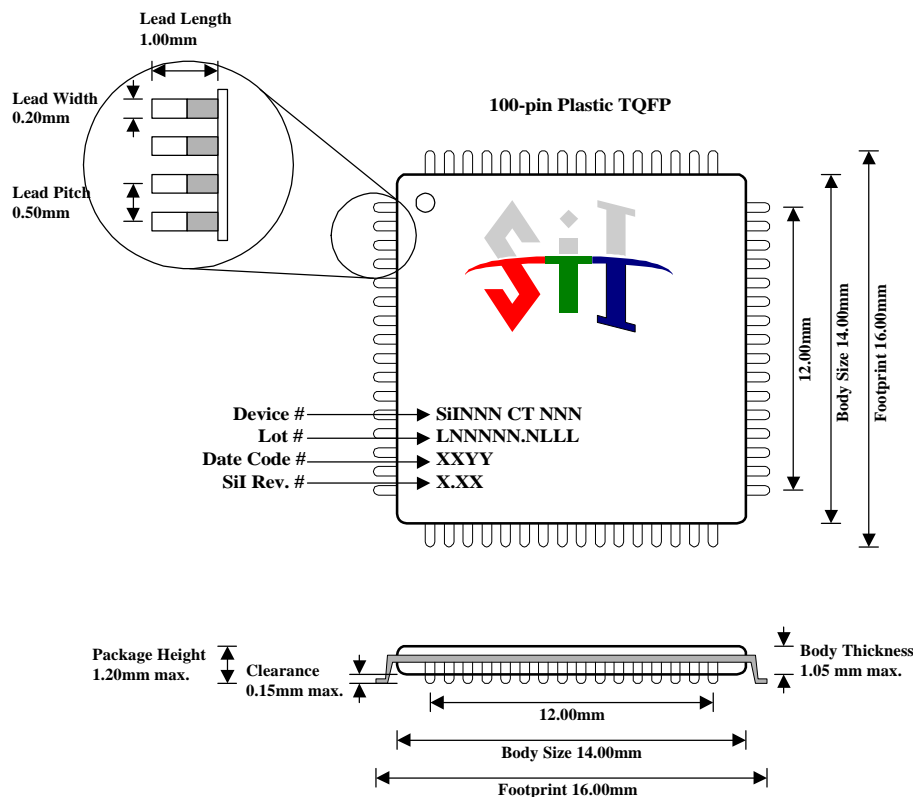
| Pin Name | Pin #          | Type   | Description                            |
|----------|----------------|--------|--|
| VCC      | 6,38,67        | Power  | Digital Core VCC, must be set to 3.3V. |
| GND      | 5,39,68        | Ground | Digital Core GND.                      |
| OVCC     | 18,29,43,57,78 | Power  | Output VCC, must be set to 3.3V.       |
| OGND     | 19,28,45,58,76 | Ground | Output GND.                            |
| AVCC     | 82,84,88,95    | Power  | Analog VCC must be set to 3.3V.        |
| AGND     | 79,83,87,89,92 | Ground | Analog GND.                            |
| PVCC     | 97             | Power  | PLL Analog VCC must be set to 3.3V.    |
| PGND     | 98             | Ground | PLL Analog GND.                        |

**Application Information**

To obtain the most updated Application Notes and other useful information for your design application, please visit the Silicon Image web site at [www.siimage.com](http://www.siimage.com), or contact your local Silicon Image sales office.

## Package Dimensions

100-pin TQFP Package Dimensions



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## Ordering Information

Part Number: SiI151CT100

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