HIGH-PRECISION VOLTAGE DETECTOR WITH A BUILT-IN DELAY CIRCUIT

S-801 Series

The S-801 Series is a series of high-precision voltage detectors with a built-in delay time generator of fixed time developed using CMOS process. The detection voltage is fixed internally, with an accuracy of ±2.0 %. Internal oscillator and counter timer can delay the release signal without external parts. Three delay times 50 ms, 100 ms, and 200 ms are available. Two output forms, Nch open-drain and CMOS output, are available.

■ Features

- Ultra-low current consumption 1.3 μA typ. (at V_{DD}=3.5 V)
- High-precision detection voltage ±2.0%
- Hysteresis width 60 mV typ.
- Three delay times A series: 50 ms typ.
  B series: 100 ms typ.
  C series: 200 ms typ.
- ON/OFF switch of delay time (DS pin)
- Operating voltage range
  0.95 V to 10.0 V
- Detection voltage
  2.2 V to 6.0 V (0.1 V step)
- Output form
  Active low Nch open-drain or active low CMOS output

■ Packages

- 5-Pin SOT-23-5 (Package drawing code: MP005-A)
- 4-Pin SNB(B) (Package drawing code: BB004-A)

■ Applications

- Power monitor for portable equipment such as notebook computers, digital cameras, PDA, and cellular phones.
- Constant voltage power monitor for cameras, video equipment and communication devices.
- Power monitor for microcomputers and reset for CPUs.

■ Block Diagrams

(1) Active low Nch open-drain

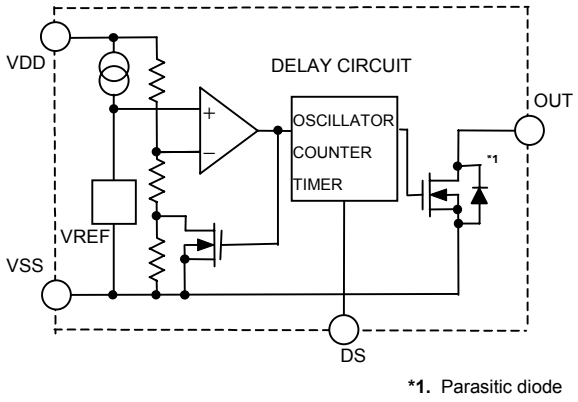


Figure 1

(2) Active low CMOS output

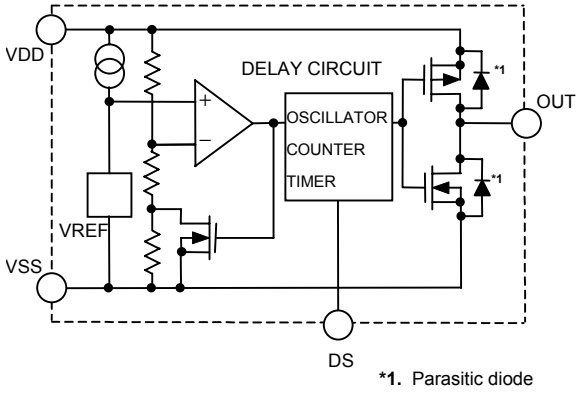


Figure 2

■ Selection Guide

1. Product Name

S-801xx x x xx - xxx - Tx

- Directions of the IC in tape form[*1]
  - T2: SOT-23-5
  - TF: 4-Pin SNB(B)
- Product code (abbreviation)[*2]
- Package code (abbreviation)
  - MC: SOT-23-5
  - BB: 4-Pin SNB(B)
- Output form
  - N: Nch open-drain (active low output)
  - L: CMOS (active low output)
- Delay time
  - A: 50 ms typ.
  - B: 100 ms typ.
  - C: 200 ms typ.
- Detection voltage (Detection voltage × 10)
  - (e.g. “22” shows that the detection voltage is 2.2 V.)

***1**. Please refer taping drawings at the end this book for directions of this IC in tape form.
TF and T2 are the standards.
***2**. Please refer the “Product name list” for product code.

2. Product Name List

2-1. SOT-23-5

Table 1

SII will line up shaded products in the table, contact our sales office for detail. (1/3)

Detection voltage range	Delay time	Nch Open-Drain (Low)	CMOS Output (Low)
2.2 V ±2.0%	50 ms typ.	S-80122ANMC-JCH-T2	S-80122ALMC-JAH-T2
	100 ms typ.	S-80122BNMC-JGH-T2	S-80122BLMC-JEH-T2
	200 ms typ.	S-80122CNMC-JKH-T2	S-80122CLMC-JIH-T2
2.3 V ±2.0%	50 ms typ.	S-80123ANMC-JCI-T2	S-80123ALMC-JAI-T2
	100 ms typ.	S-80123BNMC-JGI-T2	S-80123BLMC-JEI-T2
	200 ms typ.	S-80123CNMC-JKI-T2	S-80123CLMC-JII-T2
2.4 V ±2.0%	50 ms typ.	S-80124ANMC-JCJ-T2	S-80124ALMC-JAJ-T2
	100 ms typ.	S-80124BNMC-JGJ-T2	S-80124BLMC-JEJ-T2
	200 ms typ.	S-80124CNMC-JKJ-T2	S-80124CLMC-JIJ-T2
2.5 V ±2.0%	50 ms typ.	S-80125ANMC-JCK-T2	S-80125ALMC-JAK-T2
	100 ms typ.	S-80125BNMC-JGK-T2	S-80125BLMC-JEK-T2
	200 ms typ.	S-80125CNMC-JKK-T2	S-80125CLMC-JIK-T2
2.6 V ±2.0%	50 ms typ.	S-80126ANMC-JCL-T2	S-80126ALMC-JAL-T2
	100 ms typ.	S-80126BNMC-JGL-T2	S-80126BLMC-JEL-T2
	200 ms typ.	S-80126CNMC-JKL-T2	S-80126CLMC-JIL-T2
2.7 V ±2.0%	50 ms typ.	S-80127ANMC-JCM-T2	S-80127ALMC-JAM-T2
	100 ms typ.	S-80127BNMC-JGM-T2	S-80127BLMC-JEM-T2
	200 ms typ.	S-80127CNMC-JKM-T2	S-80127CLMC-JIM-T2
2.8 V ±2.0%	50 ms typ.	S-80128ANMC-JCN-T2	S-80128ALMC-JAN-T2
	100 ms typ.	S-80128BNMC-JGN-T2	S-80128BLMC-JEN-T2
	200 ms typ.	S-80128CNMC-JKN-T2	S-80128CLMC-JIN-T2
2.9 V ±2.0%	50 ms typ.	S-80129ANMC-JCO-T2	S-80129ALMC-JAO-T2
	100 ms typ.	S-80129BNMC-JGO-T2	S-80129BLMC-JEO-T2
	200 ms typ.	S-80129CNMC-JKO-T2	S-80129CLMC-JIO-T2
3.0 V ±2.0%	50 ms typ.	S-80130ANMC-JCP-T2	S-80130ALMC-JAP-T2
	100 ms typ.	S-80130BNMC-JGP-T2	S-80130BLMC-JEP-T2
	200 ms typ.	S-80130CNMC-JKP-T2	S-80130CLMC-JIP-T2
3.1 V ±2.0%	50 ms typ.	S-80131ANMC-JCQ-T2	S-80131ALMC-JAQ-T2
	100 ms typ.	S-80131BNMC-JGQ-T2	S-80131BLMC-JEQ-T2
	200 ms typ.	S-80131CNMC-JKQ-T2	S-80131CLMC-JIQ-T2
3.2 V ±2.0%	50 ms typ.	S-80132ANMC-JCR-T2	S-80132ALMC-JAR-T2
	100 ms typ.	S-80132BNMC-JGR-T2	S-80132BLMC-JER-T2
	200 ms typ.	S-80132CNMC-JKR-T2	S-80132CLMC-JIR-T2
3.3 V ±2.0%	50 ms typ.	S-80133ANMC-JCS-T2	S-80133ALMC-JAS-T2
	100 ms typ.	S-80133BNMC-JGS-T2	S-80133BLMC-JES-T2
	200 ms typ.	S-80133CNMC-JKS-T2	S-80133CLMC-JIS-T2
3.4 V ±2.0%	50 ms typ.	S-80134ANMC-JCT-T2	S-80134ALMC-JAT-T2
	100 ms typ.	S-80134BNMC-JGT-T2	S-80134BLMC-JET-T2
	200 ms typ.	S-80134CNMC-JKT-T2	S-80134CLMC-JIT-T2
3.5 V ±2.0%	50 ms typ.	S-80135ANMC-JCU-T2	S-80135ALMC-JAU-T2
	100 ms typ.	S-80135BNMC-JGU-T2	S-80135BLMC-JEU-T2
	200 ms typ.	S-80135CNMC-JKU-T2	S-80135CLMC-JIU-T2
3.6 V ±2.0%	50 ms typ.	S-80136ANMC-JCV-T2	S-80136ALMC-JAV-T2
	100 ms typ.	S-80136BNMC-JGV-T2	S-80136BLMC-JEV-T2
	200 ms typ.	S-80136CNMC-JKV-T2	S-80136CLMC-JIV-T2

Table 1 (Continued from page3.)

(2/3)

Detection voltage range	Delay time	Nch Open-Drain (Low)	CMOS Output (Low)
3.7 V ±2.0%	50 ms typ.	S-80137ANMC-JCW-T2	S-80137ALMC-JAW-T2
	100 ms typ.	S-80137BNMC-JGW-T2	S-80137BLMC-JEW-T2
	200 ms typ.	S-80137CNMC-JKW-T2	S-80137CLMC-JIW-T2
3.8 V ±2.0%	50 ms typ.	S-80138ANMC-JCX-T2	S-80138ALMC-JAX-T2
	100 ms typ.	S-80138BNMC-JGX-T2	S-80138BLMC-JEX-T2
	200 ms typ.	S-80138CNMC-JKX-T2	S-80138CLMC-JIX-T2
3.9 V ±2.0%	50 ms typ.	S-80139ANMC-JCY-T2	S-80139ALMC-JAY-T2
	100 ms typ.	S-80139BNMC-JGY-T2	S-80139BLMC-JEY-T2
	200 ms typ.	S-80139CNMC-JKY-T2	S-80139CLMC-JIY-T2
4.0 V ±2.0%	50 ms typ.	S-80140ANMC-JCZ-T2	S-80140ALMC-JAZ-T2
	100 ms typ.	S-80140BNMC-JGZ-T2	S-80140BLMC-JEZ-T2
	200 ms typ.	S-80140CNMC-JKZ-T2	S-80140CLMC-JIZ-T2
4.1 V ±2.0%	50 ms typ.	S-80141ANMC-JC2-T2	S-80141ALMC-JA2-T2
	100 ms typ.	S-80141BNMC-JG2-T2	S-80141BLMC-JE2-T2
	200 ms typ.	S-80141CNMC-JK2-T2	S-80141CLMC-JI2-T2
4.2 V ±2.0%	50 ms typ.	S-80142ANMC-JC3-T2	S-80142ALMC-JA3-T2
	100 ms typ.	S-80142BNMC-JG3-T2	S-80142BLMC-JE3-T2
	200 ms typ.	S-80142CNMC-JK3-T2	S-80142CLMC-JI3-T2
4.3 V ±2.0%	50 ms typ.	S-80143ANMC-JC4-T2	S-80143ALMC-JA4-T2
	100 ms typ.	S-80143BNMC-JG4-T2	S-80143BLMC-JE4-T2
	200 ms typ.	S-80143CNMC-JK4-T2	S-80143CLMC-JI4-T2
4.4 V ±2.0%	50 ms typ.	S-80144ANMC-JC5-T2	S-80144ALMC-JA5-T2
	100 ms typ.	S-80144BNMC-JG5-T2	S-80144BLMC-JE5-T2
	200 ms typ.	S-80144CNMC-JK5-T2	S-80144CLMC-JI5-T2
4.5 V ±2.0%	50 ms typ.	S-80145ANMC-JC6-T2	S-80145ALMC-JA6-T2
	100 ms typ.	S-80145BNMC-JG6-T2	S-80145BLMC-JE6-T2
	200 ms typ.	S-80145CNMC-JK6-T2	S-80145CLMC-JI6-T2
4.6 V ±2.0%	50 ms typ.	S-80146ANMC-JC7-T2	S-80146ALMC-JA7-T2
	100 ms typ.	S-80146BNMC-JG7-T2	S-80146BLMC-JE7-T2
	200 ms typ.	S-80146CNMC-JK7-T2	S-80146CLMC-JI7-T2
4.7 V ±2.0%	50 ms typ.	S-80147ANMC-JC8-T2	S-80147ALMC-JA8-T2
	100 ms typ.	S-80147BNMC-JG8-T2	S-80147BLMC-JE8-T2
	200 ms typ.	S-80147CNMC-JK8-T2	S-80147CLMC-JI8-T2
4.8 V ±2.0%	50 ms typ.	S-80148ANMC-JC9-T2	S-80148ALMC-JA9-T2
	100 ms typ.	S-80148BNMC-JG9-T2	S-80148BLMC-JE9-T2
	200 ms typ.	S-80148CNMC-JK9-T2	S-80148CLMC-JI9-T2
4.9 V ±2.0%	50 ms typ.	S-80149ANMC-JDA-T2	S-80149ALMC-JBA-T2
	100 ms typ.	S-80149BNMC-JHA-T2	S-80149BLMC-JFA-T2
	200 ms typ.	S-80149CNMC-JLA-T2	S-80149CLMC-JJA-T2
5.0 V ±2.0%	50 ms typ.	S-80150ANMC-JDB-T2	S-80150ALMC-JBB-T2
	100 ms typ.	S-80150BNMC-JHB-T2	S-80150BLMC-JFB-T2
	200 ms typ.	S-80150CNMC-JLB-T2	S-80150CLMC-JJB-T2
5.1 V ±2.0%	50 ms typ.	S-80151ANMC-JDC-T2	S-80151ALMC-JBC-T2
	100 ms typ.	S-80151BNMC-JHC-T2	S-80151BLMC-JFC-T2
	200 ms typ.	S-80151CNMC-JLC-T2	S-80151CLMC-JJC-T2
5.2 V ±2.0%	50 ms typ.	S-80152ANMC-JDD-T2	S-80152ALMC-JBD-T2
	100 ms typ.	S-80152BNMC-JHD-T2	S-80152BLMC-JFD-T2
	200 ms typ.	S-80152CNMC-JLD-T2	S-80152CLMC-JJD-T2

Table 1 (Continued from page4.)

(3/3)

Detection voltage range	Delay time	Nch Open-Drain (Low)	CMOS Output (Low)
5.3 V ±2.0%	50 ms typ.	S-80153ANMC-JDE-T2	S-80153ALMC-JBE-T2
	100 ms typ.	S-80153BNMC-JHE-T2	S-80153BLMC-JFE-T2
	200 ms typ.	S-80153CNMC-JLE-T2	S-80153CLMC-JJE-T2
5.4 V ±2.0%	50 ms typ.	S-80154ANMC-JDF-T2	S-80154ALMC-JBF-T2
	100 ms typ.	S-80154BNMC-JHF-T2	S-80154BLMC-JFF-T2
	200 ms typ.	S-80154CNMC-JLF-T2	S-80154CLMC-JJF-T2
5.5 V ±2.0%	50 ms typ.	S-80155ANMC-JDG-T2	S-80155ALMC-JBG-T2
	100 ms typ.	S-80155BNMC-JHG-T2	S-80155BLMC-JFG-T2
	200 ms typ.	S-80155CNMC-JLG-T2	S-80155CLMC-JJG-T2
5.6 V ±2.0%	50 ms typ.	S-80156ANMC-JDH-T2	S-80156ALMC-JBH-T2
	100 ms typ.	S-80156BNMC-JHH-T2	S-80156BLMC-JFH-T2
	200 ms typ.	S-80156CNMC-JLH-T2	S-80156CLMC-JJH-T2
5.7 V ±2.0%	50 ms typ.	S-80157ANMC-JDI-T2	S-80157ALMC-JBI-T2
	100 ms typ.	S-80157BNMC-JHI-T2	S-80157BLMC-JFI-T2
	200 ms typ.	S-80157CNMC-JLI-T2	S-80157CLMC-JJI-T2
5.8 V ±2.0%	50 ms typ.	S-80158ANMC-JDJ-T2	S-80158ALMC-JBJ-T2
	100 ms typ.	S-80158BNMC-JHJ-T2	S-80158BLMC-JFJ-T2
	200 ms typ.	S-80158CNMC-JLJ-T2	S-80158CLMC-JJJ-T2
5.9 V ±2.0%	50 ms typ.	S-80159ANMC-JDK-T2	S-80159ALMC-JBK-T2
	100 ms typ.	S-80159BNMC-JHK-T2	S-80159BLMC-JFK-T2
	200 ms typ.	S-80159CNMC-JLK-T2	S-80159CLMC-JJK-T2
6.0 V ±2.0%	50 ms typ.	S-80160ANMC-JDL-T2	S-80160ALMC-JBL-T2
	100 ms typ.	S-80160BNMC-JHL-T2	S-80160BLMC-JFL-T2
	200 ms typ.	S-80160CNMC-JLL-T2	S-80160CLMC-JJL-T2

2-2. 4-Pin SNB(B)

Table 2

Detection voltage range	Delay time	Nch Open-Drain (Low)	CMOS Output (Low)
2.2 V ±2.0%	50 ms typ.	—	S-80122ALBB-JAH-TF
	200 ms typ.	S-80122CNBB-JKH-TF	—
2.4 V ±2.0%	200 ms typ.	S-80124CNBB-JKJ-TF	—
2.5 V ±2.0%	50 ms typ.	—	S-80125ALBB-JAK-TF
2.7 V ±2.0%	100 ms typ.	S-80127BNBB-JGM-TF	S-80127BLBB-JEM-TF
	200 ms typ.	S-80127CNBB-JKM-TF	—
2.8 V ±2.0%	200 ms typ.	—	S-80128CLBB-JIN-TF
3.0 V ±2.0%	50 ms typ.	—	S-80130ALBB-JAP-TF
	200 ms typ.	S-80130CNBB-JKP-TF	—
4.0 V ±2.0%	200 ms typ.	S-80140CNBB-JKZ-TF	—
4.5 V ±2.0%	200 ms typ.	S-80145CNBB-JK6-TF	S-80145CLBB-JI6-TF

Remark Please contact the SII marketing department for products with an output voltage or delay time other than those specified above.

■ Pin Configurations

See the attached drawings for details of the package.

SOT-23-5
Top view

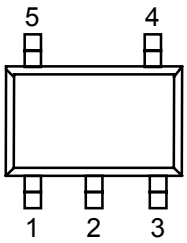


Figure 3

Table 3 Pin Description

No.	Symbol	Description
1	DS*1	ON/OFF switch for delay time
2	VSS	Ground pin
3	NC*2	non-connected
4	OUT	Voltage detection output pin
5	VDD	Voltage input pin

***1.** Refer to "2. Delay Circuit" in "■ Operation Description" for operation.
***2.** NC pin is electrically open.
Connecting this pin to VDD or VSS is allowed.

4-Pin SNB(B)
Top view

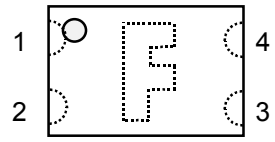


Figure 4

Table 4 Pin Description

No.	Symbol	Description
1	VSS	Ground pin
2	DS*1	ON/OFF switch for delay time
3	VDD	Voltage input pin
4	OUT	Voltage detection output pin

***1.** Refer to "2. Delay Circuit" in "■ Operation Description" for operation.

■ Absolute Maximum Ratings

Table 5

(Ta=25°C, unless otherwise specified)

Parameter		Symbol		Ratings	Unit
Power supply voltage		V_{DD}–V_{SS}		12	V
Output voltage	Nch open-drain	V_{OUT}		V_{SS}–0.3 to V_{SS}+12	V
	CMOS			V_{SS}–0.3 to V_{DD}+0.3	V
Output current		I_{OUT}		50	mA
Power dissipation		P_D	SOT-23-5	250	mW
			4-Pin SNB(B)	60	
Operating temperature		T_{opr}		–40 to +85	°C
Storage temperature		T_{stg}		–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Electrical Characteristics

Table 6

(Ta=25 °C, Unless otherwise specified)

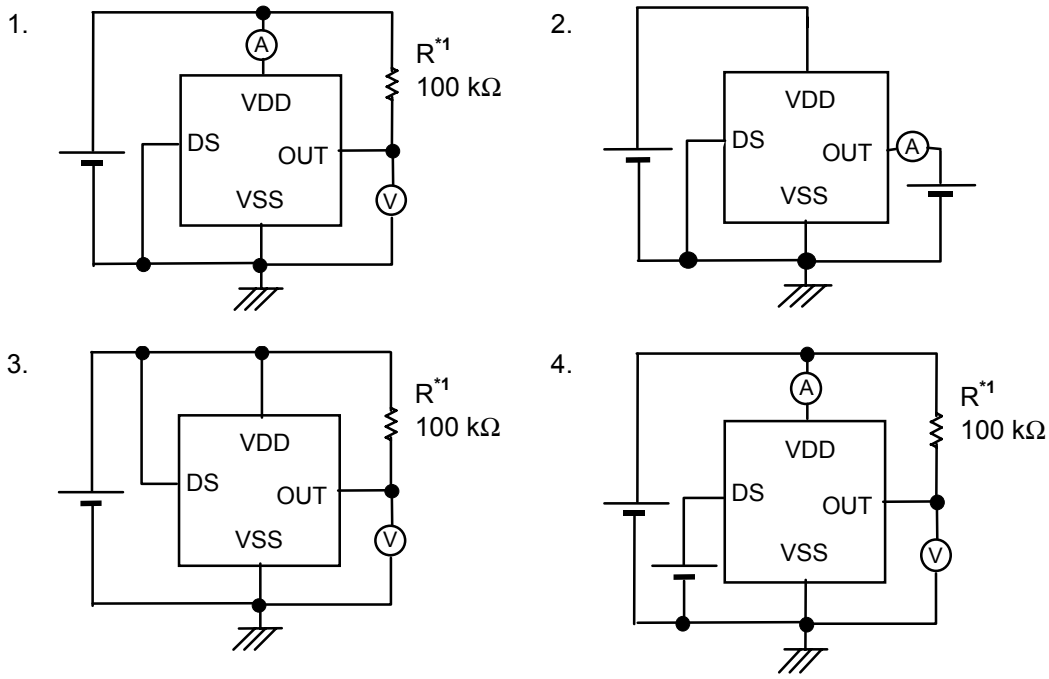
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units	Test circuit
Detection voltage	$-V_{DET}$	—		$-V_{DET}$ ×0.98	$-V_{DET}$	$-V_{DET}$ ×1.02	V	1
Hysteresis width	V_{HYS}	—		30	60	100	mV	
Operating voltage	V_{DD}	—		0.95	—	10.0	V	
Output current of output transistor	I_{OUT}	Nch V_{OUT}=0.5 V	V_{DD}=1.2 V S-80122 to 60	0.75	1.5	—	mA	2
			V_{DD}=2.4 V S-80127 to 60	3.0	6.0	—		
		Pch (applied for CMOS output products) $V_{DD}-V_{OUT}$=0.5 V	V_{DD}=4.8 V S-80122 to 39	1.0	2.0	—		
			V_{DD}=6.0 V S-80140 to 54	1.25	2.5	—		
			V_{DD}=8.4 V S-80155 to 60	1.5	3.0	—		
Leakage current of output transistor	I_{LEAK}	Nch (applied for Nch open-drain output products) V_{DD}=10.0 V, V_{OUT}=10.0 V		—	—	0.1	μA	
Temperature coefficient for detection voltage*1	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta=–40 °C to +85 °C		—	±120	±360	ppm/ °C	1
Delay time 1	t_{D1}	V_{DD}=$-V_{DET}$+1 V, DS pin: “L”	S-801xxAx	32.5	50	72.5	ms	
			S-801xxBx	65	100	145		
			S-801xxCx	130	200	290		
Delay time 2	t_{D2}	V_{DD}=$-V_{DET}$+1 V, DS pin: “H”		110	220	330	μs	3
Current consumption	I_{SS}	V_{DD}=3.5 V	S-80122 to 26	—	1.3	3.3	μA	1
		V_{DD}=4.5 V	S-80127 to 39	—	1.5	3.5		
		V_{DD}=6.5 V	S-80140 to 60	—	1.8	4.0		
Input voltage of DS pin	V_{SH}	V_{DD}=6.0 V		1.0	—	—	V	4
	V_{SL}	V_{DD}=6.0 V		—	—	0.3		

***1.** The detection voltage change by temperature (mV/°C) is calculated with the following formula:

$$\frac{\Delta -V_{DET}}{\Delta Ta}\,[\text{mV/°C}] = -V_{DET}(\text{Typ.})\,[\text{V}] \times \frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}\,[\text{ppm/°C}] \div 1000$$

- $\frac{\Delta -V_{DET}}{\Delta Ta}$ [mV/°C]: Detection voltage change by temperature
- $-V_{DET}$ (Typ.) [V]: Detection voltage
- $\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$ [ppm/°C]: Temperature coefficient for detection voltage

■ Test Circuits



***1.** R is unnecessary for CMOS output products.

Figure 5

■ Definition of Terms

1. Detection voltage ($-V_{DET}$)

Detection voltage ($-V_{DET}$) is a voltage at which the output turns to low. The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the minimum [($-V_{DET}$) min.] and the maximum [($-V_{DET}$) max.] is called the detection voltage range. (Refer to Figure 6)

Example: For the S-80122AN, the detection voltage lies in the range of $2.156 \leq (-V_{DET}) \leq 2.244$.
This means that some S-80122ANs have 2.156 V for $-V_{DET}$ and some have 2.244 V.

2. Release voltage ($+V_{DET}$)

Release voltage ($+V_{DET}$) is a voltage at which the output turns to high. The release voltage varies slightly among products of the same type. The variation of release voltages between the minimum [($+V_{DET}$) min.] and the maximum [($+V_{DET}$) max.] is called the release voltage range. (Refer to Figure 7)

Example: For the S-80122AN, the release voltage lies in the range of $2.186 \leq (+V_{DET}) \leq 2.344$.
This means that some S-80122ANs have 2.186 V for $+V_{DET}$ and some have 2.344 V.

Remark Although the detection voltage and release voltage overlap in the range of 2.186 V to 2.244 V, $+V_{DET}$ is always larger than $-V_{DET}$.

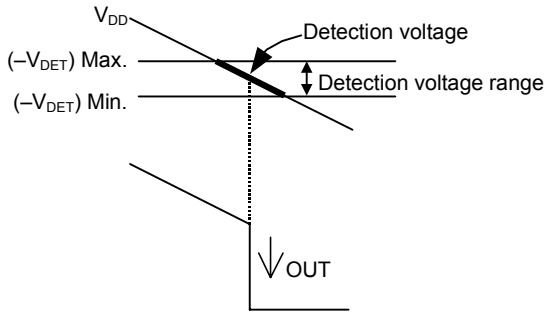


Figure 6 Detection Voltage

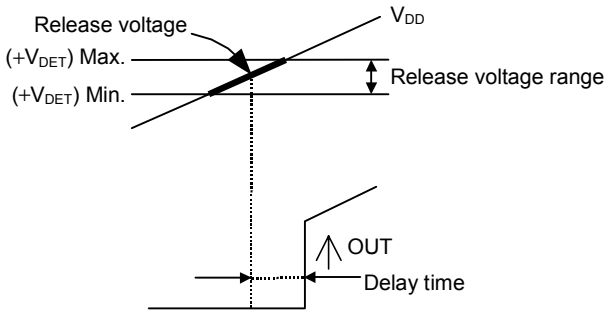


Figure 7 Release Voltage

3. Hysteresis width (V_{HYS})

Hysteresis width is the voltage difference between the detection voltage and the release voltage by giving a device hysteresis, trouble such as noise at the input is avoided. The existence of the hysteresis width avoids malfunction caused by noise on input signal.

4. Delay time (t_D)

Delay time is a time interval measured from the instant at which input voltage to the VDD pin exceeds the release voltage ($+V_{DET}$) to the point at which the output of the OUT pin inverts. The delay time is fixed in each series distinguished by A, B and C.

- S-801xxAx series: typ. 50 ms
- S-801xxBx series: typ. 100 ms
- S-801xxCx series: typ. 200 ms

The output of the OUT pin can be inverted in a short delay time t_{D2} by setting the DS pin high.

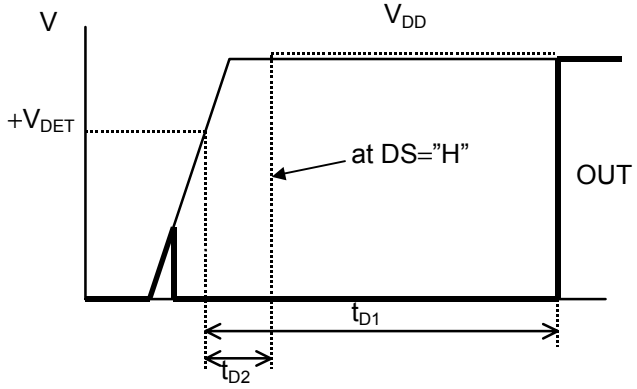


Figure 8

5. Short-circuit current

Short-circuit current refers to the current which flows instantaneously at the time of detection and release of a voltage detector. Short-circuit current flows at a frequency of 20 kHz during release delay time since the internal logic circuit operates.

6. Oscillation

In applications where a resistor is connected to the voltage detector input (Figure 9), taking a CMOS active low products for example, the short-circuit current which is generated when the output goes from low to high (release) causes a voltage drop equal to [short-circuit current] × [input resistance] across the resistor. When the input voltage falls below the detection voltage $-V_{DET}$ as a result, the output voltage goes to low level. In this state, the short-circuit current stops and its resultant voltage drop disappears, and the output goes from low to high. Short-circuit current is again generated, a voltage drop appears, and oscillation is induced by repeating the process.

An example for forbidden implementation: input voltage divider

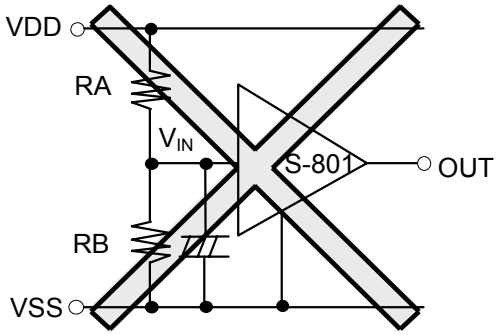
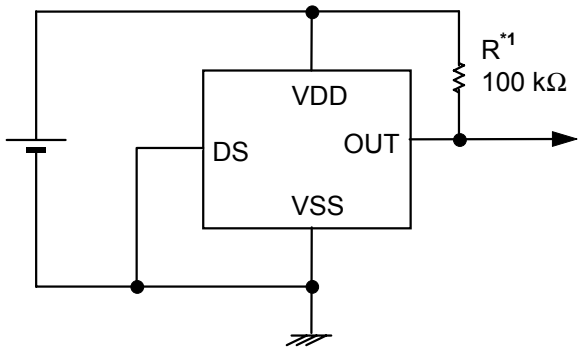


Figure 9 An example for forbidden implementation

■ Standard Circuit



***1.** R is unnecessary for CMOS output products.

Figure 10

■ Operation Description

1. Basic operation: In care of CMOS active low output

(1) When the power supply voltage V_{DD} is higher than the release voltage $+V_{DET}$, the Nch transistor is OFF and the Pch transistor is ON to provide V_{DD} (high) at the output. Since the Nch transistor N1 in Figure 11 is OFF, the comparator input voltage is (RB+RC) / (RA+RB+RC)×V_{DD}.

(2) When the V_{DD} goes below $+V_{DET}$, the output provides the V_{DD} level, as long as V_{DD} remains above the detection voltage $-V_{DET}$. When the V_{DD} falls below $-V_{DET}$ (point A in Figure 12), the Nch transistor becomes ON, the Pch transistor becomes OFF, and the V_{SS} level appears at the output. At this time the Nch transistor N1 in figure 11 becomes ON, the comparator input voltage is changed to RB / (RA+RB)×V_{DD}.

(3) When the V_{DD} falls below the minimum operating voltage, the output becomes undefined, or goes to V_{DD} when the output is pulled up to V_{DD}.

(4) The V_{SS} level appears when V_{DD} rises above the minimum operating voltage. The V_{SS} level still appears even when V_{DD} surpasses the $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

(5) When V_{DD} rises above $+V_{DET}$ (point B in Figure 12), the Nch transistor becomes OFF and the Pch transistor becomes ON to provide V_{DD} at the output. The V_{DD} at the OUT pin is delayed for t_D due to the delay circuit.

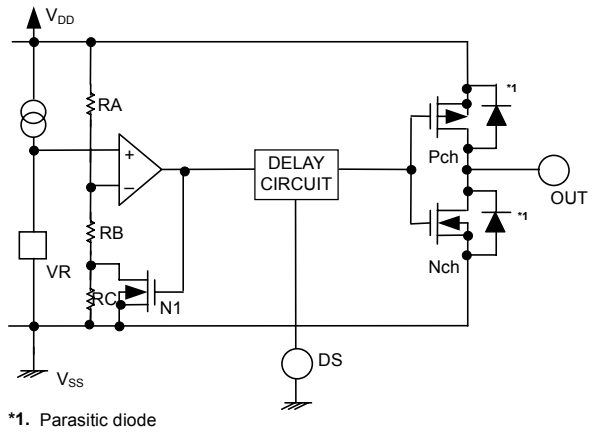


Figure 11 Operation 1

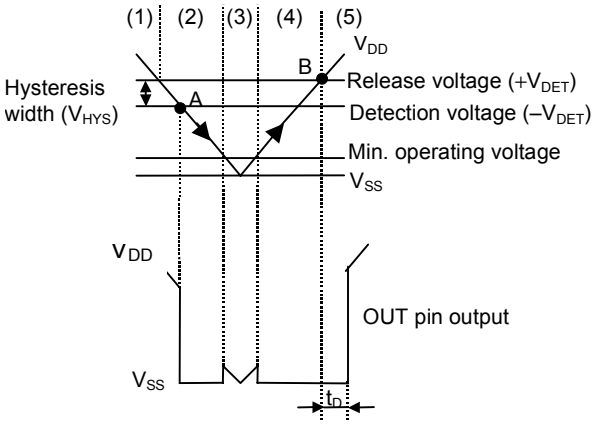


Figure 12 Operation 2

2. Delay circuit

(1) Delay time

The delay circuit delays the output signal from the time at which the power voltage V_{DD} exceeds the release voltage ($+V_{DET}$) when V_{DD} is turned on. The output signal is not delayed when the V_{DD} goes below the detection voltage ($-V_{DET}$). (Refer to Figure 12.)
The delay time (t_D) is a fixed value that is determined by a built-in oscillation circuit and counter.

(2) DS pin: ON/OFF switch for delay time

The DS pin should be connected to "
L" or "H". When the DS pin is "H", the output delay time becomes short since the output signal is taken from the middle of counter circuit. (Refer to "Delay time 2" in Table 8.)

3. Other characteristics

(1) Temperature dependence of detection voltage

The shaded parts in Figure 13 show the temperature dependence of the detection voltage.

Example: S-80122xxxx

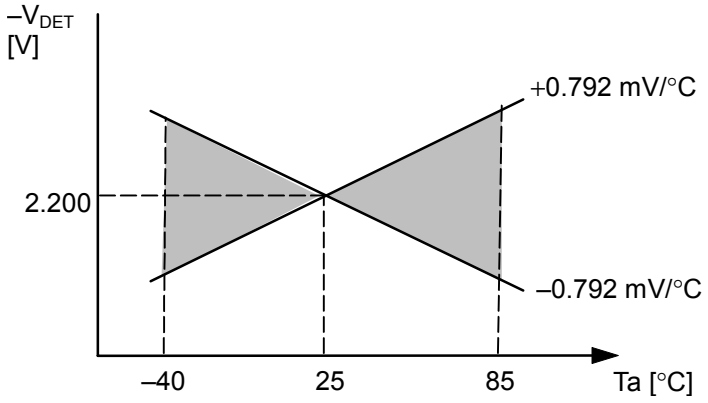


Figure 13 Temperature dependence of Detection Voltage

(2) Temperature dependence of release voltage

The temperature coefficient $\frac{\Delta + V_{DET}}{\Delta Ta}$ of the release voltage is calculated by the temperature coefficient $\frac{\Delta - V_{DET}}{\Delta Ta}$ of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

The temperature coefficients for the release voltage and the detection voltage have the same sign consequently.

(3) Temperature characteristics of hysteresis voltage

The temperature dependence of hysteresis voltage $\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}$ is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

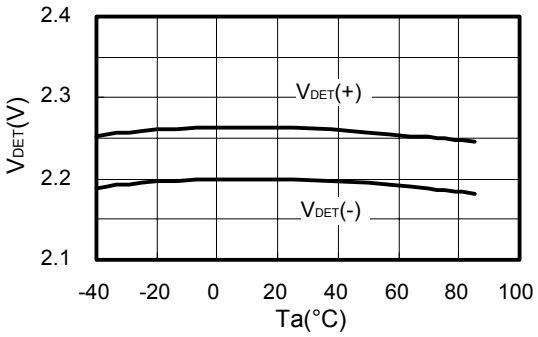
■ Precautions

- In CMOS output products of the S-801 Series, the short-circuit current flows at detection and release. If a high impedance is connected to the input, oscillation may occur due to the voltage drop by the short-circuit current during releasing.
- In the S-801 series products, the short-circuits current flows at a frequency of 20 kHz approximately during the delay time since the internal oscillator circuit and counter timer operate at voltage release. High impedance in the input may cause oscillation by the short-circuit current. When the input impedance is high, insert a capacitor between VDD pin and VSS pin to prevent oscillation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration.
  Seiko Instruments Inc. shall not bear any responsibility for the patents on the circuits described herein.

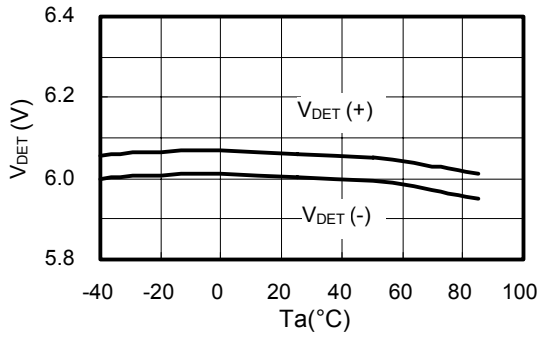
■ Characteristics (typical characteristics)

(1) Detection voltage (V_{DET}) - Temperature (Ta)

S-80122AL

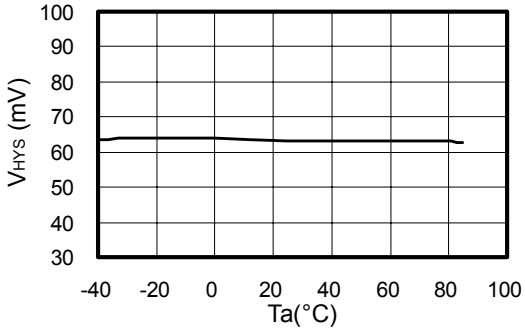


S-80160AL

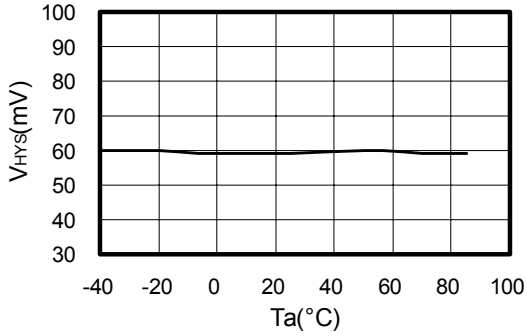


(2) Hysteresis voltage width (V_{HYS}) - Temperature (Ta)

S-80122AL

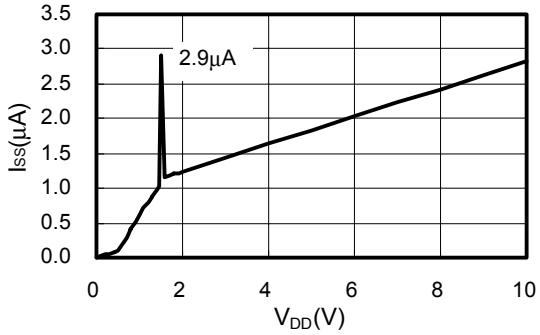


S-80160AL

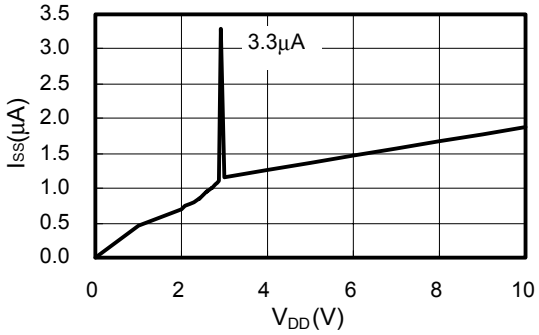


(3) Current consumption (I_{SS}) - Input voltage (V_{DD})

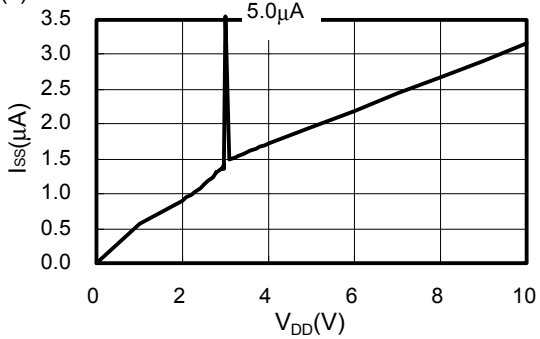
(a) S-80122AL Ta=25°C



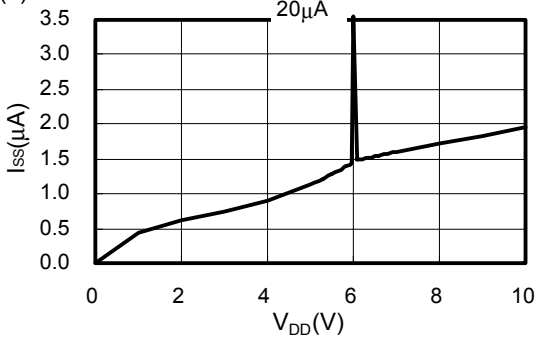
(b) S-80129AL Ta=25°C



(c) S-80130AL Ta=25°C

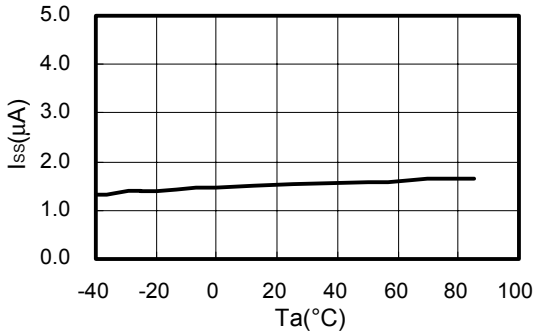


(d) S-80160AL Ta=25°C

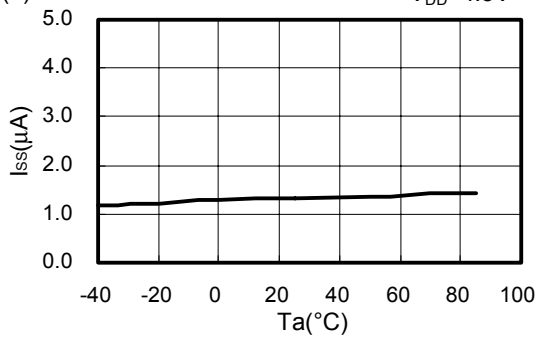


(4) Current consumption (I_{SS}) - Temperature (Ta)

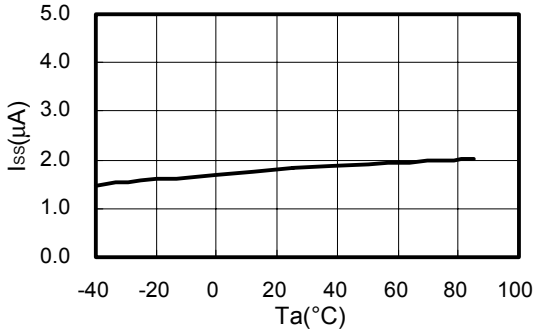
(a) S-80122AL V_{DD}=3.5V



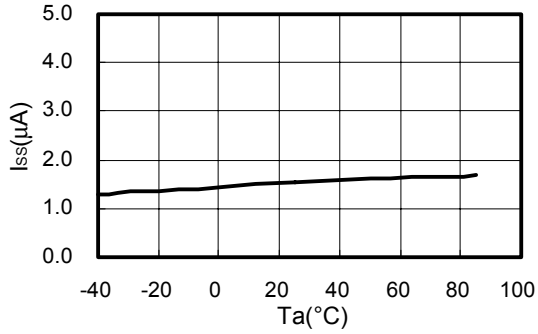
(b) S-80129AL V_{DD}=4.5V



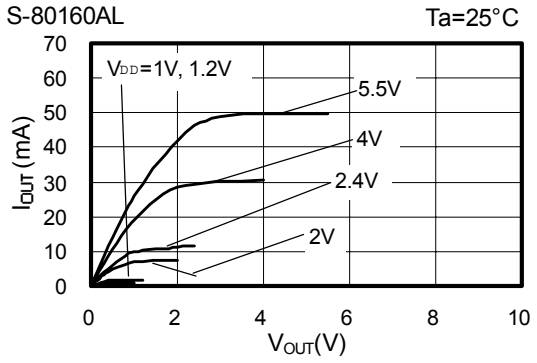
(c) S-80130AL V_{DD}=4.5V



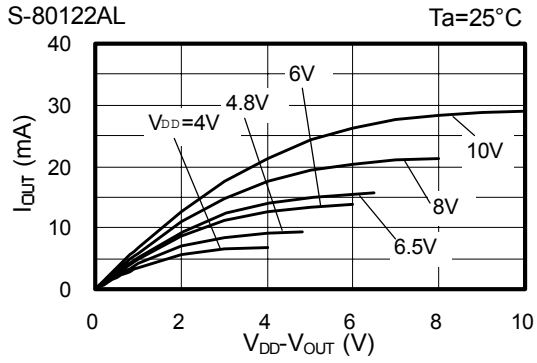
(d) S-80160AL V_{DD}=6.5V



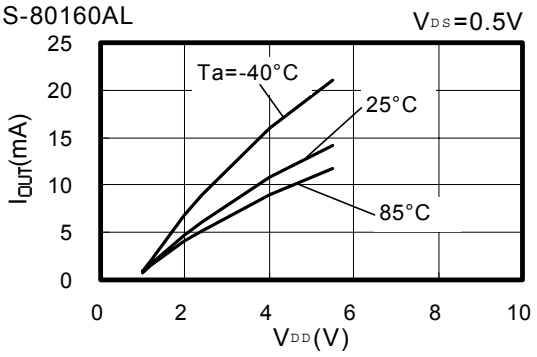
(5) Nch transistor output current (I_{OUT}) -V_{OUT}



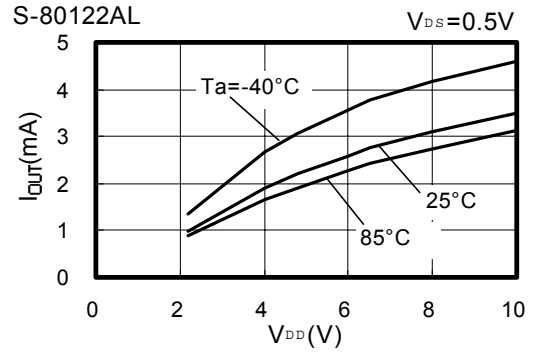
(6) Pch transistor output current (I_{OUT}) - (V_{DD}-V_{OUT})



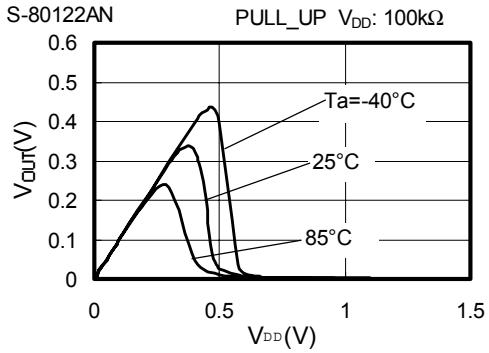
(7) Nch transistor output current (I_{OUT}) - Input voltage (V_{DD})



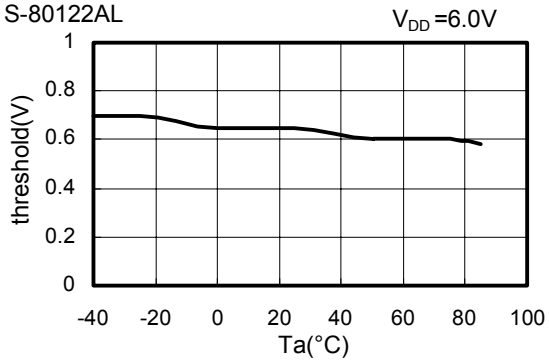
(8) Pch transistor output current(I_{OUT}) - Input voltage (V_{DD})



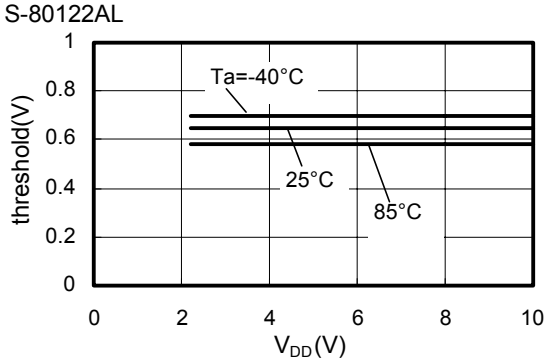
(9) Minimum operating voltage - Input voltage(V_{DD})



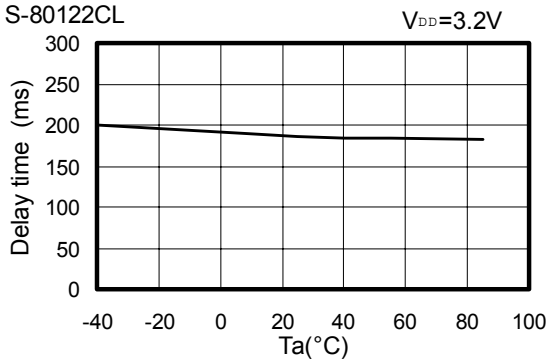
(10) Threshold voltage of DS pin - Temperature (Ta)

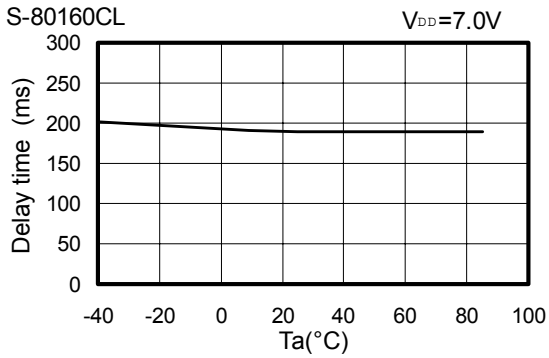


(11) Threshold voltage of DS pin - Input voltage (V_{DD})

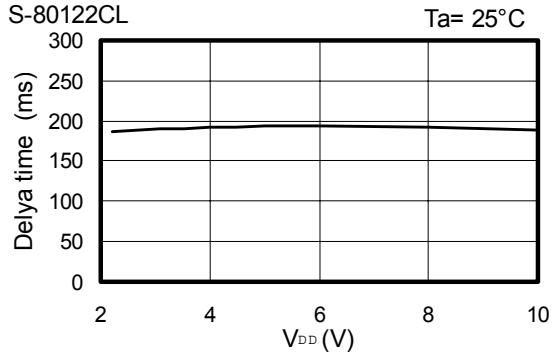


(12) Delay time 1 - Temperature (Ta)

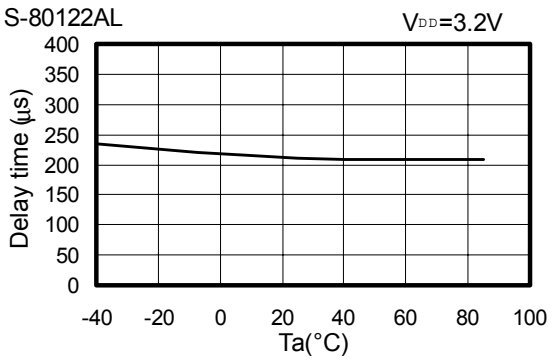


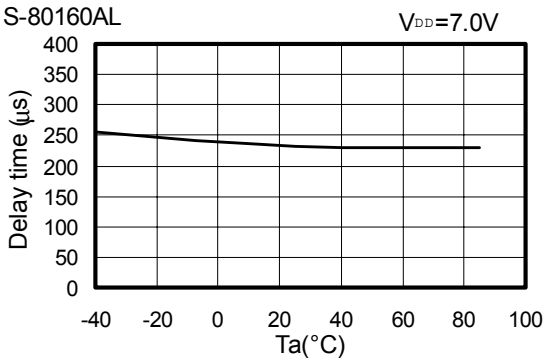


(13) Delay time 1 - Input voltage (V_{DD})

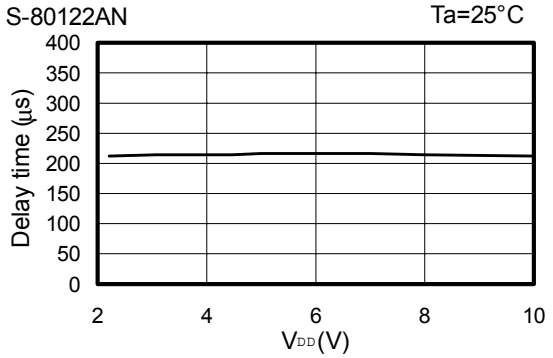


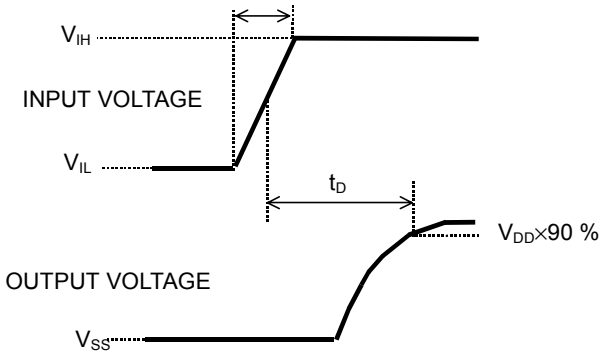
(14) Delay time 2 - Temperature (Ta)





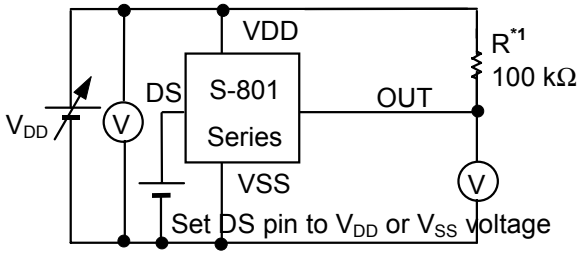
(15) Delay time 2 - Input voltage (V_{DD})





V_{IH}=10 V, V_{IL}=0.95 V

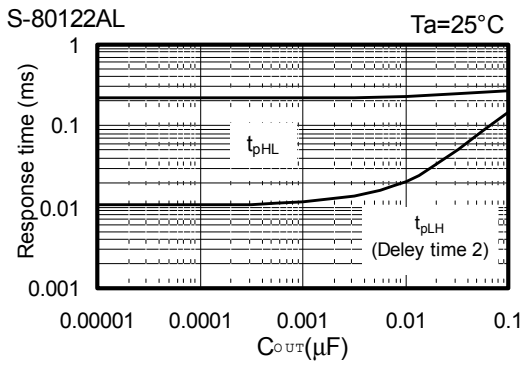
Figure 14 Measurment Condition for Delay Time

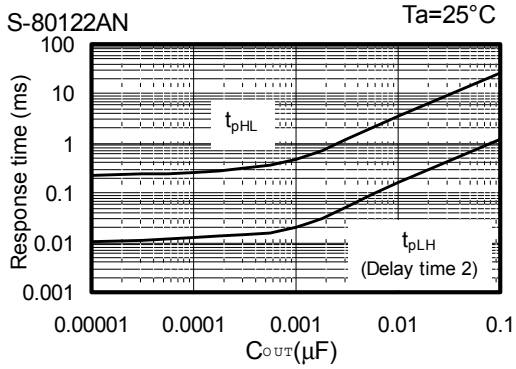


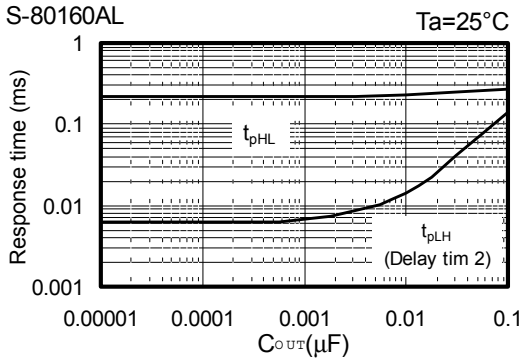
***1.** R is not necessary for CMOS output products.

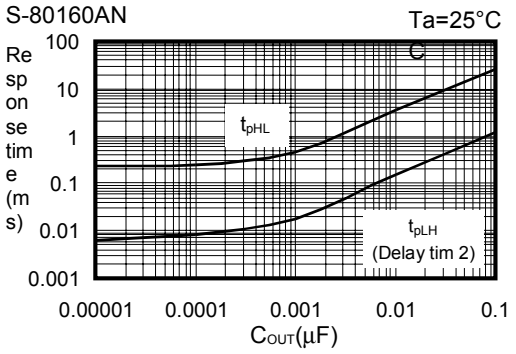
Figure 15 Measurment Circuit for Delay Time

(16) Response time - Load capacitor (C_{OUT})









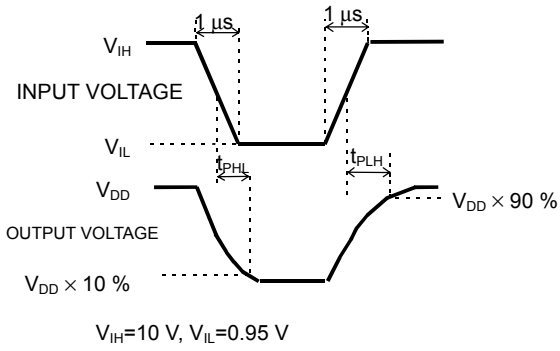
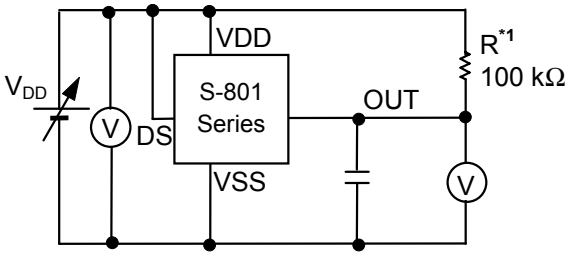


Figure 16 Measurment Condition for Response Time



***1.** R is not necessary for CMOS output

Figure 17 Measurment Circuit for Response

■ Application Circuit Examples

1. Microcomputer reset circuits

Reset circuits shown in Figures 18 and 19 can be easily constructed with the help of the S-801 series which has low operating voltage, a high-precision detection voltage, hysteresis, and a built-in delay circuit.

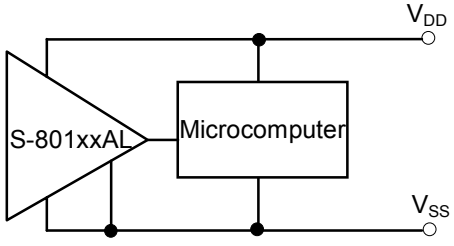
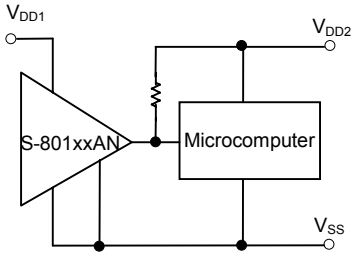


Figure 18 Reset Circuit (S-801xxAL)



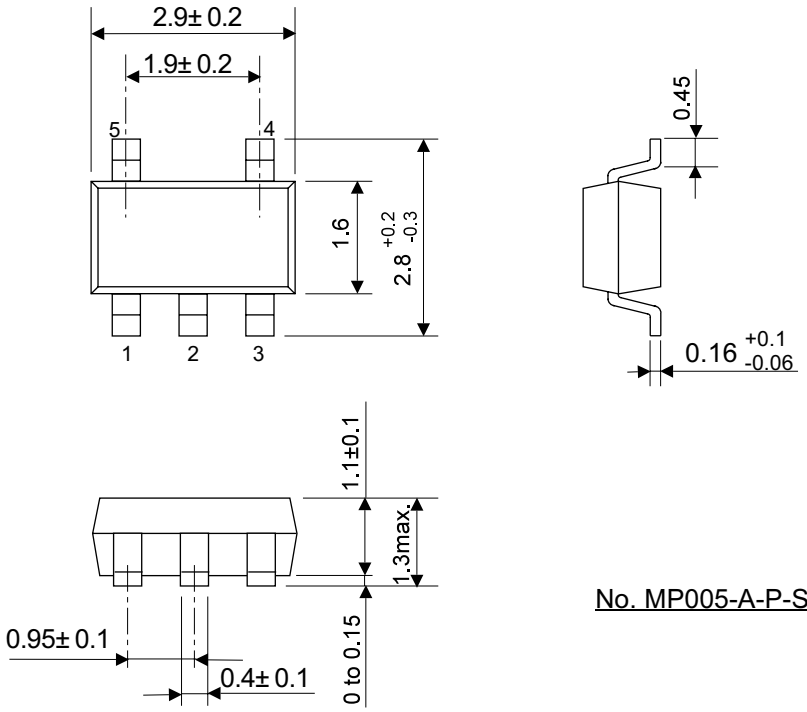
(Nch open-drain output products only)
Figure 19 Reset Circuit (S-801xxAN)

■ SOT-23-5

MP005-A Rev.2.0 021111

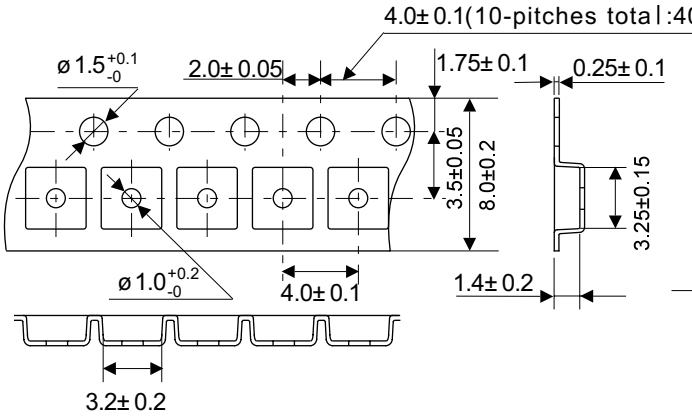
Unit : mm

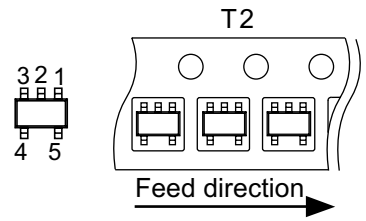
● Dimensions



No. MP005-A-P-SD-1.1

● Tape Specifications

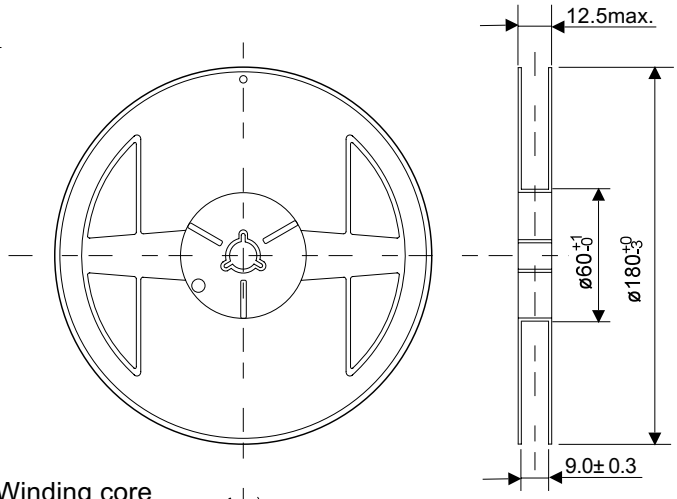




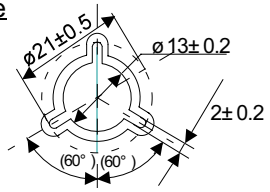
No. : MP005-A-C-SD-2.0

● Reel Specifications

1 reel holds 3000 ICs.



Winding core



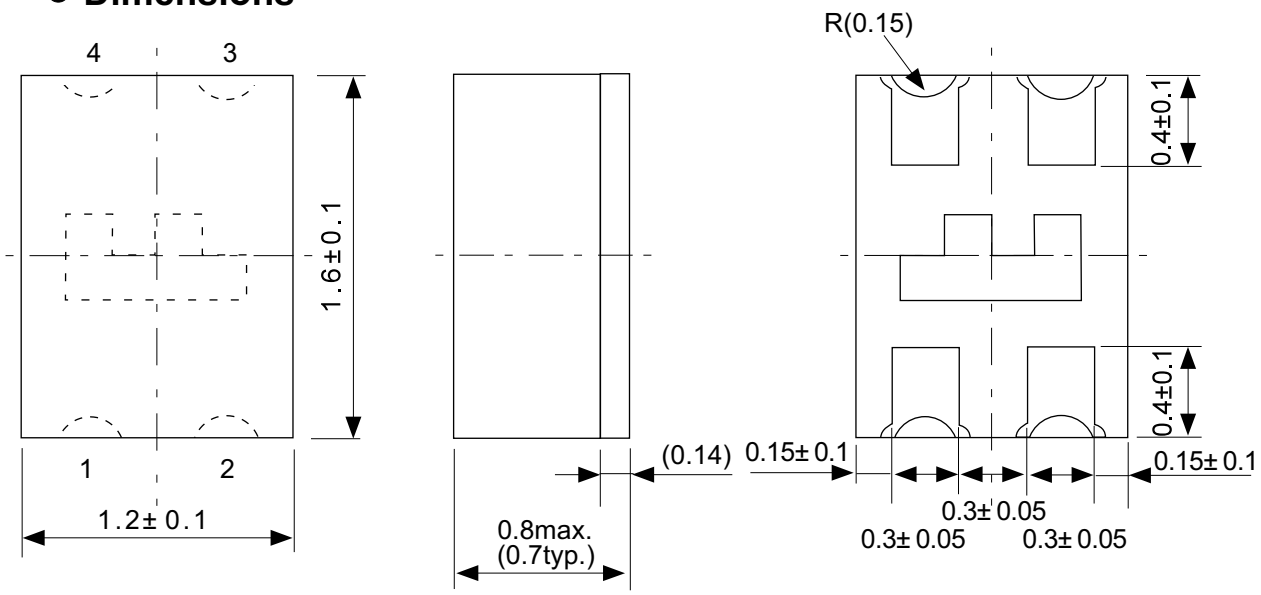
No. MP005-A-R-SD-1. 0

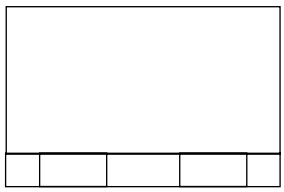
■ 4-Pin SNB(B) [SNB4B(1216)]

BB004-A 010801

Unit : mm

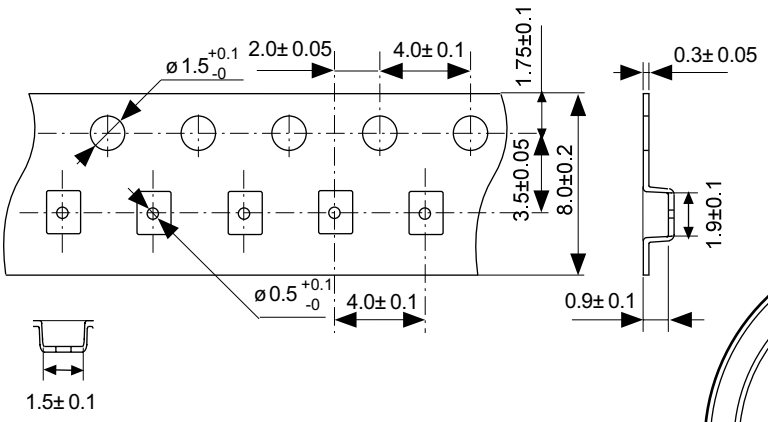
● Dimensions

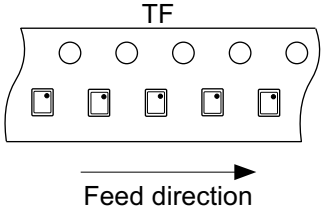




No. : BB004-A-P-SD-1.0

● Tape Specifications

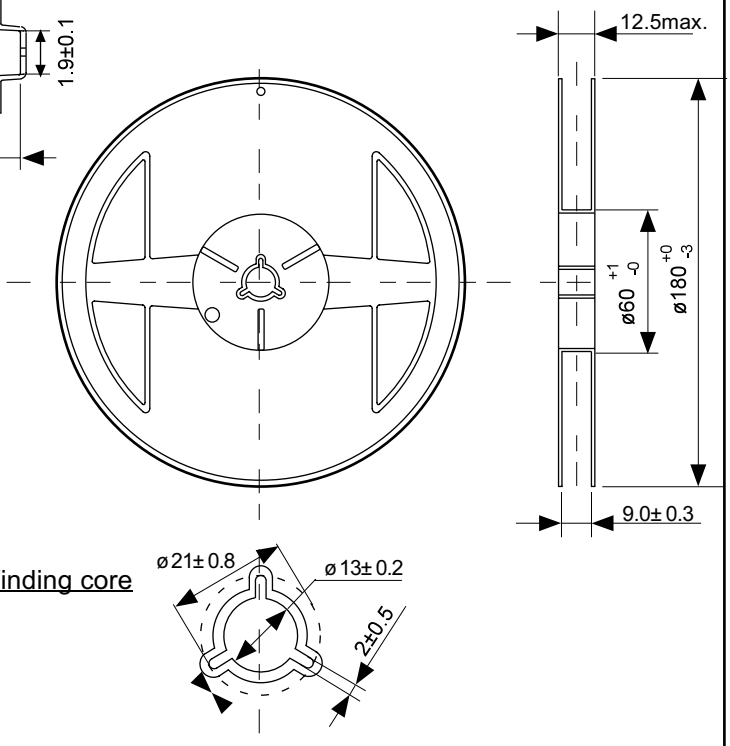




No. : BB004-A-C-SD-1.0

● Reel Specifications

5000 pcs./ reel



No. : BB004-A-R-SD-1.0

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