Contents

Real-Time Clock

S-3511A

S-3511A is a CMOS real-time clock IC , which is designed to transfer or set each data of a clock and calender as requested by a CPU. It provides connection with a CPU via three wires and has an interrupt/alarm feature, allowing the alleviation of software treatment on the side of a host.
It also works on lower power with the oscillating circuit operated at a constant voltage. Its package uses an extremely small and thin type of eight-pin SSOP.

■ Features

- Low power consumption : 0.7 μA typ. (V_{DD}=3.0 V)
- Wide area of operating voltage : 1.7 to 5.5 V
- BCD input/output of year, month, day, day of a week, hour, minute and second
- CPU interface via three wires
- Auto calender till the year of 2,099 (automatic leap year arithmetic feature included)
- Built-in power voltage detecting circuit
- Built-in constant voltage circuit
- Built-in flag generating circuit on power on/off
- Built-in alarm interrupter
- Steady-state interrupt frequency/duty setting feature
- Built-in 32 KHZ crystal oscillating circuit (Internal Cd, External Cg)
- 8-pin SSOP package (terminal pitch: 0.65 mm)

■ Applications

- Cellular phone
- PHS
- A variety of pagers
- TV set and VCR
- Camera

■ Block Diagram

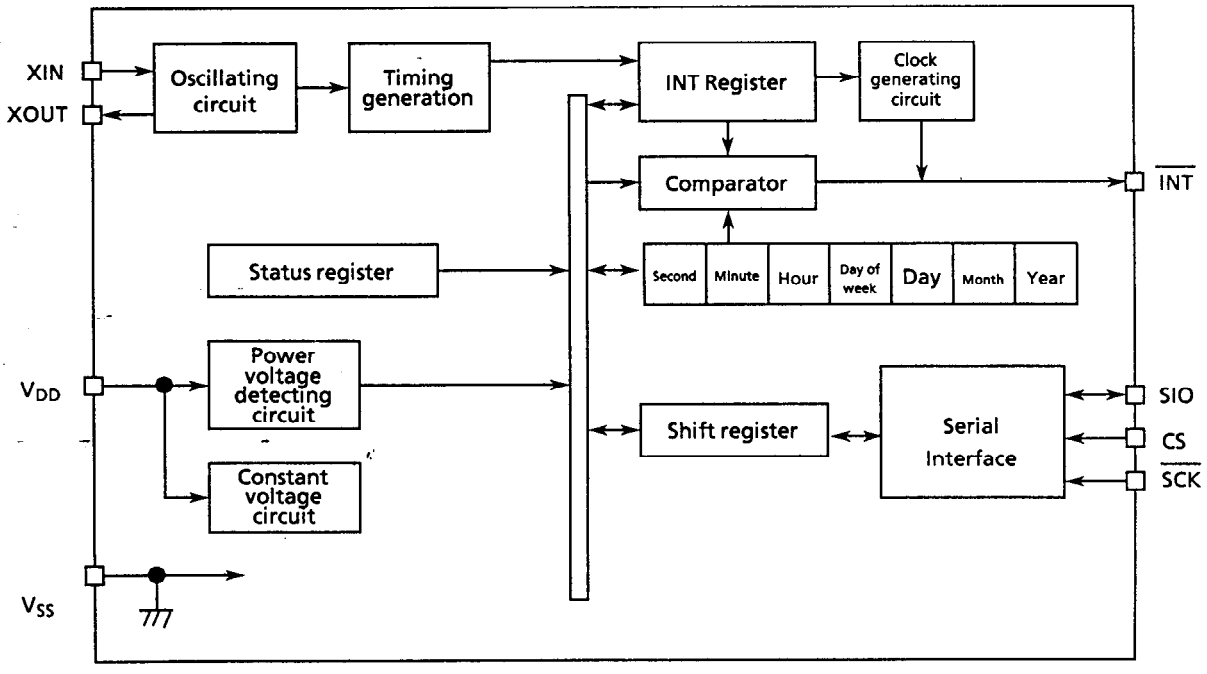


Figure 1 Block diagram

■ Pin Assignment

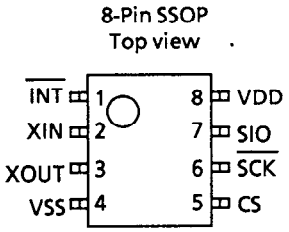


Figure 2 Pin assignment

■ Description of Terminals

Terminal Num.	Abbreviation	Description	Configuration
1	$\overline{INT}$	Alarm interrupt output terminal. Depending on the mode set by the INT register and status register, it outputs low or Clock when time is reached. It is disabled by rewriting the status register.	N-channel open drain output (No protective diode on the side of VDD)
2	XIN	Crystal oscillator connect terminal (32,768 HZ) (Internal Cd, External Cg)	—
3	XOUT		
4	VSS	Negative power supply terminal (GND)	—
5	CS	Chip select input terminal. During "H": The SIO terminal allows data input/output. The $\overline{SCK}$ terminal allows data input. During "L": The SIO terminal is in the High-Z state. The $\overline{SCK}$ terminal is in the input-disabled state.	CMOS input (Included pull-down resistance. No protective diode on the side of VDD)
6	$\overline{SCK}$	Serial clock input terminal. The input/output of data from the SIO terminal is performed in synchronization with this clock. However, the clock is not accepted while the CD terminal is "L."	CMOS input (No protective diode on the side of VDD)
7	SIO	Serial data input/output terminal. It is normally in the High-Z state while the CS terminal is "L." When the CS terminal changes from "L" to "H", the SIO terminal is set to an input terminal. It will be set to an input or output terminal, depending on an subsequently input command.	N channel open drain output (No protective diode on the side of VDD) CMOS input
8	VDD	Positive power supply terminal.	—

Table 1 Description of terminals

■ Description of Operation

1.Serial interface

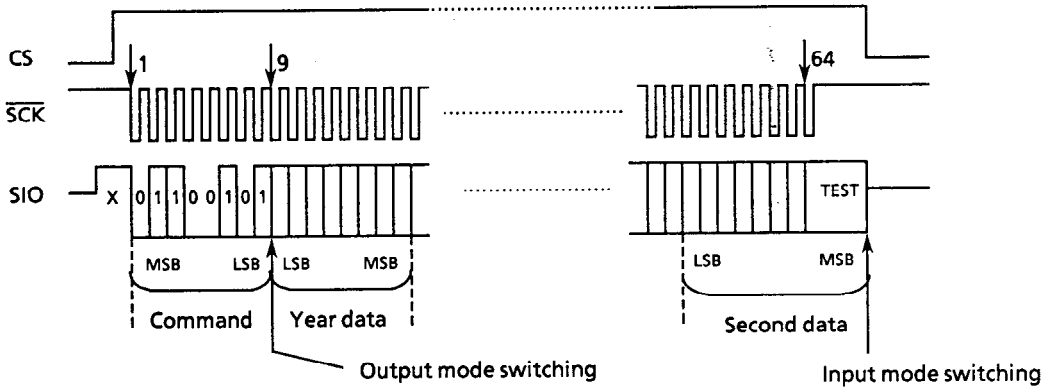
S-3511A receives various commands via a three-wire serial interface to read/write data. This section covers the transfer methods of this product.

1-1.Data reading

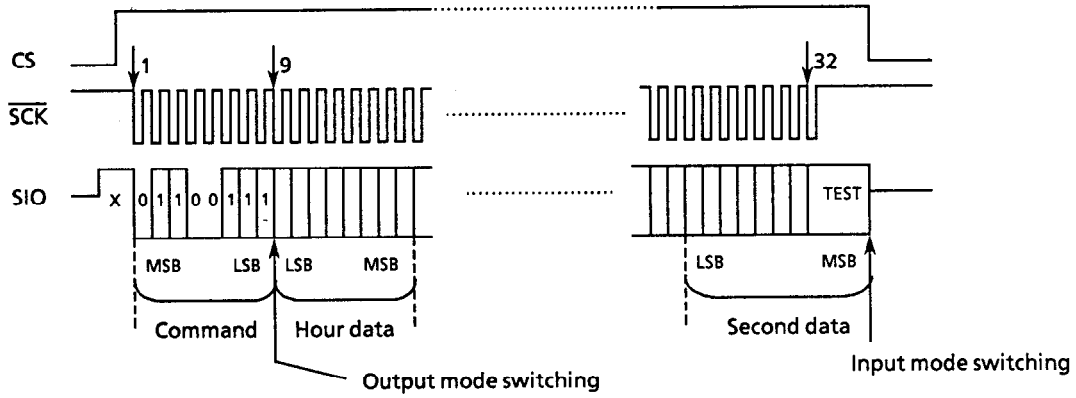
When you input data from the SIO terminal in synchronization with the falling of the SCK terminal after turning the CS terminal to "H", the data is included into the inside of S-3511A at the eighth rising of the SCK clock and the state of data reading is reached when the R/$\overline{W}$ bit has "1". The state leads to output of data corresponding each command in synchronization with the falling of subsequent SCK clock input.

【 Note 】 When the number of SCK clocks is less than eight, the state of clock waiting is reached and no processing is done.
When SCK clocks are more than required, they are processed in order from the first and the clocks other than those required are ignored.

(1) Real-time data reading 1



(2) Real-time data reading 2



(3) Status register reading

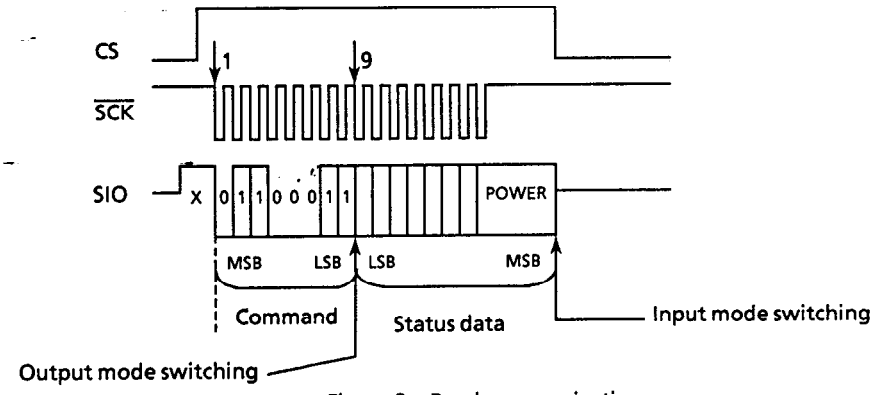
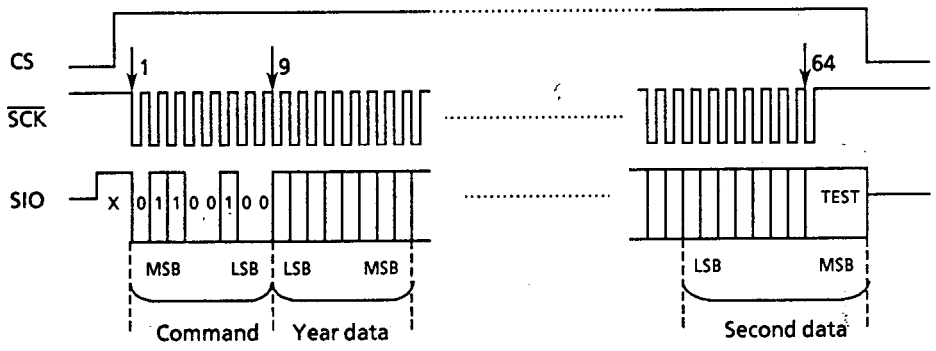


Figure 3 Read communication

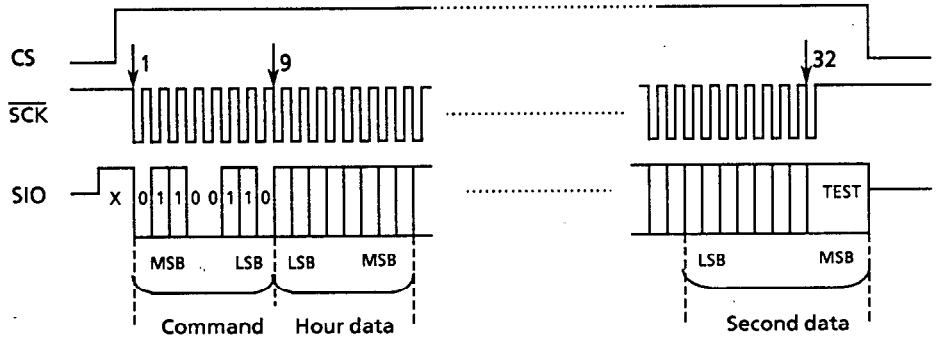
1-2.Data writing

When you input data from the SIO terminal in synchronization with the falling of the SCK terminal after turning the CS terminal to "H", the data is included into the inside of S-3511A at the eighth rising of the SCK clock and the state of data reading is reached when the R/$\overline{W}$ bit has "0". In the state, the data is written to registers according each command in synchronization with the falling of subsequent SCK clock input.

(1) Real-time data writing 1



(2) Real-time data writing 2



(3) Status register writing

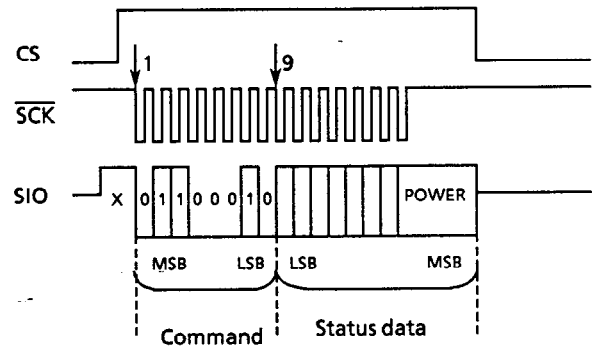


Figure 4 Write communication

1-3.Communication data configuration

After turning the CS terminal to "H", send four-bit fixed code "0110" and succeedingly transfer the command of a 3-bit length and read/write command of a one-bit length.

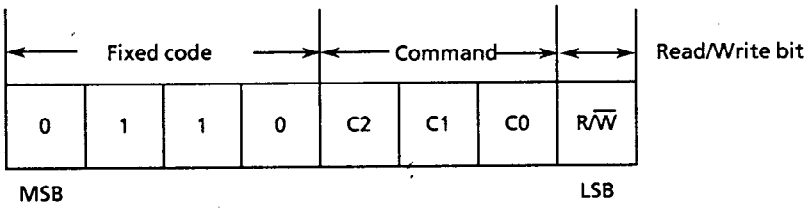


Figure 5 Communication data

2.Command configuration

There are seven types of commands which read from and write to various registers. The table below lists them. Any command that is not listed in the table provides no operation.

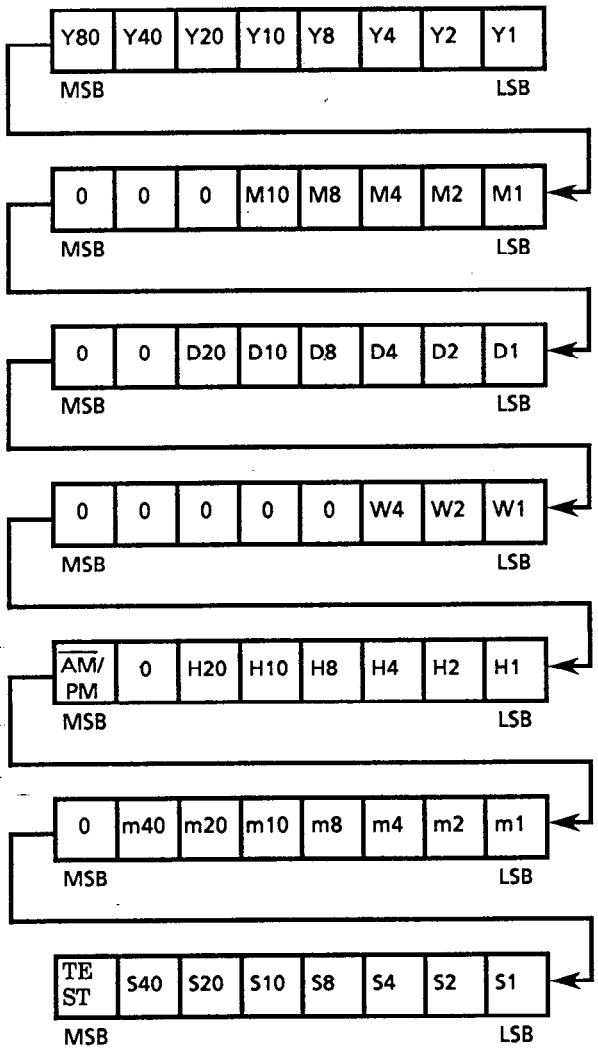
C2	C1	C0	Description
0	0	0	Reset (00 (year), 01 (month), 01 (day), 0 (day of week), 00 (minute), 00 (second)) (*1)
0	0	1	Status register access
0	1	0	Real-time data access 1 (year data to)
0	1	1	Real-time data access 2 (hour data to)
1	0	0	Alarm time/frequency duty setting 1
1	0	1	Alarm time/frequency duty setting 2
1	1	0	Test mode start (*2)
1	1	1	Test mode end (*2)

(*1) Don't care the R/$\overline{W}$ bit of this command.
(*2) This command is access-disabled due to specific use for the IC test.

Table 2 Command list

2-1. Real-time data register

The real-time data register is a fifty-six-bit register which stores the BCD code of the data of year, month, day, day of week, hour, minute and second. Any read/write operation performed by the real-time data access command sends or receives the data from LSB on the first digit of the year data.



Year data (00 to 99)

Sets the lower two digits of the Christian era (00 to 99) and links together with the auto calender feature till 2,099.

Month data (01 to 12)

The count value is automatically changed by the auto calender feature:

1 to 31 : 1, 3, 5, 7, 8, 10, 12
1 to 30 : 4, 6, 9, 11
1 to 29 : 2 (leap year)
1 to 28 : 2 (common year)

Day data (01 to 31)

Day of week data (00 to 06)

A septenary counter. Set it so that it corresponds to the day of the week.

Hour data (00 to 23 or 00 to 11)

$\overline{\text{AM}}$/PM : For 12-hour expression, 0:AM and 1:PM.
For 24-hour expression, this flag has no meaning but either "0" or "1" must be written.

Minute data (00 to 59)

Second data (00 to 59) and test flag

TEST : Turns to "1" during the test mode.

Figure 6 Real-time data register

2-2. Status register

The status register is an eight-bit register which allows you to display and set various modes. The POWER flag is read-only and others are read/write-enabled.

	B7	B6	B5	B4	B3	B2	B1	B0	
MSB	POWER	$\overline{12}$/24	INTAE	—	INTME	—	INTFE	—	LSB
	R	R/W	R/W		R/W		R/W		

Figure 7 Status register

B7:POWER This flag turns to "1" if the power voltage detecting circuit operates during power-on or changes in power voltage (below VDET). Once turning to "1", this flag does not turns back to "0" even when the power voltage reaches or exceeds the detected voltage. When the flag is "1", you must send the reset command and turn it to "0". It is a read-only flag.

B6:$\overline{12}$/24 This flag is used to set 12-hour or 24-hour expression.

0 : 12-hour expression

1 : 24-hour expression

B5:INTAE This flag is used to choose the state of $\overline{INT}$ terminal output with interrupt output set. Enable this flag after setting alarm time that forms a meeting condition in the INT register:

0 : Alarm interrupt output is disabled.

1 : Alarm interrupt output is enabled.

B3:INTME This flag is used to make the output of the $\overline{INT}$ terminal per-minute edge interrupt or per-minute steady interrupt. To make the output per-minute steady interrupt, set "1" at INTME and INTFE .

0 : Alarm interrupt or selected frequency steady interrupt output

1 : Per-minute edge interrupt or per-minute steady interrupt output

B1:INTFE This flag is used to make the output of the $\overline{INT}$ terminal per-minute steady interrupt output (a period of one minute, 50% of duty) or selected frequency steady interrupt. Note that the INT register is considered as the data of frequency/duty if selected frequency steady interrupt is chosen.

0 : Alarm interrupt or selected frequency steady interrupt output

1 : Per-minute edge interrupt or per-minute steady interrupt output

B4, B2 and B0: If having written contents, they are ignored. When they are read, "0" can be read from them.

2-3. Alarm time/Frequency duty setting register

The alarm time/frequency duty setting register is a sixteen-bit register which sets alarm time or frequency duty. They are switched by INTAE or INTFE register. $\overline{AM}$/PM flag to be set must be in accordance with 12-hour or 24-hour expression. If $\overline{AM}$/PM flag is not rightly then set hour data is not met to alarm data.The alarm time/frequency duty setting register is a write-only register.

(1) When INTAE = 1

INT register

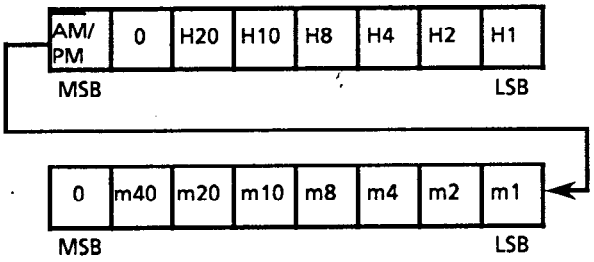


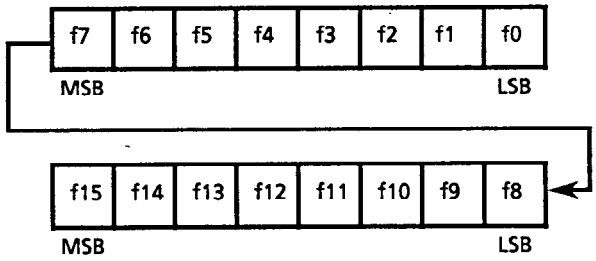
Figure 8 INT register (alarm)

INT register is considered as alarm time data. Having the same configuration as the time and minutes registers of real-time register configuration, they represent hours and minutes with BCD codes. When setting them, do not set any none-existent day. Data to be set must be in accordance with 12-hour or 24-hour expression that is set at the status register.

(2) When INTFE = 1

INT register is considered as frequency duty data. By turning each bit of the registers to "1", a frequency corresponding to each bit is chosen in an ANDed form.

INT register



f0	32768HZ	f4	2048HZ	f8	128HZ	f12	8HZ
f1	16384HZ	f5	1024HZ	f9	64HZ	f13	4HZ
f2	8192HZ	f6	512HZ	f10	32HZ	f14	2HZ
f3	4096HZ	f7	256HZ	f11	16HZ	f15	1HZ

Figure 9 INT register (frequency duty)

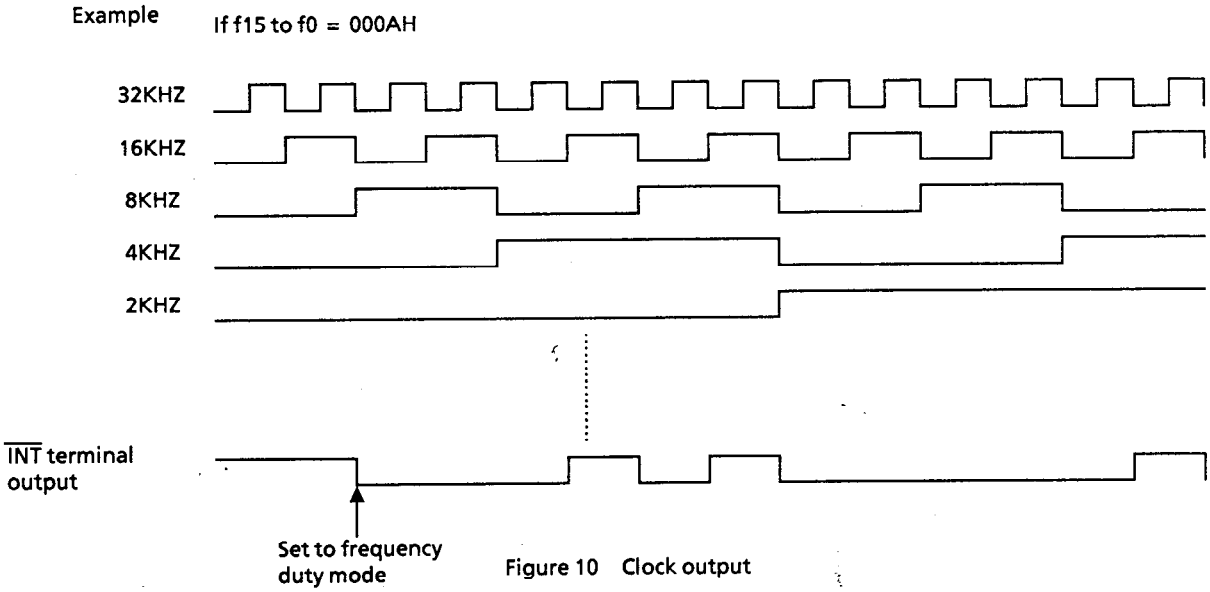


Figure 10 Clock output

2-4. Test flag

The test flag is a one-bit register which is assigned to MSB of the second data of the real-time data register. If a transferred data is considered as the test mode starting data due to the receiving of the test mode starting data or noises, "1" is set. When "1" is set, you must send the test mode ending command or reset command.

3. Initialization

Note that S-3511A has different initializing operations, depending on states.

3-1. When power is turned on

When power is turned on, the status register is set to "82h" and the INT register to "8000h" by the power-on detecting circuit. In other words, "1" is sets at the bit 7 (POWER flag) of the status register and the clock of 1HZ is output from the $\overline{\text{INT}}$ terminal. This is provided to adjust oscillating frequencies. In normal use, the reset command must be sent when power is turned on.

Real-time data register : 00 (year), 01 (month), 01 (day), 0 (day of week), 00 (hour), 00 (minute), 00 (second)
Status register : "82h"
INT register : "8000h"

3-2. When the power voltage detecting circuits operates

The power voltage detecting circuit included in S-3511A operates and sets "1" at the bit 7 (POWER flag) of the internal status register when power is turned on or power voltage is reduced. Once "1" is set, it is held even after the power voltage gets equal to or higher than the detected power voltage. When the flag has "1", you must send the reset command from CPU and initialize the flag. At this point, other registers does not change.
However, if the POWER flag has "0" during the power-on reset of CPU (S-3511A does not reach any indefinite area during backup), you do not have to send the reset command.

3-3. When the reset command is received

When the reset command is received, each register turns as follows:

Real-time data register : 00 (year), 01 (month), 01 (day), 0 (day of week), 00 (hour), 00 (minute), 00 (second)
Status register : "00h"
INT register : "0000h"

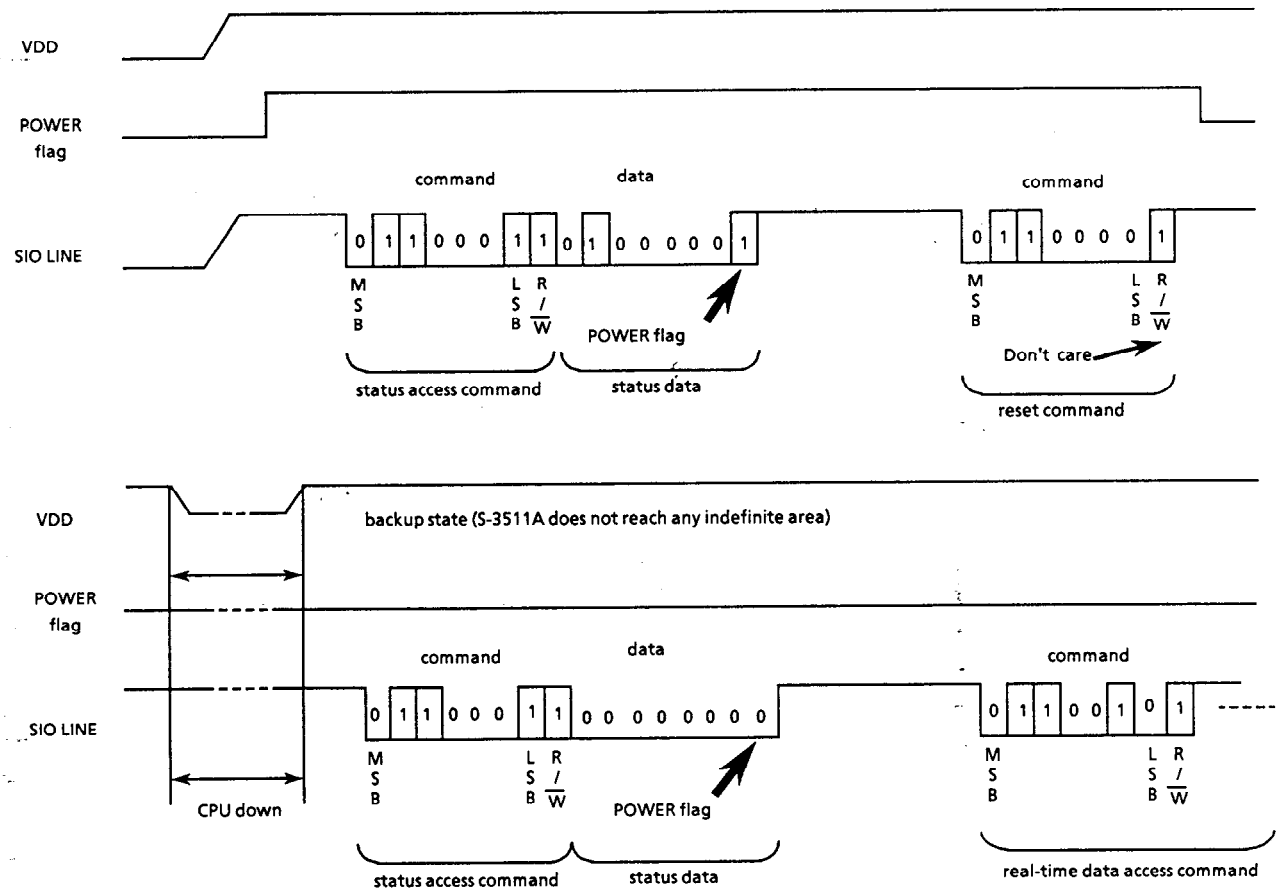


Figure 11 Initializing

4. Processing of none-existent data and end-of-month

When writing real-time data, validate it and treat any invalid data and end-of-month correction.

[None-existent data processing]

Table 3 None-existent data processing

Register	Normal data	Error data	Result
Year data	00 to 99	XA to XF, AX to FX	00
Month data	01 to 12	00, 13 to 19, XA to XF	01
Day data	01 to 31	00, 32 to 39, XA to XF	01
Day of week data	0 to 6	7	0
Hour data (24-hour) (*) (12-hour)	0 to 23 0 to 11	24 to 29, 3X, XA to XF 12 to 19, XA to XF	00 00
Minute data	00 to 59	60 to 79, XA to XF	00
Second data (**)	00 to 59	60 to 79, XA to XF	00

(*) For 12-hour expression, write the $\overline{\text{AM}}$/PM flag.
The $\overline{\text{AM}}$/PM flag is ignored in 24-hour expression, but "0" for 0 to 11 o'clock and "1" for 12 to 23 o'clock are read in a read operation.

(**) None-existent data processing for second data is performed by a carry pulse one second after the end of writing. At this point, the carry pulse is sent to the minute

[End-of-month correction]

Any none-existent day is corrected to the first day of the next month. For example, February 30 is changed to March 1. Leap-year correction is also performed here.

5. Interrupt

There are five types of output format from the $\overline{INT}$ terminal, which are selected by the INTAE, INTME and INTFE bits of the status register.

(1) Alarm interrupt output

Alarm interrupt is enabled by setting hour and minute data to the INT register and turning the status register's INTAE to "1" and INTME and INTFE to "0". When set hour data is met, low is output from the $\overline{INT}$ terminal. Since the output is held, rewrite INTAE of the status register to "0" through serial communication to turn the output to high (OFF state).

(2) Selected frequency steady interrupt output

When you set frequency/duty data to the INT register and turn the status register's INTME to "0" and INTFE to "1", clock set at the INT register is output from the $\overline{INT}$ terminal.

(3) Per-minute edge interrupt output

When a first minute carry is performed after the status register's INTME is set with "1" and INTFE with "0", low is output from the $\overline{INT}$ terminal. Since the output is held, rewrite INTAE, INTME and INTFE of the status register through a serial communication.

(4) Per-minute steady interrupt output

When a first carry is performed after the status register's INTME and INTFE are set with "1", clock is output from the $\overline{INT}$ terminal with a period of one minute (50% duty)

Note 1 : If changing an output mode, give care to the state of the INT register and output.

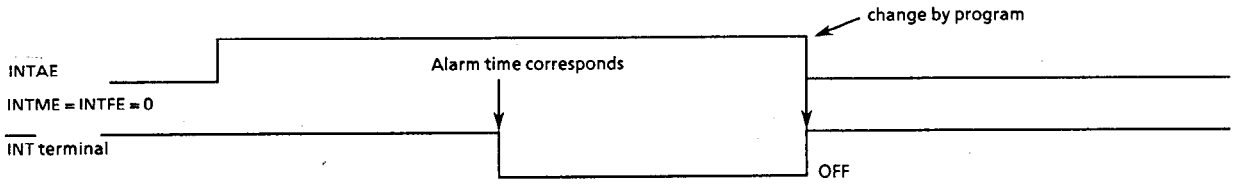
Note 2 : If per-minute edge interrupt output or per-minute steady interrupt output is chosen, the INT register have no meaning.

NO.	INTAE	INTME	INTFE	Description
0	0	0	0	Output disabled
1	*	0	1	Selected frequency steady interrupt output
2	*	1	0	Per-minute edge interrupt output
3	*	1	1	Per-minute steady interrupt output
4	1	0	0	Alarm interrupt output

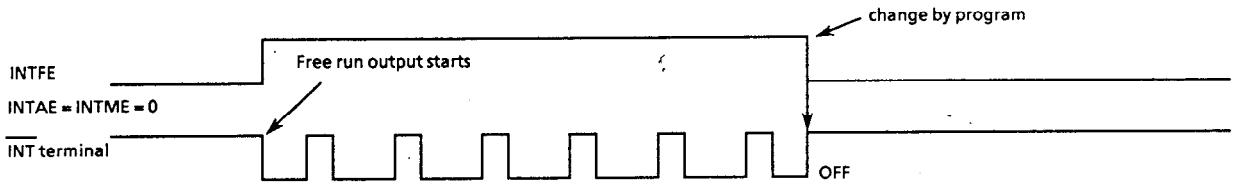
Note * : Don't care.

Table 4 Interrupt description

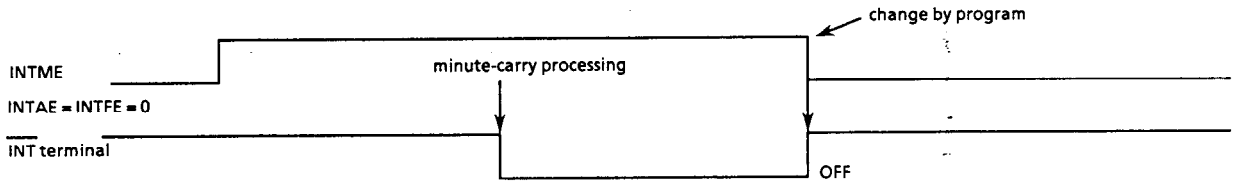
(1) Alarm interrupt output



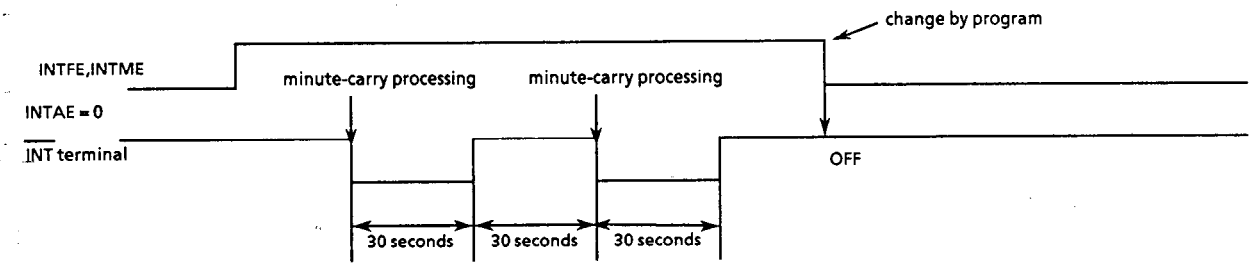
(2) Selected frequency steady interrupt output



(3) Per-minute edge interrupt output



(4) Per-minute steady interrupt output



(5) During power-on detecting circuit operation

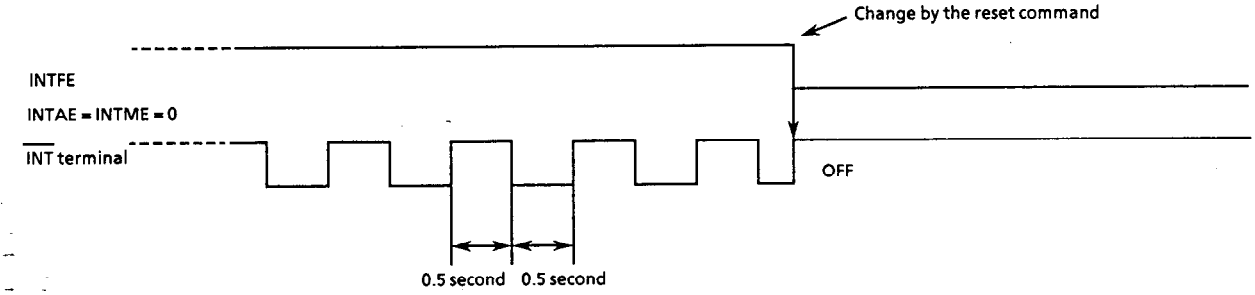


Figure 12 Output mode

6. Power voltage detecting circuit

S-3511A has an internal power voltage detecting circuit. This circuit gives sampling movement for only 15.6msec. once a second.

If the power voltage decreases below the detected voltage (VDET), sampling movement stops. Only when subsequent communication is of the status read command, the output of the latch circuit is transferred to the sift register and the sampling movement is resumed.

Decrease in power voltage can be monitored by reading the POWER flag.

That is to say, once decrease in power voltage is detected, any detecting operation is not performed and "H" is held unless you perform initialization or send the status read command.

[Note]

When power voltage is increased and the first read operation is performed after decrease in power voltage occurs and the latch circuit latches "H", "1" can be read on the POWER flag. However, if the next read operation is performed after the sampling of the detecting circuit, the POWER flag is reset since sampling is subsequently allowed. See the timing diagram below.

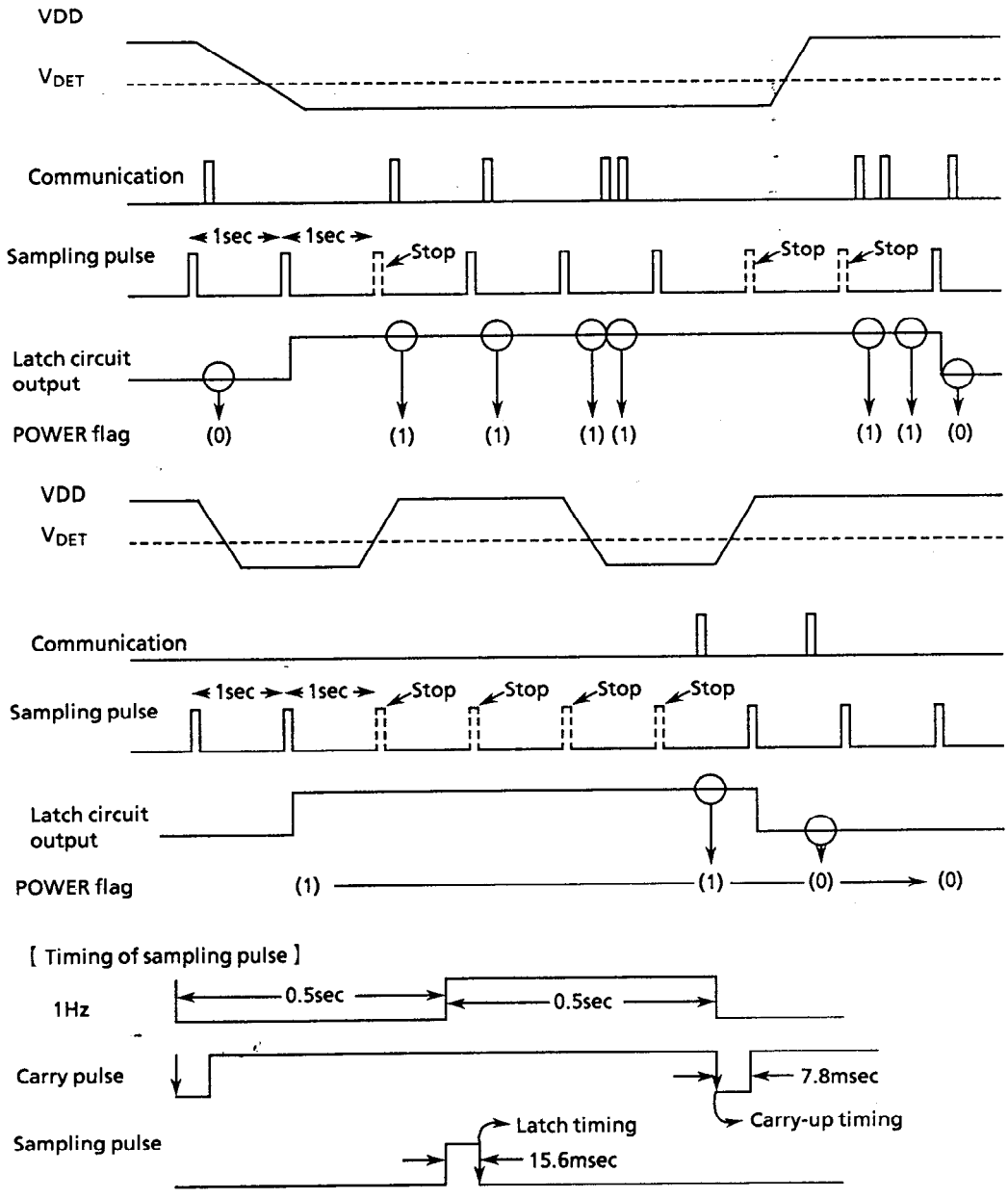
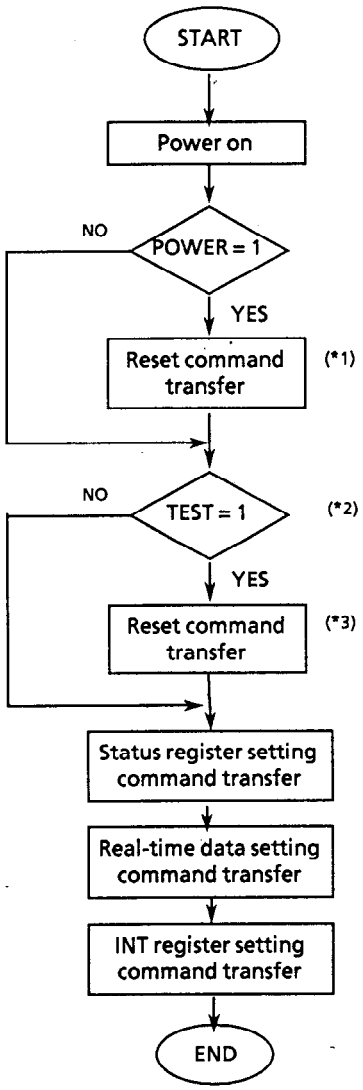


Figure 13 Timing of the power voltage detecting circuit

7. Example of software treatment

(1) Initialization flow at power-on



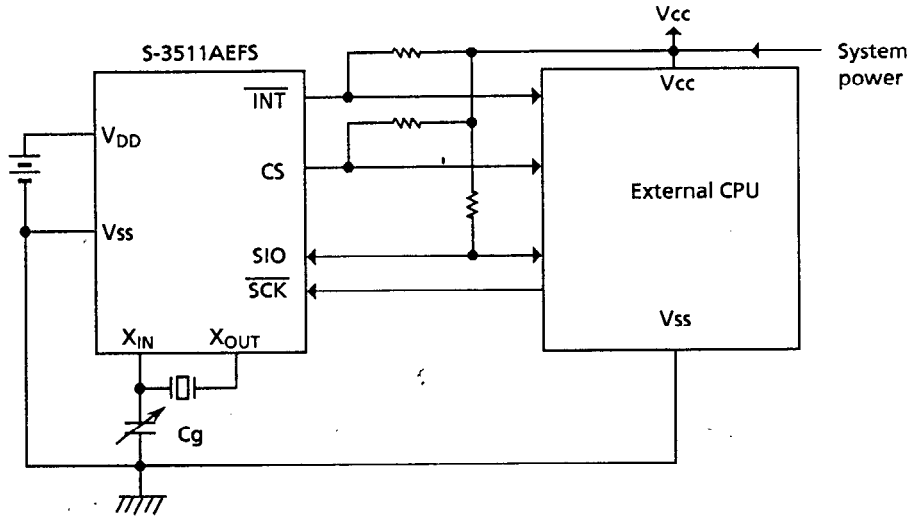
(*1) If S-3511 is back-up and power is turned on only on the CPU side, the reset command does not need transferring.

(*2) If conditions are no good (e.g., noise) and probable changes in commands occurs via serial communications, it is recommended to make sure the TEST flag.

(*3) The test ending command may be used alternately

Figure 14 Initialization flow

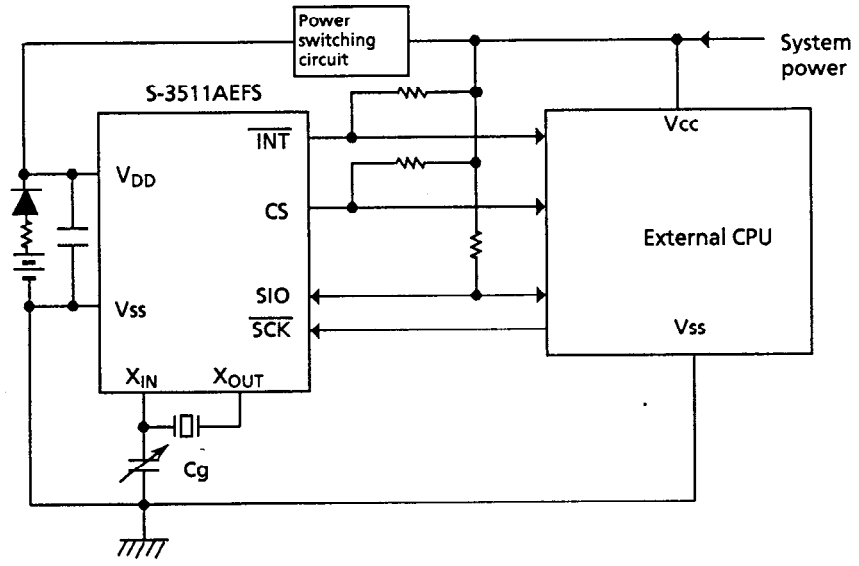
■ Samples of Applied Circuits



Due to the I/O terminal with no protective diode on the VDD side, the relation of VCC≥ VDD has no problem. But give great care to the standard.

Make communications after the system power is turned on and a stable state is obtained.

Figure 15 Applied circuit 1



Make communications after the system power is turned on and a stable state is obtained.

Figure 16 Applied circuit 2

■ Dimensional Outline Diagram (Unit: mm)

Eight-pin SSOP

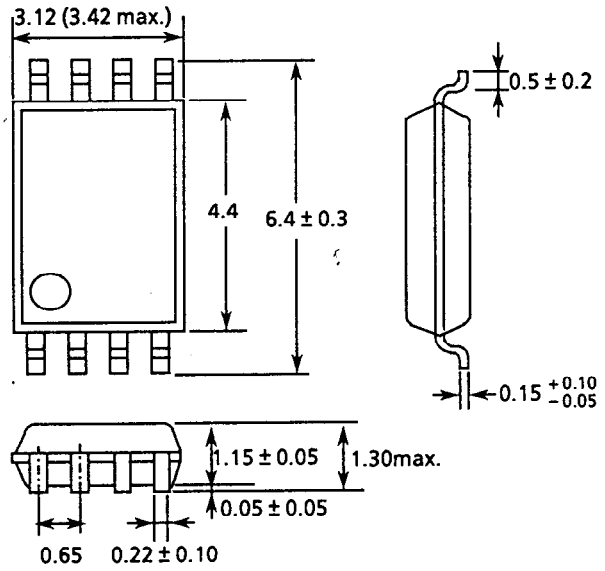


Figure 17 Dimensional outline diagram

■ Order Specification

S-3511AE FS

Package (fixed) : Eight-pin SSOP

Description (fixed)

■ Adjustment of Oscillating Frequency

1. Configuration of the oscillating circuit

Since crystal oscillation is sensitive to external noises (clock accuracy is affected), the fallowing measures must be taken in configuring the oscillating circuit:

(1) S-3511A, crystal oscillator and external capacitor (Cg) are placed as close to each other as possible.

(2) Make high the insulation resistance between terminals and the board between XIN and XOUT.

(3) Do not place any signal or power lines close to the oscillating circuit.

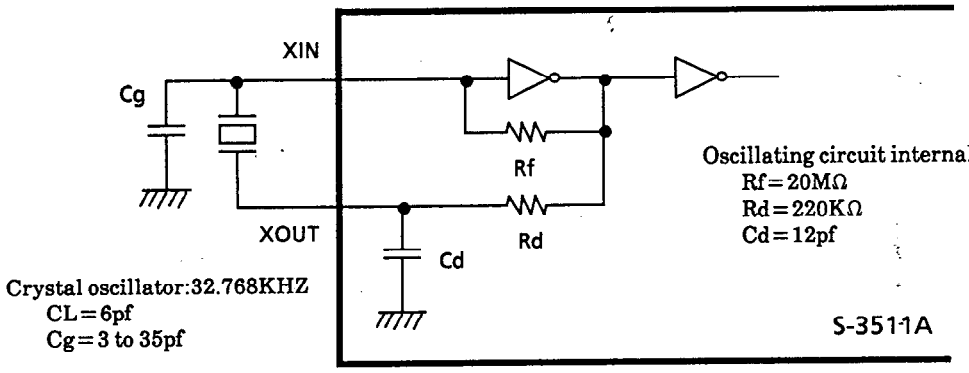


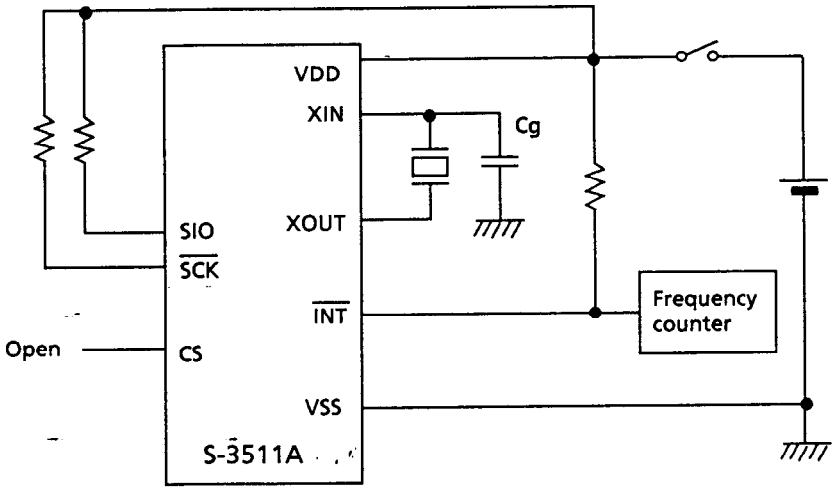
Figure 18 Connection diagram

2. Measurement of oscillating frequencies

When power is turned on, S-3511A has the internal power-on detecting circuit operating and outputs a signal of 1HZ from the $\overline{INT}$ terminal to select the crystal oscillator and optimize the Cg value. Turn power on and measure the signal with a frequency counter following the circuit configuration shown in Figure 22. Refer to 9 and 12 pages in this document for further information.

(*) If the error range is ±1ppm in relation to 1HZ, time is shifted by approximately 2.6 seconds a month:

$10^{-6(1ppm)} \times 60$ seconds × 60 minutes × 24 hours × 30 days = 2.592 seconds

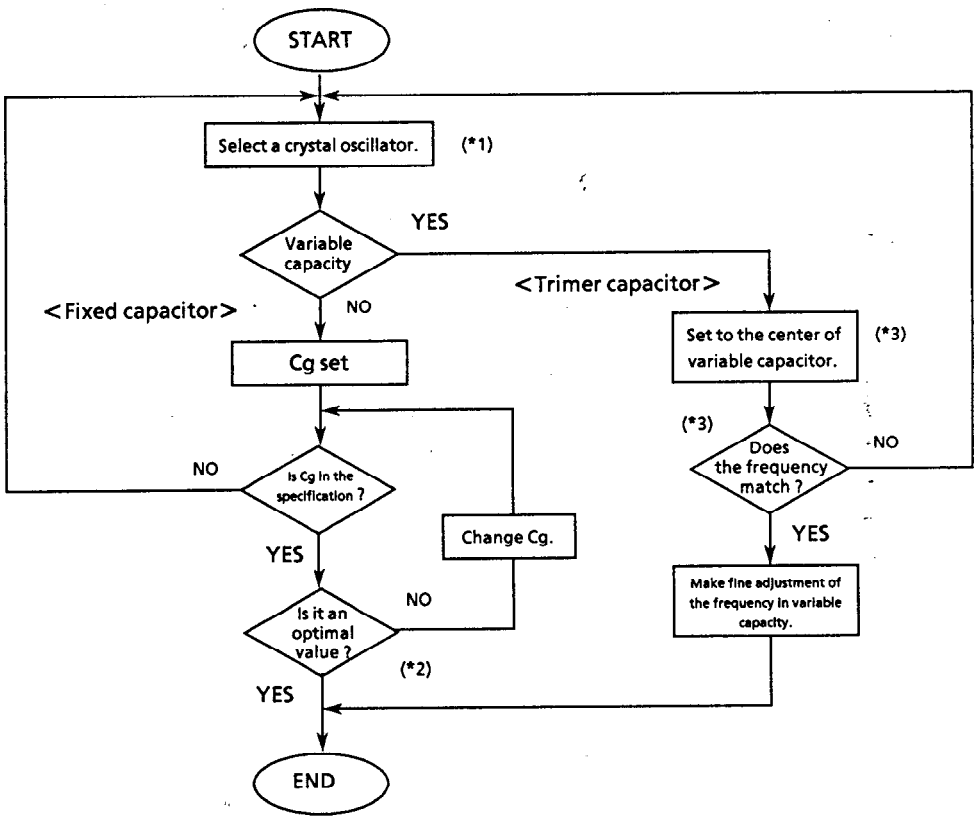


Note 1: Use a high-accuracy frequency counter (1ppm order).
Note 2: Since the 1HZ signal continues to be output, you must send the reset command in normal operation.
Note 3: Determine Cg with its frequency slow/fast range property referred.

Figure 19 Connection diagram

3. Adjustment of oscillating frequencies

Matching of a crystal oscillator with the nominal frequency must be performed with suspended capacity on the board included. Select a crystal oscillator and optimize the Cg value in accordance with the flow chart below.



(*1) For making matching adjustment of the IC with a crystal, contact an appropriate crystal maker to determine the CL value (load capacity) and RI value (equivalent serial capacity). The CL value = 6pf and RI value = 30KΩ TYP. are recommended values.

(*2) Cg value selection must be performed on the actual PCB since suspended capacity affects it. Select the Cg value in a range from 3pf to 35pf. If the frequency does not match, change the CL value of the crystal.

(*3) Adjust the rotation angle of the variable capacity so that the capacity value is somewhat smaller than the center, and confirm the oscillating frequency and the center value of the variable capacity. This is done in order to make the capacity of the center value smaller than one half of the actual capacity value because a smaller capacity value makes a greater quantity of changes in a frequency. If the frequency does not match, change the CL value of the crystal.

Note 1 : Oscillating frequencies are changed by ambient temperature and power voltage. Refer to property samples.

Note 2 : The 32KHZ crystal oscillator operates slower at higher or lower ambient temperature than 20 to 25°C. Therefore, it is recommended to adjust of set the oscillator to operate somewhat faster at normal temperature.

■ Absolute Maximum Ratings

Table 5 Absolute maximum ratings

Item	Symbol	Rating	Unit	Applicable terminal, conditions
Power voltage	VDD	− 0.3 to + 6.5	V	—
Input voltage	V_{IN}	− 0.3 to + 6.5	V	$\overline{SCK}$, SIO
Output voltage	V_{OUT}	− 0.3 to + 6.5	V	SIO, $\overline{INT}$
Operating temperature	T_{opr}	− 40 to + 85	°C	VDD = 3.0V
Retention temperature	T_{stg}	− 55 to + 125	°C	—

■ Recommended Operating Conditions

Table 6 Recommended operating conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	VDD	—	1.7	3.0	5.5	V
Operating temperature	T_{opr}	—	− 20	+ 25	+ 70	°C

■ Oscillation Characteristics

Table 7 Oscillation characteristics

(Ta = 25°C, VDD = 3V, DS-VT-200 (crystal oscillator, CL = 6pF, 32,768HZ) manufactured by Seiko Electronic Part Co., Ltd.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within ten seconds	1.7	—	5.5	V
Oscillation start time	T_{STA}	—	—	—	1	SEC
IC-to-IC frequency diversity	δIC	—	− 10	—	+ 10	ppm
Frequency voltage diversity	δV	VDD = 1.7 to 5.5V	− 3	—	+ 3	ppm/V
Input capacity	Cg	Applied to the XIN terminal	3	—	35	pF
Output capacity	Cd	Applied to the XOUT terminal	—	12	—	pF

■ DC Electrical Characteristics

Table 8 DC characteristics (3V)

(Ta = 25°C, VDD = 3V, DS-VT-200 (crystal oscillator, CL = 6pF, 32,768HZ) manufactured by Seiko Electronic Part Co., Ltd.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable terminal
Range of operating voltage	VDD	Ta = − 20 to + 70°C	1.7	3.0	5.5	V	—
Drain current 1	I_{DD1}	During no communications	—	0.7	1.5	V	—
Drain current 2	I_{DD2}	During communications (SCL = 100KHZ)	—	5.5	10	μA	—
Input leak current 1	I_{ILL1}	V_{IN} = VDD	− 0.5	—	0.5	μA	$\overline{SCK}$,SIO
Input leak current 2	I_{ILL2}	V_{IN} = VSS	− 0.5	—	0.5	μA	$\overline{SCK}$,SIO
Input current 1	I_{IL1}	V_{IN} = 5.5V	2	6	20	μA	CS
Input current 2	I_{IL2}	V_{IN} = 0.4V	40	110	300	μA	CS
Output leak current1	I_{OZH}	V_{OUT} = VDD	− 0.5	—	0.5	μA	$\overline{INT}$, SIO
Output leak current2	I_{OZL}	V_{OUT} = VSS	− 0.5	—	0.5	μA	$\overline{INT}$, SIO
Input voltage 1	V_{IH}	—	0.8xVDD	—	—	V	SIO, $\overline{SCK}$, CS
Input voltage 2	V_{IL}	—	—	—	0.2xVDD	V	SIO, $\overline{SCK}$, CS
Output current 1	I_{OL1}	V_{OUT} = 0.4V	1.5	2.5	—	mA	$\overline{INT}$
Output current 2	I_{OL2}	V_{OUT} = 0.4V	5	10	—	mA	SIO
Power voltage detecting voltage 1	V_{DET1}	Ta = + 25°C	1.8	2.0	2.2	V	—
Power voltage detecting voltage 2	V_{DET2}	Ta = − 20 to + 70°C	1.72	—	2.3	V	—

Table 9 DC characteristics (5V)

(Ta = 25°C, VDD = 3V, DS-VT-200 (crystal oscillator, CL = 6pF, 32,768HZ) manufactured by Seiko Electronic Part Co., Ltd.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable terminal
Range of operating voltage	VDD	Ta = − 20 to + 70°C	1.7	3.0	5.5	V	—
Drain current 1	I_{DD1}	During no communications	—	1.6	3.0	V	—
Drain current 2	I_{DD2}	During communications (SCL = 100KHZ)	—	12	20	μA	—
Input leak current 1	I_{ILL1}	V_{IN} = VDD	− 0.5	—	0.5	μA	$\overline{SCK}$,SIO
Input leak current 2	I_{ILL2}	V_{IN} = VSS	− 0.5	—	0.5	μA	$\overline{SCK}$,SIO
Input current 1	I_{IL1}	V_{IN} = 5.5V	10	25	50	μA	CS
Input current 2	I_{IL2}	V_{IN} = 0.4V	100	175	400	μA	CS
Output leak current1	I_{OZH}	V_{OUT} = VDD	− 0.5	—	0.5	μA	$\overline{INT}$, SIO
Output leak current2	I_{OZL}	V_{OUT} = VSS	− 0.5	—	0.5	μA	$\overline{INT}$, SIO
Input voltage 1	V_{IH}	—	0.8xVDD	—	—	V	SIO, $\overline{SCK}$, CS
Input voltage 2	V_{IL}	—	—	—	0.2xVDD	V	SIO, $\overline{SCK}$, CS
Output current 1	I_{OL1}	V_{OUT} = 0.4V	2.0	3.5	—	mA	$\overline{INT}$
Output current 2	I_{OL2}	V_{OUT} = 0.4V	6	12	—	mA	SIO
Power voltage detecting voltage 1	V_{DET1}	Ta = + 25°C	1.8	2.0	2.2	V	—
Power voltage detecting voltage 2	V_{DET2}	Ta = − 20 to + 70°C	1.72	—	2.3	V	—

■ AC Electrical Characteristics

Table 10 AC characteristics 1

(S-3511A, RL = 10KΩ, CL = 80pF)
Conditions: VDD = 1.7V to 5.5V, Ta = −20 to 70°C
Input; V_{IH} = 0.8 × VDD, V_{IL} = 0.2 × VDD, Output; V_{OH} = 0.8 × VDD, V_{OL} = 0.2 × VDD

Item	Symbol	Min.	Typ.	Max.	Unit
Clock pulse width	t_{SCK}	5	—	250000	μs
Setup time before CS rising	t_{DS}	1	—	—	μs
Hold time after CS rising	t_{CSH}	1	—	—	μs
Input data setup time	t_{ISU}	1	—	—	μs
Input data hold time	t_{IHO}	1	—	—	μs
Output data definition time	t_{ACC}	—	—	3.5	μs
Setup time before CS falling	t_{CSS}	1	—	—	μs
Hold time after CS falling	t_{DH}	1	—	—	μs
Input rising/falling time	t_R, t_F	—	—	0.1	μs

Note: Since the output form of the SIO terminal is N-channel open drain output, the rising time of t_{ACC} is determined by the values of load resistance (RL) and load capacity (CL) outside the IC. Use this as a reference value.

Table 11 AC characteristics 2

(S-3511A, RL = 10KΩ, CL = 80pF)
Conditions ; VDD = 3.0 ± 0.3V, Ta = -20~70°C
Input ; V_{IH} = 0.8 × VDD, V_{IL} = 0.2 × VDD, Output ; V_{OH} = 0.8 × VCC, V_{OL} = 0.2 × VCC(VCC = 5.0V)

項目	記号	Min.	Typ.	Max.	単位
Clock pulse width	t_{SCK}	1	—	250000	μs
Setup time before CS rising	t_{DS}	0.2	—	—	μs
Hold time after CS rising	t_{CSH}	0.2	—	—	μs
Input data setup time	t_{ISU}	0.2	—	—	μs
Input data hold time	t_{IHO}	0.2	—	—	μs
Output data definition time	t_{ACC}	—	—	1.0	μs
Setup time before CS falling	t_{CSS}	0.2	—	—	μs
Hold time after CS falling	t_{DH}	0.2	—	—	μs
Input rising/falling time	t_R, t_F	—	—	0.05	μs

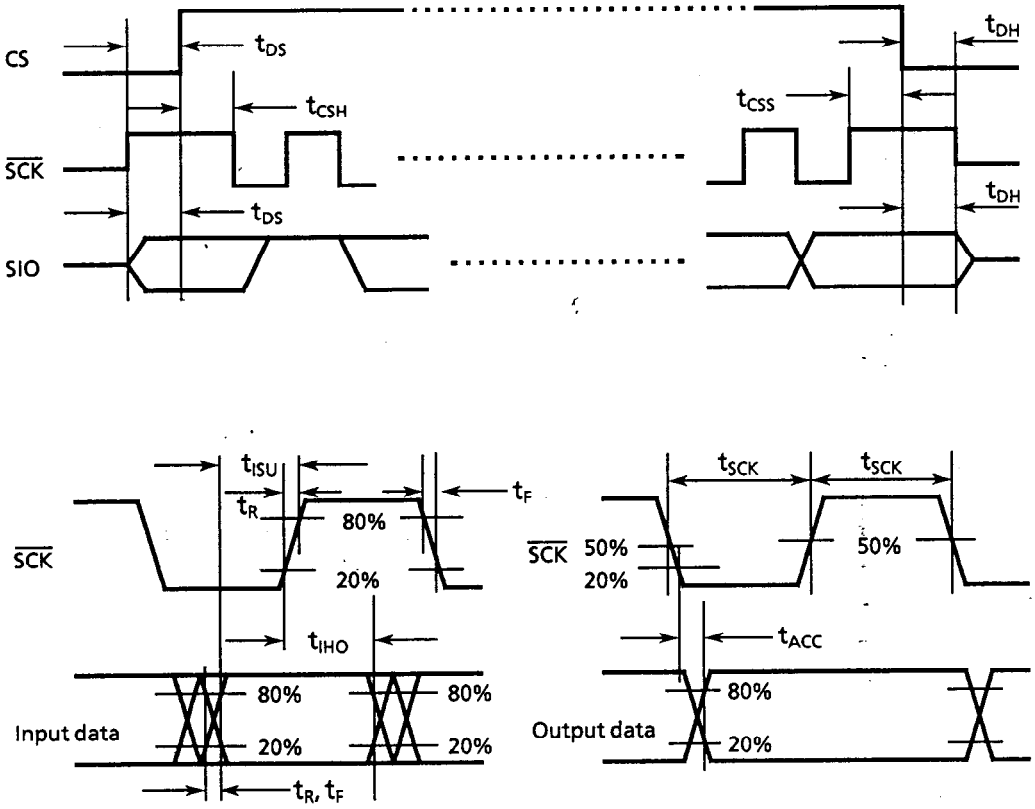
Note: Since the output form of the SIO terminal is N-channel open drain output, the rising time of t_{ACC} is determined by the values of load resistance (RL) and load capacity (CL) outside the IC. Use this as a reference value.

Table 12 AC characteristics 3

(S-3511A, RL = 10KΩ, C_L = 80pF)
Conditions: VDD = 5.0 ± 0.5V, Ta = -20 to 70°C
Input; V_{IH} = 0.8 × VDD, V_{IL} = 0.2 × VDD, Output; V_{OH} = 0.8 × VDD, V_{OL} = 0.2 × VDD

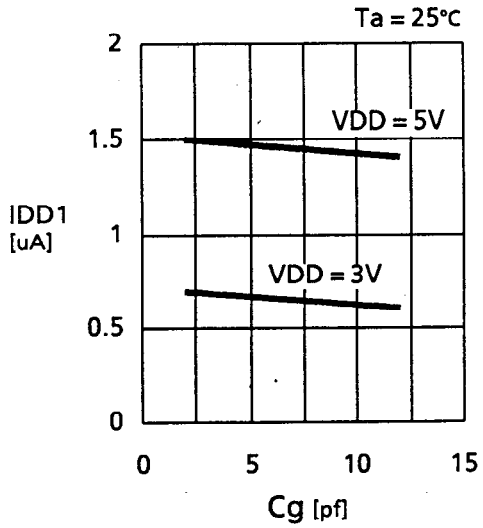
Item	Symbol	Min.	Typ.	Max.	Unit
Clock pulse width	t_{SCK}	0.5	—	250000	μs
Setup time before CS rising	t_{DS}	0.1	—	—	μs
Hold time after CS rising	t_{CSH}	0.1	—	—	μs
Input data setup time	t_{ISU}	0.1	—	—	μs
Input data hold time	t_{IHO}	0.1	—	—	μs
Output data definition time	t_{ACC}	—	—	0.3	μs
Setup time before CS falling	t_{CSS}	0.1	—	—	μs
Hold time after CS falling	t_{DH}	0.1	—	—	μs
Input rising/falling time	t_R, t_F	—	—	0.05	μs

Note: Since the output form of the SIO terminal is N-channel open drain output, the rising time of t_{ACC} is determined by the values of load resistance (RL) and load capacity (CL) outside the IC. Use this as a reference value.

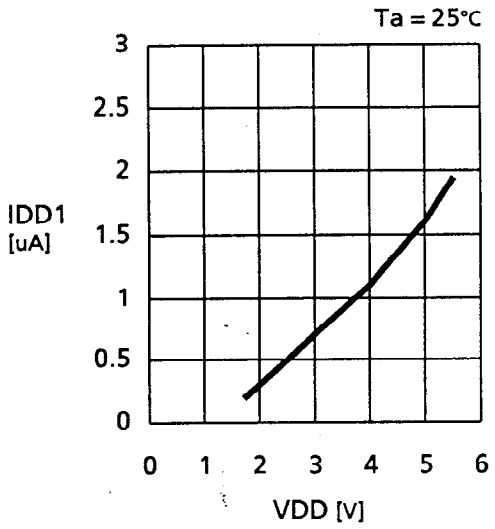

CS
SCK
SIO
tDS
tCSH
tDS
tCSS
tDH
tDH
SCK
tISU
tR
tF
80%
20%
tIHO
Input data
80%
20%
80%
20%
tR, tF
SCK
tSCK
tSCK
50%
20%
50%
tACC
Output data
80%
20%

■ Sample of Properties (Reference values)

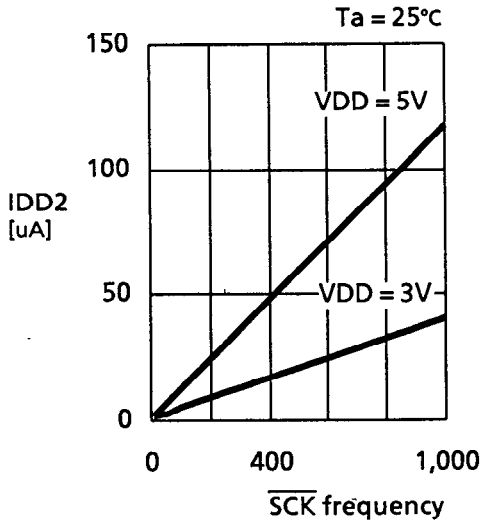
(1) Standby current versus Cg



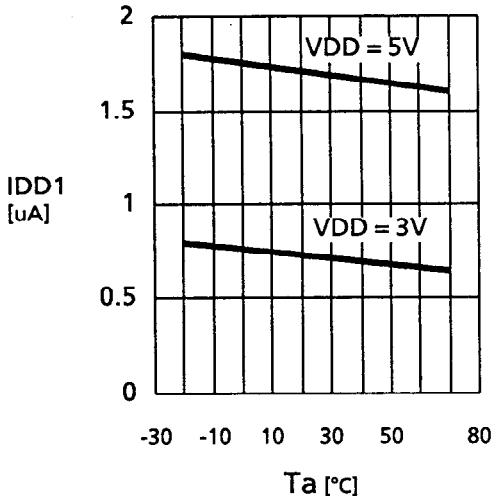
(2) Standby current versus VDD



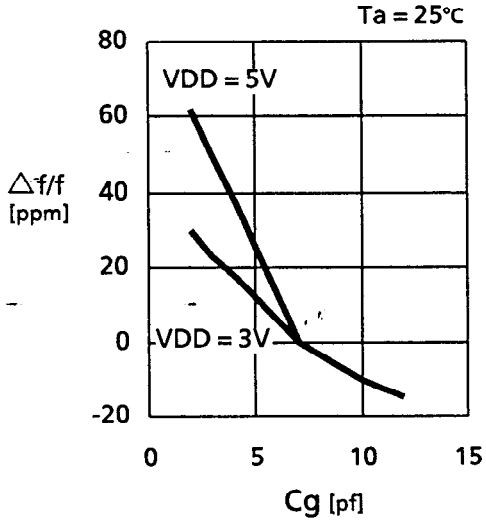
(3) Operating drain current versus Input clock



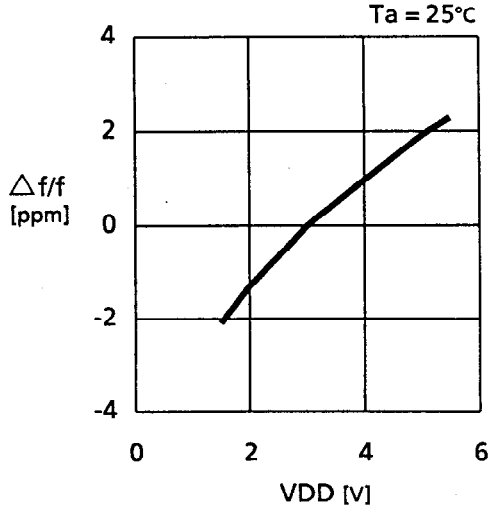
(4) Standby current versus temperature



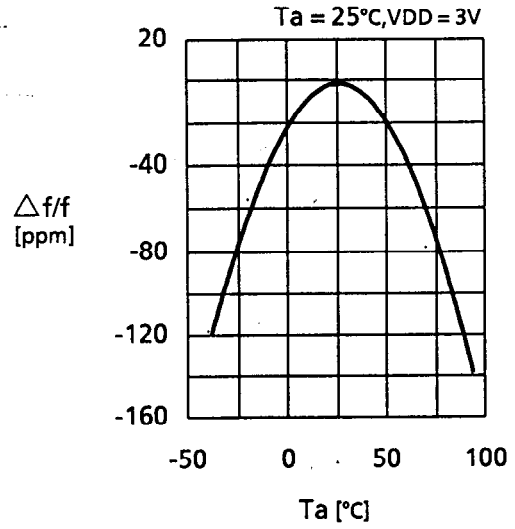
(5) Oscillating frequency versus Cg



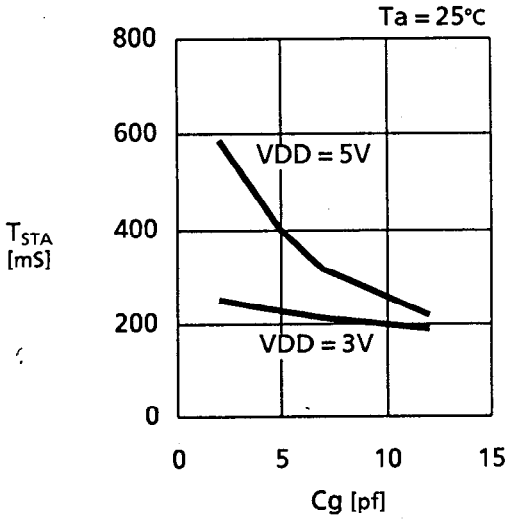
(6) Oscillating frequency versus VDD



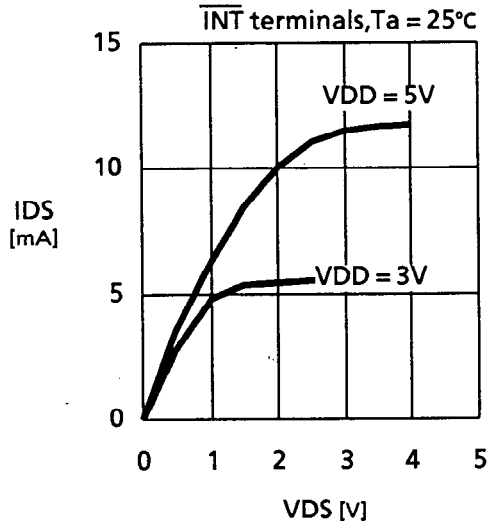
(7) Oscillating frequency versus temperature



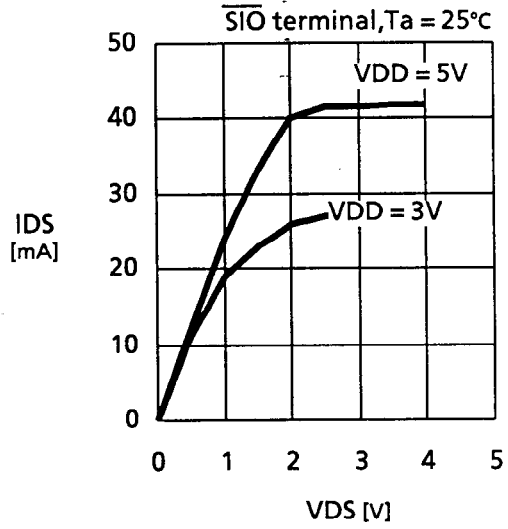
(8) Oscillation start time versus Cg



(9) Output current 1 (VDS versus IDS)



(10) Output current 2 (VDS versus IDS)



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