SIGMATEL™

Integrating Mixed-Signal Solutions

PRODUCT DATA SHEET

STAC9756/57

Two Channel AC'97 Codecs with I²S Digital I/O and SPDIF Output

2-9756-D1-3.3-0303

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1.1. List of Figures

1.2. List of Tables

2. PRODUCT BRIEF

2.1. Features

- High performance ΣΔ technology
- 18-bit full duplex stereo ADC, DACs
- Independent sample rates for ADC & DACs
- 5-Wire AC-Link protocol compliance
- ZV-Port I2S digital input
- I2S digital I/O and SPDIF output
- Digital-ready status
- 20 dB microphone boost capability
- +3.3V (STAC9757) and +5V (STAC9756) analog power supply options
- Pin compatible with the STAC9700/21/44
- SigmaTel Surround (SS3D) Stereo Enhancement
- Energy saving dynamic power modes
- Multi-Codec option (Intel AC'97 rev 2.1)
- Six analog line-level inputs
- 98 dB SNR LINE-LINE

2.2. Description

SigmaTel's STAC9756/57 are general purpose 18-bit, full duplex, audio codecs conforming to the analog component specification of AC'97 (Audio Codec 97 Component Specification Rev. 2.1). The STAC9756/57 incorporate SigmaTel's proprietary ΣΔ technology to achieve a DAC SNR in excess of 95 dB. The DACs, ADCs, and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel. The STAC9756/57 include digital input output capability for support of modern PC systems. There is an I2S input for ZV-Port audio, a dedicated I2S output and an output that supports either I2S or the SPDIF format. The STAC9756/57 is a standard 2-channel stereo codec. The STAC9756/57 may be used as a secondary codec, with the STAC9700/21/44/56/08/84 as the primary, in a multiple codec configuration conforming to the AC'97 Rev. 2.1 specification. This configuration can provide true six-channel, AC-3 playback required for DVD applications. The STAC9756/57 communicates via the five-wire AC-Link to any digital component of AC'97 providing flexibility in the audio system design. Packaged in an AC'97 compliant 48-pin TQFP, the STAC9756/57 can be placed on the motherboard, daughter boards, PCI, AMR, CNR, or ACR cards.

The STAC9756/57 block diagram is illustrated in Figure 1. It provides variable sample rate D-A & A-D conversion, mixing, and analog processing. Supported audio sample rates include 48 kHz, 44.1 kHz, 22.05 kHz, 16 kHz, 11.025 kHz, and 8 kHz; additional rates are supported in the STAC9756/57 soft audio drivers. The digital interface communicates with the AC'97 controller via the five-wire AC-Link and contains the 64-word by 16-bit registers. The two DACs convert the digital stereo PCM-out content to audio. The MIXER block combines the PCM_OUT with any

analog sources, to drive the LINE_OUT and LNLVL_OUT outputs. The MONO_OUT delivers either mic only, or a mono mix of sources from the MIXER. The stereo variable sample rate ADC's provide record capability for any mix of mono or stereo sources, and deliver a digital stereo PCM-in signal back to the AC-Link. The microphone input and mono analog mix can be recorded simultaneously, thus allowing for an all digital output in support of the digital ready initiative. All ADC's and DAC's operate at 18-bit resolution. For a digital ready record path, the microphone is connected to the left channel ADC while the mono output of the stereo mixer is connected to the right channel ADC. Make sure the microphone input is not connected to the stereo mixer when in this mode.

The STAC9756/57 supports one I^2S digital audio input, one dedicated I^2S output, and a dual mode SPDIF/I^2S output. These digital I/O options provide for a number of advance architectural implementations, with volume controls and digtial mixing capabilities built directly into the codec.

The STAC9756/57 is designed primarily to support stereo (2-speaker) audio. True AC-3 playback can be achieved for 6-speaker applications by taking advantage of the multi-codec option available in the STAC9756/57 to support multiple codecs in an AC'97 architecture. Additionally, the STAC9756/57 provides for a stereo enhancement feature, SigmaTel Surround 3D (SS3D). SS3D provides the listener with several options for improved speaker separation beyond the normal 2/4-speaker arrangements.

Together with the logic component (controller or advanced core logic chip-set) of AC'97, STAC9756/57 can be SoundBlaster® and Windows Sound System® compatible with SigmaTel's WDM driver for WIN 98/2K/ME. SoundBlaster is a registered trademark of Creative Labs. Windows is a registered trademark of Microsoft Corporation.

2.3. Ordering Information

Part Number	Package	Temp Range	Supply Range
STAC9756T	48-pin TQFP 7mm x 7mm x 1.4mm	0° C to +70° C	DVdd = 3.3V, AVdd = 5.0V
STAC9757T	48-pin TQFP 7mm x 7mm x 1.4mm	0° C to +70° C	DVdd = 3.3V, AVdd = 3.3V

2.4. STAC9756/57 Block Diagram

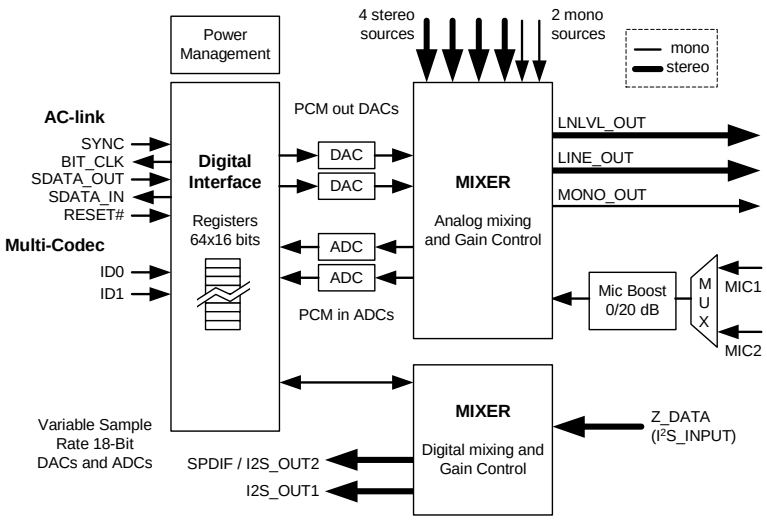


Figure 1. STAC9756/57 Block Diagram

2.5. Key Specifications

- Analog LINE_OUT SNR: 98 dB
- Digital DAC SNR: 98 dB
- Digital ADC SNR: 87 dB
- Full-scale Total Harmonic Distortion: 0.02%
- Crosstalk between Input Channels: -70 dB
- Spurious Tone Rejection: 100 dB

2.6. Related Materials

- Product Brief
- Reference Designs for MB, AMR, CNR, and ACR applications
- Audio Precision Performance Plots

2.7. Additional Support

Additional product and company information can be obtained by going to the SigmaTel website at: www.sigmatel.com

3. CHARACTERISTICS/SPECIFICATIONS

3.1. Electrical Specifications

3.1.1. Absolute Maximum Ratings:

Voltage on any pin relative to Ground	Vss - 0.3V TO Vdd + 0.3V
Operating Temperature	0 ^{O}C TO 70 ^{O}C
Storage Temperature	-55 ^{O}C TO +125 ^{O}C
Soldering Temperature	260 ^{O}C FOR 10 SECONDS
Output Current per Pin	± 4 mA except VREFout = ± 5mA
Maximum Supply Voltage	5.5 Volts = Vdd

3.1.2. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Power Supplies				
+ 3.3V Digital	3.135	3.3	3.465	V
+ 5V Analog	4.75	5	5.25	V
+ 3.3V Analog	3.135	3.3	3.465	V
Ambient Temperature	0	-	70	^{O}C

Table 1. Recommended Operating Conditions

3.1.3. Power Consumption

Parameter	Min	Typ	Max	Unit
Digital Supply Current				
+ 3.3V Digital	-	35	-	mA
Analog Supply Current				
+ 5V Analog	-	80	-	mA
+ 3.3V Analog	-	70	-	mA
Power Down Status				
PR0 +5V Analog Supply Current	-	68	-	mA
PR1 +5V Analog Supply Current	-	54	-	mA
PR2 +5V Analog Supply Current	-	30	-	mA
PR3 +5V Analog Supply Current	-	0.1	-	mA
PR4 +3.3V Digital Supply Current	-	0.1	-	mA
PR5 Internal CLK Disable	-	0.1	-	mA

Table 2. Power Consumption

3.1.4. AC-Link Static Digital Specifications

(Tambient = 25 ºC, DVdd = 3.3V ± 5%, AVss=DVss=0V; 50pF external load)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage Range	Vin	-0.30	-	DVdd + 0.30	V
Low level input range	Vil	-	-	0.35xDVdd	V
High level input voltage	Vih	0.65xDVdd	-	-	V
High level output voltage	Voh	0.90xDVdd	-	-	V
Low level output voltage	Vol	-	-	0.1xDVdd	V
Input Leakage Current (AC-Link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-Link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	4		mA

Table 3. AC-Link Static Specifications

3.1.5. STAC9756 Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
Line Inputs	-	1.0	-	Vrms
Mic Inputs (Note 1)	-	0.1	-	Vrms
Full Scale Output Voltage:				
Line Output	-	1.0	-	Vrms
Analog S/N:				
CD to LINE_OUT	90	98	-	dB
Other to LINE_OUT	-	98	-	dB
Analog Frequency Response (Note 2)	20	-	20,000	Hz
Digital S/N (Note 3)				
D/A	85	96	-	dB
A/D	75	86	-	dB
Total Harmonic Distortion:				
Line Output (Note 4)	-	-	0.02	%
D/A & A/D Frequency Response (Note 5)	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	-	Hz
Stop Band Rejection (Note 6)	85	-	-	dB
Out-of-Band Rejection (Note 7)	-	40	-	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1kHz)	-	40	-	dB
Crosstalk between Input channels	-	-	70	dB

Table 4. STAC9756 Analog Performance Characteristics

Parameter	Min	Typ	Max	Unit
Spurious Tone Rejection	-	100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance	10	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.45 x AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	10	50	mV
Deviation from Linear Phase	-	-	1	deg.
Analog Output Load Capacitance	-	-	50	pF
Analog Output Load Resistance	10	-	-	KΩ
Mute Attenuation	90	96	-	dB

Table 4. STAC9756 Analog Performance Characteristics (Continued)

Note:
1. With +20 dB Boost on, 1.0Vrms with Boost off
2. ± 1 dB limits
3. The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
4. 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

3.1.6. STAC9757 Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
Line Inputs	-	1.0	-	Vrms
Mic Inputs (Note 1)	-	0.1	-	Vrms
Full Scale Output Voltage:				
Line Inputs to LINE_OUT @ Gain Setting of -6 dB	-	0.5	-	Vrms
PCM to LINE_OUT	-	0.5	-	Vrms
MIC Inputs to LINE_OUT	-	0.5	-	Vrms
Analog S/N:				
CD to LINE_OUT	-	90	-	dB
Other to LINE_OUT	-	90	-	dB
Analog Frequency Response (Note 2)	20	-	20,000	Hz

Table 5. STAC9757 Analog Performance Characteristics

Parameter	Min	Typ	Max	Unit
Digital S/N (Note 3)				
D/A	85	90	-	dB
A/D	75	85	-	dB
Total Harmonic Distortion: Line Output (Note 4)	-	-	0.02	%
D/A & A/D Frequency Response (Note 5)	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	-	Hz
Stop Band Rejection (Note 6)	85	-	-	dB
Out-of-Band Rejection (Note 7)	-	40	-	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1kHz)	-	40	-	dB
Crosstalk between Input channels	-	-	70	dB
Spurious Tone Rejection	-	100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance	10	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.41 x AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ ^{o}C
DAC Offset Voltage	-	10	50	mV
Deviation from Linear Phase	-	-	1	degree
Analog Output Load Capacitance	-	-	50	pF
Analog Output Load Resistance	10	-	-	KΩ
Mute Attenuation	90	96	-	dB

Table 5. STAC9757 Analog Performance Characteristics (Continued)

Note:
1. With +20 dB Boost on, 1.0Vrms with Boost off
2. ± 1 dB limits
3. The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
4. 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

3.2. AC Timing Characteristics

($T_{ambient}$ = 25 °C, AVdd = 3.3V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss+0V; 50pF external load)

3.2.1. Cold Reset

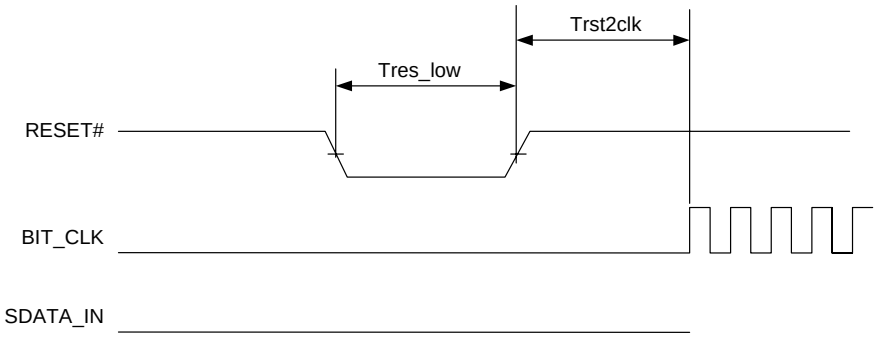


Figure 2. Cold Reset Timing

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	Tres_low	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	Trst2clk	+1.0	-	-	ns

Table 6. Cold Reset Specifications

Note: BIT_CLK and SDATAIN are in a high impedance state during reset.

3.2.2. Warm Reset

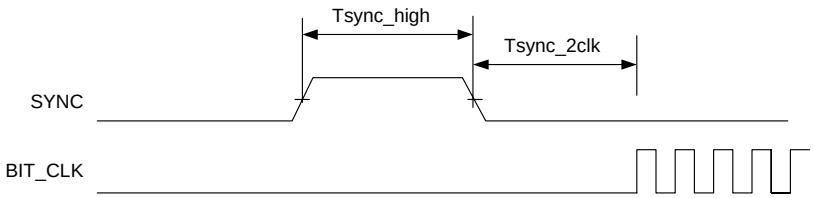


Figure 3. Warm Reset Timing

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	Tsync_high	1.0	1.3	-	us
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8	-	-	ns

Table 7. Warm Reset Specifications

3.2.3. Clocks

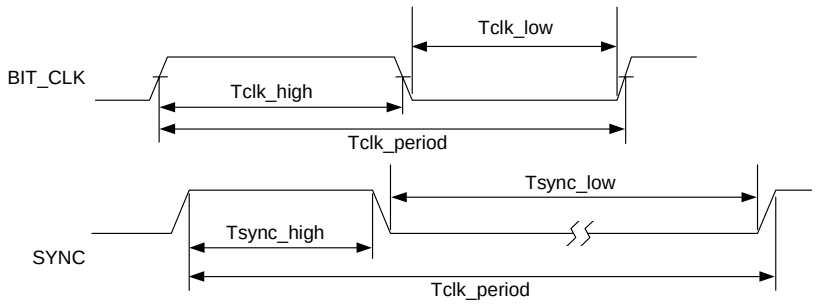


Figure 4. Clocks Timing

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	750	-	ps
BLT_CLK high pulsewidth (Note 8)	Tclk_high	32.56	40.7	48.84	ns
BIT_CLK low pulse width (Note 8)	Tclk_low	32.56	40.7	48.84	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low_pulse width	Tsync_low	-	19.5	-	us

Note: 8. Worst case duty cycle restricted to 40/60.

Table 8. Clocks Specifications

3.2.4. Data Setup and Hold

(50pF external load)

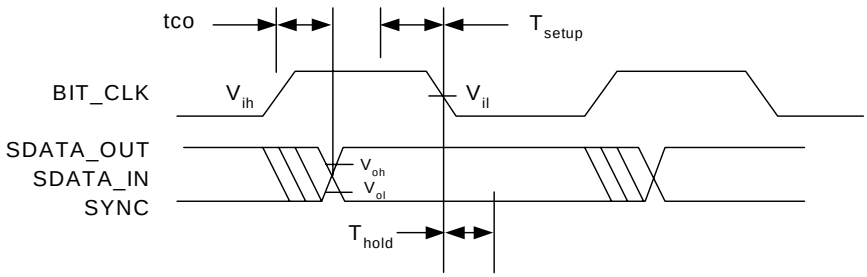


Figure 5. Data Setup and Hold Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	Tsetup	15.0	-	-	ns
Hold from falling edge of BIT_CLK	Thold	5.0	-	-	ns

Note: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

Table 9. Data Setup and Hold Specifications

3.2.5. Signal Rise and Fall Times

(50pF external load; from 10% to 90% of Vdd)

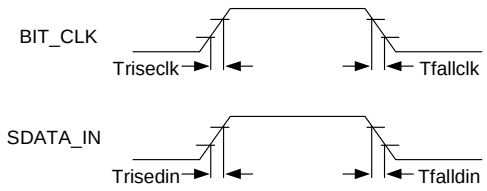


Figure 6. Signal Rise and Fall Times Timing

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	Triseclk	2	-	6	ns
BIT_CLK fall time	Tfallclk	2	-	6	ns
SDATA_IN rise time	Trisedin	2	-	6	ns
SDATA_IN fall time	Tfalldin	2	-	6	ns

Table 10. Signal Rise and Fall Times Specifications

3.2.6. AC-Link Low Power Mode Timing

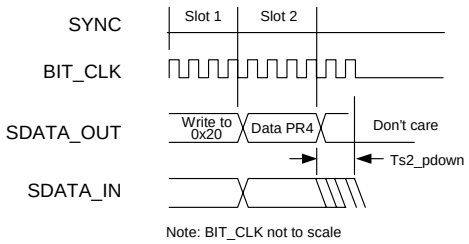


Figure 7. AC-Link Low Power Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	us

Table 11. AC-Link Low Power Mode Timing Specifications

3.2.7. ATE Test Mode

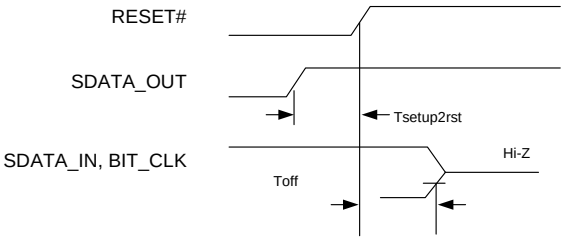


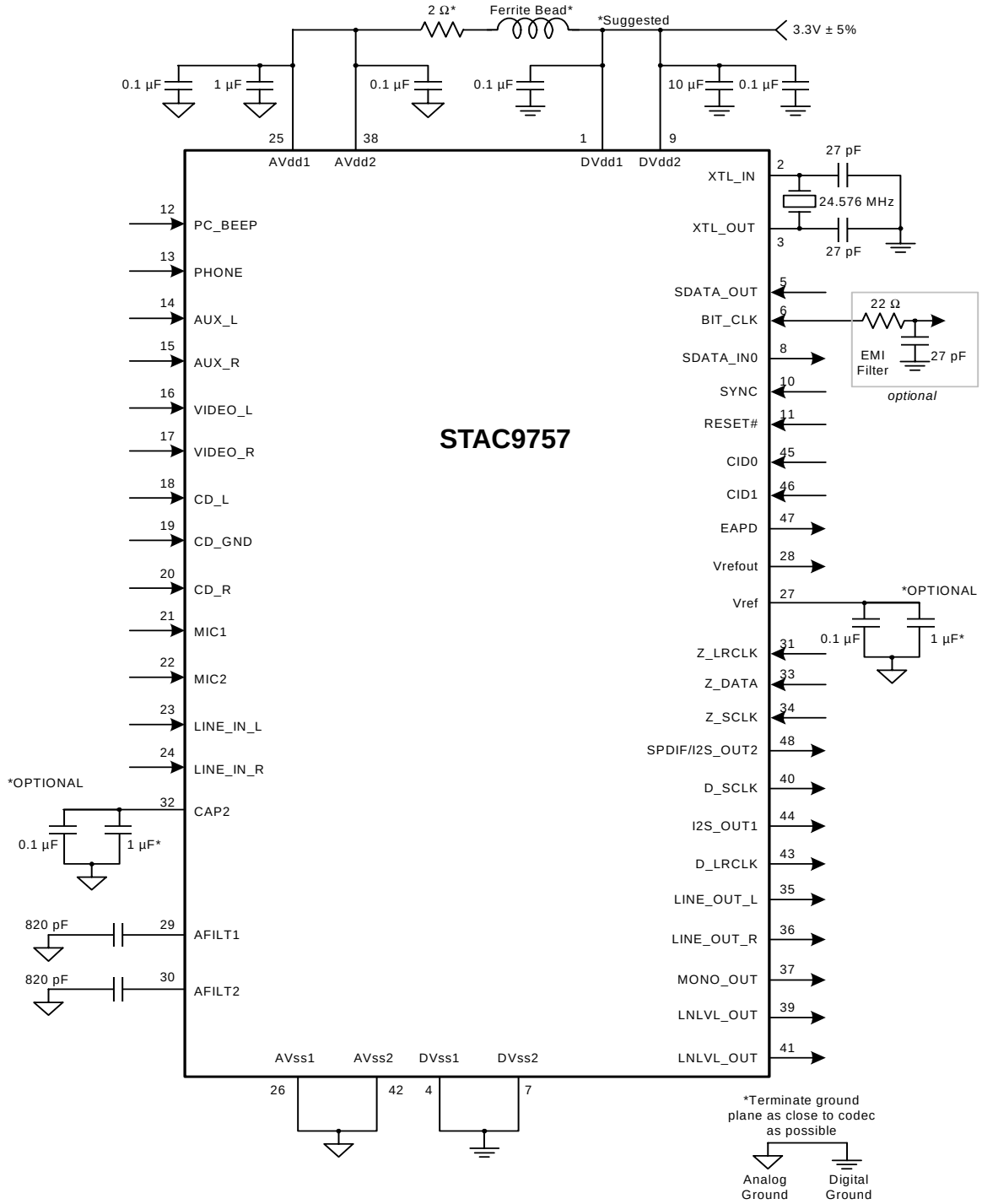
Figure 8. ATE Test Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Table 12. ATE Test Mode Specifications

Note:
1. All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes STAC9756/57 AC-Link outputs to go high impedance which is suitable for ATE in circuit testing.
2. Once the test mode has been entered, the STAC9756/57 must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.
3. # denotes active low.

4. TYPICAL CONNECTION DIAGRAM (3.3V OPERATION)



Note: 1. See Appendix B for specific connection requirements prior to operation.
2. See Figure 24 on page 58 for split supply connections.

Figure 9. STAC9757 Typical Connection Diagram

5. AC-LINK

Figure 10 shows the AC-Link point to point serial interconnect between the STAC9756/57 and its companion controller. All digital audio streams and command/status information are communicated over this AC-Link. See "Digital Interface" on page 19 for details.

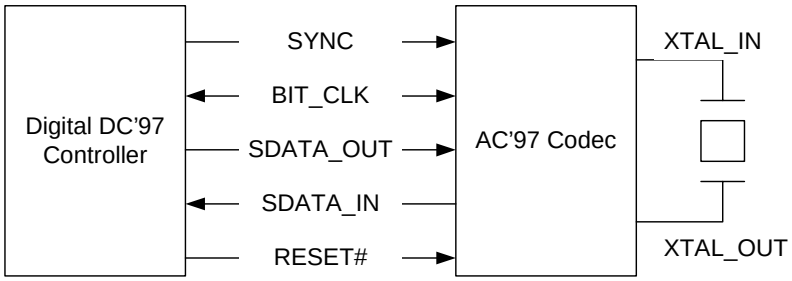


Figure 10. AC-Link to its Companion Controller

5.1. Clocking

STAC9756/57 derives its clock internally from an externally connected 24.576 MHz crystal or an oscillator through the XTAL_IN pin. Synchronization with the AC'97 controller is achieved through the BIT_CLK pin at 12.288 MHz.

The beginning of all audio sample packets, or "Audio Frames", transferred over AC-Link is synchronized to the rising edge of the "SYNC" signal driven by the AC'97 controller. Data is transitioned on AC-Link on every rising edge of BIT_CLK, and subsequently sampled by the receiving side on each immediately following falling edge of BIT_CLK.

5.2. Reset

There are 3 types of resets:

1. a "cold" reset where all STAC9756/57 logic and registers are initialized to their default state
2. a "warm" reset where the contents of the STAC9756/57 register set are left unaltered
3. a "register" reset which only initializes the STAC9756/57 registers to their default states

After signaling a reset to the STAC9756/57**,** the AC'97 controller should not attempt to play or capture audio data until it has sampled a "Codec Ready" indication via register 26h from the STAC9756/57**.**

For proper reset operation SDATA_OUT should be "0" during "cold" reset.

6. DIGITAL INTERFACE

6.1. AC-Link Digital Serial Interface Protocol

The STAC9756/57 communicates to the AC'97 controller via a 5-pin digital serial AC-Link interface, which is a bi-directional, fixed rate, serial PCM digital stream. All digital audio streams, commands and status information are communicated over this point-to-point serial interconnect. The AC-Link handles multiple inputs, and output audio streams, as well as control register accesses using a time division multiplexed (TDM) scheme. The AC'97 controller synchronizes all AC-Link data transaction. Table 13 shows the data streams available on the STAC9756/57**:**

PCM Playback	2 output slots	2 Channel composite PCM output stream
PCM Record data	2 input slots	2 Channel composite PCM input stream
Control	2 output slots	Control register write port
Status	2 input slots	Control register read port

Table 13. STAC9756/57 Available Data Streams

Synchronization of all AC-Link data transactions is handled by the AC'97 controller. The STAC9756/57 drives the serial bit clock onto AC-Link. The AC'97 controller then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-Link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-Link data, STAC9756/57 for outgoing data and AC'97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-Link protocol provides for a special 16-bit (13-bits defined, with 3 reserved trailing bit positions) time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "tagged" invalid, it is the responsibility of the source of the data, (STAC9756/57 for the input stream, AC'97 controller for the output stream), to stuff all bit positions with 0's during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Additionally, for power savings, all clock, sync, and data signals may be halted by the controller.

6.1.1. AC-Link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the STAC9756/57 DAC inputs, and control registers. Each audio output frame supports up to twelve 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits that are used for AC-Link protocol infrastructure.

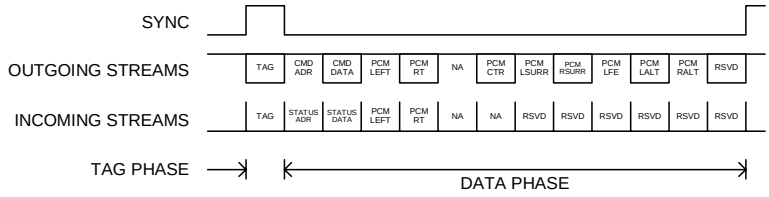


Figure 11. AC'97 Standard Bi-directional Audio Frame

Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by the STAC9756/57 indicate which of the corresponding 12 times slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-Link at its fixed 48kHz audio frame rate. The following diagram illustrates the time slot based AC-Link protocol.

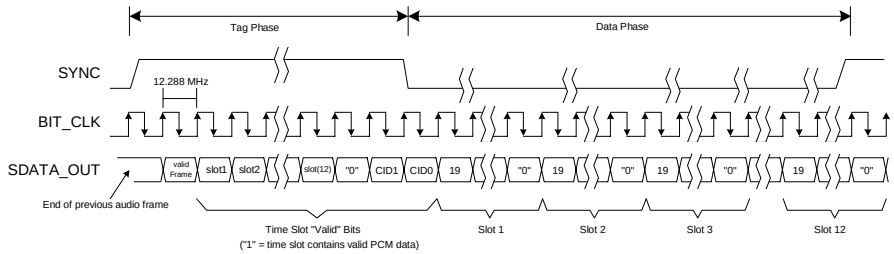


Figure 12. AC-Link Audio Output Frame

A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the STAC9756/57 samples the assertion of SYNC. This following edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC'97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK, and subsequently sampled by the STAC9756/57 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

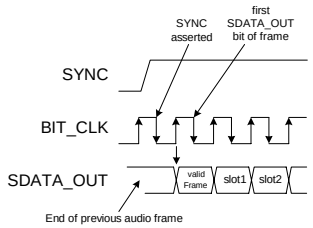


Figure 13. Start of an Audio Output Frame

SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions stuffed with 0's by the AC'97 controller.

When mono audio sample streams are sent from the AC'97 controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

6.1.1.1. Slot 1: Command Address Port

The command port is used to control features, and monitor status (see Audio Input Frame Slots 1 and 2) of the STAC9756/57 functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to sixty-four 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid. Odd accesses are considered invalid and return 0 0 0 0.

Audio output frame slot 1 communicates control register address, and write/read command information to the STAC9756/57.

Bit	Description	Comments
19	Read/Write command	1= read, 0=write
18:12	Control Register Index	sixty-four 16-bit locations, addressed on even byte boundaries
11:0	Reserved	Stuffed with 0's

Table 14. Command Address Port Bit Assignments

The first bit (MSB) sampled by STAC9756/57 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0's by the AC'97 controller.

6.1.1.2. Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19).

Bit	Description	Comments
19:4	Control Register Write Data	Stuffed with 0's if current operation is a read
3:0	Reserved	Stuffed with 0's

Table 15. Command Data Port Bit Assignments

If the current command port operation is a read then the entire slot time must be stuffed with 0's by the AC'97 controller.

6.1.1.3. Slot 3: PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical "Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is trans-

ferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

6.1.1.4. Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical "Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

6.1.1.5. Slot 5: Reserved

Audio output frame slot 5 is reserved for modem operation and is not used by the STAC9756/57.

6.1.1.6. Slot 6: PCM Center Channel

Audio output frame slot 6 is the composite digital audio center stream used in a multi-channel application where the STAC9756/57 is programmed to accept the primary DAC PCM data from slots 6 and 9. Please refer to the register programming section for details on the multi-channel programming options.

6.1.1.7. Slot 7: PCM Left Surround Channel

Audio output frame slot 7 is the composite digital audio left surround stream. As a programming option, PCM data from slots 7 and 8 may be used to supply data to the primary DACs. Please refer to the register programming section for details on the multi-channel programming options.

6.1.1.8. Slot 8: PCM Right Surround Channel

Audio output frame slot 8 is the composite digital audio right surround stream. As a programming option, PCM data from slots 7 and 8 may be used to supply data to the primary DACs. Please refer to the register programming section for details on the multi-channel programming options.

6.1.1.9. Slot 9: PCM Low Frequency Channel

Audio output frame slot 9 is the composite digital audio low frequency stream used in a multi-channel application where the STAC9756/57 is programmed to accept the primary DAC PCM data from slots 6 and 9. Please refer to the register programming section for details on the multi-channel programming options.

6.1.1.10. Slot 10: PCM Alternate Left

Audio output frame slot 10 is the composite digital audio alternate left stream used in a multi-channel applications. Please refer to the register programming section for details on the multi channel programming options.

6.1.1.11. Slot 11: PCM Alternate Right

Audio output frame slot 11 is the composite digital audio alternate right stream used in a multi-channel applications. Please refer to the register programming section for details on the multi channel programming options.

6.1.1.12. Slot 12: Reserved

Audio output frame slot 12 is reserved for modem operations and is not used by the STAC9756/57.

6.1.2. AC-Link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-Link audio input frame consists of 12, 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits that are used for AC-Link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the STAC9756/57 is in the "Codec Ready" state or not. If the "Codec Ready" bit is a 0, this indicates that STAC9756/57 is not ready for normal operation. This condition is normal following the de-assertion of power on reset, for example, while STAC9756/57's voltage references settle. When the AC-Link "Codec Ready" indicator bit is a 1, it indicates that the AC-Link and STAC9756/57 control/status registers are in a fully operational state. The AC'97 controller must further probe the Power-down Control Status Register (refer to Mixer Register section) to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting STAC9756/57 into operation the AC'97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that STAC9756/57 has become "Codec Ready". Once the STAC9756/57 is sampled "Codec Ready", the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. The following diagram illustrates the time slot based AC-Link protocol.

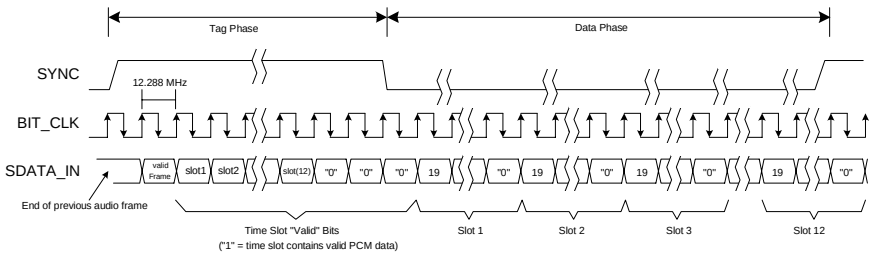


Figure 14. STAC9756/57 Audio Input Frame

A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. Immediately following the falling edge of BIT_CLK, the STAC9756/57 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the STAC9756/57 transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented

to AC-Link on a rising edge of BIT_CLK and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

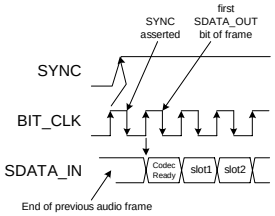


Figure 15. Start of an Audio Input Frame

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0's by STAC9756/57. SDATA_IN data is sampled on the falling edges of BIT_CLK.

6.1.2.1. Slot 1: Status Address Port

The status port is used to monitor status for STAC9756/57 functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by STAC9756/57 during slot 0)

Bit	Description	Comments
19	Reserved	Stuffed with 0's
18:12	Control Register Index	Echo of register index for which data is being returned
11:0	On Demand DAC Slot Request Bits	0 = send data, 1 = do NOT send data
	11	Slot 3 request: PCM Left Channel
	10	Slot 4 request: PCM Right Channel
	9	Slot 5 request: Modem Line 1
	8	Slot 6 request: PCM Center
	7	Slot 7 request: PCM Left Surround
	6	Slot 8 request: PCM Right Surround
	5	Slot 9 request: PCM LFE
	4	Slot 10 request: Modem Line 2 or PCM Left (n+1)
	3	Slot 11 request: Modem Handset or PCM Right (n+1)
	2	Slot 12 request: PCM Center (n+1)
	1,0	Reserved (set to 0)

Table 16. Status Address Port Bit Assignments

6.1.2.2. Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Bit	Description	Comments
19:4	Control Register Read Data	Stuffed with 0's if tagged "invalid"
3:0	Reserved	Stuffed with 0's

Table 17. Status Data Port Bit Assignments

If Slot 2 is tagged "invalid" by STAC9756/57**,** then the entire slot will be stuffed with 0's.

6.1.2.3. Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of STAC9756/57 input MUX, post-ADC.

STAC9756/57 ADCs are implemented to support 18-bit resolution.

STAC9756/57 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

6.1.2.4. Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of STAC9756/57 input MUX, post-ADC.

STAC9756/57 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

6.1.2.5. Slots 5-12: Reserved

Audio input frame slots 5-12 are not used by the STAC9756/57 and are always stuffed with 0's.

6.2. AC-Link Low Power Mode

The **STAC9756/57** AC-Link can be placed in the low power mode by programming register 26h to the appropriate value. Both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level. The AC'97 controller can wake up the **STAC9756/57** by providing the appropriate reset signals.

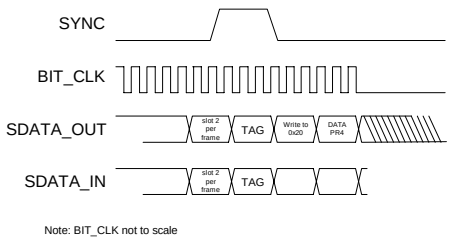


Figure 16. STAC9756/57 Powerdown Timing

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-Link into its low power mode, slots (1 and 2) are assumed to be the only valid stream in the audio output frame (all sources of audio input have been neutralized).

The AC'97 controller should also drive SYNC, and SDATA_OUT low after programming the **STAC9756/57** to this low power mode.

6.2.1. Waking up the AC-Link

Once the STAC9756/57 has halted BIT_CLK, there are only two ways to "wake up" the AC-Link. Both methods must be activated by the AC'97 controller. The AC-Link protocol provides for a "Cold AC'97 Reset", and a "Warm AC'97 Reset". The current power down state would ultimately dictate which form of reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset register) is performed, wherein the AC'97 registers are initialized to their default values, registers are required to keep state during all power down modes. Once powered down, re-activation of the AC-Link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-Link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

Cold Reset - a cold reset is achieved by asserting RESET# for the minimum specified time, and then bringing RESET# back HIGH. The reset occurs on the rising edge when RESET# is deasserted. By asserting and deasserting RESET#, BIT_CLK and SDATA_IN will be activated, or re-activated as the case may be, and all STAC9756/57 control registers will be initialized to their default power on reset values.

Note: RESET# is an asynchronous input. (# denotes active low)

Warm Reset - a warm reset will re-activate the AC-Link without altering the current STAC9756/57 register values. A warm reset is signaled by driving SYNC high for a minimum of 1us in the absence of BIT_CLK.

Note: Within normal audio frames, SYNC is a synchronous input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the STAC9756/57.

6.3. I2S (ZV_PORT) Digital Audio Interface

The I2S input is controlled by registers and Figure 17 shows the standard I2S interface timing. See the register section for details on programming the ZV_Port.

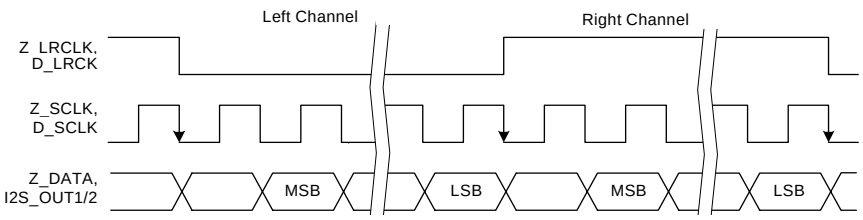


Figure 17. I2S Digital Audio Interface

7. STAC9756/57 MIXER

The STAC9756/57 includes analog and digital mixers for maximum flexibility. The analog mixer is designed to the AC'97 specification to manage the playback and record of all digital and analog audio sources in the PC environment. The analog mixer also includes several extensions of the AC'97 specification to support "all analog record" capability as well as "POP BYPASS" mode for all digital playback. The analog sources include:

- **System Audio**: digital PCM input and output for business, games and multimedia
- **CD/DVD**: analog CD/DVD-ROM audio with internal connections to Codec mixer
- **Mono microphone**: choice of desktop mic, with programmable boost and gain
- **Speakerphone**: use of system mic and speakers for telephone, DSVD, and video conferencing
- **Video**: TV tuner or video capture card with internal connections to Codec mixer
- **AUX/synth**: analog FM or wavetable synthesizer, or other internal source

The digital mixer includes inputs for the PCM DAC, the recorded ADC output, and the I2S ZV_Port data.

Z_DATA: I2S digital audio stream from the PC-CARD slot of notebook computers

Source	Function	Connection
PC_Beep	PC beep pass thru	from PC beeper output
PHONE	speakerphone or DLP in	from telephony subsystem
MIC1	desktop microphone	from mic jack
MIC2	second microphone	from second mic jack
LINE_IN	external audio source	from line-in jack
CD	audio from CD-ROM	cable from CD-ROM
VIDEO	audio from TV tuner or video camera	cable from TV or VidCap card
AUX	upgrade synth or other external source	internal connector
PCM out	digital audio output from AC'97 Controller	AC-Link
LINE_OUT	stereo mix of all sources	To output jack
DAC_OUT	surround stereo DAC output	to output jack
MONO_OUT	mic or mix for speakerphone or DLP out	to telephony subsystem
PCM in	digital data from the codec to the AC'97 Controller	AC-Link
I2S_OUT1	I2S digital output	To I2S output connector
Z_DATA	I2S digital input from secondary PC-CARD ZV-Port source	From I2S PC-CARD source
SPDIF/I2S_OUT2	I2S or SPDIF digital audio output	To I2S or SPDIF output connector

Table 18. STAC9756/57 Mixer

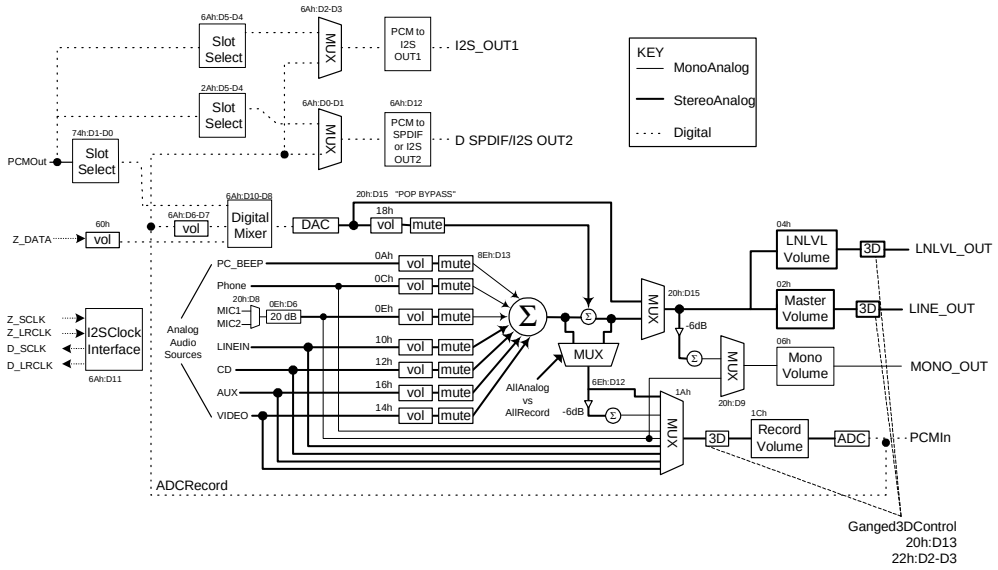


Figure 18. STAC9756 5V Analog Mode, 2-Channel Mixer Functional Diagram

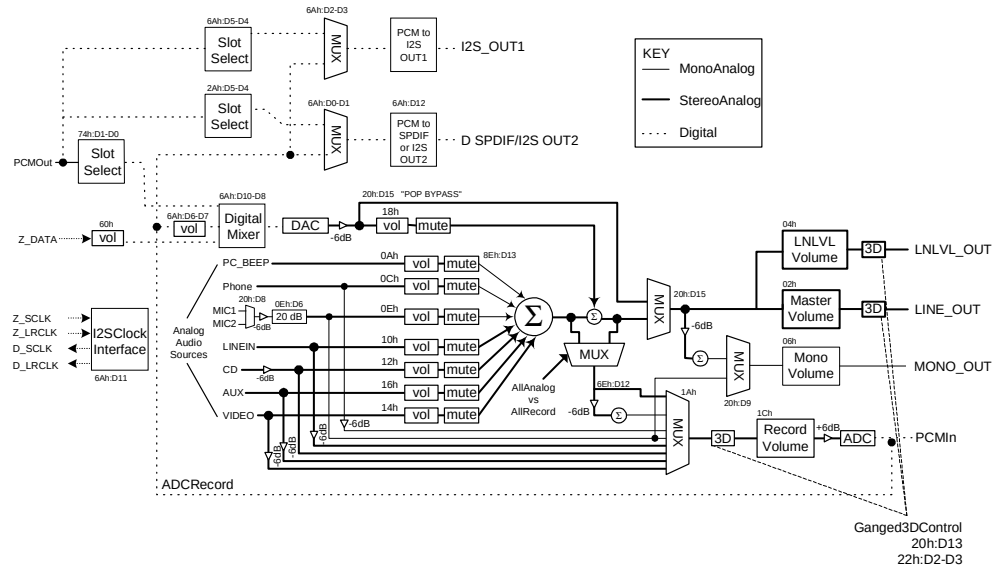


Figure 19. STAC9756 +3.3V Analog Mode and STAC9757 2-Channel Mixer Functional Diagram

7.1. Analog Mixer Input

The mixer provides recording and playback of any audio sources or output mix of all sources. The STAC9756/57 supports the following input sources:

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input w/mono output reference (mic + stereo mix)

Note: All unused inputs should be tied together and have a capacitor (0.1 µF suggested) to ground.

7.2. Mixer Analog Output

The mixer generates three distinct outputs:

- a stereo mix of all sources for output to the LINE_OUT
- a stereo mix of all sources for output to LNLVL_OUT
- a mono, mic only or mix of all sources for MONO_OUT

Note:Mono output of stereo mix is attenuated by -6 dB.

7.3. Mixer Digital Input

The digital mixer includes inputs for the PCM DAC, the recorded ADC output, and a single I2S ZV_PORT digital input. The ZV_Port input is generally used for the audio input from ZoomVideo enabled PC-CARDS for notebook computers. External DVD disk players and video capture cards are examples of typical ZoomVideo enabled PC-CARDS.

7.4. Mixer Digital Output

The STAC9756/57 SPDIF/I2S_OUT2 dual mode digital output supports both I2S and SPDIF formats. Only one format can be supported at a time. A multiplexer determines which of two input digital input streams are used for the digital output conversion process. These three streams include the PCM OUT data from the audio controller and the ADC recorded output. The normal analog LINE_OUT signal can be converted to the I2S or SPDIF formats by using the internal ADC to record the 'MIX" output which is the combination of all analog and all digital sources. Alternately, only the analog sources can be recorded using the ADC and then routed to the digital output to support docking schemes while the POP_BYPASS mode is used to route the DAC output directly to the LINE_OUT, avoiding the mixer altogether. In the case of digital controllers with support for 4 or more channels, the SPDIF output mode can be used to support compressed 6-channel output streams for delivery to home theater systems. Modern applications such as soft DVD decoders often generate compressed audio streams. These can be routed on alternate AC-Link slots to the SPDIF output, while the standard 2-channel output is delivered via slots 3 and 4 to the analog stereo outputs. If the digital controller supports 6 channels, a SPDIF output with 4 analog channels can also be configured.

7.5. PC Beep Implementation

PC Beep is active on power up and defaults to an un-muted state. The PC-BEEP input is routed directly to the MONO_OUT, LINE_OUT and LNLVL_OUT pins of the codec. Because the PC_BEEP input drive is often a full scale digital signal, some resistive attenuation of the PC_BEEP input is recommended to keep the beep tone within reasonable volume levels. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the lineout during normal operation.

7.6. Programming Registers

Address	Name	Default	Location
00h	Reset	6940h	7.6.1; page 31
02h	Master Volume	8000h	7.6.2.1; page 31
04h	LNLVL Volume	8000h	7.6.2.2; page 32 and 35
06h	Master Volume MONO	8000h	7.6.2.3; page 32
0Ah	PC Beep Mixer Volume	0000h	7.6.3; page 32
0Ch	Phone Mixer Volume	8008h	7.6.4.1; page 33
0Eh	Mic Mixer Volume	8008h	7.6.4.2; page 33
10h	Line In Mixer Volume	8808h	7.6.4.3; page 33
12h	CD Mixer Volume	8808h	7.6.4.4; page 33
14h	Video Mixer Volume	8808h	7.6.4.5; page 34
16h	Aux Mixer Volume	8808h	7.6.4.6; page 34
18h	PCM Out Mixer Volume	8808h	7.6.4.7; page 34
1Ah	Record Select	0000h	7.6.5; page 34
1Ch	Record Gain	8000h	7.6.6; page 35
20h	General Purpose	0000h	7.6.7; page 35
22h	3D Control	0000h	7.6.8; page 36
26h	Powerdown Ctrl/Stat	000Fh	7.6.9; page 36
28h	Extended Audio ID	0205h	7.6.10; page 37
2Ah	Extended Audio Control/Status	0400h	7.6.11; page 38
2Ch	PCM DAC Rate	BB80h	7.6.12.1; page 40
32h	PCM LR ADC Rate	BB80h	7.6.12.2; page 40
3Ah	SPDIF Control	2A00h	7.6.14.1; page 42
60h	Z_Data Volume	8808h	7.6.13; page 40
6Ah	Digital Audio Control	0000h	7.6.14; page 41
6Ch	Revision Code	0000h	7.6.15; page 42
6Eh	Analog Special	1000h	7.6.16; page 43
70h	72h Enable	0000h	7.6.16.1; page 43
72h	Analog Current Adjust	0000h	7.6.16.2; page 43
74h	Multi-Channel Selection	0000h	7.6.17; page 44
76h	78h Enable	0000h	7.6.18.1; page 46
78h	Clock Access	0000h	7.6.18.2; page 46
7Ch	Vendor ID1	8384h	7.6.19.1; page 47
7Eh	Vendor ID2	7656h	7.6.19.2; page 47

Table 19. Programming Registers

7.6.1. Reset (00h)

Default: 6940h

D15	D14	D13	D12	D11	D10	D9	D8
RSRVD4	SE4	SE3	SE2	SE1	SE0	ID9	ID8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part.

7.6.2. Play Master Volume Registers (Index 02h, 04h, and 06h)

These registers manage the output signal volumes. Register 02h controls the stereo LINE_OUT master volume (both right and left channels), register 04h controls the LNLVL_OUT master volume, and register 06h controls the MONO volume output. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. ML5 through ML0 is for left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel. When bits D5 and D13 are set in any of these registers it automatically writes all 1's to the next lower 5-bits.

The default value is 8000h for registers 02h, 04h, and 06h, which corresponds to 0 dB attenuation with mute on.

Mute	Mx5…Mx0	Function	Range
0	00 0000	0dB Attenuation	Req.
0	01 1111	46.5 Attenuation	Req.
1	xx xxxx	∞ dB Attenuation	Req.

Table 20. Play Master Volume Register

7.6.2.1. Master Volume (02h)

Default: 8000h

Note: If optional bits D13, D5 of register 02h or D5 of register 06h are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RSRVD	ML5	ML4	ML3	ML2	ML1	ML0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED		MR5	MR4	MR3	MR2	MR1	MR0

7.6.2.2. LNLVL Mixer Volume (04h)

Default: 8000h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RSRVD	ML5	ML4	ML3	ML2	ML1	ML0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED		MR5	MR4	MR3	MR2	MR1	MR0

7.6.2.3. Master Volume MONO (06h)

Default: 8000h

Note: If optional bits D13, D5 of register 02h or D5 of register 06h are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED		MM5	MM4	MM3	MM2	MM1	MM0

7.6.3. PC Beep Mixer Volume (Index 0Ah)

Default: 0000h

Note: PC_BEEP default to 0000h, mute off.

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			PV3	PV2	PV1	PV0	RSRVD

This register controls the level for the PC Beep input. Each step corresponds to approximately 3 dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel is set at -∞ dB. PC_BEEP supports motherboard implementations. The intention of routing PC_BEEP through the STAC9756/57 mixer is to eliminate the requirement for an onboard speaker by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times. NOTE: the PC_BEEP is routed to the mono outputs even when the STAC9756/57 is in a RESET state. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. For further PC_BEEP implementation details please refer to the AC'97 Technical FAQ sheet. The default value can be 0000h, which corresponds to 0 dB attenuation with mute off.

Mute	PV3…PV0	Function
0	0000	0 dB Attenuation
0	1111	45 dB Attenuation
1	xxxx	∞ dB Attenuation

Table 21. PC_BEEP Register

7.6.4. Analog Mixer Input Gain Registers (Index 0Ch - 18h)

These registers control the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. Register 0Eh (Mic Volume Register) has an extra bit that is for a 20 dB boost. When bit 6 is set to 1, the 20 dB boost is on. The default value for stereo registers is 8808h, corresponding to 0 dB gain with mute on.

Mute	Gx4…Gx0	Function
0	00000	+12 dB gain
0	01000	0 dB gain
0	11111	-34.5 dB gain

Table 22. Analog Mixer Input Gain Register

7.6.4.1. Phone Mixer Volume (0Ch)

Default: 8008h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GN4	GN3	GN2	GN1	GN0

7.6.4.2. Mic Mixer Volume (0Eh)

Default: 8008h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED						
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RSRVD	20dB	RSRVD	GN4	GN3	GN2	GN1	GN0

7.6.4.3. Line In Mixer Volume (10h)

Default: 8808h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.6.4.4. CD Mixer Volume (12h)

Default: 8808h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.6.4.5. *Video Mixer Volume (14h)*

Default: 8808h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.6.4.6. *AUX Mixer Volume (16h)*

Default: 8808h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.6.4.7. *PCM Out Mixer Volume (18h)*

Default: 8808h (8888h in secondary mode)

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

7.6.5. *Record Select (1Ah)*

Default: 0000h (corresponding to Mic in)

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED					SL2	SL1	SL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED					SR2	SR1	SR0

Used to select the record source independently for right and left.

SR2…SR0	Right Record Source	SL2…SL0	Left Record Source
0	Mic	0	Mic
1	CD In (right)	1	CD In (L)
2	Video In (right)	2	Video In (L)
3	Aux In (right)	3	Aux In (L)
4	Line In (right)	4	Line In (L)
5	Stereo Mix (right)	5	Stereo Mix (L)
6	Mono Mix	6	Mono Mix
7	Phone	7	Phone

Table 23. Record Select Control Registers

7.6.6. Record Gain (1Ch)

Default: 8000h (corresponding to 0 dB gain with mute on)

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED			GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				GR3	GR2	GR1	GR0

The 1Ch register adjusts the stereo input record gain. Each step corresponds to 1.5 dB. 22.5 dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at -∞ dB.

Mute	Gx3… Gx0	Function
0	1111	+22.5 dB gain
0	0000	0 dB gain
1	xxxx	-∞ gain

Table 24. Record Gain Registers

7.6.7. General Purpose (20h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
POP BYP	RSRVD	3D	RESERVED			MIX	MS
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LPBK	RESERVED						

This register is used to control some miscellaneous functions. Table 25 gives a summary of each bit and its function. The MS bit controls the mic selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-Link, allowing for full system performance measurements.

Bit	Function
3D	3D Stereo Enhancement on/off 1 = on
MIX	Mono output select 0 = Mix, 1= Mic
MS	Mic select 0 = Mic1, 1 = Mic2
POP BYP	DAC bypasses mixer and connects directly to Line Out
LPBK	ADC/DAC loopback mode

Table 25. General Purpose Register

7.6.8. 3D Control (22h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				DP3	DP2	RESERVED	

This register is used to control the 3D stereo enhancement function, ***Sigmatel Surround 3D (SS3D),*** built into the AC'97 component. Note that register bits DP3-DP2 are used to control the separation ratios in the 3D control for LINE_OUT. ***SS3D*** provides for a wider soundstage extending beyond the normal 2-speaker arrangement. Note that the 3D bit in the general purpose register (20h) must be set to 1 to enable SS3D functionality and for the bits in 22h to take effect.

DP3, DP2	LINE_OUT SEPARATION RATIO
0 0	0 (Off)
0 1	3 (Low)
1 0	4.5 (Med)
1 1	6 (High)

Table 26. 3D Control Registers

The three separation ratios are implemented as shown in Table 26. The separation ratio defines a series of equations that determine the amount of depth difference (High, Medium, and Low) perceived during two-channel playback. The ratios provide for options to narrow or widen the soundstage.

7.6.9. Powerdown Ctrl/Stat (26h)

Default: 000Fh

D15	D14	D13	D12	D11	D10	D9	D8
EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED				REF	ANL	DAC	ADC

This read/write register is used to program powerdown states and monitor subsystem readiness. The EAPD external control and GPO is also supported through this register.

Bit	Function
EAPD/GPO	External Amplifier Power Down/General Purpose Output
REF	VREF's up to nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready to playback data
ADC	ADC section ready to playback data

Table 27. Powerdown Status Registers

7.6.9.1. Ready Status

The lower half of this register is read only status, a "1" indicating that the subsection is "ready". Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7.

When the AC-Link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any are ready. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7.

7.6.9.2. Powerdown Controls

The STAC9756/57 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). See the section "Low Power Modes" for more information.

7.6.9.3. External Amplifier Power Down Control

The EAPD bit 15 of the Powerdown Control/Status Register (Index 26h) directly controls the output of the EAPD output, pin 45, and produces a logical "1" when this bit is set to logic high. This function is used to control an external audio amplifier power down. EAPD = 0 places approximately 0V on the output pin, enabling an external audio amplifier. EAPD = 1 places approximately DVdd on the output pin, disabling the external audio amplifier. Audio amplifiers that operate with reverse polarity will likely require an external inverter to maintain software driver compatibility.

7.6.10. Extended Audio ID (28h)

Default: 0205h

D15	D14	D13	D12	D11	D10	D9	D8
ID1	ID0	RESERVED				AMAP	LDAC
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SDAC	CDAC	RESERVED			SPDIF	DRA	VRA

The Extended Audio ID register is a read only register. ID1 and ID0 echo the configuration of the codec as defined by the programming of pins 45 and 46 externally. "00" returned defines the codec as the primary codec, while any other code identifies the codec as one of three secondary codec possibilities. SDAC=0 tells the controller that the STAC9756/57 is a two-channel codec as defined by the Intel spec. The default condition assumes that 0, 0 are loaded in the MC1 and MC0 bits of the Multi-Channel Programming Register (Index 74h). With 0s in the MCx bits, the codec slot assignments are as per the AC'97 specification recommendations. If the MCx bits do not contain 0s, the slot assignments are as per Table 36 in section 7.6.17, describing the Multi-Channel Programming Register (Index 74h). The VRA

bit, D0, will return a 1 indicating that the codec supports the optional variable sample rate conversion as defined by the AC'97 specification.

Bit	Function
IDx	External CID pin status
AMAP	Multi-channel slot support
LDAC	Low Frequency Effect support (always 0)
SDAC	Surround DAC support (always 0)
CDAC	Center channel support (always 0)
SPDIF	SPDIF digital audio support
DRA	Double Rate Audio support (always 0)
VRA	Variable sample rates supported

Table 28. Extended Audio ID Register Functions

7.6.11. Extended Audio Control/Status (2Ah)

Default: 0400h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED					SPCV	RESERVED	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED		SPSA1	SPSA0	RSRVD	SPDIF	RSRVD	VRA enable

7.6.11.1. Variable Rate Sampling Enable

The Extended Audio Status Control register also contains one active bit to enable or disable the Variable Sampling Rate capabilities of the DACs and ADCs. If the VRA, bit D0, is 1 the variable sample rate control registers (2Ch and 32h) are active, and "on-demand" slot data required transfers are allowed. If the VRA bit is 0, the DACs and ADCs will operate at the default 48 kHz data rate.

The **STAC9756/57** supports "on-demand" slot request flags. These flags are passed from the codec to the AC'97 controller in every audio input frame. Each time a slot request flag is set (active low) in a given audio frame, the controller will pass the next PCM sample for the corresponding slot in the audio frame that immediately follows. The VRA enable bit must be set to 1 to enable "on-demand" data transfers. If the VRA enable bit is not set, the codec will default to 48 kHz transfers and every audio frame will include an active slot request flag and data is transferred every frame.

For variable sample rate output, the codec examines its sample rate control registers, the state of the FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits are asserted during the current audio input frame for active output slots, which will require data in the next audio output frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the codec is always the master: for SDATA_IN (codec to controller), the codec sets the TAG bit; for SDATA_OUT (controller to codec), the codec sets the SLOTREQ bit and then

checks for the TAG bit in the next frame. Whenever VRA is set to 0 the PCM rate registers (2Ch and 32h) are overwritten with BB80h (48 kHz).

Note:See Section 7.6.17.1 for digital audio slot select.

7.6.11.2. SPDIF

The SPDIF bit in the Extended Audio Status Control Register is used to enable and disable the SPDIF functionality within the STAC9756/57. If the SPDIF is set to a 1, then the function is enabled and when set to a 0 it is disabled.

7.6.11.3. SPCV (SPDIF Configuration Valid)

The SPCV bit is read only and indicates whether or not the SPDIF system is set up correctly. When SPCV is a 0, it indicates the system configuration is invalid and valid if it is a 1.

7.6.11.4. SPSA1, SPSA0 (SPDIF Slot Assignment)

SPSA1 and SPSA0 combine to provide the slot assignments for the SPDIF data. The following details the slot assignment relationship between SPSA1 and SPSA0.

SPSA[1,0]	Slot Assignment	Comments
00	3 & 4	SPDIF source data slot assignment
01	7 & 8	2-ch codec default
10	6 & 9	4-ch codec default
11	10 & 11	6-ch codec default

Table 29. Slot assignment relationship between SPSA1 and SPSA0

7.6.12. PCM DAC Rate Registers (2Ch and 32h)

The internal sample rate for the DACs and ADCs are controlled by the value in these read/write registers that contain a 16-bit unsigned value between 0 and 65535 representing the conversion rate in Hz. In VRA mode (register 2Ah bit D0 = 1), if the value written to these registers is supported that value will be echoed back when read, otherwise the closest (higher in the case of a tie) sample rate is supported and returned. Per PC 99 / PC 2001 specification, independent sample rates are supported for record and playback. Whenever VRA is set to 0 the PCM rate registers (2Ch and 32h) will readback BB80h (48 kHz).

Sample Rate	SR15-SR0 Value
8 kHz	1F40h
11.025 kHz	2B11h
16 kHz	3E80h
22.05 kHz	5622h
44.1 kHz	AC44h
48 kHz	BB80h

Table 30. Hardware Supported Sample Rates

7.6.12.1. PCM DAC Rate (2Ch)

Default: BB80h

D15	D14	D13	D12	D11	D10	D9	D8
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

7.6.12.2. PCM LR ADC Rate (32h)

Default: BB80h

D15	D14	D13	D12	D11	D10	D9	D8
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

7.6.13. Z_DATA Volume (60h)

Default: 8000h

D15	D14	D13	D12	D11	D10	D9	D8
Mute	RESERVED		GL4	GL3	GL2	GL1	GL0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED			GR4	GR3	GR2	GR1	GR0

This register controls the gain/attenuation mix of the Z_DATA I2S digital input. The I2S digital input has a mute and volume control. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. The default value for this stereo register is 8000h corresponding to 0 dB gain with mute on.

Mute	Gx4…Gx0	Function
0	00000	0 dB gain
0	11111	-46.5 dB gain
1	xxxxx	-∞ dB gain

Table 31. Z_Data Register

7.6.14. Digital Audio Control (6Ah)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED			I2S SEL	I2S ENA	ZVP ENA	ADC ENA	PCM DIS
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ADMIX GAIN1	ADMIX GAIN0	I2S SSL1	I2S SSL0	DO3	DO2	DO1	DO0

Bit(s)	Name	Description
15:13	Rsrvd	Reserved
12	I2S SEL	Selects I2S_OUT2(1) or SPDIF(0 defaul) output format from D_SPDIF/I2S_OUT2
11	I2S ENA	Enables the I2S outputs
10	ZVP ENA	Enables the ZV_Port data from Z_DATA
9	ADC ENA	Enables the ADC record input
8	PCM DIS	Disables the PCM input
7:6	ADMIX GAIN[1,0]	00 = 0dB = 0.75, 01 = -3.5dB = 0.5, 10 = -9.5dB = 0.25, 11 = +2.5dB = 1.0
5:4	I2S SLS[1,0]	00 = 3 & 4, 01 = 7 & 8, 10 = 6 & 9, 11 = 10 & 11
3:2	DO[3,2]	ADC, or PCM data muxed to I2S_OUT1
1:0	DO[1,0]	ADC, or PCM data muxed to D_SPDIF/I2S_OUT2

Note: 1. I2S OUT2 slot assignment is controlled by SPSA[1,0] in Reg 2Ah.
2. See Section 7.6.17.1 for digital slot selection.

Table 32. Digital Audio Control (6Ah) Registers

This read/write register is used to program the digital mixer input status. In the default state, the PCM DAC path is enabled and the I2S Z_DATA and the ADC record inputs are disabled. The PCM DIS bit is used to disable the PCM DAC input. The ADC ENA bit is used to enable the ADC recorded input. The I2S ENA bit is used to enable the I2S Z_DATA input. The I2S_SEL bit is used to switch between the default SPDIF digital output mode and the alternate I2S output mode available at pin-48. The I2S ENA bit enables the ZV_PORT, ZV_DATA line. ADMIX GAIN1 and ADMIX GAIN0 bits control the ADC gain through the digital mixer to the DAC.

The DOx pins control the input source for the PCM to digital output converters. Table 33 describes the four available options.

I2S_OUT1 DO3, DO2	I2S_OUT2 DO1, DO0	Effect
0,0	0,0	PCM data from the AC-Link to SPDIF
0,1	0,1	Disable
1,0	1,0	ADC record data
1,1	1,1	Disable

Table 33. Digital Output Source Selection Table

Note:See Section 7.6.17.1 for digital audio slot select.

7.6.14.1. SPDIF Control (3Ah)

Default: 2A00h

D15	D14	D13	D12	D11	D10	D9	D8
#V	DRS	SPSR1	SPSR0	L	CC6	CC5	CC4
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CC3	CC2	CC1	CC0	PRE	COPY	#PCM/ AUDIO	PRO

Bit(s)	Name	Description
15	#V	Validity bit is set indicating each sub-frame's samples are invalid. If #V is 0, then it indicates that each sub-frame was transmitted and received correctly by the interface.
14	DRS	Double Rate SPDIF is not supported therefore the bit is always 0.
13:12	SPSR[1,0]	SPDIF Sample Rate is currently set to 48kHz. Optional rates are not supported.
11	L	Generation Level is defined by the IEC standard, or as appropriate.
10:4	CC[6:0]	Category Code is defined by the IEC standard or as appropriate by media.
3	PRE	Pre-emphasis is 50/15 usec when set to 1 and 0 usec when set to 0.
2	COPY	Copyright is asserted when the bit is set to 1 and not asserted if set to 0.
1	/AUDIO	Non-Audio or non-PCM format = 1, PCM data = 0.
0	PRO	Professional use of the channel = 1, Consumer use = 0.

Table 34. SPDIF Control (3Ah) Registers

Register 3Ah is a read/write register that controls SPDIF functionality and manages bit fields propagated as channel status (or sub-frame in the V case). With exception of V, this register should only be written to when the SPDIF transmitter is disabled (SPDIF bit register 2 Ah is "0"). This ensures that control and status information start up correctly at the beginning of SPDIF transmission. The default is 2A00h which sets the SPDIF output sample rate at 48kHz and the normal SPDIF expectations.

7.6.15. Revision Code (6Ch)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0

The device Revision register (index 6Ch) contains a software readable revision-specific code used to identify performance, architectural, or software differences between various device revisions. Bits 7:0 of the Revision register are user readable; bits 15:8 are not used at this time and will return zeros when read. The lower order bits of the Revision Register (bits 7:0) are currently set to 00h, and will likely change if there are any STAC9756/57 metal revisions. This value can be used by the audio driver, or miniport driver in the case of WIN98® WDM approaches, to adjust software functionality to match the feature-set of the STAC9756/57. This will allow the software driver to identify any required operational differences between the existing STAC9756/57 and any future versions.

7.6.16. Analog Special (6Eh)

Default: 1000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED			AC97 ALL MIX	RESERVED			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						DAC -6dB	ADC -6dB

The Analog Special Register has several bits used to control various functions specific to the STAC9756/57. Bit D1, DAC -6dB, is used to reduce the DAC output level by 6dB. Similarly, bit D0, ADC -6dB, attenuates any signal input to the ADC by 6dB. This second function is very useful in applications with greater than 1Vrms input levels, as is the case with many CDROMs.

The AC'97 ALL MIX, bit D12 of register 6Eh, controls the record source when the Stereo Mix option is selected for recording. If the AC97 mode is selected (default logic 1), the Stereo Mix Record option will include the sum of the analog sources with or without 3D enhancement, and the main PCM DAC output. If the "ALL Analog Record" option is selected, the Stereo Mix Record option will include the sum of the analog sources only, with or without 3D enhancement. The "AC'97 mode" is useful for recording all sound sources. The "ALL Analog" mode is useful in conjunction with the POP BYPASS mode for recording all analog sources, which are often further processed and combined with other PCM data to be output directly to the DAC outputs which are configured in POP_BYPASS mode using the General Purpose register (index 20h).

7.6.16.1. 72h Enable (70h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

7.6.16.2. Analog Current Adjust (72h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
INT APOP	RESERVED				Bias1	Bias0	RSRVD

The Analog Current Adjust register (index 72h) is a locked register and can only be properly written and read from when ABBAh has been written into register 70h. The BIASx bits allow the analog current to be adjusted with minimal reduction in performance. The –50% analog current setting is NOT recommended when a 5V analog

supply is used. The –50% setting for 3.3V supplies is recommended to reduce power consumption for notebook computers to its lowest level.

BIAS1	BIAS0	Analog Current
0	0	Normal Current
0	1	-50% Analog Current
1	0	-25% Analog Current
1	1	+25% Analog Current

Table 35. Analog Current Adjust

7.6.16.3. Internal Power-On/Off Anti-Pop Circuit

The STAC9756/57 includes an internal power supply anti-pop circuit that prevents audible clicks and pops from being heard when the codec is powered on and off. This function is accomplished by delaying the charge/discharge of the VREF capacitor (Pin 27). C_{VREF} value of 1uF will cause a turn-on delay of roughly 3 seconds, which will allow the power supplies to stabilize before the codec outputs are enabled. The delay will be extended to 30 seconds if a value of C_{VREF} value of 10uF is used. The codec outputs are also kept stable for the same amount of time at power-off to allow the system to be gracefully turned off. The INT_APOP bit D7 of register 72 allows this delay circuit to be bypassed for rapid production testing. Any external component anti-pop circuit is unaffected by the internal circuit.

7.6.17. Multi-Channel Selection (74h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RESERVED							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RESERVED						MC1	MC0

This read/write register is used to program the various options for multi-channel configurations. Only the two LSBs are used (MC0 and MC1), and they define which AC-Link slot data is supplied to the two PCM output channels on the STAC9756/57. Also see "Multiple Codec Support" discussion for information on the use of external pins CID1 and CID0.

External Pins CID1, CID0	Extended Audio ID 28h ID1, ID0	Codec Designation	Multi-Channel Selection 74h MC1, MC0	PCM OUT Left	PCM OUT Right
CID1 = DVdd or floating, CID0 = DVdd or floating	0, 0	Primary, 00	0, 0	Slot 3	Slot 4
			0, 1	Slot 7	Slot 8
			1, 0	Slot 6	Slot 9
			1, 1	Slot 10	Slot 11

Table 36. STAC9756/57 Multi-Channel Programming Register

External Pins CID1, CID0	Extended Audio ID 28h ID1, ID0	Codec Designation	Multi-Channel Selection 74h MC1, MC0	PCM OUT Left	PCM OUT Right
CID1 = DVdd or floating, CID0 = GND	0, 1	Secondary, 01	0, 0	Slot 3	Slot 4
			0, 1	Slot 7	Slot 8
			1, 0	Slot 6	Slot 9
			1, 1	Slot 10	Slot 11
CID1 = GND, CID0 = DVdd or floating	1, 0	Secondary, 10	0, 0	Slot 7	Slot 8
			0, 1	Slot 3	Slot 4
			1, 0	Slot 10	Slot 11
			1, 1	Slot 6	Slot 9
CID1 = GND, CID0 = GND	1, 1	Secondary, 11	0, 0	Slot 6	Slot 9
			0, 1	Slot 10	Slot 11
			1, 0	Slot 3	Slot 4
			1, 1	Slot 7	Slot 8

Table 36. STAC9756/57 Multi-Channel Programming Register (Continued)

7.6.17.1. Digital Audio Slot Selection

The SPSA1 and SPSA0 digital slot select bits determine which of the AC-Link slots are routed to the PCM to I2S and PCM to SPDIF converters. The SSL1 and SSL0 determine which slots are routed to the PCM to I2S1 converter. Tables 37, 38, and 39 describe the assignment options.

SPSA1, SPSA0	SPDIF Left	SPDIF Right
0, 0	Slot 3	Slot 4
0, 1	Slot 7	Slot 8
1, 0	Slot 6	Slot 9
1, 1	Slot 10	Slot 11

Table 37. SPDIF Slot Selection (Reg. 2Ah: D5, D4 with Reg. 6Ah: D12 (I2S SEL) = 0)

SPSA1, SPSA0	I2S_Out2 Left	I2S_OUT2 Right
0, 0	Slot 3	Slot 4
0, 1	Slot 7	Slot 8
1, 0	Slot 6	Slot 9
1, 1	Slot 10	Slot 11

Table 38. I2S OUT2 Slot Selection (Reg. 2Ah: D5, D4 with Reg. 6Ah: D12 (I2S SEL) = 1)

I2S SSL1, I2S SSL0	I2S_OUT1 Left	I2S_OUT1 Right
0, 0	Slot 3	Slot 4
0, 1	Slot 7	Slot 8
1, 0	Slot 6	Slot 9
1, 1	Slot 10	Slot 11

Table 39. I2S OUT1 Slot Selection (Reg. 6Ah: D5, D4)

7.6.18. Clock Access (Index 76h and 78h)

The Clock Access register (index 78h) is a locked register and can only be properly written and read from when ABBAh has been written into register 76h. The STAC9756/57 can operate as a remotely located secondary without a master clock input or local crystal. The STAC9756/57 can synchronize to the BIT_CLK after two register adjustments. The first adjustment starts the synchronization process by enabling the ALT CLK D12, CLK INV D14, and OSC PWD D10 bits of register 78h. The XTAL_IN can either be left floating, or connected to DGND with a 10kΩ or larger resistor.

7.6.18.1. 78h Enable (76h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

7.6.18.2. Clock Access (78h)

Default: 0000h

D15	D14	D13	D12	D11	D10	D9	D8
RSRVD			ALT CLK	RESERVED			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
XTAL2	XTAL1	XTAL0	DITH DIS	DITH EN1	DITH EN0	OSC PWD	HPASS FILT

Bit(s)	Name	Description
12	ALTCLK	Selects/enables clock doubler for secondary mode
7:5	XTAL[2:0]	XTAL Oscillator Power Level
4	DITH DIS	ADC Sigma Delta Modulator (SDM) Dither Disable
3:2	DITH EN[1:0]	ADC SDM Dither Rate
1	OSC PWD	XTAL Oscillator Disable (powerdown)
0	HPASS FILT	ADC High Pass Filter Bypass

Table 40. SPDIF Control (3Ah) Registers

7.6.19. Vendor ID1 and ID2 (Index 7Ch and 7Eh)

These two registers contain four 8-bit ID codes. The first three codes have been assigned by Microsoft using their Plug and Play Vendor ID methodology. The fourth code is a SigmaTel, Inc. assigned code identifying the STAC9756/57. The ID1 register (index 7Ch) contains the value 8384h, which is the first (83h) and second (84h) characters of the Microsoft ID code. The ID2 register (index 7Eh) contains the value 7656h, which is the third (76h) of the Microsoft ID code, and 56h which is the STAC9756/57 ID code.

Note: The lower half of the Vendor ID2 register (index 7Eh) currently contains the value 56h identifying the STAC9756/57. This value can be used by the audio driver, or miniport driver in the case of WIN98®, to adjust software functionality to match the feature-set of the STAC9756/57. This portion of the register will likely contain different values if the software profile of the STAC9756/57 changes, as in the case of silicon level device modifications. This will allow the software driver to identify any required operational differences between the existing STAC9756/57 and any future versions.

7.6.19.1. Vendor ID1 (7Ch)

Default: 8384h

D15	D14	D13	D12	D11	D10	D9	D8
1	0	0	0	0	0	1	1
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	0	0	0	0	1	0	0

7.6.19.2. Vendor ID2 9756 (7Eh)

Default: 7656h

D15	D14	D13	D12	D11	D10	D9	D8
0	1	1	1	0	1	1	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	1	0	1	0	1	1	0

8. LOW POWER MODES

The STAC9756/57 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down. The power down options are listed in Table 41. The first three bits , PR0..PR2, can be used individually or in combination with each other, and control power distribution to the ADC's, DAC's and Mixer. The last analog power control bit, PR3, affects analog bias and reference voltages, and can only be used in combination with PR1, PR2, and PR3. PR3 essentially removes power from all analog sections of the codec, and is generally only asserted when the codec will not be needed for long periods. PR0 and PR1 control the PCM ADC's and DAC's only. PR2 and PR3 do not need to be "set" before a PR4, but PR0 and PR1 must be "set" before PR4.

GRP Bits	Function
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (VREF still on)
PR3	Analog Mixer powerdown (VREF off)
PR4	Digital Interface (AC-Link) powerdown (extnl clk off)
PR5	Internal Clk disable

Table 41. Low Power Modes

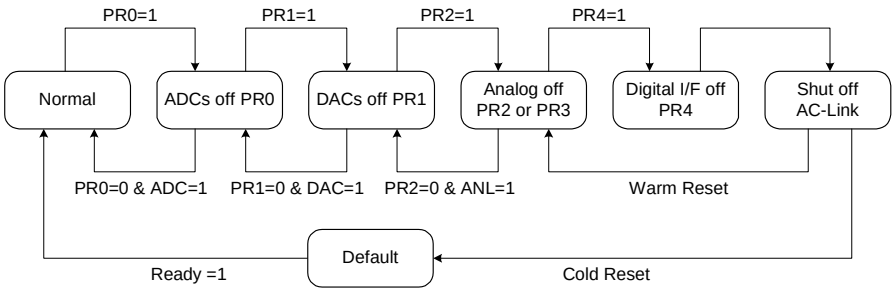


Figure 20. Example of STAC9756/57 Powerdown/Powerup flow

The Figure 20 illustrates one example procedure to do a complete powerdown of STAC9756/57. From normal operation, sequential writes to the Powerdown Register are performed to power down STAC9756/57 a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC-Link. The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC'97 controller will send an extended pulse on the sync line, issuing a warm reset. This will restart the AC-Link (resetting PR4 to zero). The

STAC9756/57 can also be woken up with a cold reset. A cold reset will reset all of the registers to their default states. When a section is powered back on, the Power-down Control/Status register (index 26h) should be read to verify that the section is ready (stable) before attempting any operation that requires it.

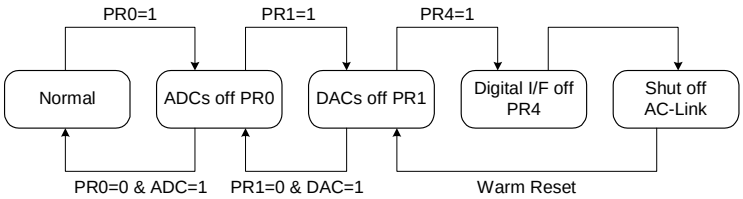


Figure 21. STAC9756/57 Powerdown/Powerup flow with analog still alive

Figure 21 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This configuration can be used when playing a CD (or external LINE_IN source) through STAC9756/57 to the speakers, while most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

9. MULTIPLE CODEC SUPPORT

The STAC9756/57 provides support for the multi-codec option according to the Intel AC'97, rev 2.1 specification. By definition there can be only one Primary Codec (Codec ID 00) and up to three Secondary Codecs (Codec IDs 01,10, and 11). The Codec ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers.

9.1. Primary/Secondary Codec Selection

In a multi-codec environment the codec ID is provided by external programming of pins 45 and 46 (CID0 and CID1). The CID pin electrical function is logically inverted from the codec ID designation. The corresponding pin state and its associated codec ID are listed in Table 42. Also see slot assignment discussion, "Multi-Channel Programming Register (Index 74)".

CID1 State	CID0 State	Codec ID	Codec Status
Dvdd or floating	Dvdd or floating	00	Primary
Dvdd or floating	0V	01	Secondary
0V	Dvdd or floating	10	Secondary
0V	0V	11	Secondary

Table 42. Codec ID Selection

9.1.1. Primary Codec Operation

As a Primary device the STAC9756/57 is completely compatible with existing AC'97 definitions and extensions. Primary Codec registers are accessed exactly as defined in the AC'97 Component Specification and AC'97 Extensions. The STAC9756/57 operates as Primary by default, and the external ID pins (45 and 46), have internal pull-ups so that these pins may be left as no-connects for primary operation.

When used as the Primary Codec, the STAC9756/57 generates the master AC-Link BIT_CLK for both the AC'97 Digital Controller and any Secondary Codecs. The STAC9756/57 can support up to 4, 10 KΩ 50 pF loads on the BIT_CLK. This is to insure that up to 4 Codec implementations will not load down the clock output.

9.1.2. Secondary Codec Operation

When the STAC9756/57 is configured as a Secondary device the BIT_CLK pin is configured as an input at power up. Using the BIT_CLK provided by the Primary Codec insures that everything on the AC-Link will be synchronous. As a Secondary device it can be defined as Codec ID 01, 10, or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

9.2. Secondary Codec Register Access Definitions

The AC'97 Digital Controller can independently access Primary and Secondary Codec registers by using a 2-bit Codec ID field (chip select) which is defined as the LSBs of Output Slot 0. For Secondary Codec access, the AC'97 Digital Controller must *invalidate* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13) and place a *non-zero* value (01, 10, or 11) into the Codec ID field (Slot 0, bits 1 and 0).

As a Secondary Codec, the STAC9756/57 will disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when it sees a 2-bit Codec ID value (Slot 0, bits 1 and 0) that matches its configuration. In a sense the Secondary Codec ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

Secondary Codecs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary Codec ID bits) if it is not valid. AC'97 Digital Controllers should set the frame valid bit for a frame with a secondary register access, even if no other bits in the output tag slot except the Secondary Codec ID bits are set.

This method is designed to be backward compatible with existing AC'97 controllers and Codecs. There is no change to output Slot 1 or 2 definitions.

Output Tag Slot (16-bits)	
Bit	**Description**
15	Frame Valid
14	Slot 1 Valid Command Address bit (†Primary Codec only)
13	Slot 2 Valid Command Data bit (†Primary Codec only)
12-3	Slot 3-12 Valid bits as defined by AC'97
2	Reserved (Set to "0")
†1-0	2-bit Codec ID field (00 reserved for Primary; 01, 10, 11 indicate Secondary)

Note: † New definitions for Secondary Codec Register Access

Table 43. Secondary Codec Register Access Slot 0 Bit Definitions

10. TESTABILITY

The STAC9756/57 has two test modes. One is for ATE in-circuit test and the other is restricted for SigmaTel's internal use. STAC9756/57 enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. Once in the ATE test mode, the digital AC-Link outputs (BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in-circuit testing of the AC'97 controller. Use of the ATE test mode is the recommended means of removing the codec from the AC-Link when another codec is to be used as the primary. This case will never occur during standard operating conditions. Once either of the two test modes have been entered, the STAC9756/57 must be issued another RESET# with all AC-link signals held low to return to the normal operating mode.

11. PIN DESCRIPTION

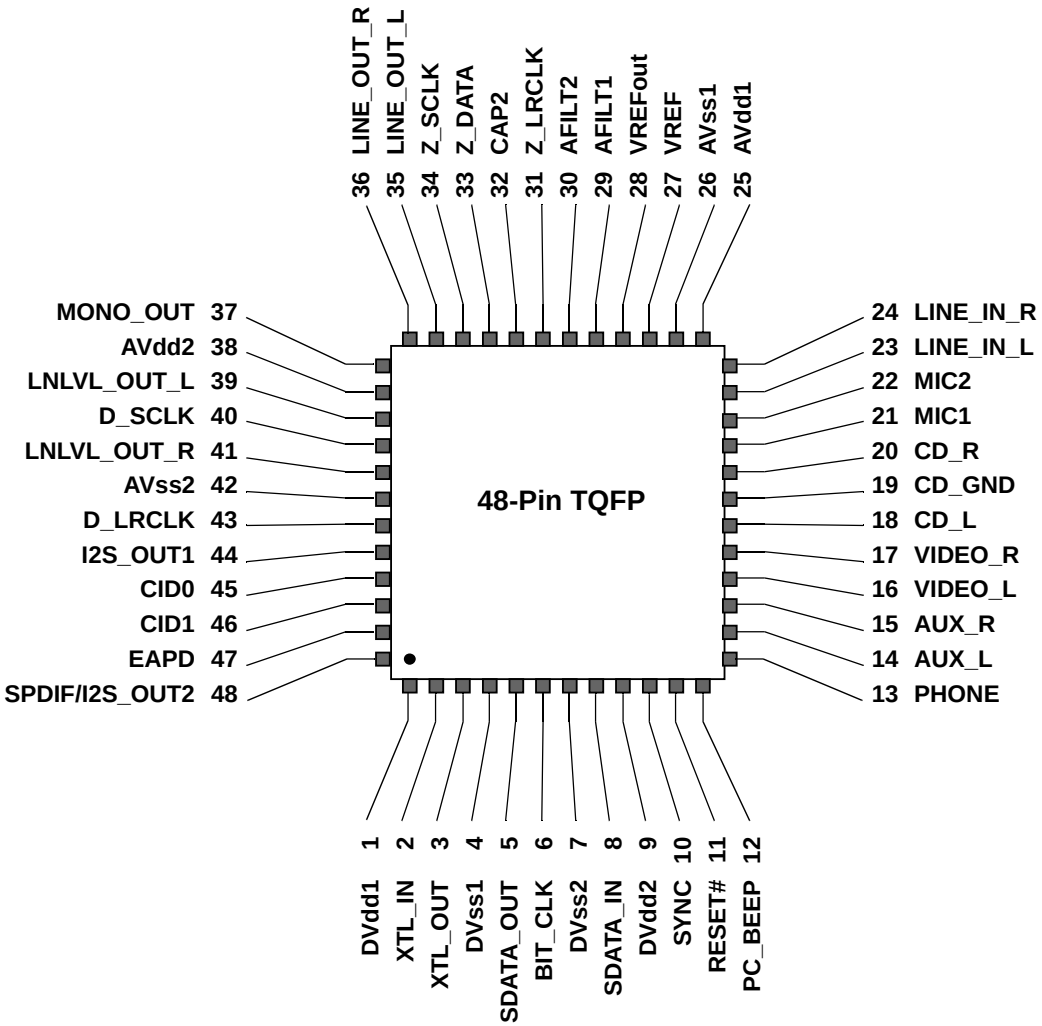


Figure 22. STAC9756/57 Pin Description Drawing

11.1. Digital I/O

These signals connect the STAC9756/57 to its AC'97 controller counterpart, an external crystal, multi-codec selection and external audio amplifier.

Pin Name	Pin #	Type	Description
RESET#	11	I	AC'97 Master H/W Reset
XTL_IN	2	I	24.576 MHz Crystal or External Oscillator
XTL_OUT	3	O	24.576 MHz Crystal
SYNC	10	I	48 kHz fixed rate sample sync
BIT_CLK	6	I/O	12.288 MHz serial data clock
SDATA_OUT	5	I	Serial, time division multiplexed, AC'97 input stream
SDATA__IN	8	O	Serial, time division multiplexed, AC'97 output stream
CID0	45	I	Multi-Codec ID select – bit 0
CID1	46	I	Multi-Codec ID select – bit 1
EAPD	47	O	External Amplifier Power Down
Z_DATA	33*	I	ZV_PORT I^2S digital data input
I2S_OUT1	44	O	I^2S digital data output
D_SCLK	40	O	I^2S digital data bit clock
D_LRCLK	43	O	I^2S digital data left/right clock
Z_SCLK	34*	I	ZV_PORT I^2S digital data bit clock
Z_LRCLK	31*	I	ZV_PORT I^2S digital data left/right clock
SPDIF/I2S_OUT2	48	O	Dual mode I^2S/SPDIF digital output

Note: * Pullups recommended if not used.

Table 44. Digital Connection Signals

11.2. Analog I/O

These signals connect the STAC9756/57 to analog sources and sinks, including microphones and speakers.

Pin Name	Pin #	Type	Description
PC-BEEP	12	I*	PC Speaker beep pass-through
PHONE	13	I*	From telephony subsystem speakerphone (or DLP:Down Line Phone)
MIC1	21	I*	Desktop Microphone Input
MIC2	22	I*	Second Microphone Input
LINE_IN_L	23	I*	Line In Left Channel
LINE_IN_R	24	I*	Line In Right Channel
CD_L	18	I*	CD Audio Left Channel
CD_GND	19	I*	CD Audio analog ground
CD_R	20	I*	CD Audio Right Channel
VIDEO_L	16	I*	Video Audio Left Channel
VIDEO_R	17	I*	Video Audio Right Channel
AUX_L	14	I*	Aux Left Channel
AUX_R	15	I*	Aux Right Channel
LINE_OUT_L	35	O	Line Out Left Channel
LINE_OUT_R	36	O	Line Out Right Channel
MONO_OUT	37	O	To telephony subsystem speakerphone (or DLP – Down Line Phone)
LNLVL_OUT_L	39	O	Line Level Out Left Channel
LNLVL_OUT_R	41	O	Line Level Out Right Channel

Table 45. Analog Connection Signals

Note: * any unused input pins should be tied together through a capacitor (0.1 µF suggested) to ground, except the MIC inputs which should have their own capacitor to ground if not used.

11.3. Filter/References

These signals are connected to resistors, capacitors, specific voltages.

Signal Name	Pin Number	Type	Description
VREF	27	O	Reference Voltage
VREFout	28	O	Reference Voltage out 5mA drive (intended for mic bias)
AFILT1	29	O	Anti-Aliasing Filter Cap - ADC channel
AFILT2	30	O	Anti-Aliasing Filter Cap - ADC channel
CAP2	32	O	ADC reference Cap

Table 46. Filtering and Voltage References

11.4. Power and Ground Signals

Pin Name	Pin #	Type	Description
AVdd1	25	I	Analog Vdd = 5.0V or 3.3V
AVdd2	38	I	Analog Vdd = 5.0V or 3.3V
AVss1	26	I	Analog Gnd
AVss2	42	I	Analog Gnd
DVdd1	1	I	Digital Vdd = 3.3V
DVdd2	9	I	Digital Vdd = 3.3V
DVss1	4	I	Digital Gnd
DVss2	7	I	Digital Gnd

Table 47. Power and Ground Signals

12. PACKAGE DRAWING

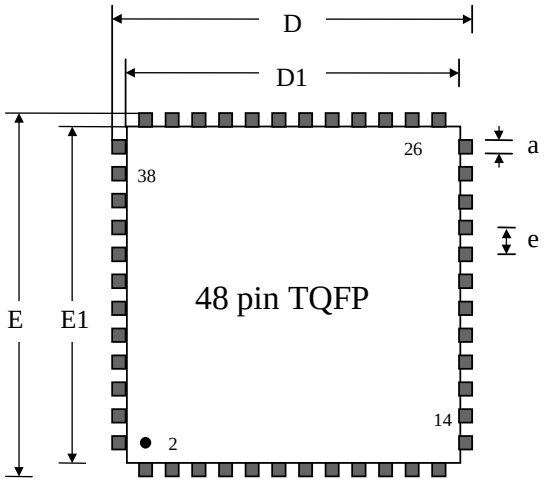


Figure 23. 48-Pin TQFP Package Drawing

Key	TQFP Dimensions
D	9.00 mm
D1	7.00 mm
E	9.00 mm
E1	7.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
thickness	1.4 mm

Table 48. 48-Pin TQFP Package Dimensions

13. APPENDIX A: SPLIT INDEPENDENT POWER SUPPLY OPERATION

In PC applications, one power supply input to the STAC9756/57 may be derived from a supply regulator (as shown in Figure 24) and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's codecs would be subject to on-chip SCR type latch-up.

SigmaTel's STAC9756/57 specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the codec. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up.

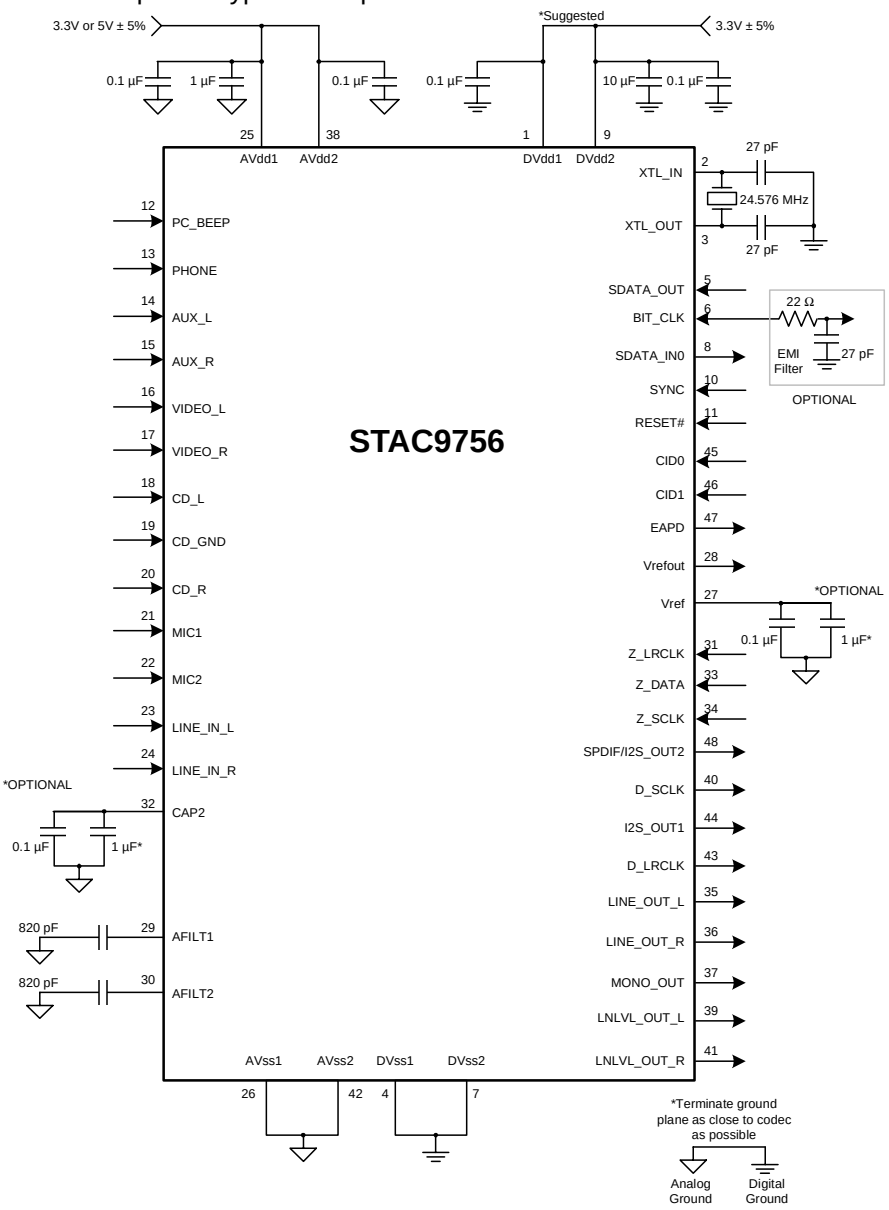


Figure 24. STAC9756 Split Independent Power Supply Operation Typical Connection Diagram

14. APPENDIX C: PROGRAMMING REGISTERS

Reg #	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	RSRVD	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6940h
02h	Master Volume	Mute	RSRVD	ML5	ML4	ML3	ML2	ML1	ML0	RESERVED		MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	LNLVL_OUT Mixer Volume	Mute	RSRVD	ML5	ML4	ML3	ML2	ML1	ML0	RESERVED		MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute	RESERVED									MM5	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	RESERVED										PV3	PV2	PV1	PV0	RSRVD	0000h
0Ch	Phone volume	Mute	RESERVED										GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	RESERVED								20dB	RSRVD	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RESERVED			GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RESERVED			GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RESERVED			GR4	GR3	GR2	GR1	GR0	8808h
16h	AUX Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RESERVED			GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RESERVED			GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	RESERVED					SL2	SL1	SL0	RESERVED					SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	RESERVED			GL3	GL2	GL1	GL0	RESERVED				GR3	GR2	GR1	GR0	8000h
20h	General Purpose	POP BYP	RSRVD	3D	RESERVED			MIX	MS	LPBK	RESERVED							0000h
22h	3D Control	RESERVED												DP3	DP2	RESERVED		0000h
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	RESERVED				REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0	RESERVED				AMAP	LDAC	SDAC	CDAC	RSVD			SPDIF	DRA	VRA	0205h
2Ah	Extended Audio Control/ Status	RESERVED					SPCV	RSRVD				SPSA1	SPSA0	RSRVD	SPDIF	RSRVD	VRA enable	0400h
2Ch	PCM DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
3Ah	SPDIF Control	#V	DRS	SPSR1	SPSR2	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	#PCM/ AUDIO	PRO	2A00h
60h	Z_DATA Volume	Mute	RESERVED		GL4	GL3	GL2	GL1	GL0	RESERVED			GR4	GR3	GR2	GR1	GR0	8808h
6Ah	Digital Audio Control	RESERVED			I2S SEL	I2S ENA	ZVP ENA	ADC ENA	PCM DIS	ADMIX GAIN1	ADMIX GAIN0	I2S SSL1	I2S SSL0	DO3	DO2	DO1	DO0	0000h
6Ch	Revision Code	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
6Eh	Analog Special	RESERVED			AC97 ALL MIX	RESERVED										DAC -6dB	ADC -6dB	1000h
70h	72h Enable	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	0000h
72h	Analog Current Adjust	RESERVED								INT APOP	RESERVED				Bias1	Bias0	RSRVD	0000h
74h	Multi-Channel Selection	RESERVED														MC1	MC0	0000h
76h	78h Enable	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	0000h
78h	Clock Access	RSRVD			ALT CLK	RESERVED				XTAL2	XTAL1	XTAL0	DITH DIS	DITH EN1	DITH EN0	OSC PWD	HPASS FILT	0000h
7Ch	Vendor ID1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	8384h
7Eh	Vendor ID2 9756	0	1	1	1	0	1	1	0	0	1	0	1	0	1	1	0	7656h

Note:
1. All registers not shown and bits containing an X are reserved. They can be written to but are don't care upon read back.
2. PC_BEEP default to 0000h, mute off.
3. If optional bits D13, D5 of register 02h or D5 of register 06h are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 1Fh as a value for this attenuation/gain block.
4. If in secondary mode the default for Reg. 18h = 8888h., otherwise 8808h for primary mode.