SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

C504

Data Sheet 05.96

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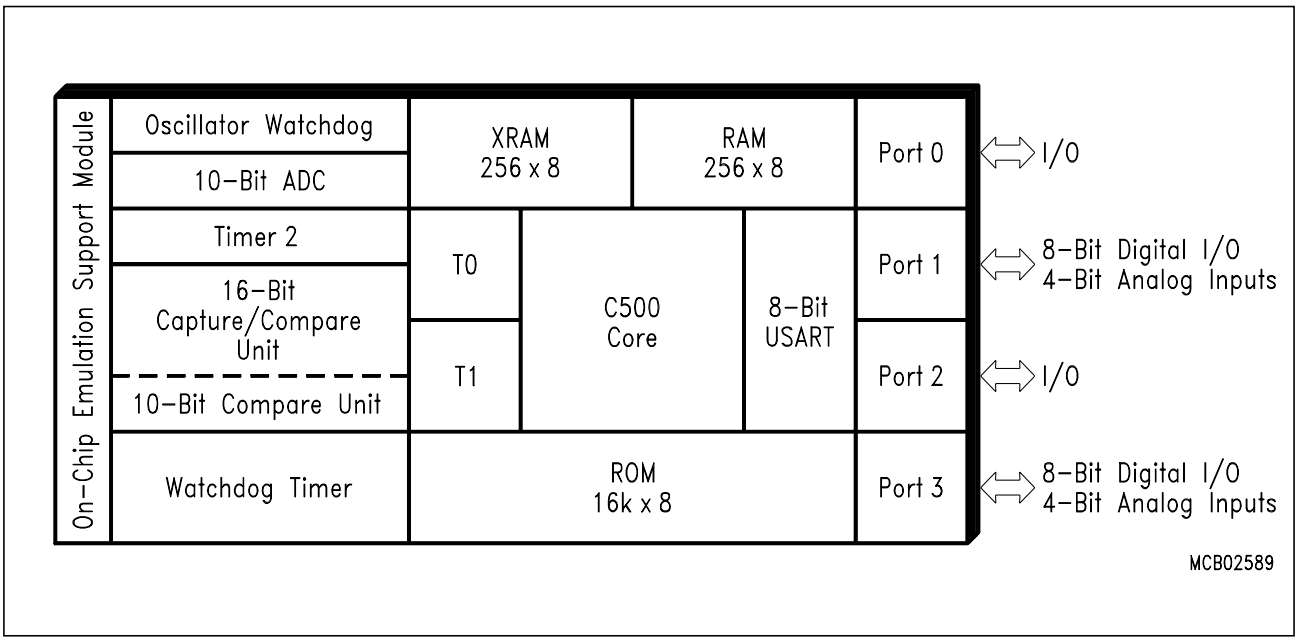
8-Bit CMOS Microcontroller C504

Advance Information

- Fully compatible to standard 8051 microcontroller
- Up to 40 MHz operating frequency
- 16 K×8 ROM (C504-2R only, optional ROM protection)
- 256×8 RAM
- 256×8 XRAM
- Four 8-bit ports, (2 ports with mixed analog/digital I/O capability)
- Three 16-bit timers/counters (timer 2 with up/down counter feature)
- Capture/compare unit for PWM signal generation and signal capturing
  - 3-channel, 16-bit capture/compare unit
  - 1-channel, 10-bit compare unit
- Compare unit
- USART
- 10-bit A/D Converter with 8 multiplexed inputs
- Twelve interrupt sources with two priority levels
- On-chip emulation support logic (Enhanced Hooks Technology ™)
- Programmable 15-bit Watchdog Timer
- Oscillator Watchdog
- Fast Power On Reset
- Power Saving Modes
- M-QFP-44 package
- Temperature ranges: SAB-C504 T_A : 0 to 70°C
  SAF-C504 T_A : – 40 to 85°C
  SAH-C504 T_A : – 40 to 110°C (max. operating frequency.: TBD)
  SAK-C504 T_A : – 40 to 125°C (max. operating frequency.: 12 MHz)



The C504 with its capture compare unit (CCU) especially provides a functionality, which allows to use the microcontroller in motor control applications. Further, the C504 is functionally upward compatible with the SAB 80C52/C501 microcontroller and can replace it in existing applications.
The C504-2R contains a non-volatile 16K×8 read-only program memory, a volatile on-chip 512×8 read/write data memory, four 8-bit wide ports, three 16-bit timers/counters, a 16-bit capture/compare unit with compare timer, a 10-bit compare timer, a twelve source, two priority level interrupt structure, a serial port, versatile fail save mechanisms, on-chip emulation support logic, and a genuine 10-bit A/D converter. The C504-L is identical to the C504-2R, except that it lacks the program memory on chip. Therefore, the term C504 refers to all versions within this data sheet unless otherwise noted.

Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C504-LM	Q67120-C1048	P-MQFP-44	for external memory (12 MHz)
SAB-C504-L24M	Q67120-C1049	P-MQFP-44	for external memory (24 MHz)
SAB-C504-L40M	Q67120-C1050	P-MQFP-44	for external memory (40 MHz)
SAB-C504-2RM	Q67120-DXXXX	P-MQFP-44	with mask-programmable ROM (12 MHz)
SAB-C504-2R24M	Q67120-DXXXX	P-MQFP-44	with mask-programmable ROM (24 MHz)
SAB-C504-2R40M	Q67120-DXXXX	P-MQFP-44	with mask-programmable ROM (40 MHz)

Note: Versions for extended temperature ranges – 40 °C to 110 °C (SAH-C504) and – 40 °C to 125 °C (SAK-C504) are available on request.
The ordering number of ROM types (DXXXX extensions) is defined after program release (verification) of the customer.

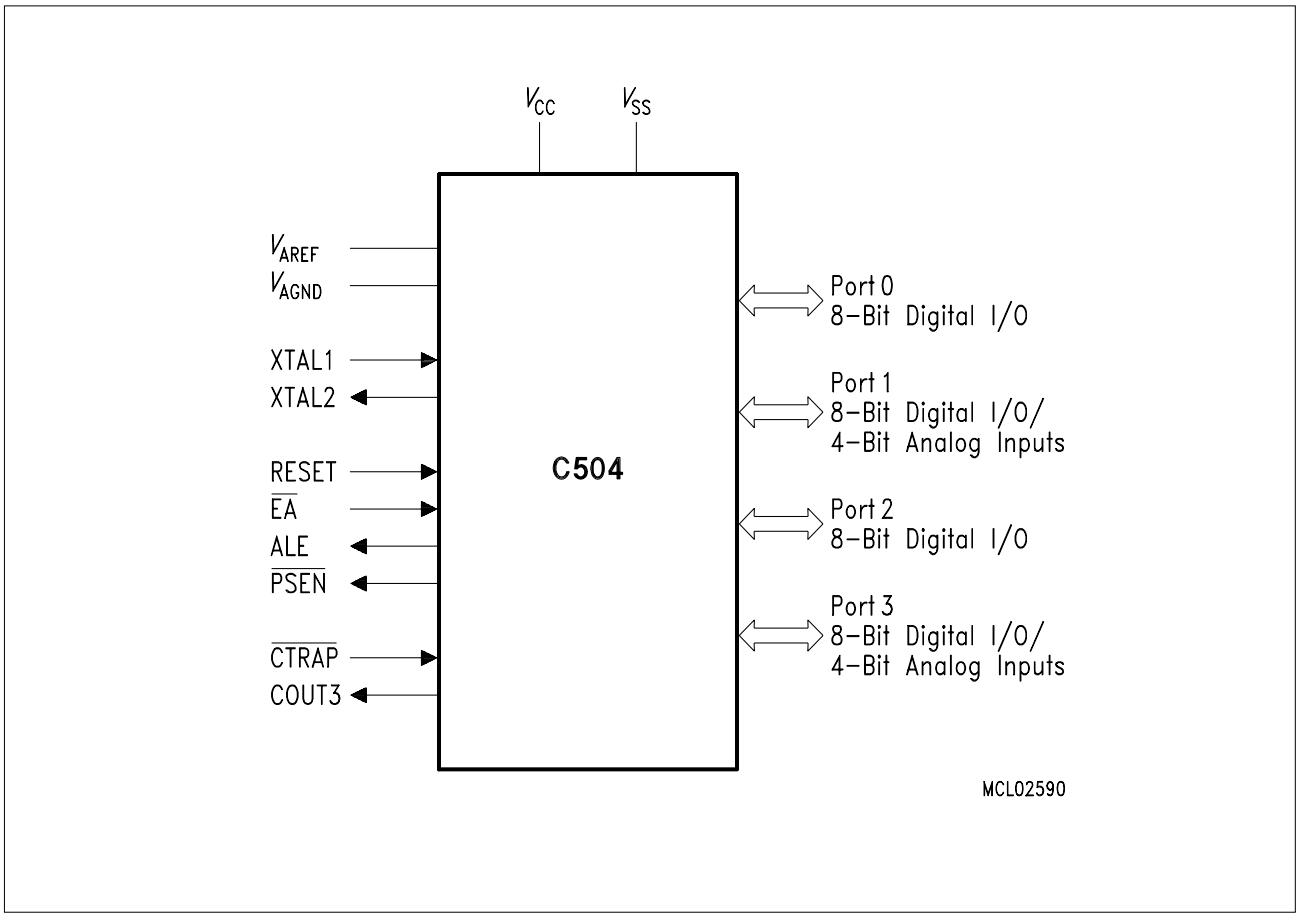


Figure 1
Logic Symbol

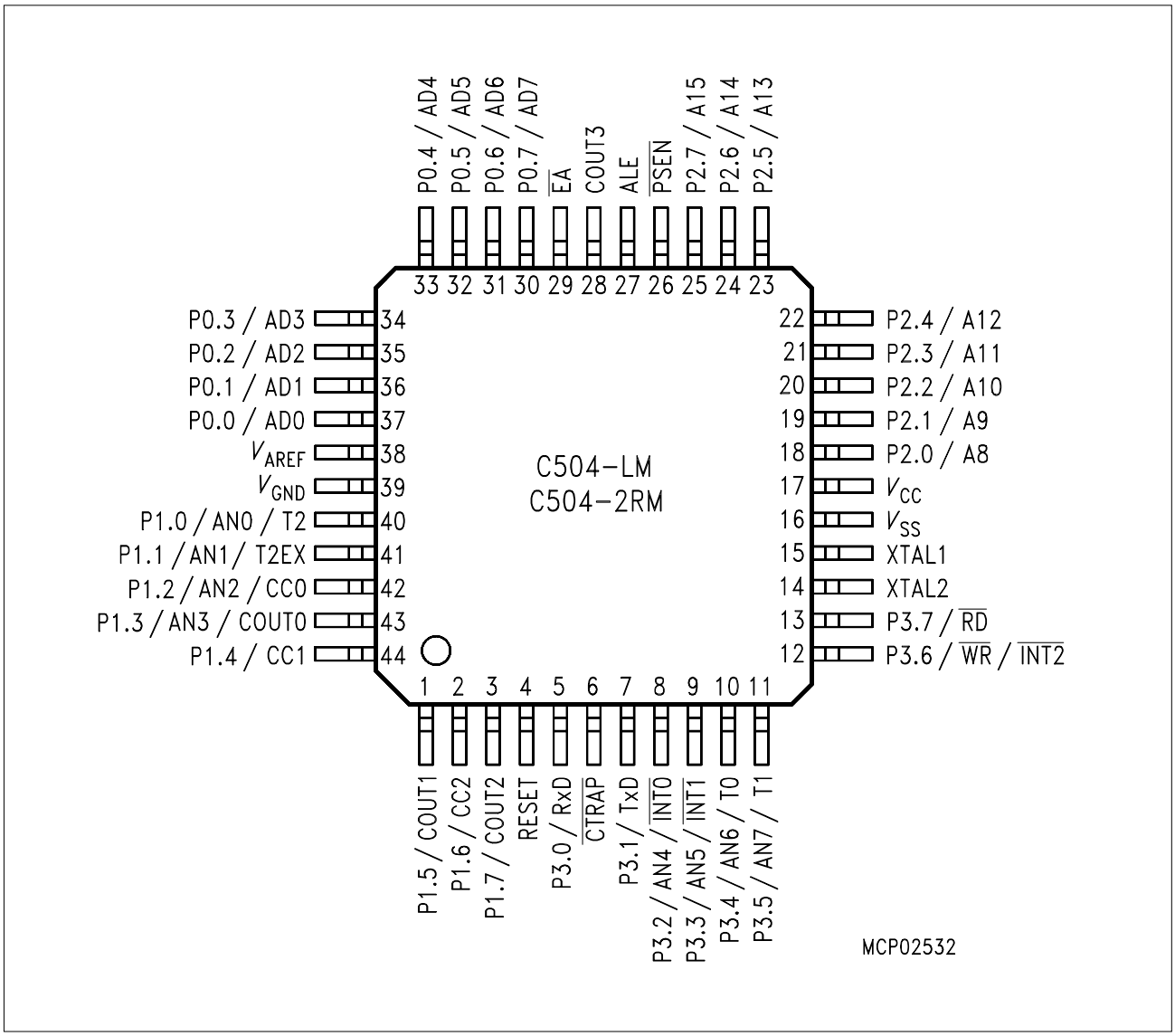


Figure 2
Pin Configuration (top view)

Table 1
Pin Definitions and Functions

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
P1.0-P1.7	40-44, 1-3	I/O	**Port 1** is an 8-bit bidirectional port. Port pins can be used for digital input/output. P1.0 - P1.3 can also be used as analog inputs of the A/D-converter. As secondary digital functions, port 1 contains the timer 2 pins and the capture/compare inputs/outputs. Port 1 pins are assigned to be used as analog inputs via the register P1ANA. The functions are assigned to the pins of port 1 as follows:
	40		P1.0 / AN0 / T2 — Analog input channel 0 / input to counter 2
	41		P1.1 / AN1 / T2EX — Analog input channel 1 / capture/reload trigger of timer 2 / up-down count
	42		P1.2 / AN2 / CC0 — Analog input channel 2 / input/output of capture/compare channel 0
	43		P1.3 / AN3 / COUT0 — Analog input channel 3 / output of capture/compare channel 0
	44		P1.4 / CC1 — Input/output of capture/compare channel 1
	1		P1.5 / COUT1 — Output of capture/compare channel 1
	2		P1.6 / CC2 — Input/output of capture/compare channel 2
	3		P1.7 / COUT2 — Output of capture/compare channel 2
RESET	4	I	**RESET** A high level on this pin for one machine cycle while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
P3.0-P3.7	5, 7-13	I/O	**Port 3** is an 8-bit bidirectional port. P3.0 (R×D) and P3.1 (T×D) operate as defined for the C501. P3.2 to P3.7 contain the external interrupt inputs, timer inputs, input and as an additional optinal function four of the analog inputs of the A/D-converter. Port 3 pins are assigned to be used as analog inputs via the bits of SFR P3ANA. P3.6/$\overline{WR}$ can be assigned as a third interrupt input. The functions are assigned to the pins of port 3 as follows:
	5		P3.0 / RxD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	7		P3.1 / TxD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	8		P3.2 / AN4 / $\overline{INT0}$ — Analog input channel 4 / external interrupt 0 input / timer 0 gate control input
	9		P3.3 / AN5 / $\overline{INT1}$ — Analog input channel 5 / external interrupt 1 input / timer 1 gate control input
	10		P3.4 / AN6 / T0 — Analog input channel 6 / timer 0 counter input
	11		P3.5 / AN7 / T1 — Analog input channel 7 / timer 1 counter input
	12		P3.6 / $\overline{WR}$ / $\overline{INT2}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory / external interrupt 2 input
	13		P3.7 / $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory
$\overline{CTRAP}$	6	I	**$\overline{CCU\ Trap\ Input}$** With $\overline{CTRAP}$ = low the compare outputs of the CAPCOM unit are switched to the logic level as defined in the COINI register (if they are enabled by the bits in SFR TRCON). $\overline{CTRAP}$ is an input pin with an internal pullup resistor. For power saving reasons, the signal source which drives the $\overline{CTRAP}$ input should be at high or floating level during power-down mode.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
XTAL2	14	–	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	15	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.
P2.0-P2.7	18-25	I/O	**Port 2** is a bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteris-tics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{PSEN}}$	26	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periodes except during external data memory accesses. Remains high during internal program execution.
ALE	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periodes except during an external data memory access. When instructions are executed from internal ROM ($\overline{\text{EA}}$=1) the ALE generation can be disabled by bit EALE in SFR SYSCON.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number (P-MQFP-44)	I/O *)	Function
COUT3	28	O	**10-Bit compare channel output** This pin is used for the output signal of the 10-bit compare timer 2 unit. COUT3 can be disabled and set to a high or low state.
$\overline{EA}$	29	I	**$\overline{External\ Access}$ Enable** When held at high level, instructions are fetched from the internal ROM (C504-2R only) when the PC is less than 4000_H.When held at low level, the C504 fetches all instructions from external program memory. For the C504-L this pin must be tied low.
P0.0-P0.7	37-30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impendance inputs.Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup resistors when issuing 1 s. Port 0 also outputs the code bytes during program verification in the C504-2R. External pullup resistors are required during program (ROM) verification.
V_{AREF}	38	–	**Reference voltage** for the A/D converter.
V_{AGND}	39	–	**Reference ground** for the A/D converter.
V_{SS}	16	–	**Ground** (0V)
V_{CC}	17	–	**Power Supply** (+5V)

*) I = Input
O = Output

Functional Description

The C504 basic architecture is fully compatible to the standard 8051 microcontroller family. While maintaining all architectural and operational characteristics of the SAB 80C52 / C501, the C504 incorporates some enhancements such as on-chip XRAM, A/D converter, fail save mechanisms, and a versatile capture/compare unit.
Figure 3 shows a block diagram of the C504.

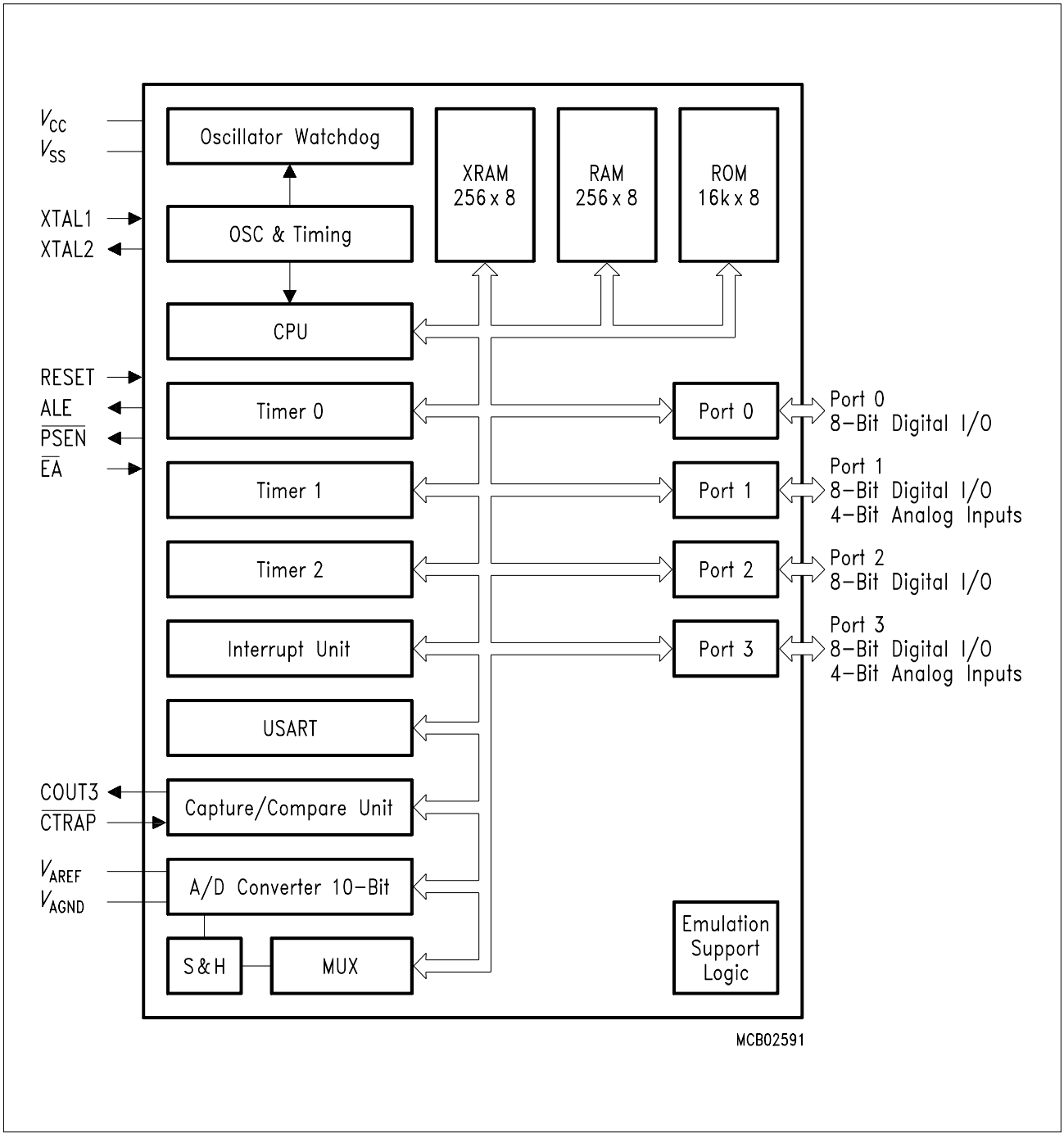


Figure 3
Block Diagram of the C504

CPU

The C504 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15 % three-byte instructions. With a 12 MHz crystal, 58 % of the instructions are executed in 1.0µs (24 MHz: 500 ns, 40 MHz : 300 ns).

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.
OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

Memory Organization

The C504 CPU manipulates operands in the following four address spaces:

- up to 64 Kbyte of external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- 256 bytes of internal XRAM data memory
- a 128 byte special function register area

Figure 4 illustrates the memory address spaces of the C504.

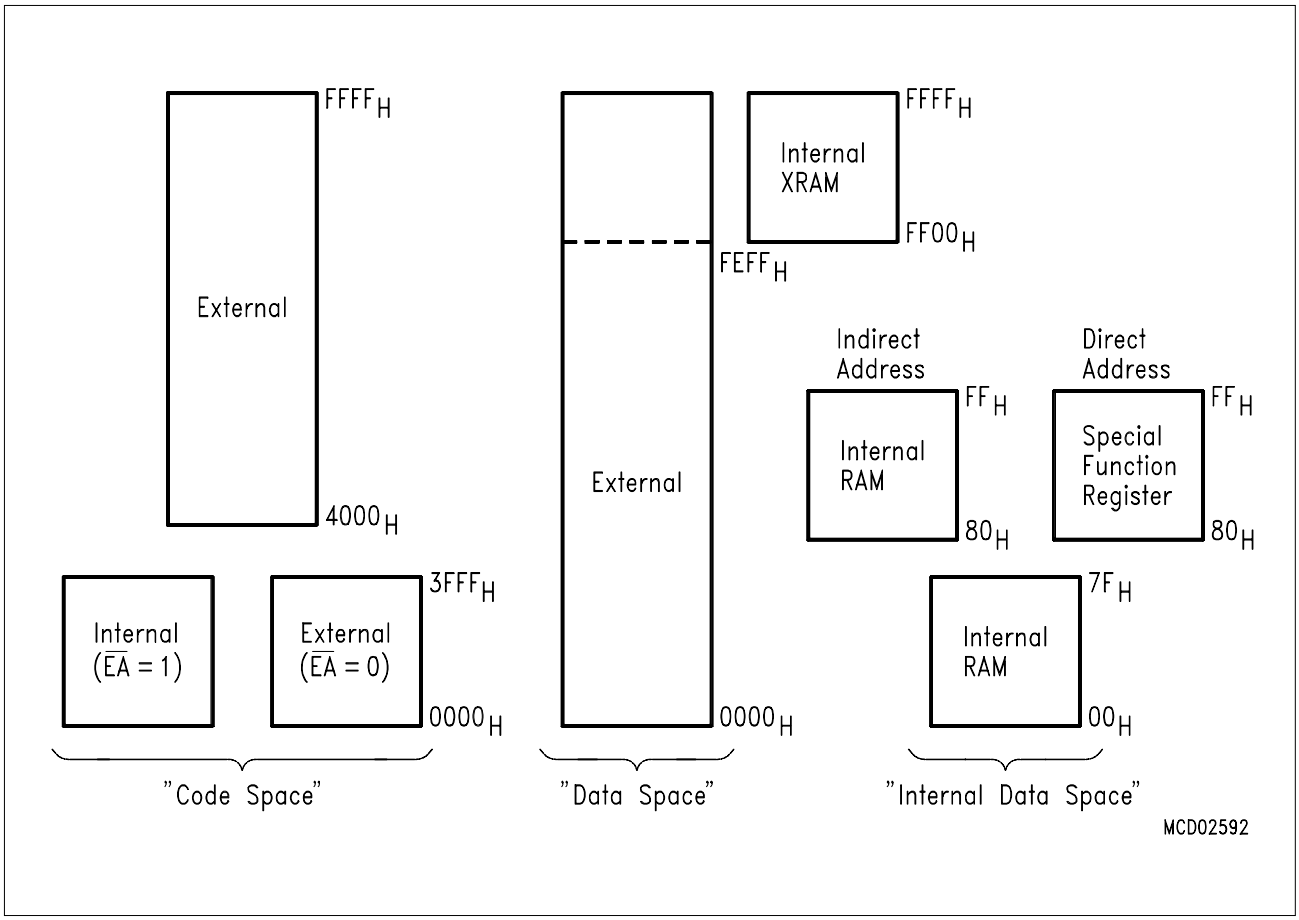


Figure 4
C504 Memory Map

The XRAM in the C504 is a memory area that is logically located at the upper end of the external memory space, but is integrated on the chip. Because the XRAM is used in the same way as external data memory the same instruction types (MOVX instructions) must be used for accessing the XRAM. The XRAM can be enabled and disabled by the XMAP bit in the SYSCON register.

ROM Protection

The C504-2R ROM version allows to protect the content of the internal ROM against read out by non authorized people. The type of ROM protection (protected or unprotected) is fixed with the ROM mask. Therefore, the customer of a C504-2R ROM version has to define whether ROM protection has to be selected or not.

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.
The 63 special function register (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.
The SFRs of the C504 are listed in **table 2** and **table 3**. In **table 2** they are organized in groups which refer to the functional blocks of the C504. **Table 3** illustrates the contents of the SFRs in numeric order of their addresses.

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** 1)	00_H
	B	B-Register	**$F0_H$** 1)	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	**$D0_H$** 1)	00_H
	SP	Stack Pointer	81_H	07_H
	SYSCON	System Control Register	$B1_H$	$XX10XXX0_B$ 3)
Interrupt System	IEN0	Interrupt Enable Register 0	**$A8_H$** 1)	$0X000000_B$ 3)
	IEN1	Interrupt Enable Register 1	$A9_H$	$XX000000_B$ 3)
	CCIE 2)	Capture/Compare Interrupt Enable Reg.	$D6_H$	00_H
	IP0	Interrupt Priority Register 0	**$B8_H$** 1)	$XX000000_B$ 3)
	IP1	Interrupt Priority Register 1	$B9_H$	$XX000000_B$ 3)
	ITCON	Interrupt Trigger Condition Register	$9A_H$	00101010_B
Ports	P0	Port 0	**80_H** 1)	FF_H
	P1	Port 1	**90_H** 1)	FF_H
	P1ANA 2)	Port 1 Analog Input Selection Register	**90_H** 1) 4)	$XXXX1111_B$ 3)
	P2	Port 2	**$A0_H$** 1)	FF_H
	P3	Port 3	**$B0_H$** 1)	FF_H
	P3ANA 2)	Port 3 Analog Input Selection Register	**$B0_H$** 1) 4)	$XX1111XX_B$ 3)
A/D-Converter	ADCON0	A/D Converter Control Register 0	**$D8_H$** 1	$XX000000_B$ 3)
	ADCON1	A/D Converter Control Register 1	DC_H	$01XXX000_B$ 3)
	ADDATH	A/D Converter Data Register High Byte	$D9_H$	00_H
	ADDATL	A/D Converter Data Register Low Byte	DA_H	$00XXXXXX_B$ 3)
	P1ANA 2)	Port 1 Analog Input Selection Register	90_H 4)	$XXXX1111_B$ 3)
	P3ANA 2)	Port 3 Analog Input Selection Register	$B0_H$ 4)	$XX1111XX_B$ 3)
Serial Channels	PCON 2)	Power Control Register	87_H	$000X0000_B$
	SBUF	Serial Channel Buffer Register	99_H	XX_H 3)
	SCON	Serial Channel Control Register	**98_H** 1)	00_H
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is undefined and the location is reserved

4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 2
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Timer 2	T2CON	Timer 2 Control Register	**$C8_H$** [1]	00_H
	T2MOD	Timer 2 Mode Register	$C9_H$	$XXXXXXX0_B$ [3]
	RC2H	Timer 2 Reload Capture Register, High Byte	CB_H	00_H
	RC2L	Timer 2 Reload Capture Register, Low Byte	CA_H	00_H
	TH2	Timer 2 High Byte	CD_H	00_H
	TL2	Timer 2 Low Byte	CC_H	00_H
Capture / Compare Unit	CT1CON	Compare timer 1 control register	$E1_H$	00010000_B
	CCPL	Compare timer 1 period register, low byte	DE_H	00_H
	CCPH	Compare timer 1 period register, high byte	DF_H	00_H
	CT1OFL	Compare timer 1 offset register, low byte	$E6_H$	00_H
	CT1OFH	Compare timer 1 offset register, high byte	$E7_H$	00_H
	CMSEL0	Capture/compare mode select register 0	$E3_H$	00_H
	CMSEL1	Capture/compare mode select register 1	$E4_H$	00_H
	COINI	Compare output initialization register	$E2_H$	FF_H
	TRCON	Trap enable control register	CF_H	00_H
	CCL0	Capture/compare register 0, low byte	$C2_H$	00_H
	CCH0	Capture/compare register 0, high byte	$C3_H$	00_H
	CCL1	Capture/compare register 1, low byte	$C4_H$	00_H
	CCH1	Capture/compare register 1, high byte	$C5_H$	00_H
	CCL2	Capture/compare register 2, low byte	$C6_H$	00_H
	CCH2	Capture/compare register 2, high byte	$C7_H$	00_H
	CCIR	Capture/compare interrupt request flag reg.	$E5_H$	00_H
	CCIE [2]	Capture/compare interrupt enable register	$D6_H$	00_H
	CT2CON	Compare timer 2 control register	$C1_H$	00010000_B
	CP2L	Compare timer 2 period register, low byte	$D2_H$	00_H
	CP2H	Compare timer 2 period register, high byte	$D3_H$	$XXXXXX00_B$ [3]
	CMP2L	Compare timer 2 compare register, low byte	$D4_H$	00_H
	CMP2H	Compare timer 2 compare register, high byte	$D5_H$	$XXXXXX00_B$ [3)]
	BCON	Block commutation control register	$D7_H$	00_H
Watchdog	WDCON	Watchdog Timer Control Register	**$C0_H$** [1]	$XXXX0000_B$ [3]
	WDTREL	Watchdog Timer Reload Register	86_H	00_H
Power Save Mode	PCON [2]	Power Control Register	87_H	$000X0000_B$ [3]
	PCON1	Power Control Register 1	88_H [4]	$0XXXXXXX_B$ [3]

1) Bit-addressable special function registers

2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.

3) X means that the value is undefined and the location is reserved

4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3
Contents of the SFRs, SFRs in Numeric Order of their Addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H [2)]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	$000X\text{-}0000_B$	SMOD	PDS	IDLS	–	GF1	GF0	PDE	IDLE
88_H [2)]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H [3)]	PCON1	$0XXX\text{-}XXXX_B$	EWPD	–	–	–	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H [2)]	P1	FF_H	.7	.6	.5	.4	.3	.2	T2EX	T2
90_H [2)3)]	P1ANA	$XXXX\text{-}1111_B$	–	–	–	–	EAN3	EAN2	EAN1	EAN0
98_H [2)]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$9A_H$	ITCON	$0010\text{-}1010_B$	IT2	IE2	I2ETF	I2ETR	I1ETF	I1ETR	I0ETF	I0ETR
$A0_H$ [2)]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$ [2)]	IEN0	$0X00\text{-}0000_B$	EA	–	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IEN1	$XX00\text{-}0000_B$	–	–	ECT1	ECCM	ECT2	ECEM	EX2	EADC
$B0_H$ [2)]	P3	FF_H	RD	WR	T1	T0	INT1	INT0	TxD	RxD

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3
Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$B0_H$[2)3)]	P3ANA	XX11-11XX_B	–	–	EAN7	EAN6	EAN5	EAN4	–	–
$B1_H$	SYSCON	XX10-XXX0_B	–	–	EALE	RMAP	–	–	–	XMAP
$B8_H$[2)]	IP0	XX00-0000$_B$	–	–	PT2	PS	PT1	PX1	PT0	PX0
$B9_H$	IP1	XX00-0000$_B$	–	–	PCT1	PCCM	PCT2	PCEM	PX2	PADC
$C0_H$[2)]	WDCON	XXXX-0000$_B$	–	–	–	–	OWDS	WDTS	WDT	SWDT
$C1_H$	CT2CON	0001-0000$_B$	CT2P	ECT2O	STE2	CT2 RES	CT2R	CLK2	CLK1	CLK0
$C2_H$	CCL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$[2)]	T2CON	00_H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	XXXX-XXX0_B	–	–	–	–	–	–	–	DCEN
CA_H	RC2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	RC2H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CF_H	TRCON	00_H	TRPEN	TRF	TREN5	TREN4	TREN3	TREN2	TREN1	TREN0
$D0_H$[2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D2_H$	CP2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3
Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D3_H$	CP2H	XXXX. $XX00_B$	–	–	–	–	–	–	.1	.0
$D4_H$	CMP2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D5_H$	CMP2H	XXXX. $XX00_B$	–	–	–	–	–	–	.1	.0
$D6_H$	CCIE	00_H	ECTP	ECTC	CC2 FEN	CC2 REN	CC1 FEN	CC1 REN	CC0 FEN	CC0 REN
$D7_H$	BCON	00_H	BCMP BCEM	PWM1	PWM0	EBCE	BCERR	BCEN	BCM1	BCM0
$D8_H$[2)]	ADCON0	XX00- 0000_B	–	–	IADC	BSY	ADM	MX2	MX1	MX0
$D9_H$	ADDATH	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADDATL	00XX- $XXXX_B$	.1	.0	–	–	–	–	–	–
DC_H	ADCON1	01XX- $X000_B$	ADCL1	ADCL0	–	–	–	MX2	MX1	MX0
DE_H	CCPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
DF_H	CCPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E1_H$	CT1CON	0001- 0000_B	CTM	ETRP	STE1	CT1 RES	CT1R	CLK2	CLK1	CLK0
$E2_H$	COINI	FF_H	COUT 3I	COUTX I	COUT 2I	CC2I	COUT 1I	CC1I	COUT 0I	CC0I
$E3_H$	CMSEL0	00_H	CMSEL 13	CMSEL 12	CMSEL 11	CMSEL 10	CMSEL 03	CMSEL 02	CMSEL 01	CMSEL 00
$E4_H$	CMSEL1	00_H	0	0	0	0	CMSEL 23	CMSEL 22	CMSEL 21	CMSEL 20
$E5_H$	CCIR	00_H	CT1FP	CT1FC	CC2F	CC2R	CC1F	CC1R	CC0F	CC0R
$E6_H$	CT1OFL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E7_H$	CT1OFH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved

2) Bit-addressable special function registers

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4**.

Table 4
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/$\overline{T}$	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{OSC}/_{12 \times 32}$	$f_{OSC}/_{24 \times 32}$
1	16-bit timer/counter	X	X	1	1	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$
2	8-bit timer/counter with 8-bit autoreload	X	X	0	0	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$

In the “timer” function (C/T = ‘0’) the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/12$.
In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs INT0 and INT1 (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 5** illustrates the input clock logic.

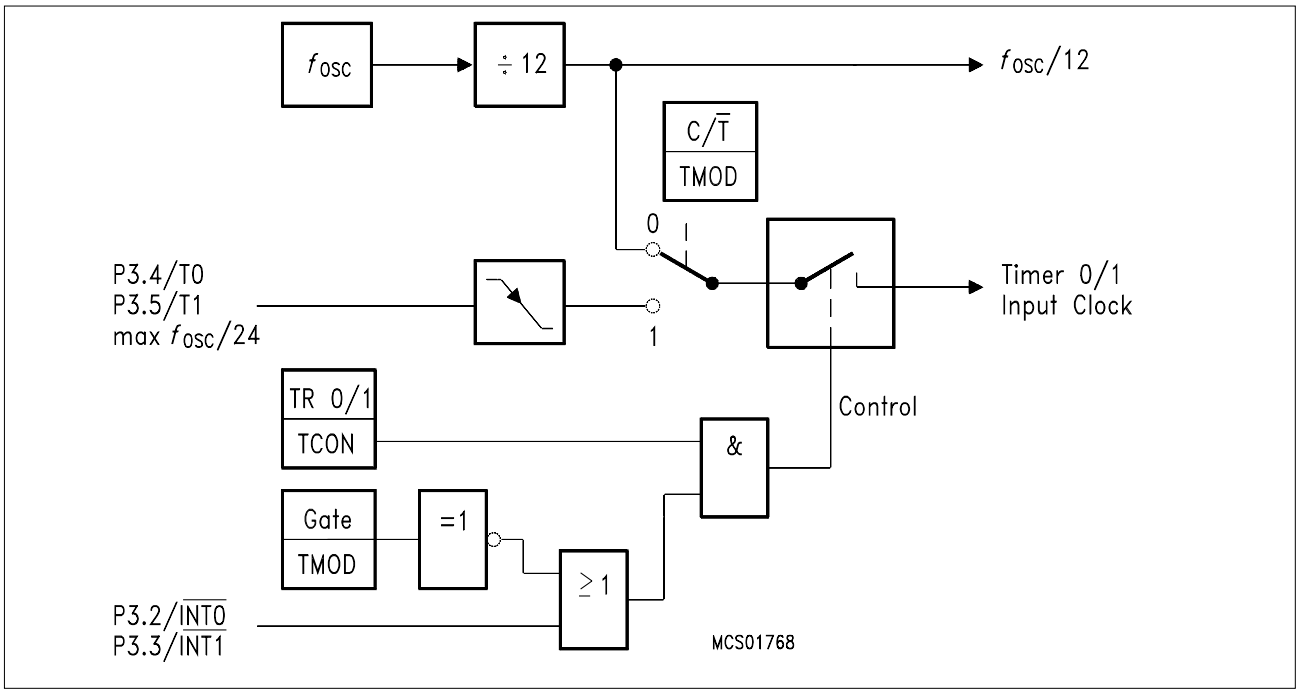


Figure 5
Timer/Counter 0 and 1 Input Clock Logic

Timer 2

Timer 2 is a 16-bit Timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/T2 (T2CON.1). It has three operating modes as shown in **table 5**.

Table 5
Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	R×CLK or T×CLK	$\overline{CP}$/ $\overline{RL2}$	TR2	DCEN	EXEN			internal	external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	$f_{osc}/12$	max $f_{osc}/24$
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Cap-ture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting)	$f_{osc}/12$	max $f_{osc}/24$
	0	1	1	X	1	↓	capture TH2, TL2 → RC2H, RC2L		
Baud Rate Gene-rator	1	X	1	X	0	X	no overflow interrupt	$f_{osc}/2$	max $f_{osc}/24$
	1	X	1	X	1	↓	request (TF2) extra external interrupt (“Timer 2”)		
off	X	X	0	X	X	X	Timer 2 stops	–	–

Note: ↓ = falling edge

Capture/Compare Unit

The Capture / Compare Unit (CCU) of the C504 is built up by a 16-bit 3-channel capture/compare unit (CAPCOM) and a 10-bit 1-channel compare unit (COMP). In compare mode, the CAPCOM unit provides two output signals per channel, which can have inverted signal polarity and non-overlapping pulse transitions. The COMP unit can generate a single PWM output signal and is further used to modulate the CAPCOM output signals. In capture mode, the value of the compare timer 1 is stored in the capture registers if a signal transition occurs at the pins CCx. **Figure 6** shows the block diagram of the CCU.

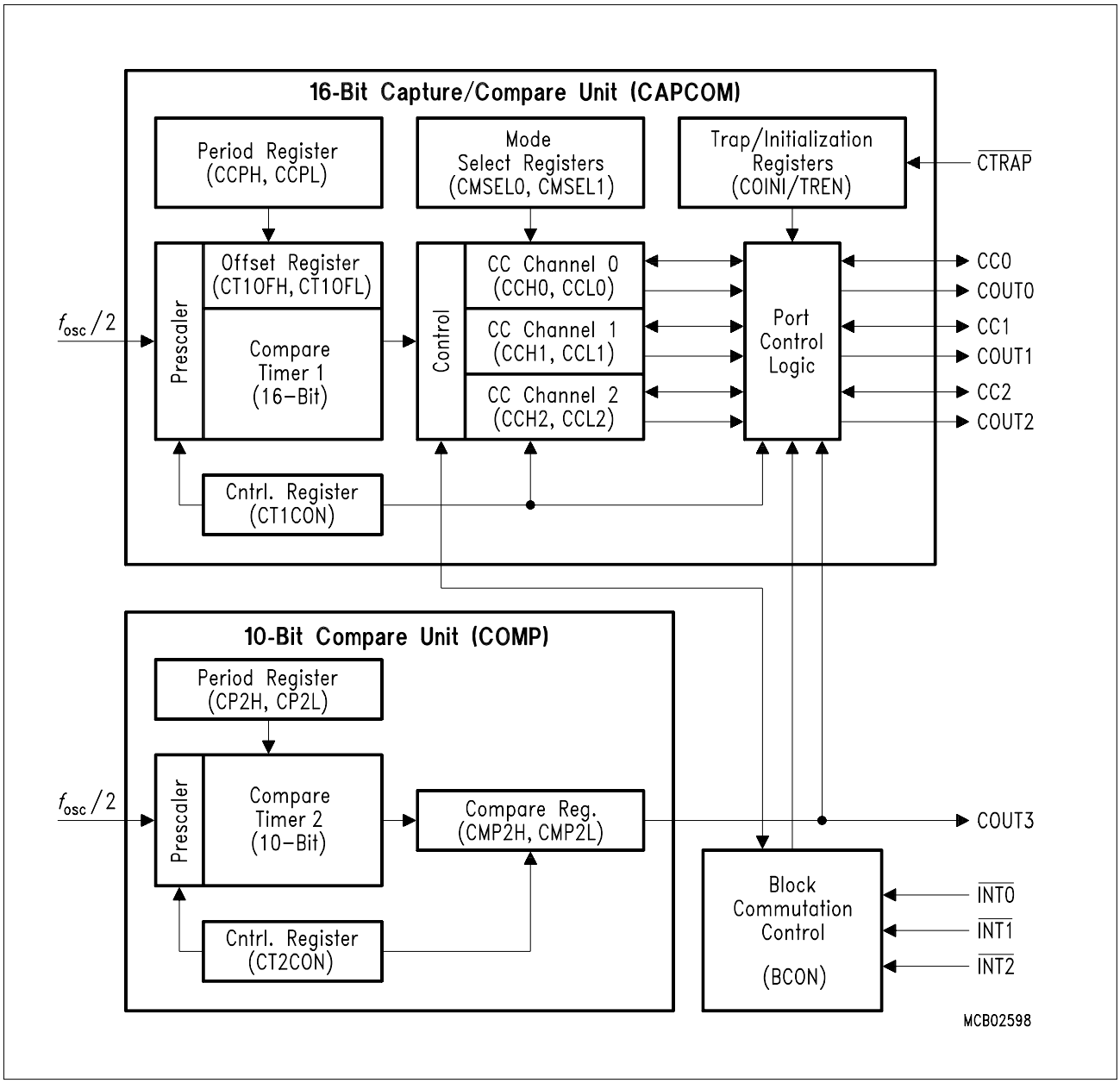


Figure 6
Block Diagram of the CCU

The compare timer 1 and 2 are free running, processor clock coupled 16-bit / 10-bit timers which have each a count rate with a maximum of $f_{OSC}/2$ up to $f_{OSC}/256$. The compare timer operations with its possible compare output signal waveforms are shown in **figure 7**.

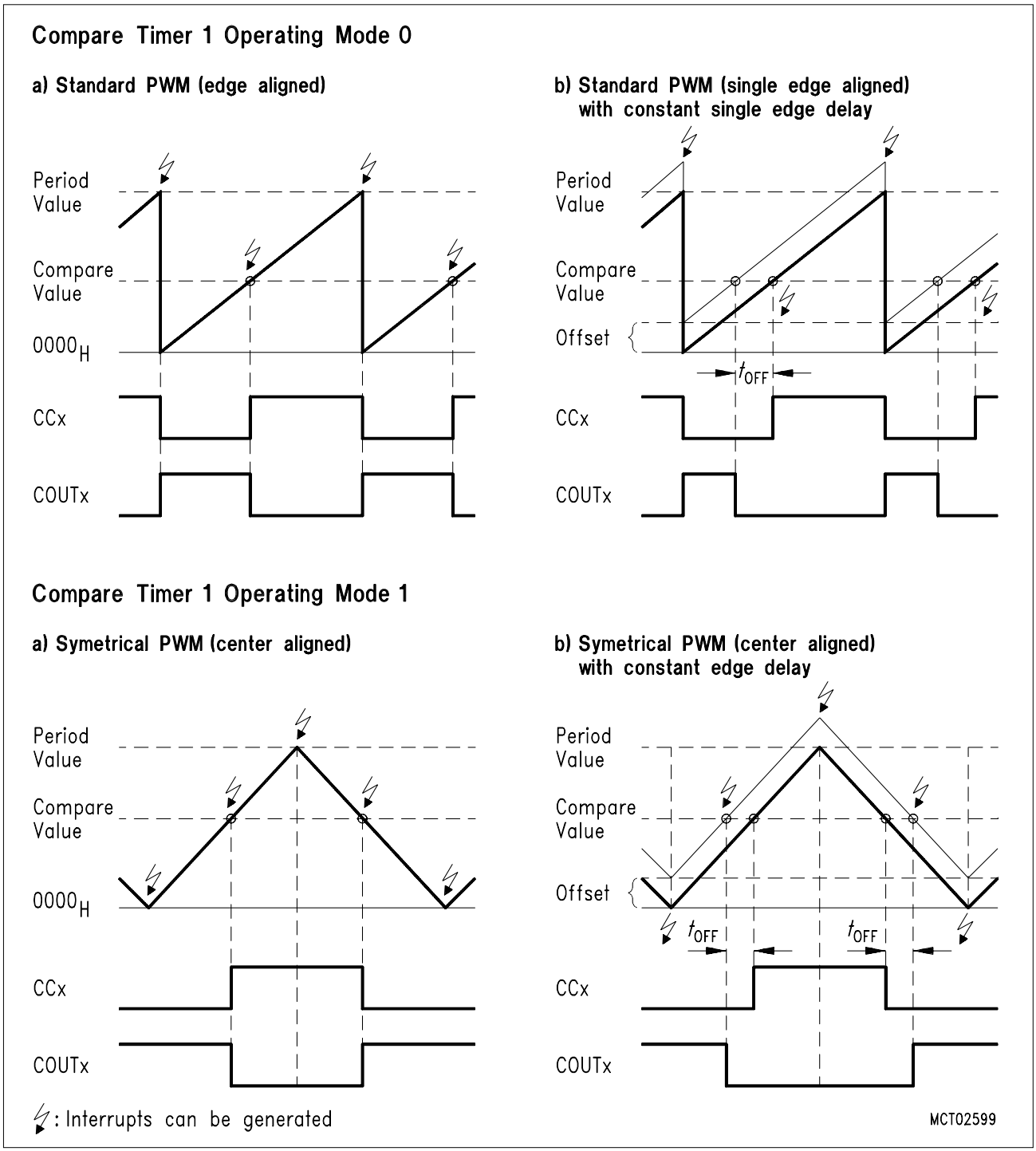


Figure 7
Basic Operating Modes of the CAPCOM Unit

Compare timer 1 runs only in operating mode 1 with one output signal of selectable signal polarity at the pin COUT3.

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6**. The possible baudrates can be calculated using the formulas given in **table 6**.

Table 6
USART Operating Modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{OSC}/12$	Serial data enters and exits through R×D. T×D outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through T×D) or received (R×D)
2	1	0	$f_{OSC}/32$ or $f_{OSC}/64$	9-bit UART 11 bits are transmitted (T×D) or received (R×D)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

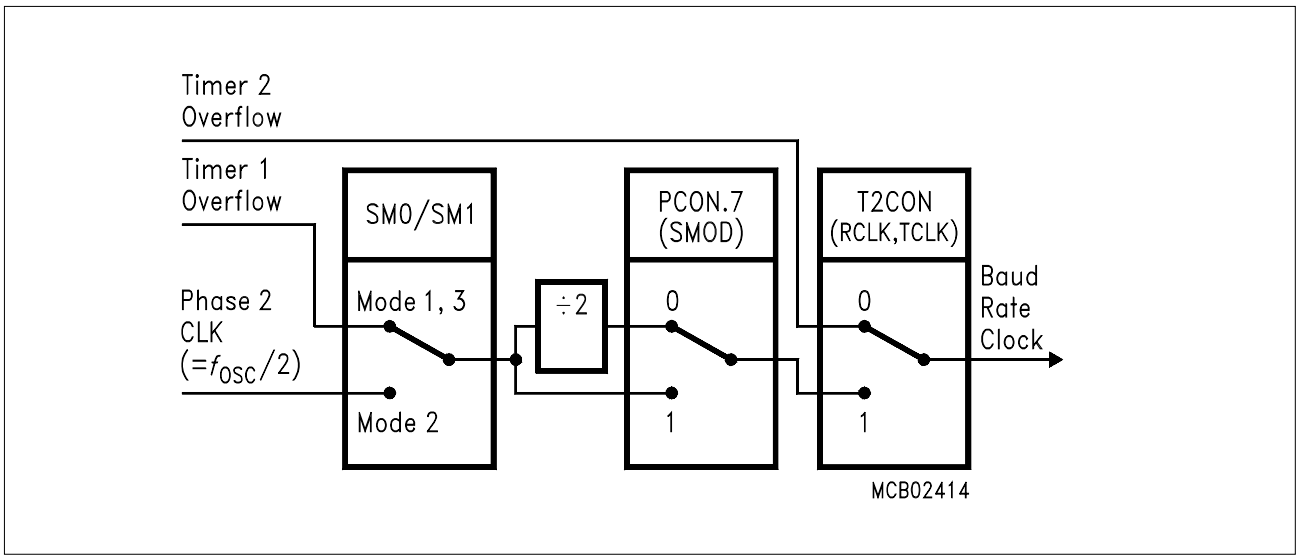


Figure 8
Block Diagram of Baud Rate Generation for the Serial Interface

The possible baudrates can be calculated using the formulas given in **table 7**.

Table 7
Formulas for Calculating Baudrates

Baud Rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{OSC}/12$ $(2^{SMOD} \times f_{OSC}) / 64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times$ timer 1 overflow rate$) /32$ $(2^{SMOD} \times f_{OSC}) / (32 \times 12 \times (256-TH1))$
Timer 2	1,3	$f_{OSC} / (32 \times (65536-(RC2H, RC2L))$

10-Bit A/D Converter

The C504 has a high performance 10-bit A/D converter (**figure 9**) with 8 inputs included which uses successive approximation technique for the conversion of analog input voltages.

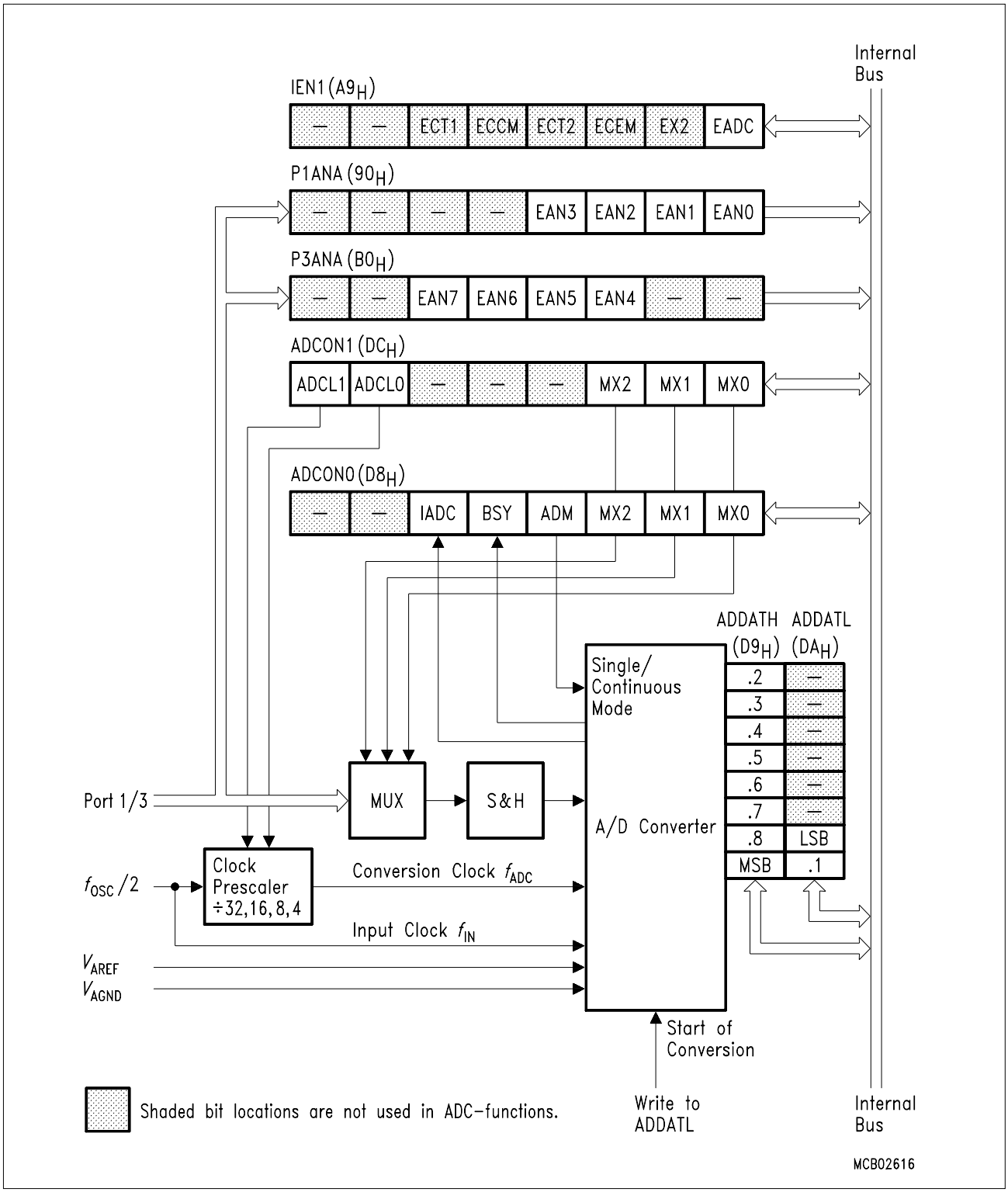
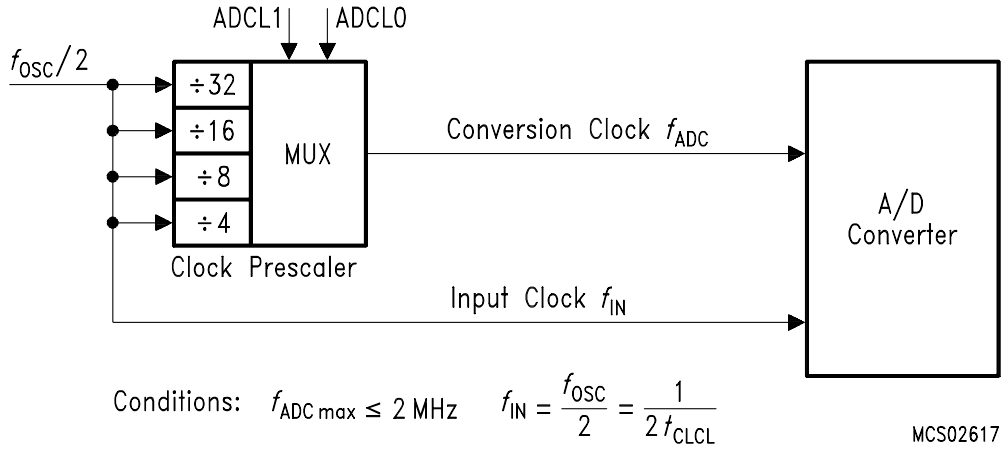


Figure 9
A/D Converter Block Diagram

The A/D converter uses two clock signals for operation : the conversion clock f_{ADC} (= 1/ t_{ADC}) and the input clock f_{IN} (= 1/ t_{IN}). Both clock signals are derived from the C504 system clock f_{OSC} which is applied at the XTAL pins. The duration of an A/D conversion is a multiple of the period of the f_{IN} clock signal. The table in **figure 10** shows the prescaler ratios and the resulting A/D conversion times which must be selected for typical system clock rates.



MCU System Clock Rate (f_{OSC})	f_{IN} [MHz]	Prescaler			f_{ADC} [MHz]	A/D Conversion Time [µs]
		Ratio	ADCL1	ADCL0		
3.5 MHz	1.75	÷ 4	0	0	.438	48 x t_{IN} = 27.4
12 MHz	6	÷ 4	0	0	1.5	48 x t_{IN} = 8
16 MHz	8	÷ 4	0	0	2	48 x t_{IN} = 6
24 MHz	12	÷ 8	0	1	1.5	96 x t_{IN} = 8
32 MHz	16	÷ 8	0	1	2	96 x t_{IN} = 6
40 MHz	20	÷ 16	1	0	1.25	192 x t_{IN} = 9.6

Figure 10
A/D Converter Clock Selection

The analog inputs are located at port 1 and port 3 (4 lines on each port). The corresponding port 1 and port 3 pins have a port structure, which allows to use it either as digital I/Os or analog inputs. The analog input function of these mixed digital/analog port lines is selected via the registers P1ANA and P3ANA.

Interrupt System

The C504 provides 12 interrupt sources with two priority levels. **Figure 11** and **12** give a general overview of the interrupt sources and illustrate the interrupt request and control flags.

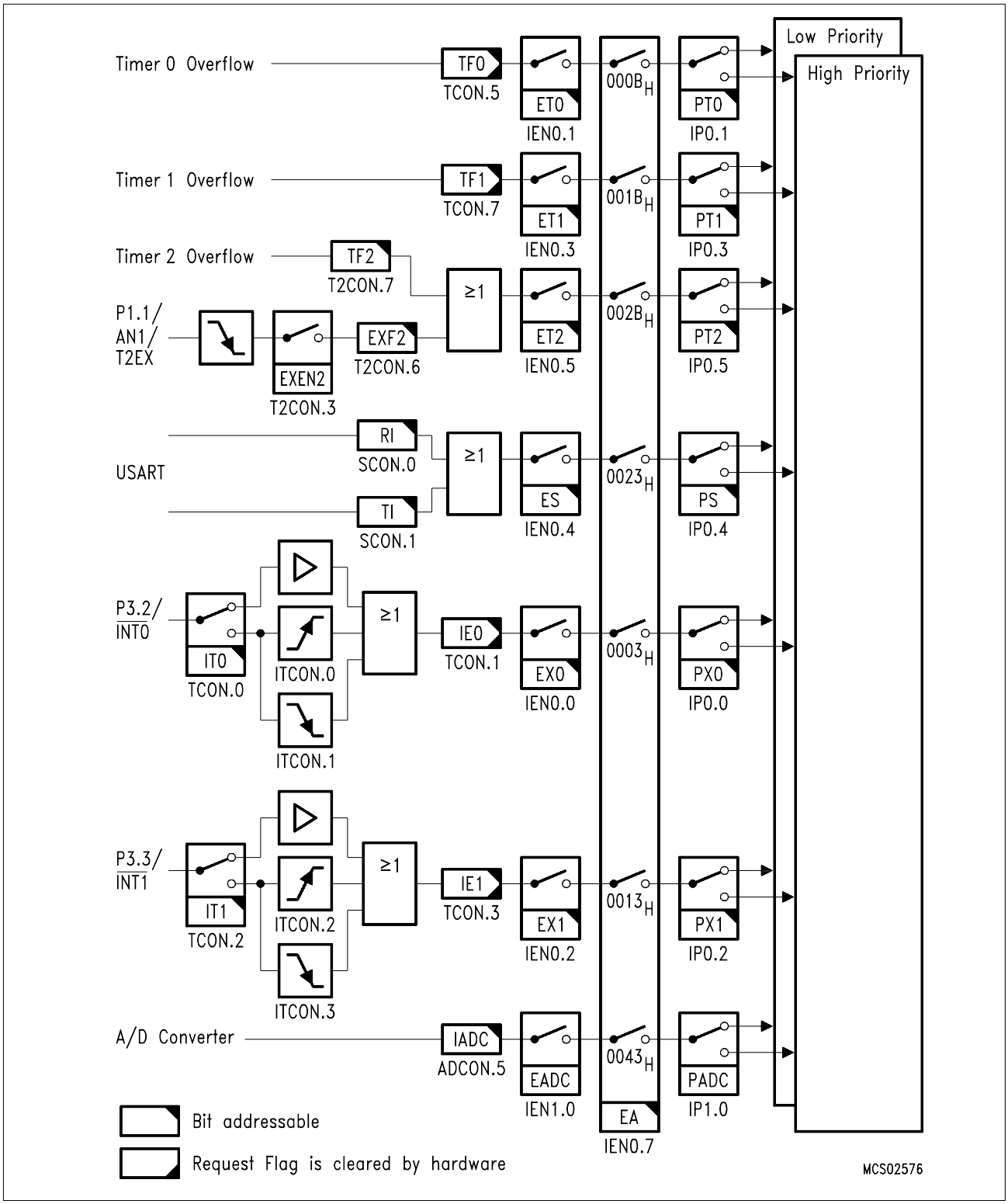


Figure 11
Interrupt Request Sources (Part 1)

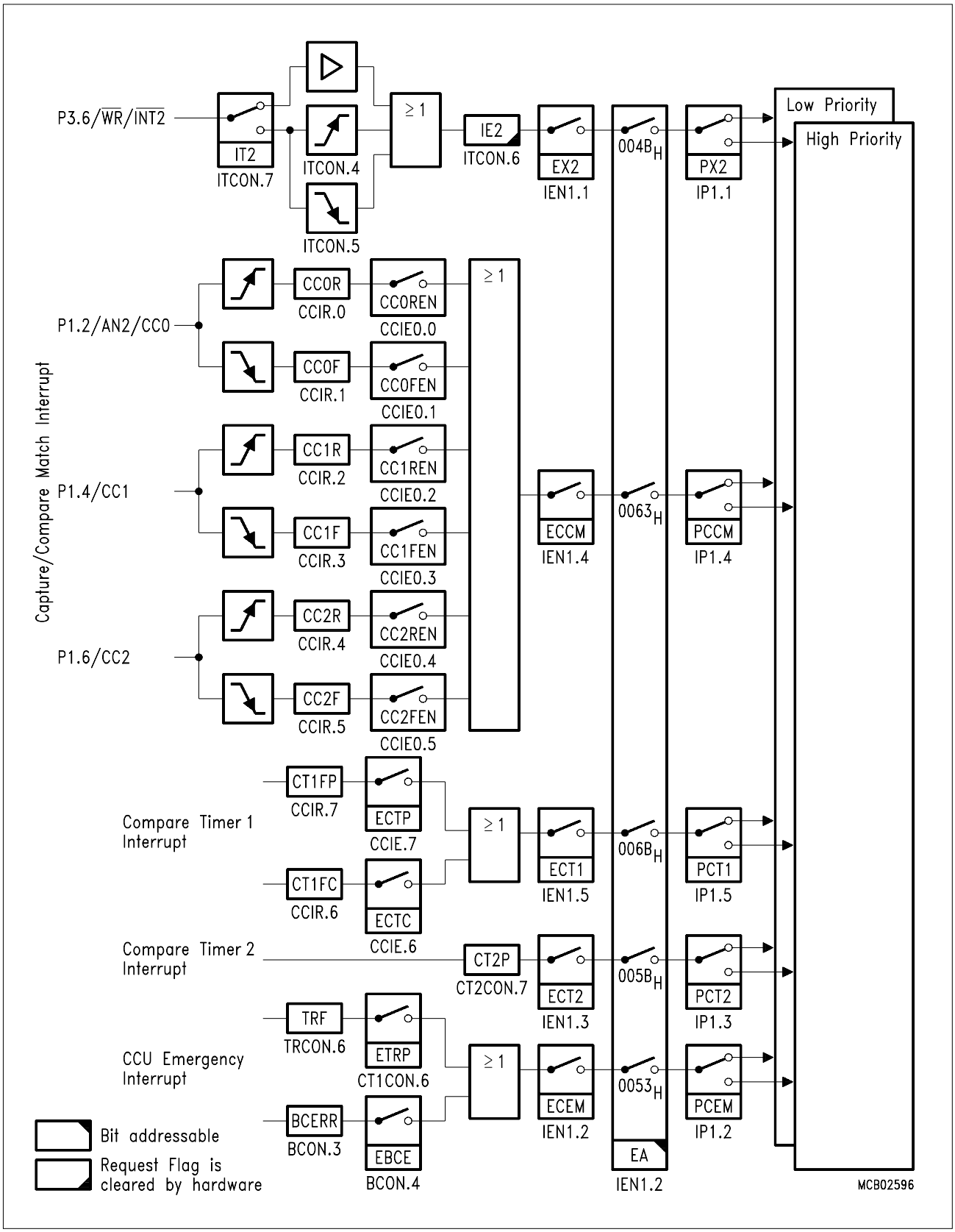


Figure 12
Interrupt Request Sources (Part 2)

Table 8
Interrupt Vector Addresses

Request Flags	Interrupt Source	Vector Address
IE0	External interrupt 0	0003_H
TF0	Timer 0 interrupt	$000B_H$
IE1	External interrupt 1	0013_H
TF1	Timer 1 interrupt	$001B_H$
RI + TI	Serial port interrupt	0023_H
TF2 + EXF2	Timer 2 interrupt	$002B_H$
IADC	A/D converter interrupt	0043_H
IE2	External interrupt 2	$004B_H$
TRF, BCERR	CAPCOM emergency interrupt	0053_H
CT2P	Compare timer 2 interrupt	$005B_H$
CC0F-CC2F, CC0R-CC2R	Capture / compare match interrupt	0063_H
CT1FP, CT1FC	Compare timer 1 interrupt	$006B_H$
–	Power-down interrupt	$007B_H$

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.
If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 9**.

Table 9
Interrupt Source Structure

Interrupt Source		**Priority**
High Priority →	Low Priority	
External Interrupt 0	A/D Converter	High h
Timer 0 Interrupt	External Interrupt 2	
External Interrupt 1	CCU Emergency Interrupt	
Timer 1 Interrupt	Compare Timer 2 Interrupt	
Serial Channel	Capture / Compare Match Interrupt	
Timer 2 Interrupt	Compare Timer 1 Interrupt	Low

Fail Save Mechanisms

The C504 offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure.

- 15-bit reloadable watchdog timer
- Oscillator Watchdog

Watchdog Timer

The watchdog timer in the C504 is a 15-bit timer, which is incremented by a count rate of either f_{SOC}/12 or f_{CYCLE}/32. From the 15-bit watchdog timer count value only the upper 7 bits can be programmed. **Figure 5** shows the block diagram of the programmable watchdog timer.

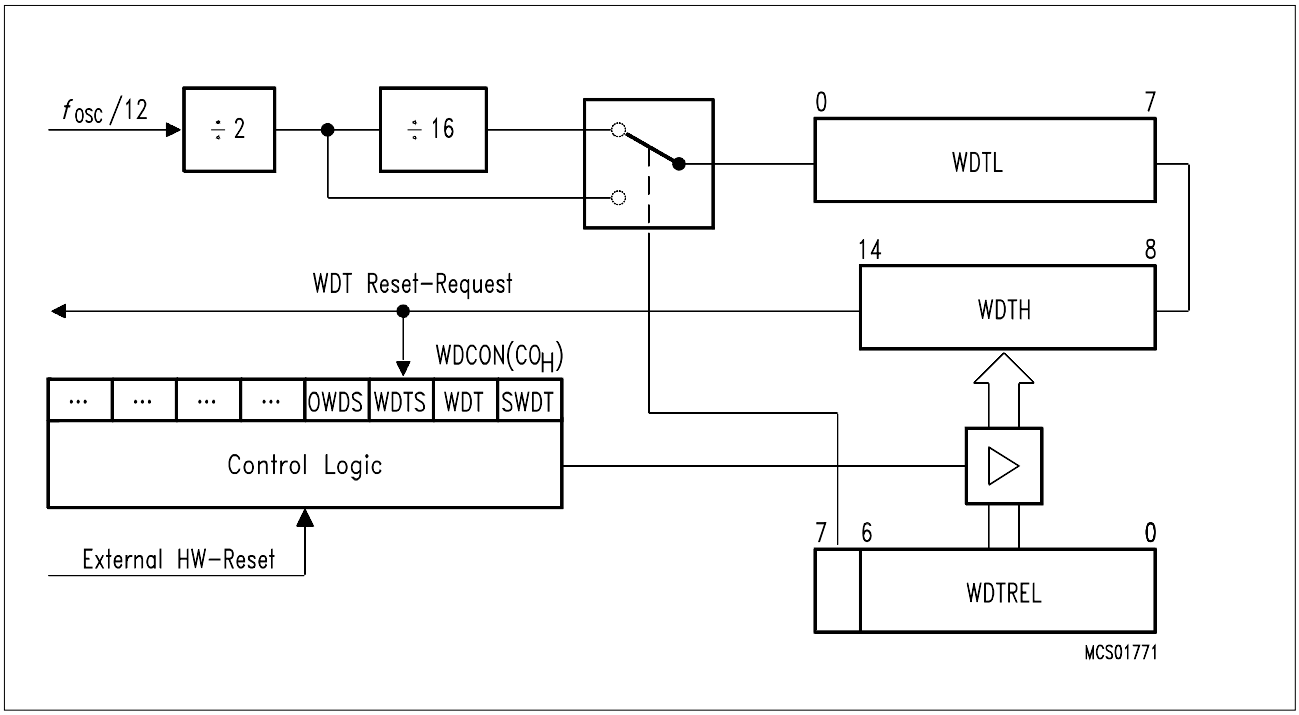


Figure 13
Block Diagram of the Programmable Watchdog Timer

The watchdog timer can be started by software (bit SWDT in SFR WDCON), but it cannot be stopped during active mode of the device. If the software fails to refresh the running watchdog timer an internal reset will be initiated. The reset cause (external reset or reset caused by the watchdog) can be examined by software (status flag WDTS in WDCON is set). A refresh of the watchdog timer is done by setting bits WDT (SFR WDCON) and SWDT consecutively. This double instruction sequence has been implemented to increase system security.

It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor. Therefore, it is possible to use the idle mode in combination with the watchdog timer function.

Oscillator Watchdog

The oscillator watchdog of the C504 serves for three functions :

- **Monitoring of the on-chip oscillator's function**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of an auxiliary RC oscillator, the internal clock is supplied by this RC oscillator and the C504 is put into reset state; if the failure condition again disappears, the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- **Fast internal reset after power-on**
  The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.
- **Control of external wake-up from software power-down mode**
  When the power-down mode is left by a low level at the $\overline{\text{INT0}}$ pin, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts operation after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.

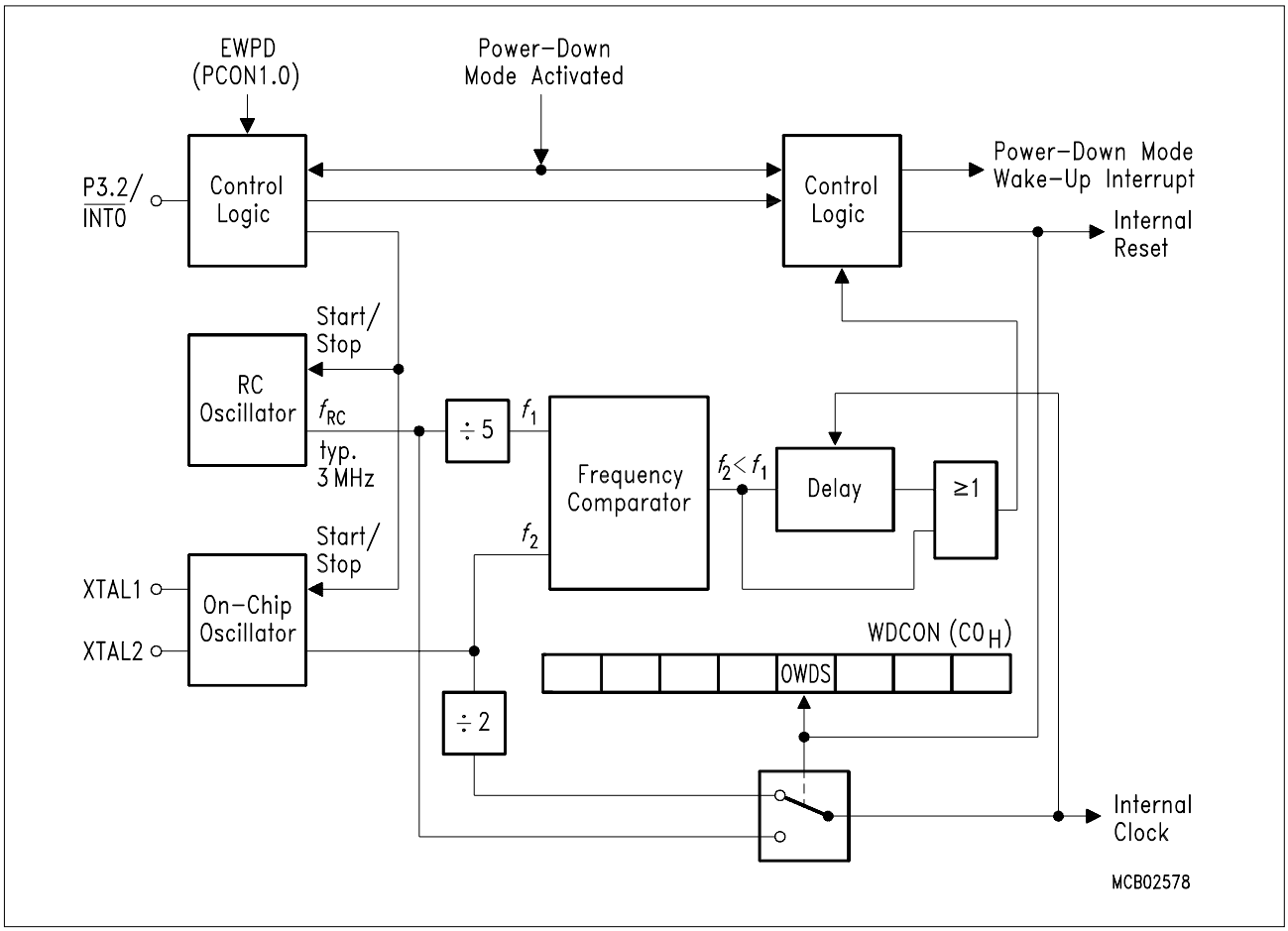


Figure 14
Block Diagram of the Programmable Watchdog Timer

Power Saving Modes

Two power down modes are available, the idle mode and power down mode.

- In the **idle mode** the oscillator of the C504 continues to run, but the CPU is gated off from the clock signal. However, the interrupt system, the serial port, the A/D converter, and all timers with the exception of the watchdog timer are further provided with the clock. The CPU status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode.
- In the **power down** mode, the RC oscillator and the on-chip oscillator which operates with the XTAL pins is stopped. Therefore all functions of the microcontroller are stopped and only the contents of the on-chip RAM, XRAM and the SFR's are maintained. The port pins, which are controlled by their port latches, output the values that are held by their SFR's.

Table 10 gives a general overview of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering 2-Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H ORL PCON, #20H	Ocurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Power-Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR’s are maintained;
		Wake-up from power down	

In the power down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the power down mode is invoked, and that V_{CC} is restored to its normal operating level, before the power down mode is terminated.
The idle mode can be terminated by activating any enabled peripheral interrupt or by resetting the C504. The power down mode can be terminated using an interrupt by a short low pulse at the pin P3.2/AN4/$\overline{\text{INT0}}$ or by resetting the C504. If a power saving mode is left through an interrupt, the microcontroller state (CPU, ports, peripherals) remains preserved. If a power saving mode is left by a reset operation, the microcontroller state is disturbed and replaced by the reset state of the C504.

Absolute Maximum Ratings

Ambient temperature under bias (T_A) ..... 0 ˚C to + 70 ˚C
Storage temperature (T_{ST}).....– 65 ˚C to + 150 ˚C
Voltage on V_{CC} pins with respect to ground (V_{SS}) .....– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS}).....– 0.5 V to V_{CC} + 0.5 V
Input current on any pin during overload condition.....– 10 mA to + 10 mA
Absolute sum of all input currents during overload condition .....| 100 mA |
Power dissipation.....TBD

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504
T_A = – 40 to 110 °C for the SAH-C504
T_A = – 40 to 125 °C for the SAK-C504

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET, $\overline{CTRAP}$)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	V_{IL1}	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET, $\overline{CTRAP}$)	V_{IL2}	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except XTAL1, RESET and $\overline{CTRAP}$)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	V_{IH1}	0.7 V_{CC}	V_{CC} + 0.5	V	–
Input high voltage to RESET and $\overline{CTRAP}$	V_{IH2}	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3, COUT3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	V_{OL1}	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (ports 1,3 pins in push-pull mode and COUT3)	V_{OH1}	0.9 V_{CC}	–	V	I_{OH} = – 800 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	V_{OH2}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA [2], I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	–	± 5	mA	[7] [8]

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. [9]	max.		
Power supply current:					
Active mode, 12 MHz [4]	I_{CC}	16	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 12 MHz [5]	I_{CC}	8	TBD	mA	V_{CC} = 5 V, [5]
Active mode, 24 MHz [4]	I_{CC}	25	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 24 MHz [5]	I_{CC}	13	TBD	mA	V_{CC} = 5 V, [5]
Active mode, 40 MHz [4]	I_{CC}	38	TBD	mA	V_{CC} = 5 V, [4]
Idle mode, 40 MHz [5]	I_{CC}	17	TBD	mA	V_{CC} = 5 V, [5]
Power-down mode	I_{PD}	1	50	µA	V_{CC} = 2…5.5 V [3]

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (power-down mode) is measured under following conditions:
EA = Port0 = V_{CC} ; RESET = V_{SS} ; XTAL2 = N.C.; XTAL1 = V_{SS} ; V_{AGND} = V_{SS} ; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH} , t_{CHCL} = 5 ns , V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
EA = Port0 = Port1 = RESET = V_{CC} ; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH} , t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = EA = V_{SS} ; Port0 = V_{CC} ; all other pins are disconnected.

6) $I_{CC\ max}$ at other frequencies is given by:
active mode: TBD
idle mode: TBD
where f_{osc} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

7) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. V_{OV} > V_{CC} + 0.5 V or V_{OV} < V_{SS} – 0.5 V). The supply voltage V_{CC} and V_{SS} must remain within the specified limits. The absolute sum of input currents on all port pins may not exceed 50 mA.

8) Not 100 % tested, guaranteed by design characterization.

9) The typical I_{CC} values are periodically measured at T_A = +25 °C but not 100% tested.

A/D Converter Characteristics

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V
4V ≤ V_{AREF} ≤ V_{CC} + 0.1 V;
V_{SS} – 0.1 V ≤ V_{AGND} ≤ V_{SS} + 0.2 V;

T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504
T_A = – 40 to 110 °C for the SAH-C504
T_A = – 40 to 125 °C for the SAK-C504

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	64 x t_{IN} 32 x t_{IN} 16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	384 x t_{IN} 192 x t_{IN} 96 x t_{IN} 48 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS} + 0.5V ≤ V_{IN} ≤ V_{CC} – 0.5V 4)
		–	± 4	LSB	V_{SS} < V_{IN} < V_{SS} + 0.5V V_{CC} – 0.5V < V_{IN} < V_{CC} 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 – 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 – 0.25	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	32 x t_{IN}	64 x t_{IN}	384 x t_{IN}
÷ 16	1	0	16 x t_{IN}	32 x t_{IN}	192 x t_{IN}
÷ 8	0	1	8 x t_{IN}	16 x t_{IN}	96 x t_{IN}
÷ 4	0	0	4 x t_{IN}	8 x t_{IN}	48 x t_{IN}

Further timing conditions : t_{ADC} min = 500 ns
t_{IN} = 2 / f_{OSC} = 2 t_{CLCL}

Notes:

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{CC} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100 % tested, but guaranteed by design characterization.

AC Characteristics for C504-L / C504-2R

V_{CC} = 5 V + 10%, – 15%; V_{SS} = 0 V

T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504
T_A = – 40 to 110 °C for the SAH-C504
T_A = – 40 to 125 °C for the SAK-C504

(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL} - 40$	–	ns
Address setup to ALE	t_{AVLL}	43	–	$t_{CLCL} - 40$	–	ns
Address hold after ALE	t_{LLAX}	30	–	$t_{CLCL} - 23$	–	ns
ALE low to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL} - 100$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	$t_{CLCL} - 25$	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL} - 35$	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL} - 100$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	63	–	$t_{CLCL} - 20$	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	75	–	$t_{CLCL} - 8$	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL} - 115$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C504 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for C504-L / C504-2R (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	114	–	$2t_{CLCL} - 53$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	294	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics for C504-L24 / C504-2R24

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504

(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	–	$2t_{CLCL}$ – 40	–	ns
Address setup to ALE	t_{AVLL}	17	–	t_{CLCL} – 25	–	ns
Address hold after ALE	t_{LLAX}	17	–	t_{CLCL} – 25	–	ns
ALE low to valid instr in	t_{LLIV}	–	80	–	$4t_{CLCL}$ – 87	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	22	–	t_{CLCL} – 20	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	95	–	$3t_{CLCL}$ – 30	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	60	–	$3t_{CLCL}$ – 65	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	32	–	t_{CLCL} – 10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	37	–	t_{CLCL} – 5	–	ns
Address to valid instr in	t_{AVIV}	–	148	–	$5t_{CLCL}$ – 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C504 to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for C504-L24 / C504-2R24 (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	–	$6t_{CLCL} - 70$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	–	$6t_{CLCL} - 70$	–	ns
Address hold after ALE	t_{LLAX2}	56	–	$2t_{CLCL} - 27$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	118	–	$5t_{CLCL} - 90$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0		0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	63	–	$2t_{CLCL} - 20$	ns
ALE to valid data in	t_{LLDV}	–	200	–	$8t_{CLCL} - 133$	ns
Address to valid data in	t_{AVDV}	–	220	–	$9t_{CLCL} - 155$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	75	175	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$	t_{AVWL}	67	–	$4t_{CLCL} - 97$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	17	67	$t_{CLCL} - 25$	$t_{CLCL} + 25$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 37$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	170	–	$7t_{CLCL} - 122$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	15	–	$t_{CLCL} - 27$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	41.7	294	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	12	ns
Fall time	t_{CHCL}	–	12	ns

AC Characteristics for C504-L40 / C504-2R40

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V T_A = 0 to 70 °C for the SAB-C504
T_A = – 40 to 85 °C for the SAF-C504

(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	$2t_{CLCL}$ – 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	t_{CLCL} – 15	–	ns
Address hold after ALE	t_{LLAX}	10	–	t_{CLCL} – 15	–	ns
ALE low to valid instr in	t_{LLIV}	–	55	–	$4t_{CLCL}$ – 45	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	t_{CLCL} – 15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	60	–	$3t_{CLCL}$ – 15	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	25	–	$3t_{CLCL}$ – 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	20	–	t_{CLCL} – 5	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	t_{CLCL} – 5	–	ns
Address to valid instr in	t_{AVIV}	–	65	–	$5t_{CLCL}$ – 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	– 5	–	– 5	–	ns

*) Interfacing the C504 to devices with float times up to 25 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for C504-L40 / C504-2R40 (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40-MHz clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	$6t_{CLCL} - 30$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	$6t_{CLCL} - 30$	–	ns
Address hold after ALE	t_{LLAX2}	35	–	$2t_{CLCL} - 15$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	$5t_{CLCL} - 50$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0		0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	$2t_{CLCL} - 12$	ns
ALE to valid data in	t_{LLDV}	–	150	–	$8t_{CLCL} - 50$	ns
Address to valid data in	t_{AVDV}	–	150	–	$9t_{CLCL} - 75$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	$3t_{CLCL} - 15$	$3t_{CLCL} + 15$	ns
Address valid to $\overline{WR}$	t_{AVWL}	70	–	$4t_{CLCL} - 30$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	$t_{CLCL} - 15$	$t_{CLCL} + 15$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 20$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	$7t_{CLCL} - 50$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	$t_{CLCL} - 20$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	294	ns
High time	t_{CHCX}	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	10	ns
Fall time	t_{CHCL}	–	10	ns

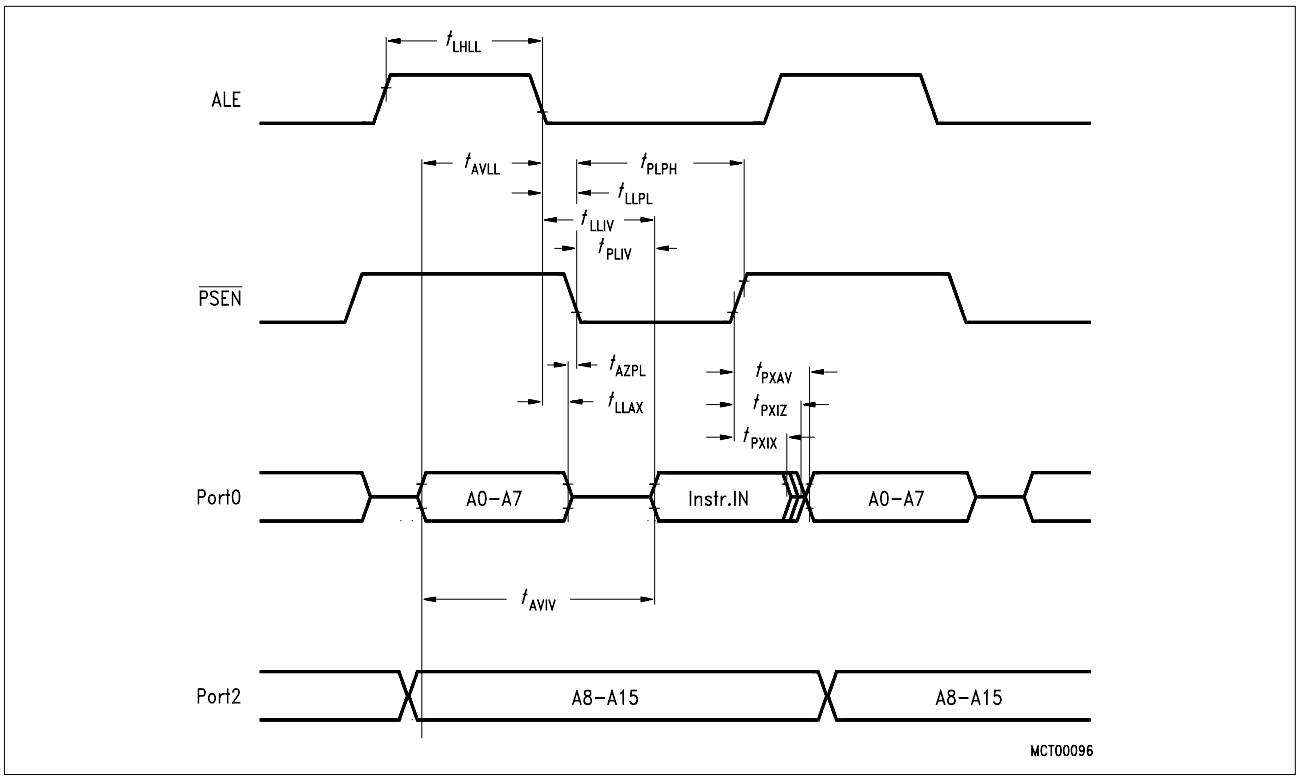


Figure 15
Program Memory Read Cycle

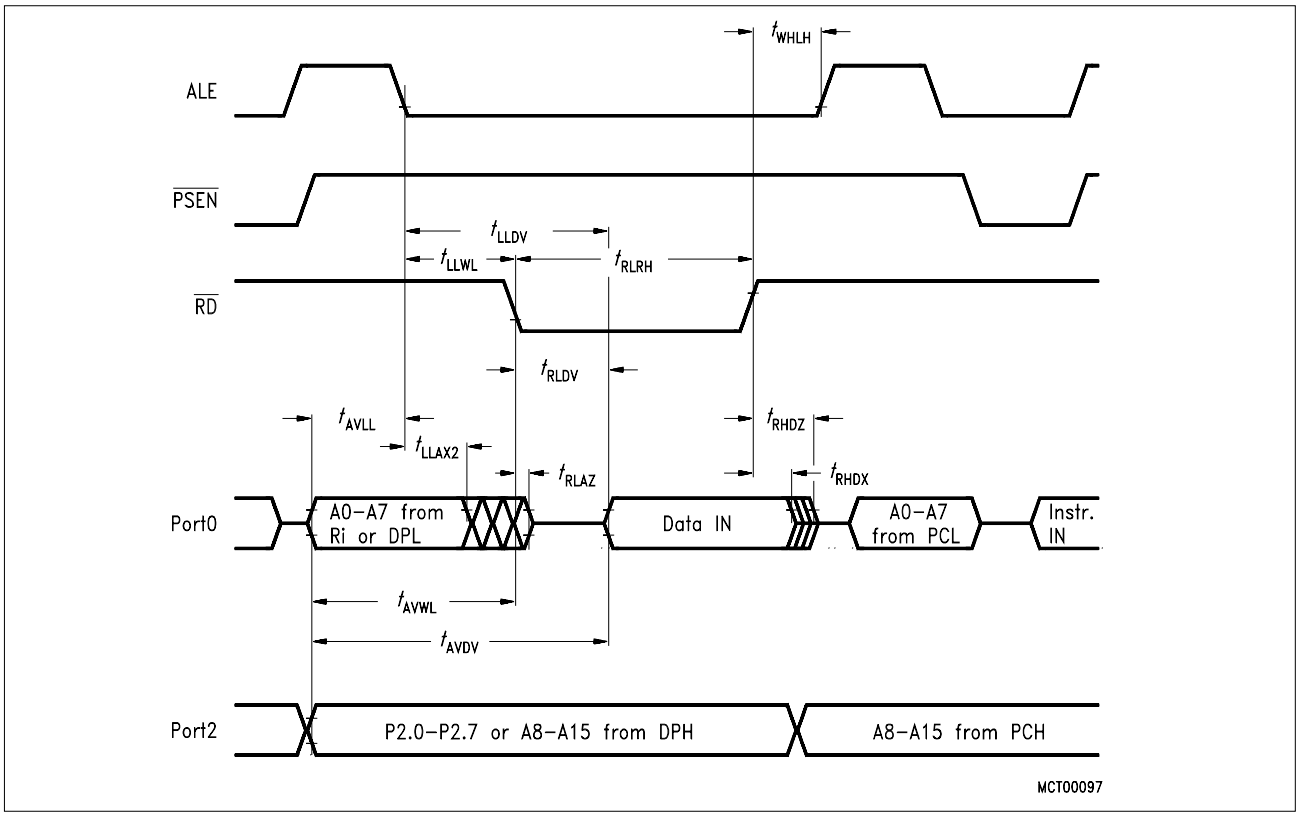


Figure 16
Data Memory Read Cycle

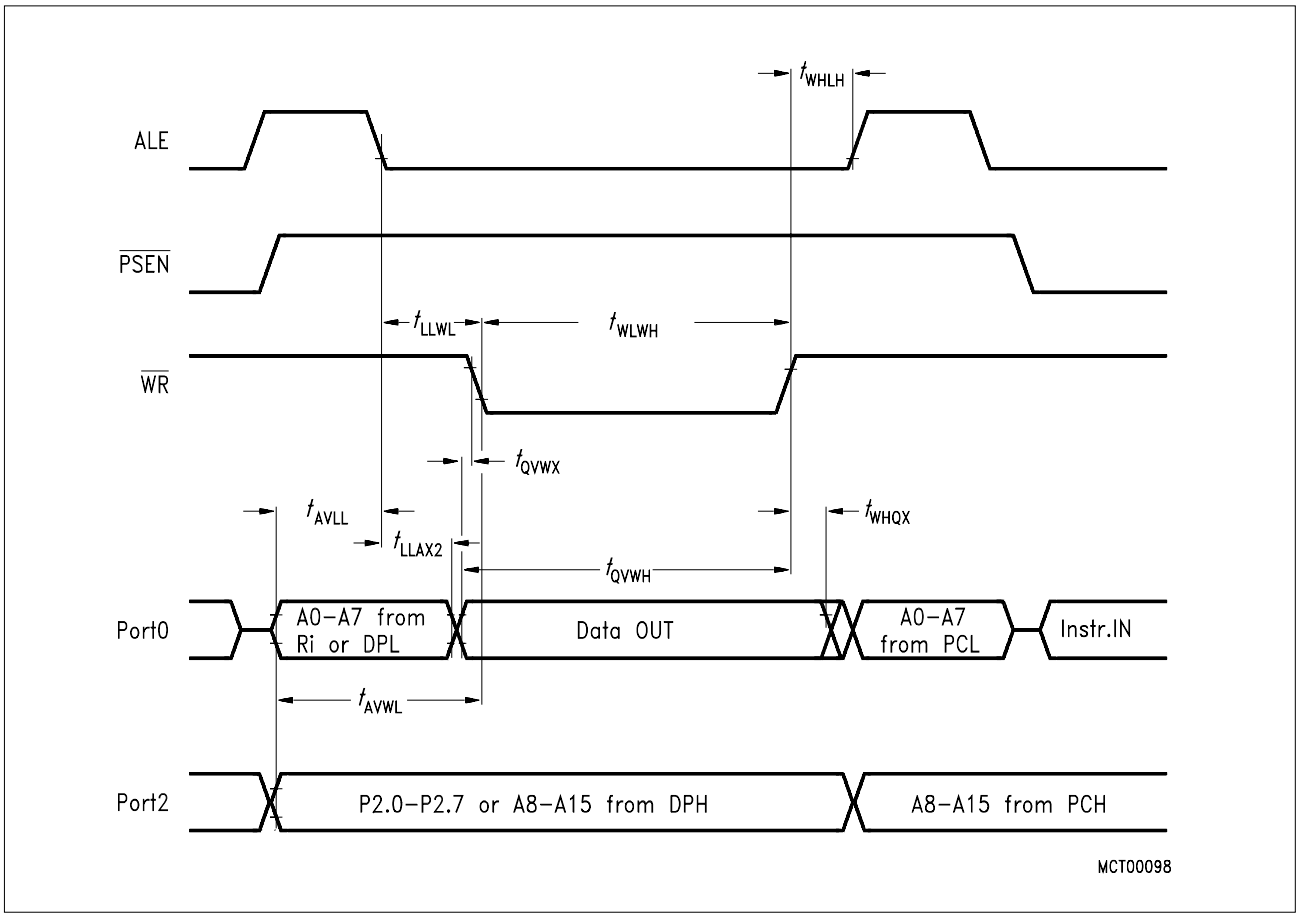


Figure 17
Data Memory Write Cycle

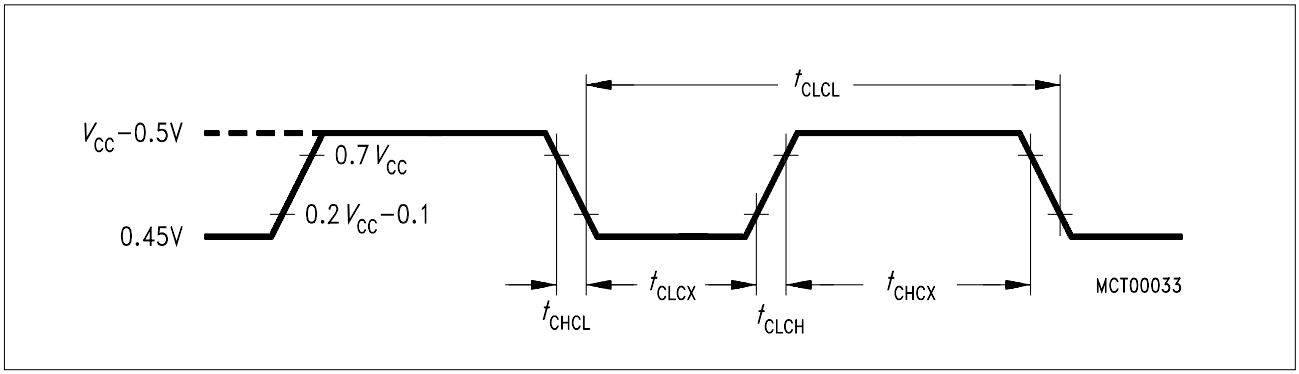
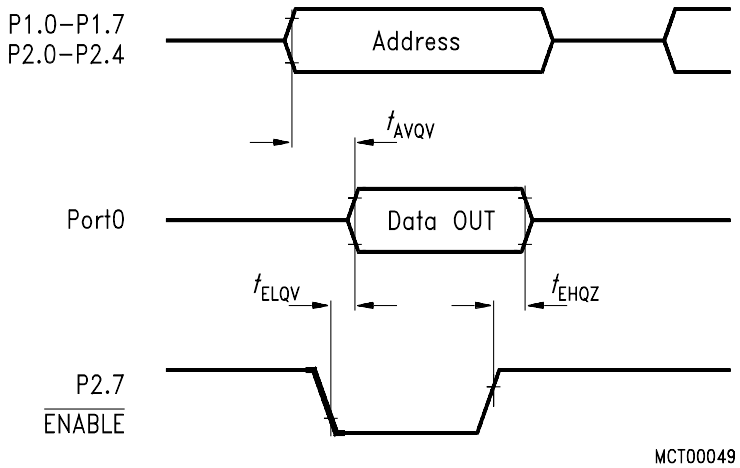


Figure 18
External Clock Cycle

ROM Verification Characteristics for C504-2R

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0–P1.7=A0–A7
P2.0–P2.4=A8–A12
Data: P0.0–P0.7=D0–D7

Inputs: P2.5–P2.6, $\overline{PSEN}=V_{SS}$
ALE, $\overline{EA}=V_{IH}$
RESET = V_{IH1}

Figure 19
ROM Verification Mode 1

ROM Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	2 t_{CLCL}	–	ns
ALE period	t_{ACY}	–	12 t_{CLCL}	–	ns
Data valid after ALE	t_{DVA}	–	–	4 t_{CLCL}	ns
Data stable after ALE	t_{DSA}	8 t_{CLCL}	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CLCL}	–	ns
Oscillator frequency	$1/t_{CLCL}$	4	–	6	MHz

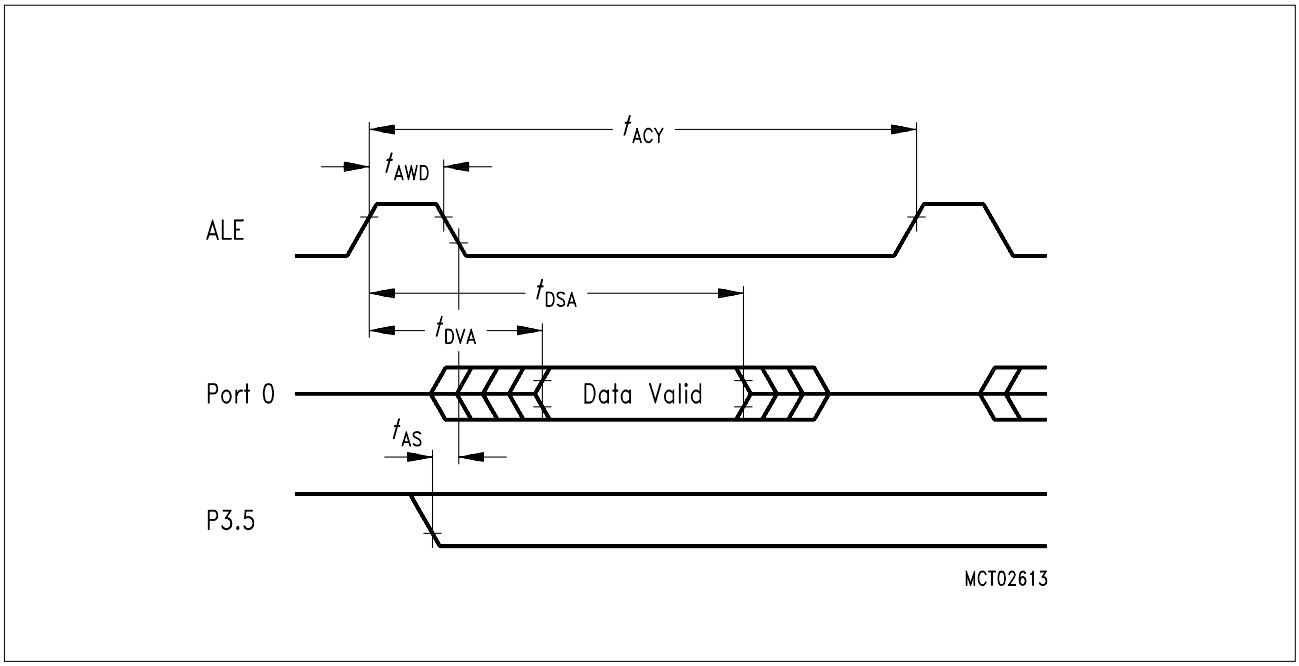
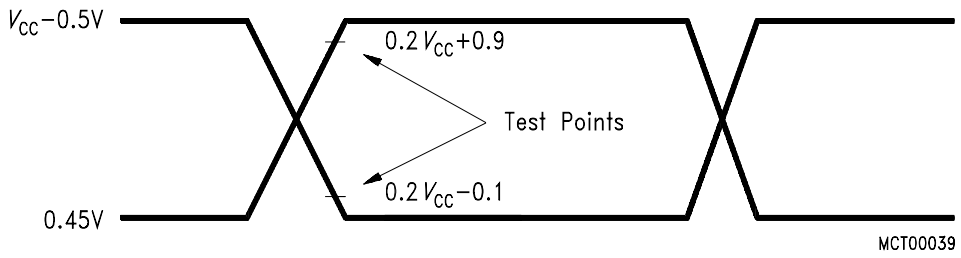
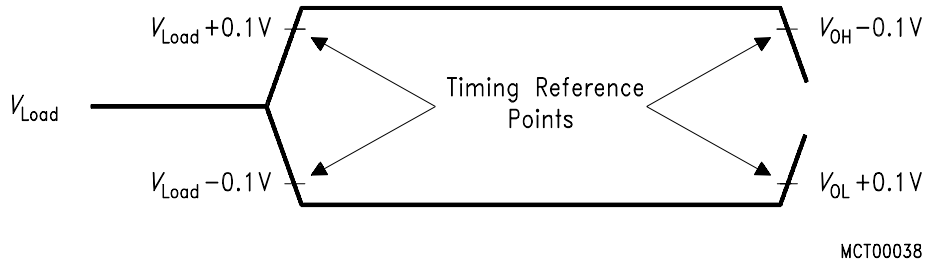


Figure 20
ROM Verification Mode 2



AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 21
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 22
AC Testing : Float Waveforms

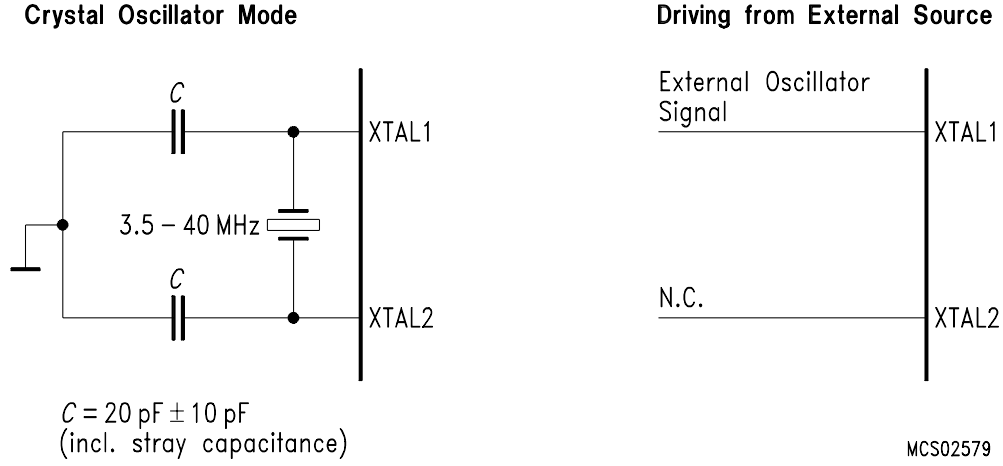


Figure 23
Recommended Oscillator Circuits for Crystal Oscillator