

**Document Title**

**128Kx24 Bit High-Speed CMOS Static RAM(3.3V Operating)  
Operated at Commercial and Industrial Temperature Ranges.**

**Revision History**

<b><u>Rev.No.</u></b>	<b><u>History</u></b>	<b><u>Draft Data</u></b>	<b><u>Remark</u></b>
Rev. 0.0	Design-In Specification	Dec. 05. 2000	Design-In
Rev. 0.1	Pin Configurations Modified ( page 2 ) Add Timing Diagram page 6 ~ 8 )	Mar. 07. 2001	Preliminary
Rev. 0.2	Modified Read Cycle Timing(2)	April. 04.2001	Preliminary
Rev. 0.3	1) Version change from M to D 2) Cin from 20 to 15 pF 3) Icc from 300 to 170mA for 9ns products from 270 to 150mA for 10ns products from 240 to 130mA for 12ns products 4) Isb ( TTL ) from 120 to 40 mA for all products ( CMOS ) from 30 to 15 mA for all products 5) Part number change from -9 to -09 for 9ns products	June. 23.2001	Preliminary
Rev. 0.4	Change write parameter( tDW) from 6ns to 5ns at -10	Oct. 31. 2001	Preliminary
Rev. 1.0	Final Specification Release	Dec. 19. 2001	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

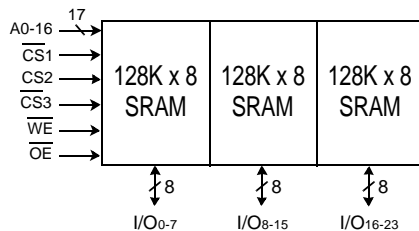


## 128K x 24 Bit High-Speed CMOS Static RAM(3.3V Operating)

## FEATURES

- Fast Access Time 9,10,12ns
- Power Dissipation
  - Standby (TTL) : 40mA(Max.)
  - (CMOS) : 15mA(Max.)
- Operating K6R3024V1D-09 : 170mA(Max.)
- K6R3024V1D-10 : 150mA(Max.)
- K6R3024V1D-12 : 130mA(Max.)
- Single 3.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- 119(7x17)Pin Ball Grid Array Package(14mmx22mm)
- Operating in Commercial and Industrial Temperature range.

## FUNCTIONAL BLOCK DIAGRAM



## ORDERING INFORMATION

K6R3024V1D-HC09/HC10/HC12	Commercial Temp.
K6R3024V1D-HI09/HI10/HI12	Industrial Temp.

## PIN CONFIGURATIONS(TOP VIEW)

## K6R3024V1D

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	CS <sub>1</sub>	A	A	NC
C	I/O	NC	CS <sub>2</sub>	NC	CS <sub>3</sub>	NC	I/O
D	I/O	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O
E	I/O	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	I/O
F	I/O	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O
G	I/O	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	I/O
H	I/O	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O
J	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>
K	I/O	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O
L	I/O	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	I/O
M	I/O	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O
N	I/O	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	I/O
P	I/O	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>CC</sub>	I/O
R	I/O	NC	NC	NC	NC	NC	I/O
T	NC	A	A	WE	A	A	NC
U	NC	A	A	OE	A	A	NC

## GENERAL DESCRIPTION

The K6R3024V1D is a 3,145,728-bit high-speed Static Random Access Memory organized as 131,072 words by 24 bits. The K6R3024V1D uses 24 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R3024V1D is a three megabit static RAM constructed on an multilayer laminate substrate using three 3.3V, 128K x 8 static RAMS encapsulated in a Ball Grid Array(BGA).

## PIN FUNCTION

Pin Name	Pin Function
A <sub>0</sub> - A <sub>16</sub>	Addresses Inputs
WE	Write Enable
CS <sub>1</sub> , CS <sub>2</sub> , CS <sub>3</sub>	Chip Select
OE	Output Enable
I/O <sub>0</sub> ~ I/O <sub>23</sub>	Data Inputs/Outputs
V <sub>CC</sub>	Power(+3.3v)
V <sub>SS</sub>	Ground
NC	No Connection

## ABSOLUTE MAXIMUM RATINGS\*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V <sub>CC</sub>	-0.5 to 4.6	V
Power Dissipation		P <sub>d</sub>	2	W
Storage Temperature		T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	Commercial	T <sub>A</sub>	0 to 70	°C
	Industrial	T <sub>A</sub>	-40 to 85	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## TRUTH TABLE

$\overline{\text{CS}}_1$	$\text{CS}_2$	$\overline{\text{CS}}_3$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O	Power
H	X	X	X	X	Standby	High-Z	Standby
X	L	X	X	X	Standby	High-Z	Standby
X	X	H	X	X	Standby	High-Z	Standby
L	H	L	L	H	Read	DATA <sub>OUT</sub>	Active
L	H	L	X	L	Write	DATA <sub>IN</sub>	Active
L	H	L	H	H	Outputs Disabled	High-Z	Active

RECOMMENDED DC OPERATING CONDITIONS\*(T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3***	V
Input Low Voltage	V <sub>IL</sub>	-0.3**	-	0.8	V

\* The above parameters are also guaranteed at industrial temperature range.

\*\* V<sub>IL</sub>(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

\*\*\* V<sub>IH</sub>(Max) = V<sub>CC</sub> + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

**DC AND OPERATING CHARACTERISTICS\***( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{CC}=3.3\pm0.3\text{V}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>ss</sub> to V <sub>CC</sub>		-	6	μA
Output Leakage Current	I <sub>LO</sub>	CS=V <sub>IH</sub> or OE=V <sub>IH</sub> or WE=V <sub>IL</sub> V <sub>OUT</sub> =V <sub>SS</sub> to V <sub>CC</sub>		-	2	μA
Operating Current	I <sub>CC</sub>	Min. Cycle, 100% Duty CS=V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	-09	-	170	mA
			-10	-	150	mA
			-12	-	130	mA
Standby Current	I <sub>SB</sub>	Min. Cycle, CS=V <sub>IH</sub>	-09	-	40	mA
			-10	-	40	mA
			-12	-	40	mA
	I <sub>SB1</sub>	f=0MHz, CS ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V	-09	-	15	mA
			-10	-	15	mA
			-12	-	15	mA
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> =8mA		-	0.4	V
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> =-4mA		2.4	-	V

\* The above parameters are also guaranteed at industrial temperature range.

\*  $\overline{CS}$  represents  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{CS3}$  in this data sheet.  $\overline{CS2}$  as of opposite polarity to  $\overline{CS1}$  and  $\overline{CS3}$ .

**CAPACITANCE\***( $T_A=25^\circ\text{C}$ ,  $f=1.0\text{MHz}$ )

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	-	8	pF
Input Capacitance	$C_{IN}$	$V_{IN}=0\text{V}$	-	15	pF

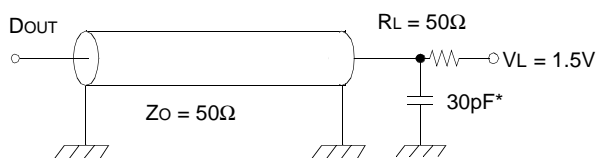
\* Capacitance is sampled and not 100% tested

**AC TEST CONDITIONS\***( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{CC}=3.3\pm0.3\text{V}$ , unless otherwise specified)

Parameter	Value
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and output Timing Reference Levels	1.5V
Output Load	See Below

\* The above parameters are also guaranteed at industrial temperature range.

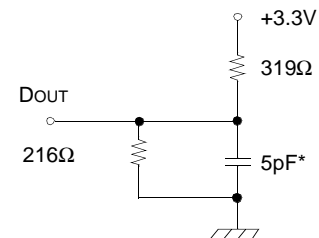
Output Loads(A)



\* Capacitive Load consists of all components of the test environment.

Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



\* Including Scope and Jig Capacitance

## READ CYCLE\*

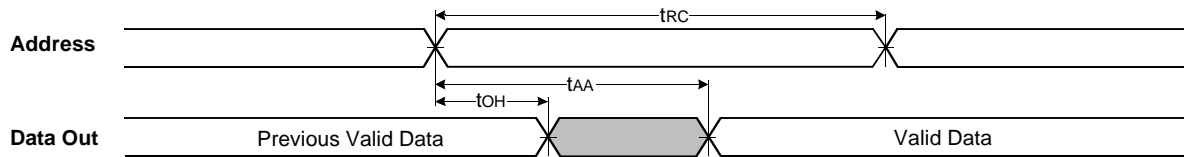
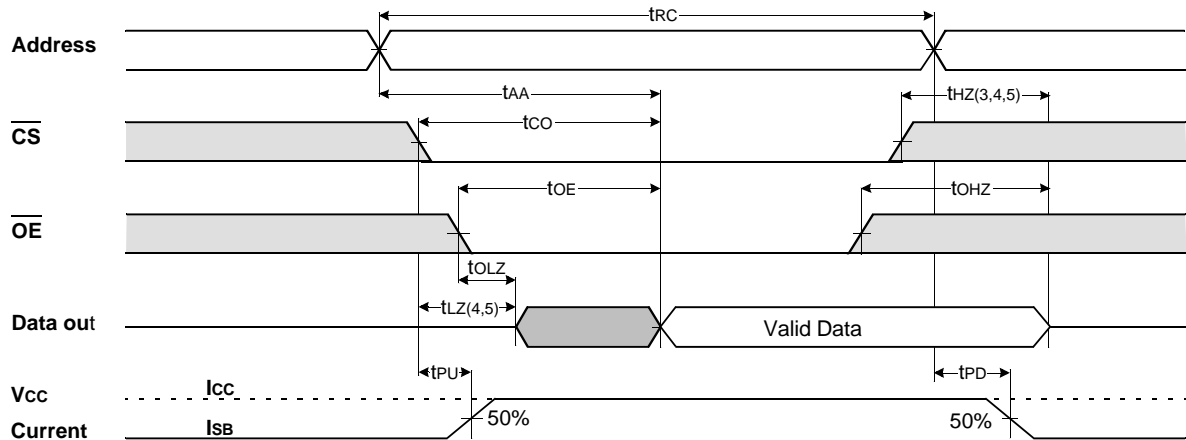
Parameter	Symbol	K6R3024V1D-09		K6R3024V1D-10		K6R3024V1D-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	9	-	10	-	12	-	ns
Address Access Time	t <sub>AA</sub>	-	9	-	10	-	12	ns
Chip Select to Output	t <sub>CO</sub>	-	9	-	10	-	12	ns
Output Enable to Valid Output	t <sub>OE</sub>	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	t <sub>LZ</sub>	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	5	0	6	0	7	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	ns
Chip Select to Power-Up Time	t <sub>PU</sub>	0	-	0	-	0	-	ns
Chip Deselect to Power DownTime	t <sub>PD</sub>	-	9	-	10	-	12	ns

## WRITE CYCLE\*

Parameter	Symbol	K6R3024V1D-09		K6R3024V1D-10		K6R3024V1D-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	9	-	10	-	12	-	ns
Chip Select to End of Write	t <sub>CW</sub>	7	-	7	-	8	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Address Valid to End of Write	t <sub>AW</sub>	7	-	7	-	8	-	ns
Write Pulse Width( $\overline{\text{OE}}$ High)	t <sub>WP</sub>	7	-	7	-	8	-	ns
Write Pulse Width( $\overline{\text{OE}}$ Low)	t <sub>WP1</sub>	9	-	9	-	10	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	ns
Write to Output High-Z	t <sub>WHZ</sub>	0	5	0	5	0	5	ns
Data to Write Time Overlap	t <sub>DW</sub>	5	-	5	-	7	-	ns
Data Hold from Write Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
End Write to Output Low-Z	t <sub>OW</sub>	3	-	3	-	3	-	ns

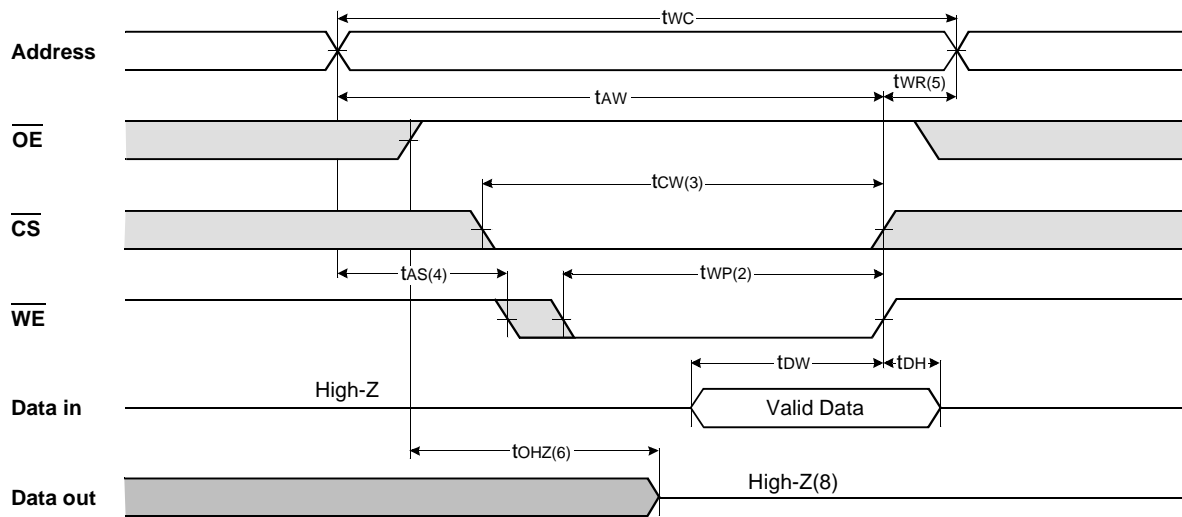
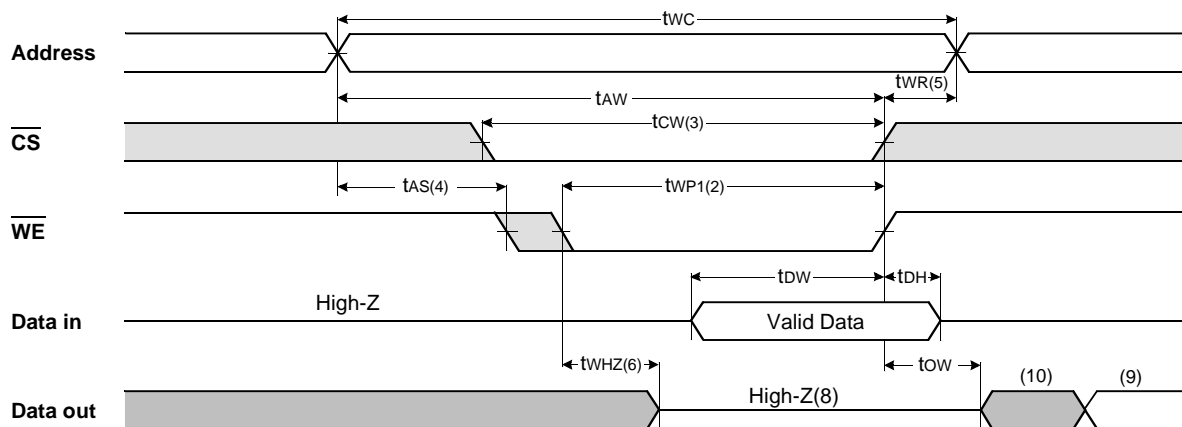
\* This parameter is guaranteed by design but not tested.  
 These specifications are for the individual K6R3024V1D Static RAMs.

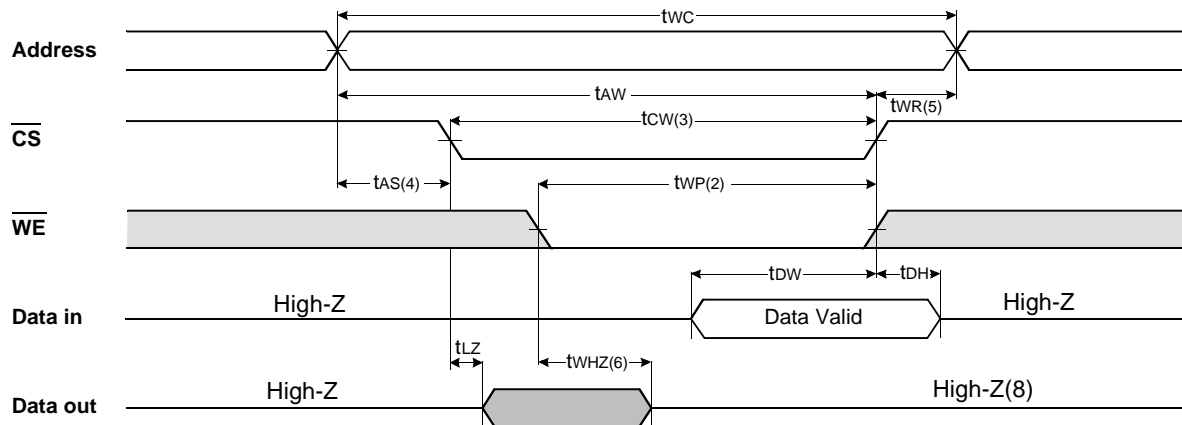
## TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )

## NOTES(READ CYCLE)

1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device.
5. Transition is measured  $\pm 200\text{mV}$  from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CS}=V_{IL}$ .
7. Address valid prior to coincident with  $\overline{CS}$  transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
9.  $\overline{CS}$  represents  $\overline{CS1}$ ,  $\overline{CS2}$  and  $\overline{CS3}$  in this data sheet.  $\overline{CS2}$  as of opposite polarity to  $\overline{CS1}$  and  $\overline{CS3}$ .

TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}$ = Clock)TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{OE}$ =Low Fixed)

TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{\text{CS}}$  = Controlled)

## NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low  $\overline{\text{CS}}$  and  $\overline{\text{WE}}$ . A write begins at the latest transition  $\overline{\text{CS}}$  going low and  $\overline{\text{WE}}$  going low ; A write ends at the earliest transition  $\overline{\text{CS}}$  going high or  $\overline{\text{WE}}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
3.  $t_{CW}$  is measured from the later of  $\overline{\text{CS}}$  going low to end of write.
4.  $t_{AS}$  is measured from the address valid to the beginning of write.
5.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{\text{CS}}$  or  $\overline{\text{WE}}$  going high.
6. If  $\overline{\text{OE}}$ ,  $\overline{\text{CS}}$  and  $\overline{\text{WE}}$  are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If  $\overline{\text{CS}}$  goes low simultaneously with  $\overline{\text{WE}}$  going or after  $\overline{\text{WE}}$  going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When  $\overline{\text{CS}}$  is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.
11.  $\overline{\text{CS}}$  represents  $\overline{\text{CS}}_1$ ,  $\overline{\text{CS}}_2$  and  $\overline{\text{CS}}_3$  in this data sheet.  $\overline{\text{CS}}_2$  as of opposite polarity to  $\overline{\text{CS}}_1$  and  $\overline{\text{CS}}_3$ .



## 119 BGA PACKAGE DIMENSIONS

