DATA SHEET

TZA1032
Laser driver and controller circuit

Preliminary specification

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CONTENTS

Laser driver and controller circuit TZA1032

1 FEATURES

- Separate 3.3 V digital, analog and output driver power supplies
- Selective power-down of internal functions via I²C-bus for power saving
- Low voltage-swing of the differential Run Length Limited Code (RLC) inputs for high speed transmission and good electromagnetic compatibility
- High-impedance input switching to control two or more TZA1032 ICs in parallel for double writer applications
- Supports I²C-bus interface up to 400 kbits/s with block transfer feature in slave mode only
- 3.3 and 5 V tolerant input logic
- Supports any RLC code with run lengths from 1 to 15
- Automatic write-read switching for run lengths ≥16
- Channel decoding rate up to 105 Mbits/s, according to DVD 4×
- Look back function to enable write pre-compensation by data dependent write strategy with a land-pit compensation up to five
- Supports Forced Erase (FE) mode for quick initialisation of disc
- Fixed propagation delay within RLC clock periods to allow accurate data linking on disc
- Supports CD-R, CD-RW, DVD+RW, DVD-R, DVD-RW and DVR formats or any comparable existing or future format
- Programmable write strategy via I²C-bus; completely flexible up to a maximum of two output level transitions per RLC clock period
- Pulse timing resolution of 2 ns at 500 MHz internal clock
- Minimum pulse width of 4 ns at 500 MHz internal clock
- Four programmable threshold current levels with an 8-bit resolution, and eight programmable delta levels with an 8-bit resolution
- Independent laser threshold and laser delta current control
- Programmable modulation unit
- Pointer memory mapping to allow compact write strategy coding
- PLL oscillator features a self-learning oscillator mode for non-locked operation during read
- Wide frequency range: PLL locking factor ≥2.5
- Two output channels, delta and threshold current levels, each capable of delivering 240 mA delta and 200 mA threshold peak current to the output
- Rise and fall times of 1 to 2 ns, depending on package and laser
- Typical output resistance of 120 Ω
- Programmable current step size for a threshold level of 0 to 1 mA at a 16-bit resolution, and a delta level of 0 to 1.2 mA at an 8-bit resolution
- Internal modulator up to 565 MHz
- Forward Sense (FS) Laser Power Control (LPC) loop to compensate laser drift due to temperature and aging
- Internal set point generation to allow read-write switching without any transient effects
- Digital LPC algorithm based on FS feedback
- Single forward sense diode connection
- Programmable FS input current gain to allow for spread in FS efficiency
- Supports running Optimum Power Control (OPC) loop, so called alpha loop, to monitor and control the quality of writing
- Programmable loop bandwidths: up to 1 kHz for the LPC, and up to 50 kHz for the alpha loop
- Programmable minimum and maximum limiting of laser currents and running OPC range
- Programmable OPC stepper.

2 GENERAL DESCRIPTION

The TZA1032 is a laser driver circuit which is intended for a wide range of recordable and re-writable optical drives. Figure 3 shows a function diagram of TZA1032 in relation to a disc recording system. The TZA1032 is intended to be located close to the laser diode on the Optical Pick-up Unit (OPU). It can be used in CD-R/RW systems with 1×, 2×, 4×, 8×, 12×, 16× and 24× (24× is not guaranteed yet: evaluation pending) speed and in DVD-R/RW systems with 1×, 2× and 4× speed (4× is not guaranteed yet). Furthermore, it is suitable for future standards like DVR.

The TZA1032 fulfils three main functions:

- Drives the laser with a sequence of programmable write strategy pulses with high timing accuracy and high peak current levels
- Encodes the input modulated data to a sequence of write strategy pulses. This encoding is flexible with respect to input modulation code (EFM, EFMplus, 17 pp, etc.). Any RLC with run lengths in the range from 1 to 15 is possible. The write strategy is programmable with high flexibility for CD-R/RW, DVD-R/RW, DVR or other optical recording systems using comparable write strategies. For this purpose the TZA1032 includes two Random Access Memories (RAMs) which can be loaded (non real-time) via an I^2C-bus from a PC or microcontroller
- Controls the exact light power levels coming from the laser and controls the exact power absorbed by the disc during recording. This is not trivial since the laser characteristics (both threshold and gain) are strongly temperature dependent. A first control loop controls the laser power levels based on the signal from a forward sense diode (FS control). This will make the laser virtually temperature and aging independent. The loop is fully self-contained, only an external forward sense diode must be connected. A second control loop controls the laser power based on an alpha signal, generated by additional electronics based on signals from the diode during writing. It is primarily intended to compensate for writing performance variations due to imperfections in the optical path and/or disc (e.g. finger prints). The alpha signal is a measure of the power absorption of the disc material during the writing process or in general of the writing quality on the disc. For this second loop, a method of stepping the set point under external control is provided. The TZA1032 contains a programmable counter that can be clocked via the external OPC-strobe (pin OPC). This function is typically used during OPC in order to calibrate the optimum laser writing power.

When required, non-real time control is possible via an interrupt feedback signal at pin $\overline{IRQ}$.

The TZA1032 can supply the analog, digital and driver part separately to obtain maximum performance.

The TZA1032 features three independent power supplies. These are the analog and digital power supplies and a local power supply for the laser driver function. The supplies can be delivered separately to obtain maximum output performance of the TZA1032 in environments with large and highly dynamic current flows. The driver supply has no accompanying ground because the laser driver block only sources current to the laser. Ensure that all power supply pins are connected to the appropriate voltage rails.

For evaluation purposes only (by special request) the TZA1032 can be delivered in a LQFP64 package.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA1032UK	–	bare die with solder bumps	–

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$V_{DD[1\ to\ 3]}$	output supply voltage		3.0	3.3	3.6	V
$I_{OUT[1\ to\ 3]}$	output current (threshold)		1	–	200	mA
	output current (delta)		0	–	240	mA
$R_{OUT[1\ to\ 3]}$	output resistance		–	120	–	Ω
t_r, t_f	rise and fall time	depends on package and load	–	–	1 to 2	ns
rI_{min}	decodable run length		1	–	15	
$B_{LPC(-3dB)}$	−3dB LPC bandwidth		–	1	–	kHz
$B_{alpha(-3dB)}$	−3dB alpha bandwidth		–	50	–	kHz
f_{mod}	modulator frequency	PLL locked to external clock	250	–	565	MHz
		PLL in Current Controlled Oscillator (CCO) mode	240	–	440	MHz
$t_{W(min)}$	minimum pulse width		4	–	–	ns
t_{res}	timing resolution		2	–	–	ns

5 BLOCK DIAGRAM

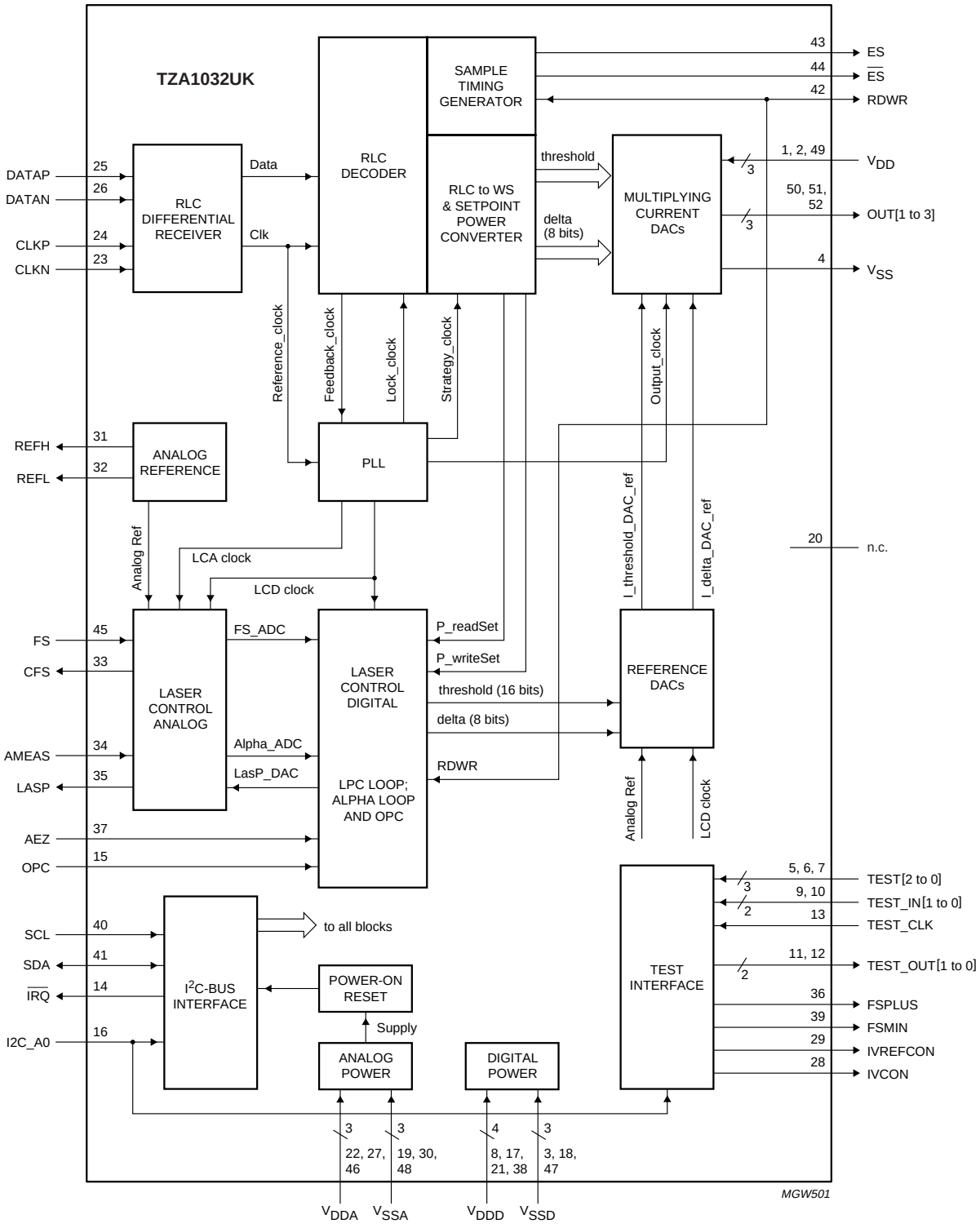


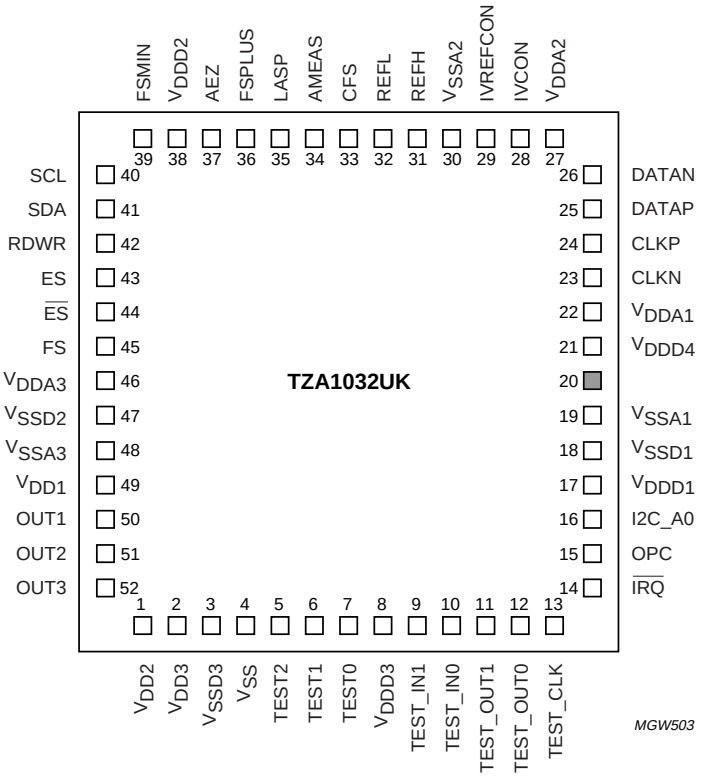
Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	TYPE	DESCRIPTION
V_{DD2}	1	P	laser driver power supply
V_{DD3}	2	P	laser driver power supply
V_{SSD3}	3	P	IC digital ground
V_{SS}	4	P	laser driver ground
V_{DDD3}	8	P	IC digital power supply
$\overline{IRQ}$	14	O	interrupt request; digital output (open drain sink). $\overline{IRQ}$ is an active LOW interrupt service request output line to the microprocessor. This line is set (made LOW) by internal laser driver events and is cleared (made HIGH) when a register in the laser driver is read via I^2C-bus.
OPC	15	I	OPC strobe; digital input with pull-down resistor. The system controller during OPC issues the OPC (strobe) signal. This signal tells the laser driver that a step in a set point value should be made during OPC mode.
I2C_A0	16	I	digital input pin with pull-down resistor whose function is to select which I^2C-bus address range applies to the IC. This allows two laser drivers to be used in parallel on one I^2C-bus. This pin is also used as test mode selection pin for test mode.
V_{DDD1}	17	P	IC digital power supply
V_{SSD1}	18	P	IC digital ground
V_{SSA1}	19	P	IC analog ground
V_{SSD4}	20	P	not connected
V_{DDD4}	21	P	IC digital power supply
V_{DDA1}	22	P	IC analog power supply
CLKN	23	I	clock pulse; analog current input. The anti-phase clock signal is used together with CLKP to allow balanced transmission.
CLKP	24	I	clock pulse; analog current input. Provides clock reference for EFMplus data plus the clock reference for the internal PLL.
DATAP	25	I	data input; analog current input. This is the input for the run length variable code (in non-return to zero form) from which the laser driver knows which laser pulses to generate.
DATAN	26	I	data input; analog current input. The anti-phase data signal (CLKN) used together with DATAN to allow balanced transmission.
V_{DDA2}	27	P	IC analog power supply
V_{SSA2}	30	P	IC analog ground
REFH	31	O	band-gap reference output (for external smoothing capacitor)
REFL	32	O	band-gap ground connection (for external smoothing capacitor)
CFS	33	O	capacitor forward sense; analog connection for external smoothing capacitor. An external capacitor of 560 pF combined with an internal resistor of 70 kΩ can be used to create a RC filter for the FS input before the ADC unit in order to prevent slew-rate effects. This capacitor is placed between this pin and REFL.

SYMBOL	PAD	TYPE	DESCRIPTION
AMEAS	34	I	alpha measure; analog current sink input. AMEAS (alpha measure) is the value of the measured disk writing quality. This is used in the alpha control loop in order to regulate the actual laser power as a function of non-laser system and medium drift.
LASP	35	O	laser power; analog current source output. Pin LASP indicates the laser power level. The read power is constant and the write power level (which is added during laser driver write mode) is alpha corrected. This signal is used in order to normalise signals with respect to laser power.
AEZ	37	I	alpha error zero; digital input with pull-down resistor. Depending on the programming of an internal mode bit one of two effects occurs when this input is asserted. alpha error zero (AEZ): the output of the alpha error adder is forced to zero. alpha set zero (ASZ): the alpha error adder positive input (i.e. the alpha set point) is forced to zero.
V_{DDD2}	38	P	IC digital power supply
SCL	40	I	digital input for I^2C-clock (the laser driver is a slave device)
SDA	41	I/O	digital bi-directional port with open-drain sink output for I^2C-bus data
RDWR	42	O	read-write; digital output line. This signal indicates whether the laser driver is in read mode (HIGH) or write mode (LOW).
ES	43	O	analog output line. This signal indicates when valid signals from the photo-detector can be expected for sampling purposes (used in CD-R applications).
$\overline{ES}$	44	O	analog output line. The ES anti-phase signal used together with ES to allow balanced transmission.
FS	45	I	forward sense; analog current sink input. This is the value of the measured laser power (e.g. measured by a photodiode which receives a set fraction of laser output directly). This is used in the laser power control loop in order to regulate the actual laser power to a given set of values as a function of laser temperature drift.
V_{DDA3}	46	P	IC analog power supply
V_{SSD2}	47	P	IC digital ground
V_{SSA3}	48	P	IC analog ground
V_{DD1}	49	P	laser driver power supply
OUT1	50	O	analog current output to the laser
OUT2	51	O	analog current output to the laser
OUT3	52	O	analog current output to the laser
Laser driver IC test pads			
TEST2	5	I	digital input bus for test mode control. Normal functional mode (normal application use) is: all pins with an internal pull-down resistor and code = 0.
TEST1	6	I	digital input bus for test mode control. Normal functional mode (normal application use) is: all pins with an internal pull-down resistor and code = 0.
TEST0	7	I	digital input bus for test mode control. Normal functional mode (normal application use) is: all pins with an internal pull-down resistor and code = 0.

SYMBOL	PAD	TYPE	DESCRIPTION
TEST_IN1	9	I	digital input bus with internal pull-down resistors for test data input. High-impedance state in functional mode.
TEST_IN0	10	I	digital input bus with internal pull-down resistors for test data input. High-impedance state in functional mode.
TEST_OUT1	11	O	digital output bus for test data output. High-impedance state in functional mode.
TEST_OUT0	12	O	digital output bus for test data output. High-impedance state in functional mode.
TEST_CLK	13	I	digital input pin with internal pull-down resistor for test data clock. High-impedance state in functional mode.
IVCON	28	O	analog current output related to the PLL loop-filter. High-impedance state in functional mode.
IVREFCON	29	O	analog current output related to the PLL loop-filter. High-impedance state in functional mode.
FSPLUS	36	O	analog voltage output from LCA FS/alpha pre-amp circuit. High-impedance state in functional mode.
FSMIN	39	O	analog voltage output from LCA FS/alpha pre-amp circuit. High-impedance state in functional mode.



Pad number 20 is not connected.

Fig.2 Bare die with solder bumps (flip-chip).

7 FUNCTIONAL DESCRIPTION

7.1 The I²C-bus interface

The TZA1032 has two possible I²C-bus addresses that can be selected via pin I2C_A0, an active HIGH digital CMOS input. This allows two TZA1032 ICs to be independently applied using the same I²C-bus (e.g. for double write applications), one with pin I2C_A0 HIGH and the other with pin I2C_A0 LOW. The TZA1032 operates as a slave only I²C-bus device.

Table 1 TZA1032 I²C-bus addresses

I2C_A0	I²C-BUS WRITE ADDRESS	I²C-BUS READ ADDRESS
0 = LOW	1101 1100 (DCH)	1101 1101 (DDH)
1 = HIGH	1101 1110 (DEH)	1101 1111 (DFH)

Each I²C-bus register has an 8-bit register address bus. The various modes in which an external controller can use the I²C-bus interface are shown in Table 2. The special RAM Write mode allows fast block transfer of data via one single I²C-bus register address.

Table 2 I²C-bus communication modes supported by TZA1032

I²C-BUS MODE	I²C-BUS INFORMATION
Write	start; TZA1032_write_address; acknowledge; register_address (n); acknowledge; data_to_register_address (n); acknowledge; stop
Incremental write	start; TZA1032_write_address; acknowledge; register_address (n); acknowledge; data_to_register_address (n); acknowledge; data_to_register_address (n + 1); acknowledge; .... ; data_to_register_address (n + r); acknowledge; stop
RAM write	start; TZA1032_write_address; acknowledge; register_address (= RAM x), acknowledge; data_to_RAM x (0), acknowledge; data_to_RAM x (1), acknowledge; .... ; data_to_RAM x (m); acknowledge; stop
Read	start; TZA1032_write_address; acknowledge; register_address (n); acknowledge; stop start; TZA1032_read_address; acknowledge; data_from_register_address (n); $\overline{\text{acknowledge}}$; stop
Successive read	start; TZA1032_write_address; acknowledge; register_address (n); acknowledge; start; TZA1032_read_address; acknowledge; data_from_register_address (n), acknowledge; data_from_register_address (n); acknowledge; .... ; data_from_register_address (n); $\overline{\text{acknowledge}}$; stop

7.2 Interrupt request

The $\overline{\text{IRQ}}$ is built as an active LOW open-drain output pin so it can be linked to the system controller together with similar signals in a wired-or approach. An IRQ register is present to select the conditions which can cause the $\overline{\text{IRQ}}$ line to be active. Possible conditions for an interrupt can be overrun or under-run of threshold or delta laser current or several other selectable conditions.

The status register allows extra signals to be monitored in non-interrupt mode (e.g. by polling). The IRQ and status registers in combination with the $\overline{\text{IRQ}}$ line allow a very efficient way of controlling TZA1032.

In addition, the IRQ_enable register allows selectable masking of most of the IRQ conditions to the $\overline{\text{IRQ}}$ line.

7.3 Soft reset and power-down

TZA1032 has a soft reset register that can reset most of the internal blocks, and is automatically synchronized with the I²C-bus SCL input.

Most of the blocks in the TZA1032 are provided with a power-down input. The IC features a special power-down register which can be programmed via I²C-bus. An active bit in the register causes a block to go into a low dissipation standby mode. This offers the user the possibility to save power when TZA1032 operates in a register mode (e.g. during read).

7.4 The Phase Locked Loop

The PLL is phase locked to the incoming RLC clock signal. A single external clock signal is sufficient for a complete task of TZA1032. The PLL unit provides all internal clocking with the exception of the I²C-bus interface that can run on its own SCL clock.

The PLL can be used in closed loop or as a stable open-loop oscillator (in read mode for example) when no input clock is present. For this purpose the PLL features a self-learning oscillator mode for non-locked operation.

Furthermore, the PLL is designed for wide range frequency locking (factor ≥2.5). The frequency multiplication factor is programmable for flexible selection of write strategy timing resolution for different standards (CD 1× to 24×, DVD 1×, 2×, 4× and DVR).

For PLL characteristics see Table 3 for the possible PLL frequencies and write strategy resolutions with respect to the incoming RLC clock. The TZA1032 features are much more flexible than shown in Table 3. The PLL frequency and write strategy resolution can be programmed according to the specific requirements of the user.

Table 3 Examples of PLL clock ratio programming

STANDARD	RLC FREQUENCY f_{rlc} (MHz)	PLL FREQUENCY f_o (MHz)	WRITE STRATEGY RESOLUTION(1)
CD × 1	4.3218	518.616	8
CD × 2	8.6436	518.616	8
CD × 4	17.2872	553.1904	8
CD × 8	34.5744	553.1904	8
CD × 12	51.8616	414.8928	8
CD × 16	69.1488	553.1904	8
CD × 24	103.7232	414.8928	4
DVD × 1	26.16	523.2	20
DVD × 2	52.32	523.2	10
DVD × 2.5	65.4	392.4	6
DVD × 4	104.64	418.56	4
DVR-1	65.625	525	8
DVR-2	93.75	562.5	6

Note

1. The write strategy resolution is defined as the number of bits per RLC clock period.

7.5 The differential receiver

A differential RLC receiver (DRX) with low voltage-swing is present to allow high data rates in combination with low electromagnetic interference. The receiver features impedance matching with typical flex foils. Furthermore, single side operation is optionally possible by connecting additional external resistors.

High-impedance input switching allows two or more TZA1032 ICs to operate in parallel. The high-impedance input switch is controlled by a single I²C-bus control register that can individually select DRX clock and/or data lines for high-impedance mode. A high-impedance input mode is also entered during $\overline{\text{Reset}}$ or power-down.

Table 4 Truth table for RLC differential receiver; note 1

CLOCK INPUT	POWER-DOWN	High_Z	High_Z_clk	$\overline{\text{Reset}}$	OUT	BIAS	INPUT SWITCH
CLKP	L	L	L	H	H	on	closed
CLKN	L	L	L	H	L	on	closed
X	H	X	X	X	H	off	open (high impedance)
X	L	H	X	X	H	on	open (high impedance)
X	L	X	H	X	H	on	open (high impedance)
X	L	X	X	H	H	on	open (high impedance)

Note

1. X = don't care; L = LOW; H = HIGH.

7.6 The RLC decoder

The RLC decoder and write strategy generator feature a look back function to enable write pre-compensation by data dependent write strategies. The write strategy for the current received run length (rlc_n) depends on the previous received run length (rlc_{n-1}). Table 5 shows that TZA1032 is capable of decoding 64 possible combinations of rlc_n and rlc_{n-1} including a read state.

The read state is entered after detecting run lengths ≥16. The decoder automatically toggles between the status write and erase in normal writing mode, and the RLC data inputs can be made edge sensitive only, or edge and level sensitive. It should be noticed that erase strategies are possible. A forced erase mode can be entered via I^2C-bus for quick disc initialisation. The RLC decoder (and the complete TZA1032) have a fixed propagation delay of 28 RLC clock periods to allow accurate data linking on disc.

Table 5 List of possible RLC decoder combinations; note 1

rlc_n	rlc_{n-1}	EFFECT	rlc_n	rlc_{n-1}	EFFECT	rlc_n	rlc_{n-1}	EFFECT	rlc_n	rlc_{n-1}	EFFECT
Read	X	0	E8	X	16	W2	E3	32	W5	E1	48
E1	X	1	E9	X	17	W2	E4	33	W5	E2	49
E2	X	2	E10	X	18	W2	E5	34	W5	E3	50
E3	W3	3	E11	X	19	W2	X	35	W5	E4	51
E3	W4	4	E12	X	20	W3	E1	36	W5	E5	52
E3	W5	5	E13	X	21	W3	E2	37	W5	X	53
E3	X	6	E14	X	22	W3	E3	38	W6	X	54
E4	W3	7	E15	X	23	W3	E4	39	W7	X	55
E4	W4	8	W1	E1	24	W3	E5	40	W8	X	56
E4	W5	9	W1	E2	25	W3	X	41	W9	X	57
E4	X	10	W1	E3	26	W4	E1	42	W10	X	58
E5	W3	11	W1	E4	27	W4	E2	43	W11	X	59
E5	W4	12	W1	E5	28	W4	E3	44	W12	X	60
E5	X	13	W1	X	29	W4	E4	45	W13	X	61
E6	X	14	W2	E1	30	W4	E5	46	W14	X	62
E7	X	15	W2	E2	31	W4	X	47	W15	X	63

Note

1. X = don't care; E = erase; W = write.

7.7 Write strategy generator

The write strategy generator makes use of pointer memory mapping to allow compact write strategy coding. Only 1600 bytes have to be transferred to TZA1032 to load the most complex write strategy including write pre-compensation. Due to the pointer memory structure common strategies can be loaded in an even more compact manner (e.g. CD strategies). Loading can be done efficiently via I^2C-bus block transfer mode.

The write strategy code includes:

- Data for selection of output power levels from 4 threshold and 8 delta values (these 8-bit values can be programmed asynchronously via I^2C-bus)
- Pulse timing information
- Modulation information.

The modulation information enables the user to switch on modulation in pre-selected parts of the write strategy on a real time basis. The modulation amplitude can be programmed asynchronously via I^2C-bus.

7.8 Laser Power Control

The Forward Sense Diode (FSD) is a reversed biased diode that receives a small percentage of the laser output light and converts it into a current. The FSD can be connected directly to the TZA1032 without additional components. The TZA1032 features a current input with programmable gain (6-bit resolution). Furthermore a 12-bit ADC is used.

Internal set point generation is present to allow read-write switching without any transient effects. A digital loop filter with programmable loop gain is used. This allows tailoring of loop bandwidth according to the requirements of the application. A unique laser power control algorithm is used. This algorithm ensures not only average power control but it really makes the laser virtual temperature and aging independent for any possible write strategy. This loop operates with or without the alpha (running OPC) loop.

The TZA1032 supports a full running optimum power control loop when required by the user. The loop is also referred to as the alpha loop. The input signal is based on disc Absorption MEASurements (AMEAS). This signal is processed in a similar way as the FS input current. A current input is provided with programmable gain (4-bit) and an 8-bit ADC is used.

Again a digital loop filter with programmable loop gain is used. This allows tailoring of loop bandwidth according to the requirements of the application. The alpha loop does not interfere with the FS laser power control loop. Therefore, both control loops can be used simultaneously. The set point is programmable via I^2C-bus or is under control of a programmable OPC stepper.

8 FUNCTIONAL DIAGRAM

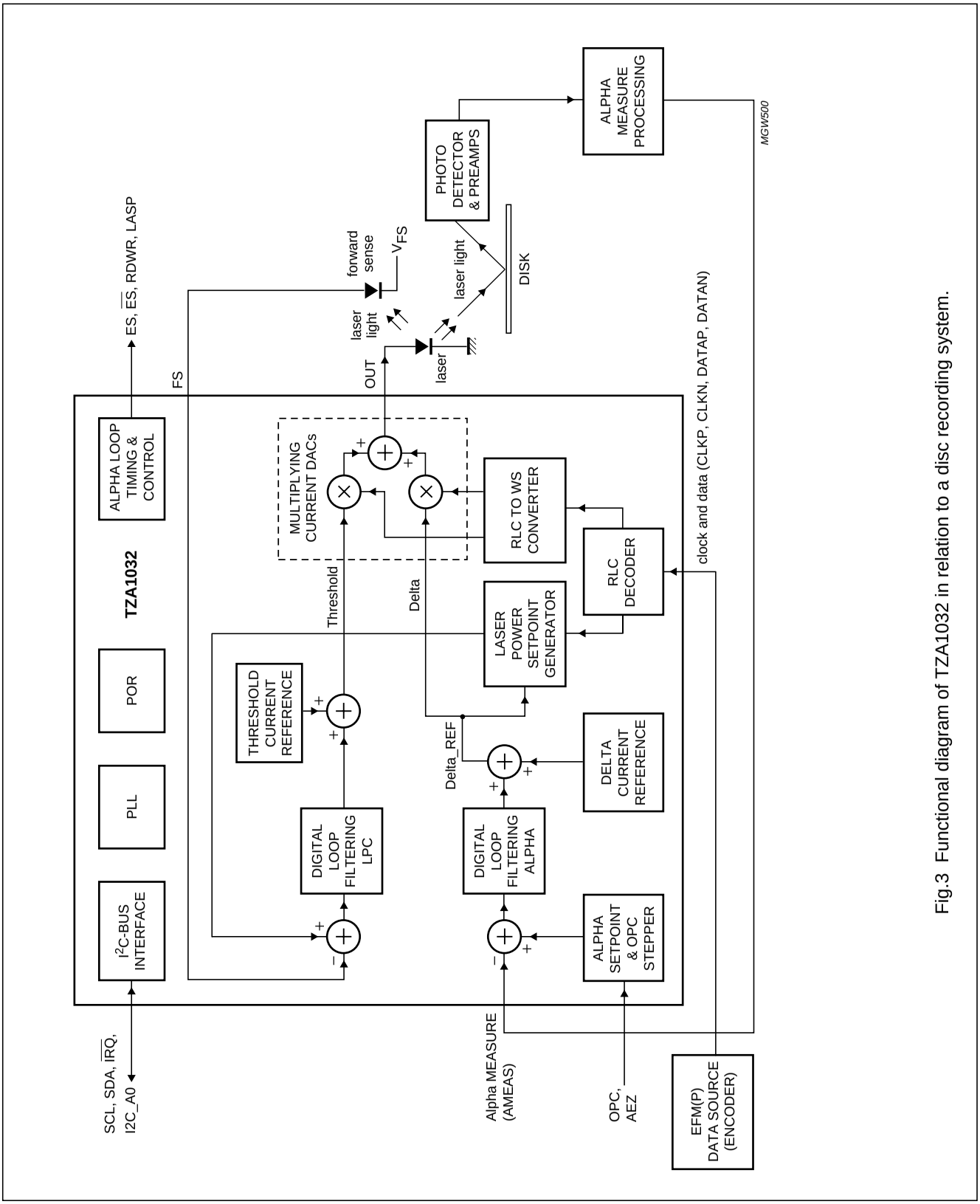


Fig.3 Functional diagram of TZA1032 in relation to a disc recording system.

9 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current driver						
$V_{DD[1\ to\ 3]}$	output supply voltage		3.0	3.3	3.6	V
$I_{OUT[1\ to\ 3]}$	output current (threshold)		1	–	200	mA
	output current (delta)		0	–	240	mA
$R_{OUT[1\ to\ 3]}$	output resistance		–	120	–	Ω
t_r, t_f	rise and fall times	depends on package and load	–	–	1 to 2	ns
PLL						
$f_{o(R)}$	PLL output frequency(1)	read mode	240	375	440	MHz
$f_{o(W)}$	PLL output frequency	write mode	320	523.2	565	MHz
$f_{i(rlc)}$	PLL input frequency		0	26.16	105	MHz
FS buffer and ADC combination						
V_{FS}	voltage at pin FS	virtual ground	1.220	1.225	1.230	V
I_{FS}	current at pin FS		0	1000	4000	µA
	DC input current	code −2048	–	0	–	µA
		code 2047; nominal gain	–	1000	–	µA
N	resolution	signed	–	12	–	bit
B_{-3dB}	analog bandwidth		3.08	4.06	5.64	kHz
Reg_FS	programmable gain register	6 bits	0	–	63	
Alpha buffer and ADC						
I_{alpha}	input current	into pin AMEAS	0	100	400	µA
V_{alpha}	input voltage	virtual ground	1.3	1.4	1.5	V
N	resolution	signed	–	8	–	bit
I_alpha	DC input current	code −128	–	0	–	µA
		code 127; nominal gain	–	100	–	µA
B_{-3dB}	analog bandwidth		520	650	850	kHz
Alpha_Reg	programmable gain register	4 bits	0	–	15	
DRX input						
$I_{DRXD(HIZ)}$	DRX data input current	high-impedance mode	0	0	100	µA
$I_{DRXC(HIZ)}$	DRX clock input current	high-impedance mode	0	0	100	µA
V_{DATA}	DRX data input voltage	low-impedance mode	–	120	–	mV
V_{CLK}	DRX clock input voltage	low-impedance mode	–	120	–	mV
I^2C-bus interface						
$R_{ON(SDA)}$	on resistance SDA line		100	150	250	Ω
$R_{ON(SCL)}$	on resistance SCL line		100	150	250	Ω

Note

1. Use low range CCO mode only.

10 APPLICATION INFORMATION

A typical application diagram of the TZA1032 is shown in Fig.4. As can be seen from this figure the CLKP, CLKN, DATAP and DATAN inputs allow differential data transfer for electromagnetic compatibility issues. Input series resistors can be connected to obtain low voltage swing when using standard 3.3 or 5 V drivers. This will further reduce electromagnetic interference.

This application diagram shows separated 3.3 V supplies to obtain maximum output performance. Only few decoupling capacitors are needed for the total application.

The forward sense loop is fully self-contained. Only a forward sense diode has to be connected, which can be biased with an external voltage.

The TZA1032 can be mounted with ‘flip-chip’ technology as a bare die on the flex foils. For this purpose the bond pads of the silicon die can be bumped with solder dots. In this configuration parasitic components (e.g. inductors) can be further reduced leading to even better performance of the TZA1032.

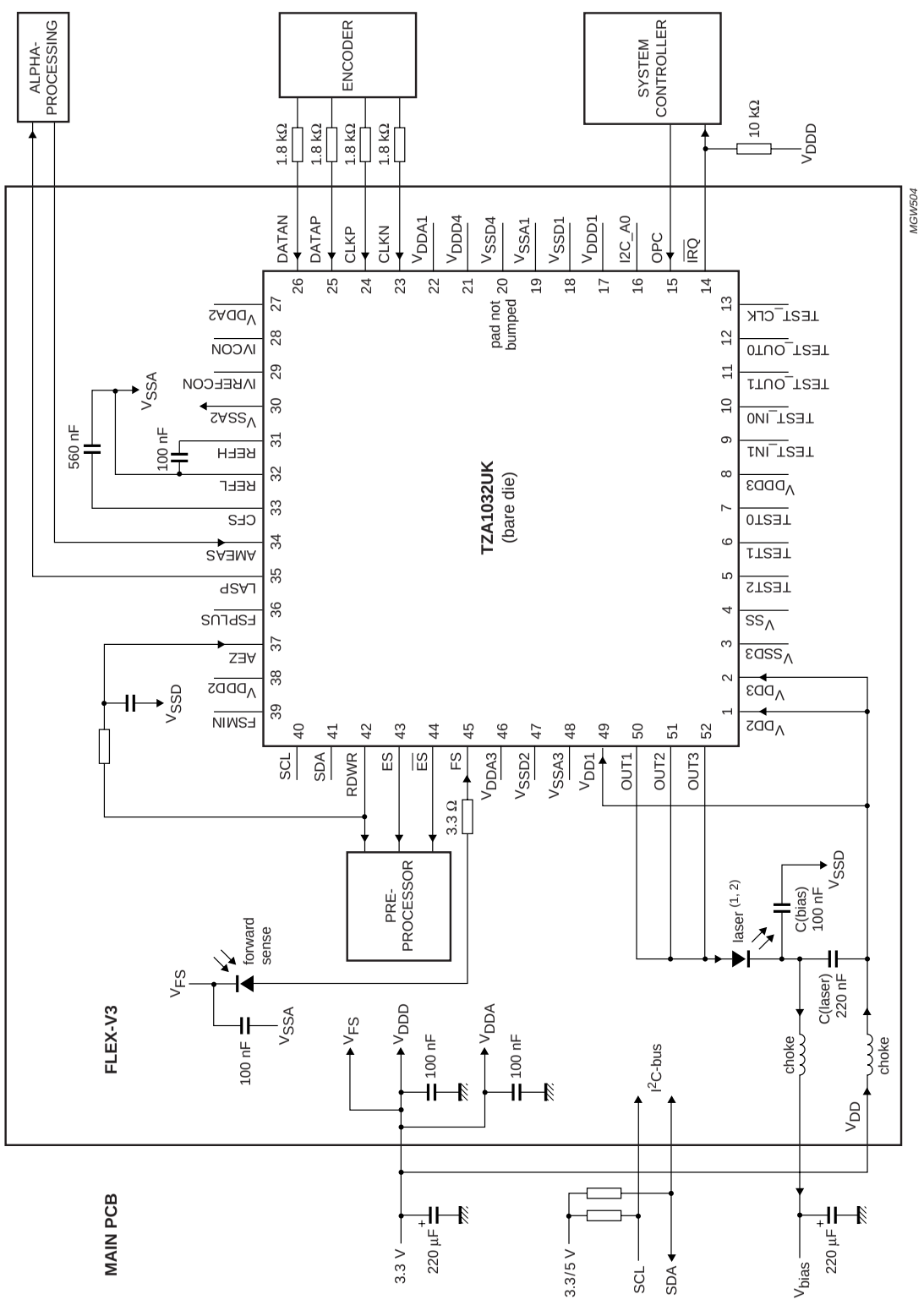


Fig.4 Typical application diagram for TZA1032UK on flex foil.

(1) The loop format by OUT1, OUT2 and OUT3, laser anode, laser cathode, C(laser) and V_{DDD} must be kept as small as possible.

(2) The ground pad of C(bias) must be placed as close to V_{SS} as possible.

11 BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES(1)	
		x	y
V_{DD2}	1	–1.469	–1.758
V_{DD3}	2	–1.2215	–1.758
V_{SSD3}	3	–0.974	–1.758
V_{SS}	4	–0.7265	–1.758
TEST2	5	–0.4775	–1.758
TEST1	6	–0.230	–1.758
TEST0	7	+0.019	–1.758
V_{DDD3}	8	+0.2665	–1.758
TEST_IN1	9	+0.5155	–1.758
TEST_IN0	10	+0.763	–1.758
TEST_OUT1	11	+1.012	–1.758
TEST_OUT0	12	+1.2595	–1.758
TEST_CLK	13	+1.5085	–1.758
$\overline{IRQ}$	14	+1.758	–1.469
OPC	15	+1.758	–1.2215
I2C_A0	16	+1.758	–0.974
V_{DDD1}	17	+1.758	–0.7265
V_{SSD1}	18	+1.758	–0.4775
V_{SSA1}	19	+1.758	–0.230
V_{SSD4}	20	+1.758	+0.019
V_{DDD4}	21	+1.758	+0.2665
V_{DDA1}	22	+1.758	+0.5155
CLKN	23	+1.758	+0.763
CLKP	24	+1.758	+1.012
DATAP	25	+1.758	+1.2595
DATAN	26	+1.758	+1.5085
V_{DDA2}	27	+1.5085	+1.758
IVCON	28	+1.2595	+1.758
IVREFCON	29	+1.012	+1.758
V_{SSA2}	30	+0.763	+1.758
REFH	31	+0.5155	+1.758
REFL	32	+0.2665	+1.758
CFS	33	+0.019	+1.758
AMEAS	34	–0.230	+1.758
LASP	35	–0.4775	+1.758
FSPLUS	36	–0.7265	+1.758
AEZ	37	–0.974	+1.758
V_{DDD2}	38	–1.2215	+1.758
FSMIN	39	–1.469	+1.758
SCL	40	–1.758	+1.5085
SDA	41	–1.758	+1.2595
RDWR	42	–1.758	+1.012
ES	43	–1.758	+0.763
$\overline{ES}$	44	–1.758	+0.5155
FS	45	–1.758	+0.2665
V_{DDA3}	46	–1.758	+0.019
V_{SSD2}	47	–1.758	–0.230
V_{SSA3}	48	–1.758	–0.4775
V_{DD1}	49	–1.758	–0.7265
OUT1	50	–1.758	–0.974
OUT2	51	–1.758	–1.2215
OUT3	52	–1.758	–1.469

Note

1. All x and y coordinates represent the position of the centre of the pad in mm with respect to the centre of the die (see Fig.5).

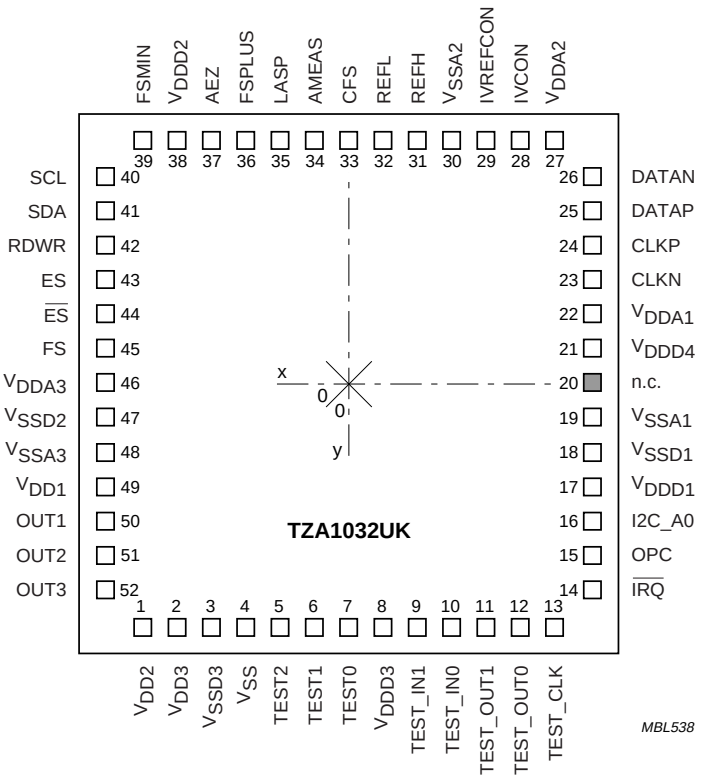


Fig.5 Bonding pad locations.

12 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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