DATA SHEET

SAA7706H
Car radio Digital Signal Processor (DSP)

Product specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

1.1 Hardware

- 5-bitstream 3rd-order sigma-delta Analog-to-Digital Converters (ADCs) with anti-aliasing broadband input filter
- 1-bitstream 1st-order sigma-delta ADC with anti-aliasing broadband input filter
- 4-bitstream Digital-to-Analog Converters (DACs) with 128-fold oversampling and noise shaping
- Integrated semi-digital filter; no external post filter required for DAC
- Dual media support: allowing separate front-seat and rear-seat signal sources and separate control
- Simultaneous radio and audio processing
- Digital FM stereo decoder
- Digital FM interference suppression
- RDS demodulation via separate ADC; with buffered output option
- Two mono Common-Mode Rejection Ratio (CMRR) input stages for voice signals from phone and navigation inputs
- Phone and navigation mixing at DAC front outputs
- Two stereo CMRR input stages (CD-walkman and CD-changer etc.)
- Analog single-ended TAPE and AUX input
- Separate AM-left and AM-right inputs in the event of use of external AM stereo decoder
- One digital input: I^{2}S-bus or LSB-justified format
- Two digital inputs: SPDIF format
- Co-DSP support via I^{2}S-bus or LSB-justified format
- Audio output short-circuit protected
- I^{2}C-bus controlled (including fast mode)
- MOST bus interfacing (details in separate manual)
- Phase-locked loop derives the internal clocks from one common fundamental crystal oscillator
- Combined AM/FM level input
- Pin compatible with SAA7705 and SAA7708
- All digital inputs are tolerant of 5 V input levels
- All analog inputs have high GSM immunity
- Low number of external components required
- –40 to +85 °C operating temperature range
- Easy applicable.

1.2 Software

- Improved FM weak signal processing
- Integrated 19 kHz MPX filter; de-emphasis and stereo detection
- Electronic adjustments: FM or AM level, FM channel separation, Dolby®(1) level
- Baseband audio processing (treble, bass, balance, fader and volume)
- Four channel 5-band parametric equalizer
- 9-bands mono audio spectrum analyzer
- Extended beep functions with tone sequencer for phone rings
- Large volume jumps e-power interpolated to prevent zipper noise
- Dual media support; allowing separate front-seat and rear-seat signal sources and separate control
- Dynamic loudness or bass boost
- Audio level monitor
- Tape equalization and Music Search System (MSS) detection for tape
- Dolby-B tape noise reduction (at 44.1 kHz only)
- Dynamics compression available in all modes
- CD de-emphasis processing
- Voice-over possibility for phone and navigation signals
- Improved AM signal processing
- Digital AM CQUAM stereo decoder (not in all rom_codes available)
- Digital AM interference suppression
- Soft audio mute
- RDS update processing: pause detection, mute and signal-quality sensor-freeze
- General purpose tone generator

(1) **Dolby** — Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

- Noise generator allows for frequency response measurements
- Boot-up ROM for fast start-up
- Signal level, noise and multipath detection for AM or FM signal quality information
- AM co-channel and adjacent channel detection (not in all rom_codes available).

2 APPLICATIONS

- High-end car radio systems.

3 GENERAL DESCRIPTION

The SAA7706H performs all the signal functions in front of the power amplifiers and behind the car radio tuner AM and FM outputs and the CD, tape and phone inputs. These functions are:

- Interference absorption
- Stereo decoding for FM and AM (stereo)
- RDS-demodulation
- FM and AM weak signal processing (soft mute, sliding stereo and high cut)
- Dolby-B tape noise reduction
- CD de-emphasis function
- Audio controls for volume, balance, fader, tone and dynamics compression.

Some functions have been implemented in hardware (FM stereo decoder, RDS-demodulator and FM Interference Absorption Circuit (IAC) and are not freely programmable.

Digital audio signals from external sources with the Philips I^2S-bus and the LSB-justified 16, 18, 20 and 24 bits format or SPDIF format are accepted.

The big advantage of this SAA7706H device is the ‘dual media support’; this enables independent front seat and rear seat audio sources and control.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	operating supply voltage	all V_{DD} pins with respect to V_{SS}	3	3.3	3.6	V
I_{DDD}	supply current of the digital part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	110	150	mA
I_{DDA}	supply current of the analog part	zero input and output signal	–	40	60	mA
P_{tot}	total power dissipation	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	540	750	mW
FM_MPX input						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)	THD < 1%; VOLFM = 00H	0.33	0.368	–	V
THD	total harmonic distortion	input signal 0.368 V (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	–70	–65	dB
			–	0.03	0.056	%
S/N	signal-to-noise ratio input stereo	input signal at 1 kHz; bandwidth = 40 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H	75	81	–	dB
CD, TAPE, AUX and AM inputs						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)	THD < 1%	0.6	0.66	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz	–	–85	–75	dB
S/N	signal-to-noise ratio	input signal at 1 kHz; bandwidth = 20 kHz; 0 dB reference = 0.55 V (RMS)	85	90	–	dB
FSDAC						
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio (measured with system one)	at 0 dB	–	–90	–85	dB
		at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio (measured with system one)	code = 0; A-weighted	–	105	–	dB
Crystal oscillator						
f_{xtal}	crystal frequency		–	11.2896	–	MHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7706H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2

6 BLOCK DIAGRAM

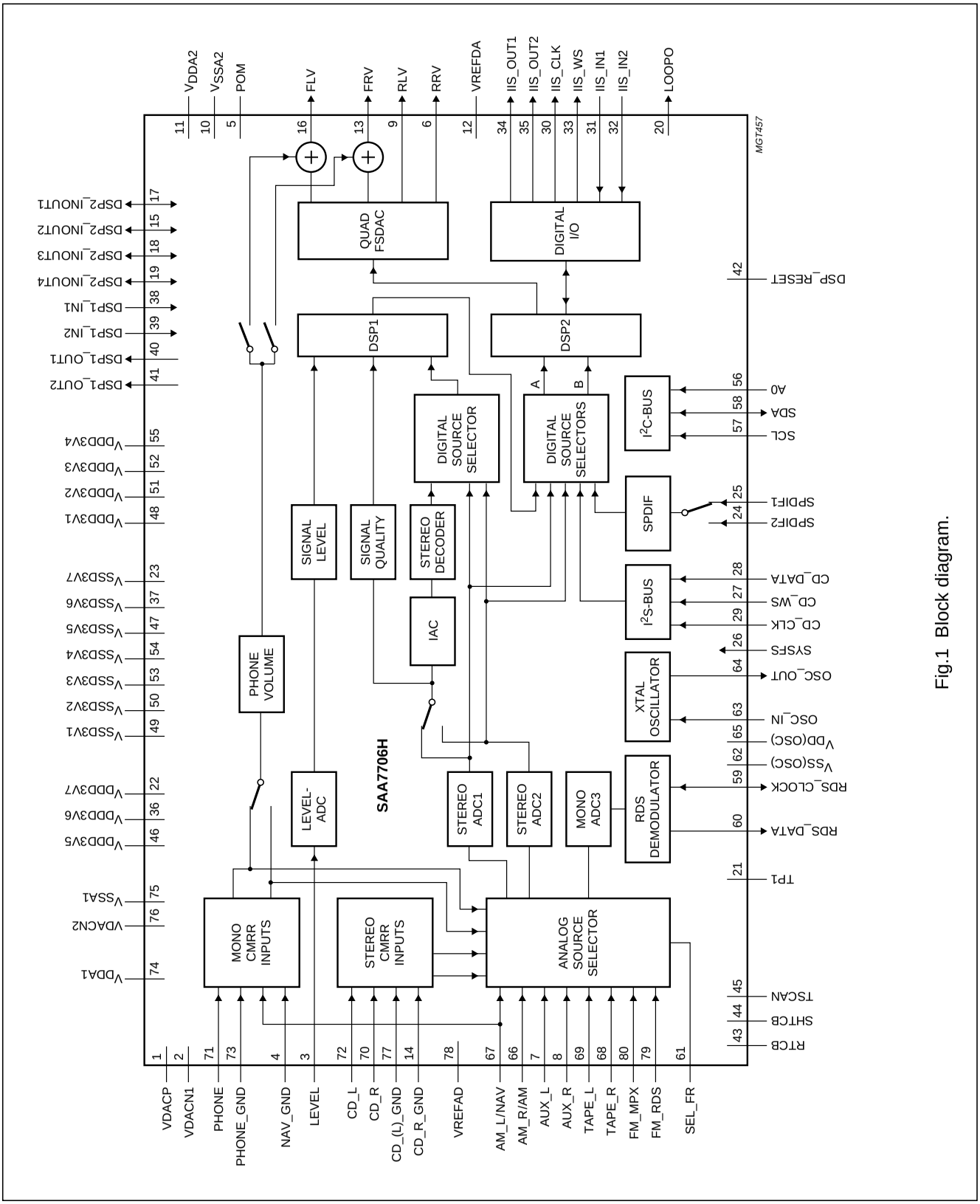


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	PIN TYPE	DESCRIPTION
VDACP	1	apio	positive reference voltage ADC1, ADC2, ADC3 and level-ADC
VDACN1	2	apio	ground reference voltage ADC1
LEVEL	3	apio gsmcap	LEVEL input pin; via this pin the level of the FM signal or level of the AM signal is fed to the DSP1; the level information is used in the DSP1 for dynamic signal processing
NAV_GND	4	apio gsmcap	common mode reference input pin of the navigation signal (pin AM_L/NAV)
POM	5	apio	power-on mute of the QFSDAC; timing is determined by an external capacitor
RRV	6	apio	rear; right audio output of the QFSDAC
AUX_L	7	apio	left channel of analog AUX input
AUX_R	8	apio	right channel of analog AUX input
RLV	9	apio	rear; left audio output of the QFSDAC
V_{SSA2}	10	vssco	ground supply analog part of the QFSDAC and SPDIF bitslicer
V_{DDA2}	11	vddco	positive supply analog part of the QFSDAC and SPDIF bitslicer
VREFDA	12	apio	voltage reference of the analog part of QFSDAC
FRV	13	apio	front; right audio output of the QFSDAC
CD_R_GND	14	apio	common-mode reference input pin for analog CD_R or TAPE_R in the event of separated ground reference pins for left and right are used
DSP2_INOUT2	15	bpts5thdt5v	flag input/output 2 of the DSP2-core (DSP2-flag) I^2C-bus configurable
FLV	16	apio	front; left audio voltage output of the QFSDAC
DSP2_INOUT1	17	bpts5thdt5v	flag input/output 1 of the DSP2-core (DSP2-flag) I^2C-bus configurable
DSP2_INOUT3	18	bpts5thdt5v	flag input/output 3 of the DSP2-core (DSP2-flag) I^2C-bus configurable
DSP2_INOUT4	19	bpts5thdt5v	flag input/output 4 of the DSP2-core (DSP2-flag) I^2C-bus configurable
LOOPO	20	bpts5tht5v	SYSCLK output ($256f_s$)
TP1	21	ipthdt5v	for test purpose only; this pin may be left open or connected to ground
V_{DDD3V7}	22	vdde	positive supply (peripheral cells only)
V_{SSD3V7}	23	vsse	ground supply (peripheral cells only)
SPDIF2	24	apio	SPDIF input 2; can be selected instead of SPDIF1 via I^2C-bus bit
SPDIF1	25	apio	SPDIF input 1; can be selected instead of SPDIF2 via I^2C-bus bit
SYSFS	26	ipthdt5v	system f_s clock input
CD_WS	27	ipthdt5v	digital CD-source word select input; I^2S-bus or LSB-justified format
CD_DATA	28	bpts10thdt5v	digital CD-source left-right data input; I^2S-bus or LSB-justified format
CD_CLK	29	ipthdt5v	digital CD-source clock input I^2S-bus or LSB-justified format
IIS_CLK	30	ots10ct5v	clock output for external I^2S-bus receiver; for example headphone or subwoofer
IIS_IN1	31	ipthdt5v	data 1 input for external I^2S-bus transmitter; e.g. audio co-processor
IIS_IN2	32	ipthdt5v	data 2 input for external I^2S-bus transmitter; e.g. audio co-processor
IIS_WS	33	ots10ct5v	word select output for external I^2S-bus receiver; for example headphone or subwoofer
IIS_OUT1	34	ots10ct5v	data 1 output for external I^2S-bus receiver or co-processor
IIS_OUT2	35	ots10ct5v	data 2 output for external I^2S-bus receiver or co-processor

SYMBOL	PIN	PIN TYPE	DESCRIPTION
V_{DDD3V6}	36	vdde	positive supply (peripheral cells only)
V_{SSD3V6}	37	vsse	ground supply (peripheral cells only)
DSP1_IN1	38	bpts10thdt5v	flag input 1 of the DSP1-core
DSP1_IN2	39	bpts10thdt5v	flag input 2 of the DSP1-core
DSP1_OUT1	40	op4mc	flag output 1 of the DSP1-core
DSP1_OUT2	41	op4mc	flag output 2 of the DSP1-core
DSP_RESET	42	iptut5v	general reset of chip (active LOW)
RTCB	43	ipthdt5v	asynchronous reset test control block; connect to ground (internal pull-down)
SHTCB	44	ipthdt5v	shift clock test control block (internal pull-down)
TSCAN	45	ipthdt5v	scan control active high (internal pull-down)
V_{DDD3V5}	46	vdde	positive supply (peripheral cells only)
V_{SSD3V5}	47	vsse	ground supply (peripheral cells only)
V_{DDD3V1}	48	vddi	positive supply (core only)
V_{SSD3V1}	49	vssis	ground supply (core only)
V_{SSD3V2}	50	vssco	ground supply (core only)
V_{DDD3V2}	51	vddco	positive supply (core only)
V_{DDD3V3}	52	vddco	positive supply (core only)
V_{SSD3V3}	53	vssco	ground supply (core only)
V_{SSD3V4}	54	vssis	ground supply (core only)
V_{DDD3V4}	55	vddi	positive supply (core only)
A0	56	ipthdt5v	slave sub-address I^2C-bus selection or serial data input test control block
SCL	57	iptht5v	serial clock input I^2C-bus
SDA	58	iic400kt5v	serial data input/output I^2C-bus
RDS_CLOCK	59	bpts10tht5v	radio data system bit clock output or RDS external clock input I^2C-bus bit controlled
RDS_DATA	60	ops10c	radio data system data output
SEL_FR	61	iptht5v	AD input selection switch to enable high ohmic FM_MPX input at fast tuner search on FM_RDS input
$V_{SS(OSC)}$	62	vssco	ground supply (crystal oscillator only)
OSC_IN	63	apio	crystal oscillator input
OSC_OUT	64	apio	crystal oscillator output
$V_{DD(OSC)}$	65	vddco	positive supply (crystal oscillator only)
AM_R/AM	66	apio gsmcap	right channel AM audio frequency or AM input in the event of mono; analog input pin
AM_L/NAV	67	apio gsmcap	left channel AM audio frequency or input of common mode navigation signal; analog input pin
TAPE_R	68	apio gsmcap	right channel of analog TAPE input
TAPE_L	69	apio gsmcap	left channel of analog TAPE input
CD_R	70	apio gsmcap	right channel of analog CD input
PHONE	71	apio gsmcap	common mode PHONE signal, analog input pin
CD_L	72	apio gsmcap	left channel of analog CD input

SYMBOL	PIN	PIN TYPE	DESCRIPTION
PHONE_GND	73	apio gsmcap	common mode reference input pin of the PHONE signal
V_{DDA1}	74	vddco	positive supply analog (ADC1, ADC2, ADC3 and level-ADC only)
V_{SSA1}	75	vssco	ground supply analog (ADC3 and level-ADC only)
VDACN2	76	apio	ground reference voltage (ADC2)
CD_(L)_GND	77	apio gsmcap	common mode reference input pin for analog CD or TAPE or in the event of separated ground reference pins used for CD_L or TAPE_L
VREFAD	78	apio	common mode reference voltage ADC1, ADC2, ADC3 and level-ADC
FM_RDS	79	apio gsmcap	FM RDS signal; analog input pin
FM_MPX	80	apio gsmcap	FM multiplex signal; analog input pin

Table 1 Brief explanation of used pin types

PIN TYPE	EXPLANATION
apio	3-state I/O analog; I/O pad cell; actually pin type vddco
apio gsmcap	3-state I/O analog; I/O pad cell; actually pin type vddco with high GSM immunity
bpts5thdt5v	43 MHz bidirectional pad; push-pull input; 3-state output; 5 ns slew rate control; TTL; hysteresis; pull-down; 5 V tolerant
bpts10tht5v	21 MHz bidirectional pad; push-pull input; 3-state output; 10 ns slew rate control; TTL; hysteresis; 5 V tolerant
bpts10thdt5v	21 MHz bidirectional pad; push-pull input; 3-state output; 10 ns slew rate control; TTL; hysteresis; pull-down; 5 V tolerant
iic400kt5v	I^2C-bus pad; 400 kHz I^2C-bus specification; TTL; 5 V tolerant
ipthtt5v	input pad buffer; TTL; hysteresis; 5 V tolerant
ipthdt5v	input pad buffer; TTL; hysteresis; pull-down; 5 V tolerant
iptut5v	input pad buffer; TTL; pull-up; 5 V tolerant
op4mc	output pad buffer; 4 mA output drive; CMOS; slew rate control; 50 MHz
ots10ct5v	output pad buffer; 3-state, 10 ns slew rate control; CMOS; 5 V tolerant
ops10c	output pad buffer; 4 mA output drive; CMOS; slew rate control; 21 MHz
vdde	V_{DD} supply peripheral only
vsse	V_{SS} supply peripheral only
vddco	V_{DD} supply to core only
vssco	V_{SS} supply to core only (vssco does not connect the substrate)
vddi	V_{DD} supply to core and peripheral
vssis	V_{SS} supply to core and peripheral; with substrate connection

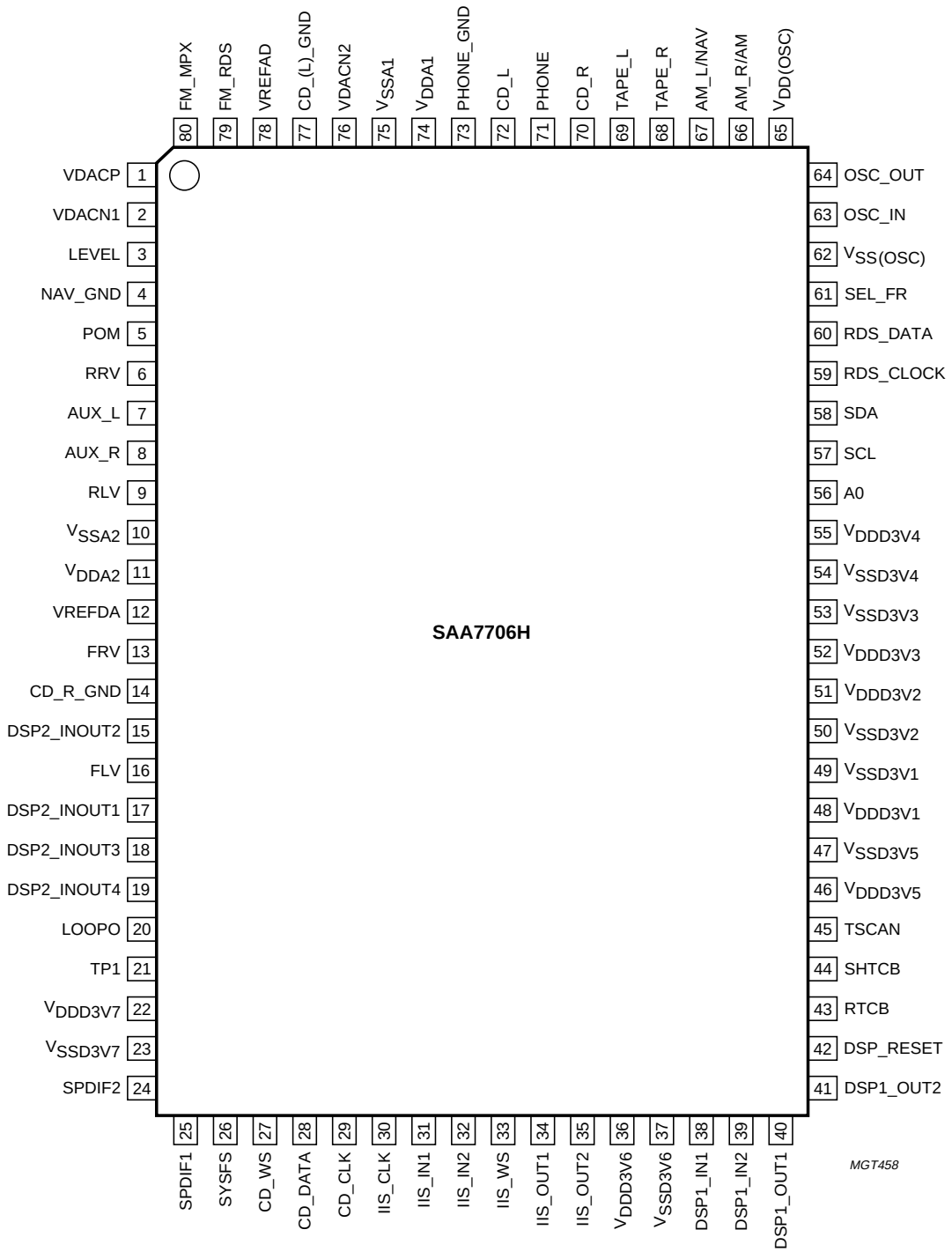


Fig.2 Pinning diagram.

8 FUNCTIONAL DESCRIPTION

8.1 Analog front-end

The analog front-end consists of two identical sigma-delta stereo ADCs (ADC1 and ADC2) with several input control blocks for handling common mode signals and acting as input selector. A mono version (ADC3) is added for handling RDS signals. Also a first-order sigma-delta ADC for tuner level information is incorporated.

The switches S1 and S2 select (see Fig.3) between the FM_MPX/FM_RDS and the CD, TAPE, AUX, AM, PHONE and NAV connection to ADC1 and ADC2. The inputs CD, TAPE, AUX, AM, PHONE and NAV can be selected with the audio input controls (AIC1/2). The ground reference (G0 and G1) can be selected to be able to handle common mode signals for CD or TAPE. The ground reference G0 is connected to an external pin and G1 is internally referenced (see Fig.4).

The PHONE and NAV inputs have their own CMRR input stage and can be redirected to ADC1/2 via the Audio Input Control (AIC). For pin compatibility with SAA7704, SAA7705 and SAA7708 the AM is combined with the NAV input. It is also possible to directly mix PHONE or NAV (controlled with MIXC) with the front FSDAC channels after volume control. The FM inputs (FM_MPX/FM_RDS) can be selected with external pin SEL_FR. The FM and RDS input sensitivity can be adjusted with VOLFM and VOLRDS via I^2C-bus.

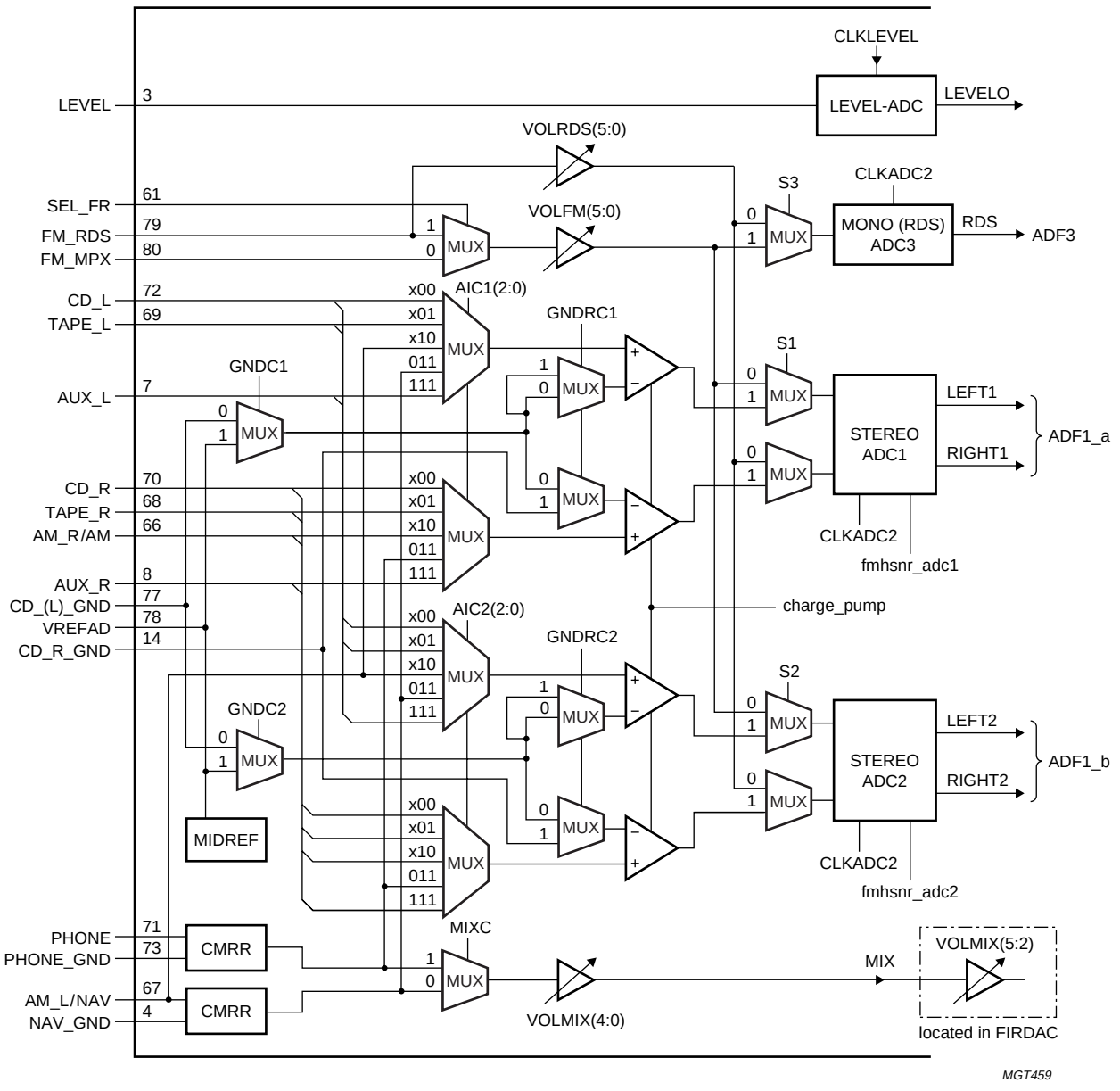


Fig.3 Analog front-end switch diagram.

8.1.1 THE REALIZATION OF COMMON MODE INPUT WITH AIC

A high common mode rejection ratio can be created by the use of the ground return pin. Pin CD_(L)_GND can be used in the case that the left and right channel have one ground return line. CD_(L)_GND and CD_R_GND can be used for separated left and right ground return lines. The ground return lines can be connected via the switch GNDC1/2 and GNDRC1/2 (see Fig.4) to the plus input of the second operational amplifier in the signal path. The signal of which a high common mode rejection ratio is required has a signal and a common signal as input. The common signal is connected to the CD_(L)_GND and/or CD_R_GND input. The actual input can be selected with audio input control AIC1/2(1:0).

In Fig.4 the CD input is selected. In this situation both signal lines going to S1/2 in front of the ADC will contain the common mode signal. The ADC itself will suppress this common mode signal with a high rejection ratio. The inputs CD_L and CD_R in this example are connected via an external resistor tap of 82 kΩ and 100 kΩ to be able to handle larger input signals. The 100 kΩ resistors are needed to provide a DC biasing of the operational amplifiers OA1 and OA2. The 1 MΩ resistor provides DC biasing of OA3 and OA4. If no external resistor tap is needed the resistors of 100 kΩ and 1 MΩ still have to provide DC biasing. Only the 82 kΩ resistor can be removed. The impedance level in combination with parasitic capacitance at input CD_L or CD_R determines for a great deal the achievable common rejection ratio.

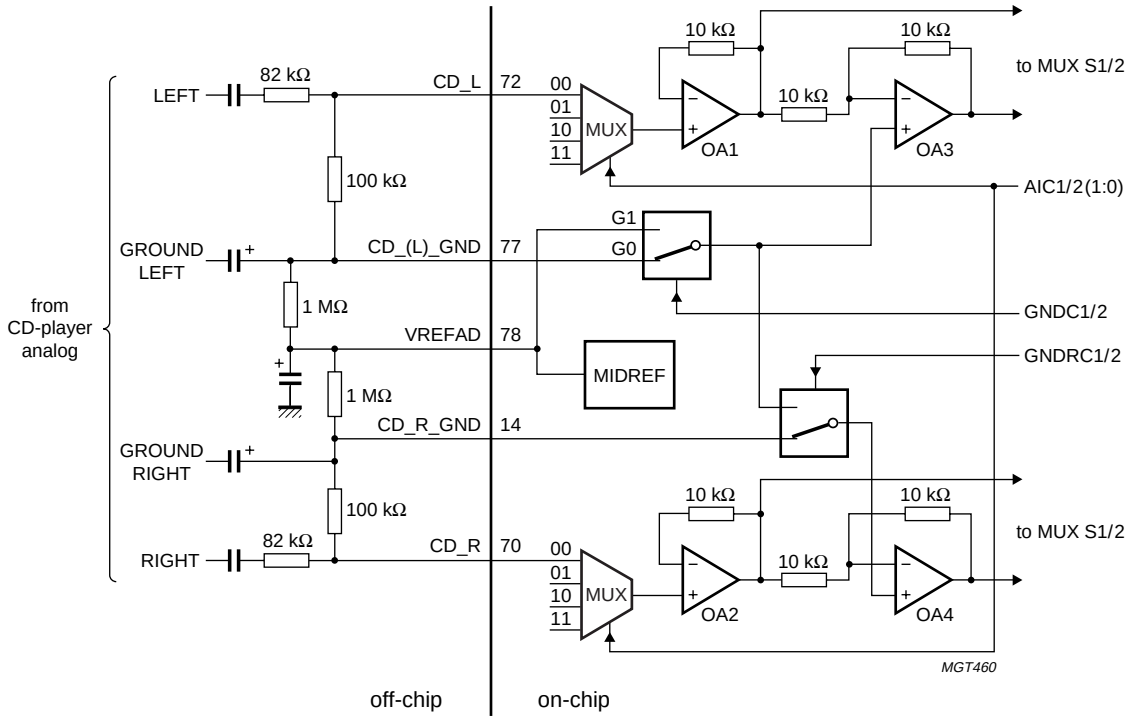


Fig.4 Example of the use of common mode analog input in combination with input resistor tap.

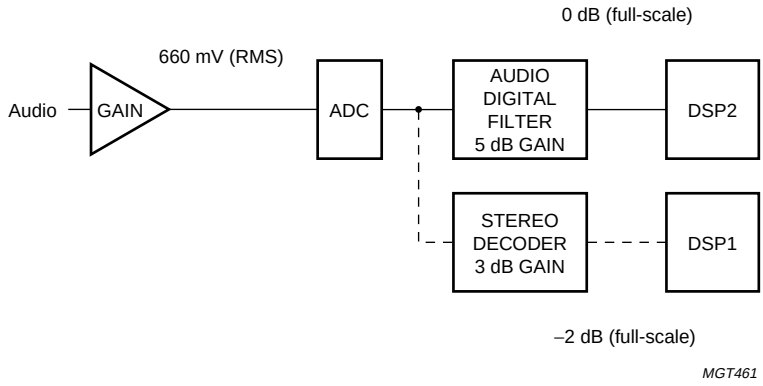


Fig.5 Audio gain through ADC and digital filter path to DSP.

8.1.2 Realization of the auxiliary input with volume control

A differential input with volume control for mixing to the front left or front right of both DAC outputs is provided. The inputs consist of a PHONE and NAV input. Both are accompanied with their ground return lines. After selection of PHONE or NAV the volume can be changed from about +18 to −22.5 dB in 27 steps and mute (MIX output). This signal can be added to the left and/or right front DAC channels.

The output signals of both input circuits can also be switched to ADC1 and/or ADC2, depending on the settings of audio input control 1 (AIC1) and audio input control 2 (AIC2), without volume control (see Fig.3).

8.1.3 Realization of the FM input control

The gain of the circuit has a maximum of 2.26 (7.08 dB). This results in an input level of 368 mV for full-scale, which means 0 dB (full-scale) at the DSP1 input via the stereo decoder (see Fig.6). The gain can be reduced in steps of 1.5 dB. When the gain is set to −3.4 dB the input level becomes 1229 mV for full-scale. This setting accounts for the 200 mV (RMS) input sensitivity at 22.5 kHz sweep and a saturation of the input at 138 kHz sweep.

RDS update: for RDS update the fast access pin SEL_FR must be made HIGH. In that case the FM_RDS signal also goes through the path that was set for FM_MPX. In this situation the signal must be obtained via the FM_RDS input and a noise sample can be retrieved. The input FM_MPX gets high-ohmic. Charging of the coupling capacitor connected to pin FM_MPX is no longer possible.

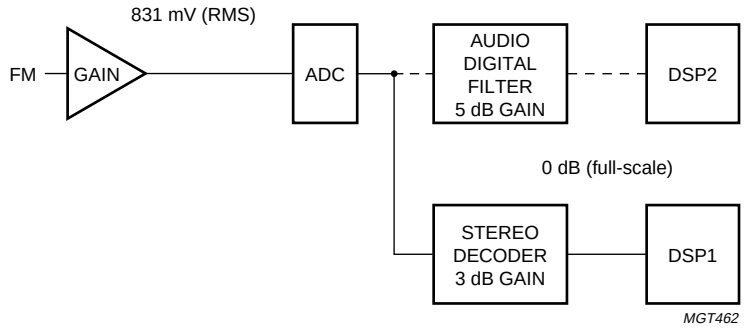


Fig.6 FM gain path through stereo decoder to DSP1.

8.1.4 PINS VDACN1, VDACN2 AND VDACP

These pins are used as negative and positive reference for the ADC1, 2, 3 and the level-ADC. They have to be directly connected to the V_{SSA1} and filtered V_{DDA1} for optimal performance (see Figs 25 and 26).

8.1.5 PIN VREFAD

Via this pin the midref voltage of the ADCs is filtered. This midref voltage is used as half supply voltage reference of the ADCs. External capacitors (connected to V_{SSA1}) prevent crosstalk between switch cap DACs of the ADCs and buffers and improves the power supply rejection ratio of all components. This pin is also used in the application as reference for the inputs TAPE and CD (see Fig.4). The voltage on pin VREFAD is determent by the voltage on pins VDACP and VDACN1 or VDACN2 and is found as:

$$V_{VREFAD} = \frac{V_{VDACP} - V_{VDACN1,2}}{2}$$

8.1.6 SUPPLY OF THE ANALOG INPUTS

The analog input circuit has separate power supply connections to allow maximum filtering. These pins are V_{SSA1} for the analog ground and V_{DDA1} for the analog power supply.

8.2 The signal audio path for input signals CD, TAPE, AUX, PHONE, NAV and AM

The left and right channels are converted and down-sampled by the ADF1_a, ADF1_b. This data stream is converted into a serial format and fed to the DSP1 and DSP2 source selectors. In Figs 7 and 8 the overall and detailed frequency response curves of the analog-to-digital audio decimation path based on a 44.1 kHz sample frequency are shown.

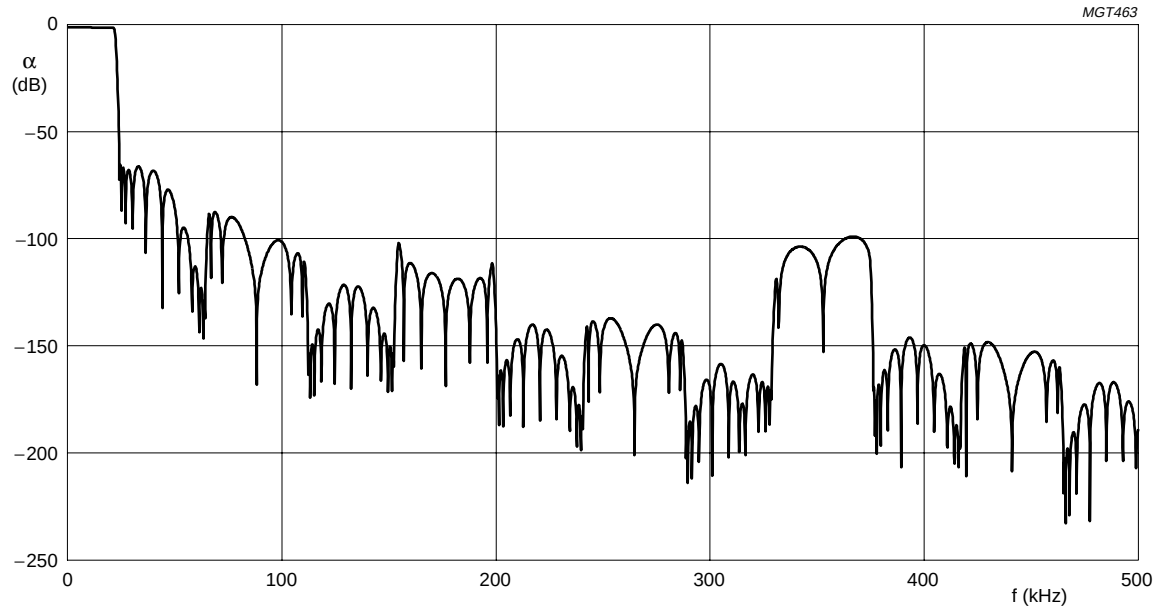


Fig.7 Overall frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

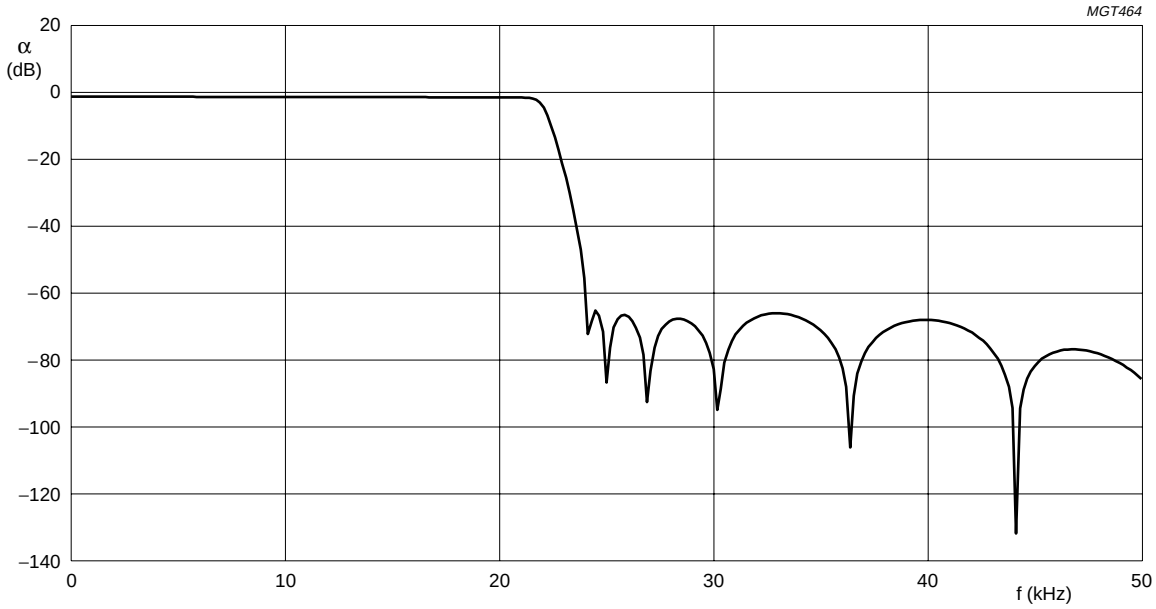


Fig.8 Detailed frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

8.3 Signal path for level information

For FM weak signal processing, for AM and FM purposes (absolute level and multipath) a level input is implemented (pin LEVEL). In the event of radio reception the clocking of the filters and the level-ADC is based on a 38 kHz sampling frequency. A DC input signal is converted by a bitstream sigma-delta ADC followed by a decimation filter.

The input signal has to be obtained from a radio part. The tuner must deliver the level information of either AM or FM to pin LEVEL.

The input signal for level must be in the range 0 to 3.3 V ($V_{VDACP} - V_{VDACN}$). The 9-bit level-ADC converts this input voltage in steps with a resolution better than at least 14 mV over the 3.3 V range.

The tolerance on the gain is less than 2%. The MSB is always logic 0 to represent a positive level. Input level span can be increased by an external resistor tap. The high input impedance of the level-ADC makes this possible.

The decimation filter reduces in the event of an 38 kHz based clocking regime the bandwidth of the incoming signal to a frequency range of 0 to 29 kHz with a resulting f_s = 76 kHz. The response curve is given in Fig.9.

The level information is sub-sampled by the DSP1 to obtain a field strength and a multipath indication. These values are stored in the coefficient or data RAM. Via the I^2C-bus they can be read and used in other microcontroller programs.

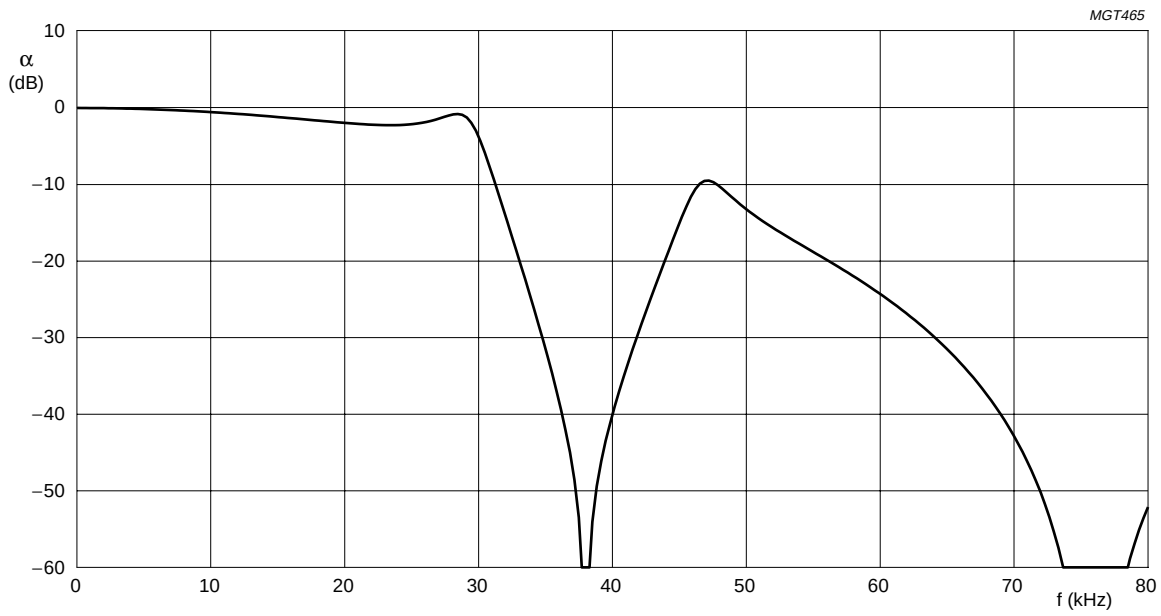


Fig.9 Frequency response level-ADC and decimal filter.

8.4 Signal path from FM_MPX input to IAC and stereo decoder

The FM_MPX signal is after selection available at one of three ADCs (ADC1, 2 and 3). The multiplex FM signal is converted to the digital domain in ADC1, 2 and 3 through a bitstream ADC. Improved performance for FM stereo can be achieved by means of adapting the noise shaper curve of the ADC to a higher bandwidth.

The first decimation takes place in two down-sample filters. These decimation filters are switched by means of the I^2C-bus bit wide_narrow in the wide or narrow band position. In the event of FM reception it must be in the narrow position.

After selection of one of the ADCs, the FM_MPX path it is followed by the IAC and the FM stereo decoder. One of the two MPX filter outputs contains the multiplex signal with a frequency range of 0 to 60 kHz. The overall low-pass frequency response of the decimation filters is shown in Fig.10.

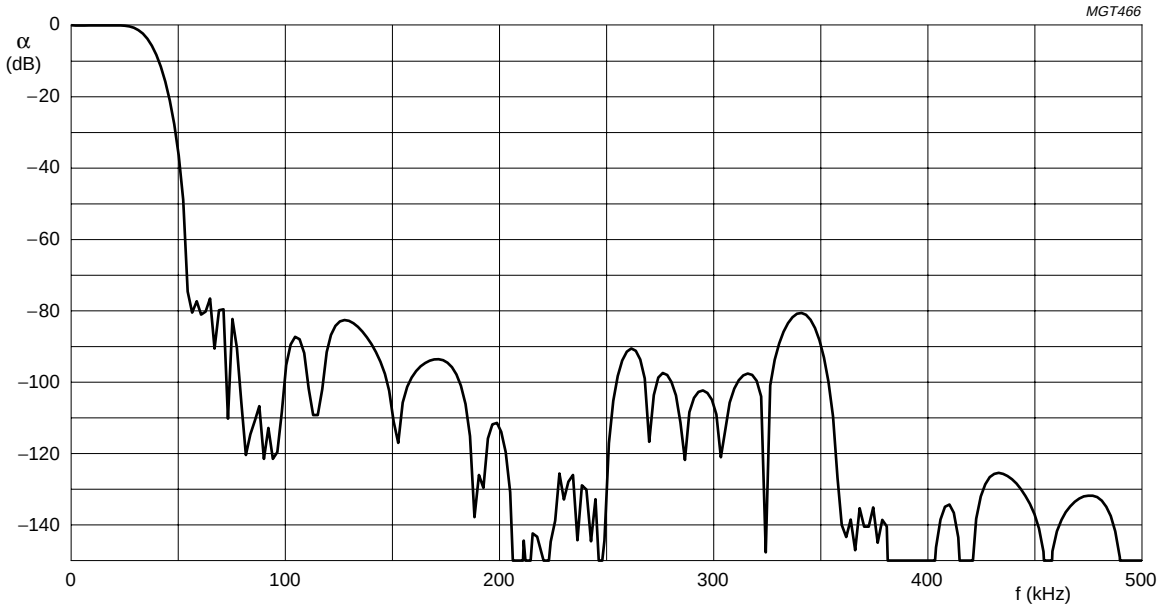


Fig.10 Overall frequency response of ADC1, ADC2 and decimation filters.

The outputs of the stereo decoder to the DSP1, which are all running on a sample frequency of 38 kHz are:

- Pilot presence indication: pilot-I. This 1-bit signal is LOW for a pilot frequency deviation <4 kHz and HIGH for a pilot frequency deviation >4 kHz and locked on a pilot tone.
- 'Left' and 'right' FM reception stereo signal: this is the 18-bit output of the stereo decoder after the matrix decoding.
- Noise level (see also Section 8.4.1): which is retrieved from the high-pass output of the MPX filter. The noise level is detected and filtered in the DSP1 and is used to optimize the FM weak signal processing.

Normally the FM_MPX input and the FM_RDS input have the same source. If the FM input contains a stereo radio channel, the pilot information is switched to the Digitally Controlled Sampling (DCS) clock generation and the DCS clock is locked to the 256 $\times$ 38 kHz of the pilot. In this case this locked frequency is also used for the RDS path ensuring the best possible performance.

Except from the above mentioned theoretical response also the non-flat frequency response of the ADC has to be compensated in the DSP1 program.

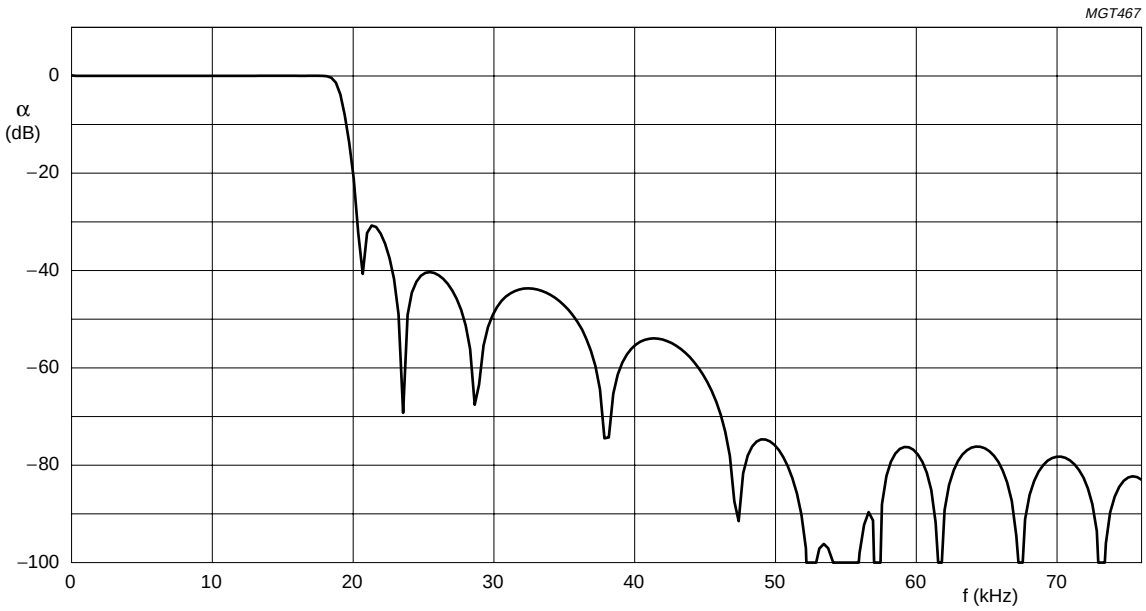
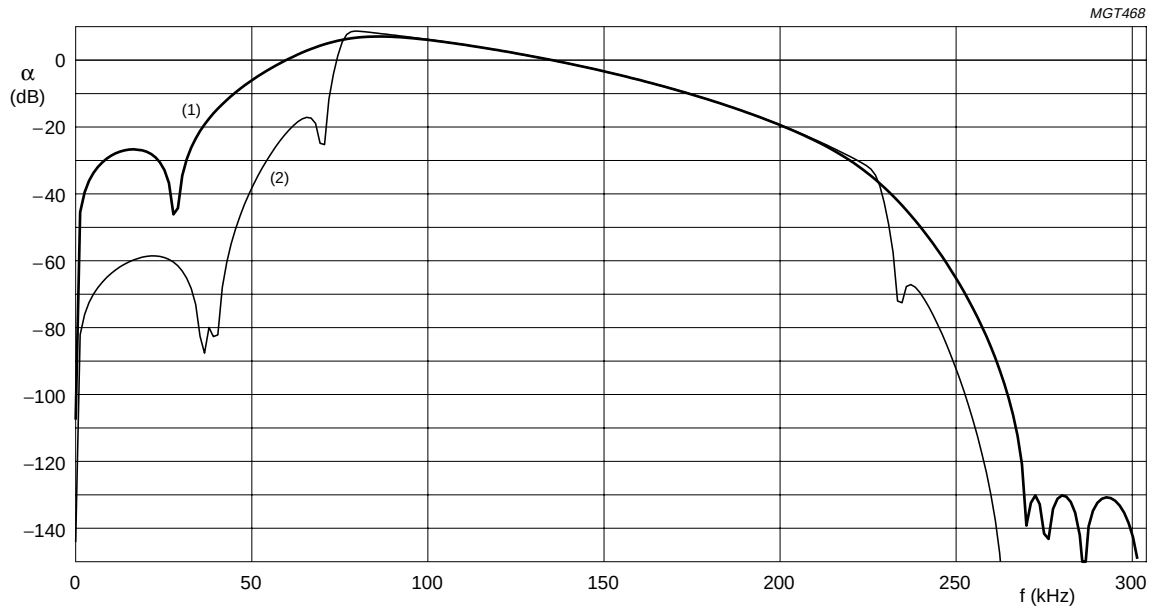


Fig.11 Transfer of MPX signal at the output of the stereo decoder.

8.4.1 NOISE LEVEL

The high-pass 1 (HP1 or narrow band noise level filter) output of the second MPX decimation filter in a band from 60 kHz to 120 kHz is detected with an envelope detector and decimated to a frequency of 38 kHz. The response time of the detector is 100 µs. Another option is the high-pass 2 (HP2 or wide band noise level filter). This output of the first MPX decimation filter is in a band from 60 to 240 kHz. It has the same properties and is also decimated to the same 38 kHz. Which of the signals is used (HP1 or HP2) is determined by the I^2C-bus bit sel_nsdec.

The resulting noise information is rectified and has a word length of 10 bits. This means that the lowest and/or the highest possible level is not used. The noise level can be detected and filtered in the DSP1-core and be used to optimize the FM weak signal processing. The transfer curves of both filters before decimation are shown in Fig.12.



(1) Noise with wide band digital filter.
(2) Noise with small band digital filter.

Fig.12 Frequency response of noise level before decimation.

8.4.2 MONO OR STEREO SWITCHING

The DCS block uses a sample rate converter to derive from the XTAL clock, via a PLL, a 512 multiple of 19 kHz (9.728 MHz). In the event of mono reception the DCS circuit generates a preset frequency of n × 19 kHz ±2 Hz. In the event of stereo reception the frequency is exactly n × 19 kHz (DCS locked to N × pilot tone). The detection of the pilot and the stereo indication is done in the DSP program.

8.4.3 THE AUTOMATIC LOCK SYSTEM

The VCO of the DCS block will be at 19 kHz ±2 Hz exact based in the event of no-pilot FM_MPX reception or in the event of only RDS reception. In the event of stereo reception the phase error is zero for a pilot tone with a frequency of exactly 19 kHz.

8.5 DCS clock

In radio mode the stereo decoder, the ADC3 and RDS demodulator, the ADC1 or ADC2 and the level decimation filters have to run synchronously to the 19 kHz pilot. Therefore a clock signal with a controlled frequency of a multiple of 19 kHz (9.728 MHz = 512 × 19 kHz) is needed.

In the SAA7706H the patented method of non-equidistant digitally controlled sampling DCS clock has been implemented. By a special dividing mechanism a frequency of 9.728 MHz from the PLL2 clock frequency of >40 MHz is generated. The dividing can be changed by means of I²C-bus bits to cope with the different input frequencies of the DCS block.

The DCS system is controlled by up or down information from the stereo decoder. In the event of mono transmissions or 44.1 kHz ADC1 or ADC2 usage the DCS clock is still controlled by the stereo decoder loop. The output keeps the DCS free running on a multiple frequency of 19 kHz ±2 Hz if the correct clock setting is applied. In

tape/cd of either 38 or 44.1 kHz and AM mode the DCS clock always has to be put in preset mode with a bit in the I²C-bus memory map definitions.

8.6 The Interference Absorption Circuit (IAC)

8.6.1 General description

The IAC detects and suppresses ignition interference. This hardware IAC is a modified, digitized and extended version of the analog circuit which is in use for many years already.

The IAC consists of an MPX mute function switched by mute pulses from ignition interference pulse detectors. The input signal of a second IAC detection circuit is the FM level signal (the output of the level-ADC). This detector performs optimally in lower antenna voltage circumstances. It is therefore complementary to the first detector.

The input signal of a first IAC detection circuit is the output signal of one of the down-sample paths coming from ADC1 or ADC2. This interference detector analyses the high-frequency contents of the MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic such as algorithm and is based on probability calculations. This detector performs optimally in higher antenna voltage circumstances. On detection of ignition interference, this logic will send appropriate pulses to the MPX mute switch.

The characteristics of both IAC detectors can be adapted to the properties of different FM front-ends by means of the predefined coefficients in the IAC control registers. The values can be changed via the I²C-bus. Both IAC detectors can be switched on or off independently of each other. Both IAC detectors can mute the MPX signal independently of each other.

A third IAC function is the dynamic IAC circuit. This block is intended to switch off the IAC completely the moment the MPX signal has a too high frequency deviation which in the event of small IF filters can result in AM modulation. This AM modulation could be interpreted by the IAC circuitry as interference caused by the car's engine.

8.7 The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7.1 Interpolation filter

The digital filter interpolates from 1 to $64f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 2 Digital interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass band ripple	$0 - 0.45f_s$	±0.03
Stop band	$>0.55f_s$	–50
Dynamic range	$0 - 0.45f_s$	116.5
Gain	DC	–3.5

8.7.2 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

8.7.3 Function of pin POM

With pin POM it is possible to switch off the reference current of the DAC. The capacitor on pin POM determines the time after which this current has a soft switch-on. So at power-on the current audio signal outputs are always muted. The loading of the external capacitor is done in two stages via two different current sources. The loading starts at a current level that is lower than the current loading after the voltage on pin POM has past a particular level. This results in an almost dB-linear behaviour. This must prevent 'plop' effects during power on or off.

8.7.4 Power-off plop suppression

To avoid plops in a power amplifier, the supply voltage of the analog part of the DAC and the rest of the chip can be fed from a separate power supply of 3.3 V. A capacitor connected to this power supply enables to provide power to the analog part at the moment the digital voltage is switching off fast. In this event the output voltage will decrease gradually allowing the power amplifier some extra time to switch off without audible plops.

8.7.5 Pin VREFDA for internal reference

With two internal resistors half the supply voltage V_{DDA2} is obtained and used as an internal reference. This reference voltage is used as DC voltage for the output operational amplifiers and as reference for the DAC.

In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground, preferably close to the analog pin V_{SSA2}.

8.7.6 Supply of the filter stream DAC

The entire analog circuitry of the DACs and the operational amplifiers are supplied by 2 supply pins: V_{DDA2} and V_{SSA2}. V_{DDA2} must have sufficient decoupling to prevent total harmonic distortion degradation and to ensure a good power supply rejection ratio. The digital part of the DAC is fully supplied from the chip core supply.

8.8 Clock circuit and oscillator

The chip has an on-chip crystal clock oscillator. The block diagram of this Pierce oscillator is shown in Fig.13. The active element needed to compensate for the loss resistance of the crystal is the block G_m. This block is placed between the external pins OSC_IN and OSC_OUT. The gain of the oscillator is internally controlled by the AGC block. A sine wave with a peak-to-peak voltage close to the oscillator power supply voltage is generated. The AGC block prevents clipping of the sine wave and therefore the higher harmonics are as low as possible. At the same time the voltage of the sine wave is as high as possible which reduces the jitter going from sine wave to the clock signal.

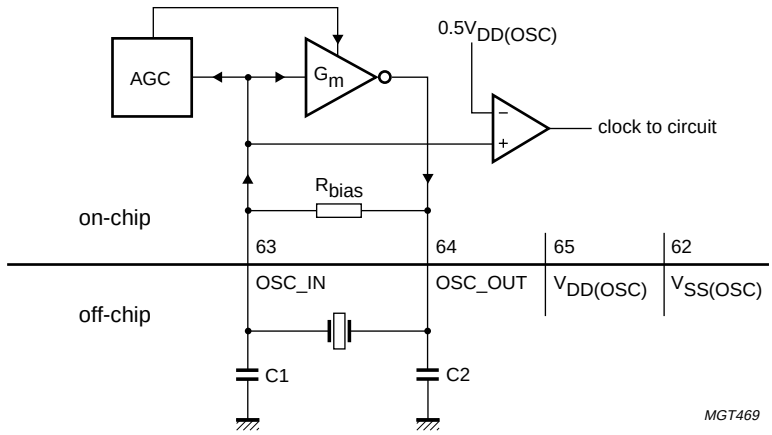


Fig.13 Block diagram oscillator circuit.

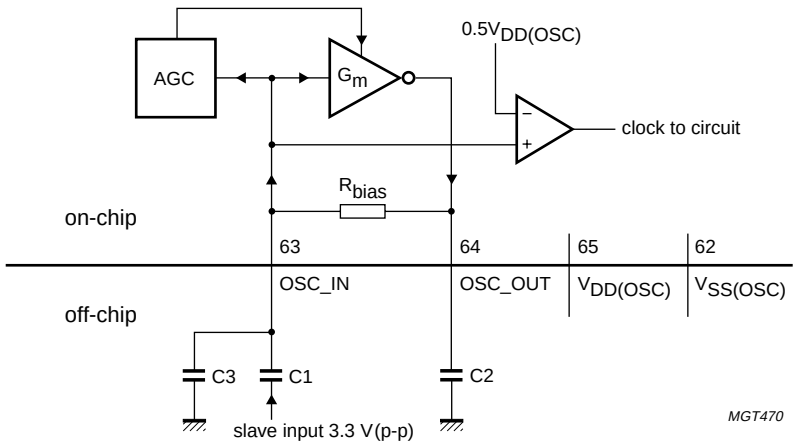


Fig.14 Block diagram of the oscillator in slave mode.

8.8.1 Supply of the crystal oscillator

The power supply connections of the oscillator are separated from the other supply lines. This is done to minimize the feedback from the ground bounce of the chip to the oscillator circuit. Pin $V_{SS(OSC)}$ is used as ground supply and pin $V_{DD(OSC)}$ as positive supply. A series resistor plus capacitance is required for proper operating on pin $V_{DD(OSC)}$, see Figs 25 and 26. See also important remark in Section 8.10.

8.9 The phase-locked loop circuit to generate the DSPs and other clocks

There are several reasons why a PLL circuit is used to generate the clock for the DSPs:

- The PLL makes it possible to switch in the rare cases that tuning on a multiple of the DSP clock frequency occurs to a slightly higher frequency for the clock of the DSP. In this way an undisturbed reception with respect to the DSP clock frequency is possible.
- Crystals for the crystal oscillator in the range of twice the required DSP clock frequency, so approximately 100 MHz, are always third overtone crystals and must also be manufactured on customer demand. This makes these crystals expensive. The PLL1 enables the use of a crystal running in the fundamental mode and also a general available crystal can be chosen. For this circuit a 256×44.1 kHz = 11.2896 MHz crystal is chosen. This type of crystal is widely used.
- Although a multiple of the frequency of the used crystal of 11.2896 MHz falls within the FM reception band, this will not disturb the reception because the relatively low frequency crystal is driven in a controlled way and the sine wave of the crystal has in the FM reception band only very minor harmonics.

8.10 Supply of the digital part (V_{DDD3V1} to V_{DDD3V4})

The supply voltage on pins V_{DDD3V1} to V_{DDD3V4} must be for at least 10 ms earlier active than the supply voltage applied to pin $V_{DD(OSC)}$.

8.11 CL_GEN, audio clock recovery block

When an external I^2S-bus or SPDIF source is connected, the FSDAC circuitry needs an $256f_s$ related clock. This clock is recovered from either the incoming WS of the digital serial input or the WS derived from the SPDIF1/SPDIF2 input. There is also a possibility to provide the chip with an external clock, in that case it must be a $256f_s$ clock with a fixed phase relation to the source.

8.12 External control pins

8.12.1 DSP1

For external control two input pins have been implemented. The status of these pins can be changed by applying a logic level. The status is saved in the DSP1 status register. The function of each pin depends on the DSP1 program.

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.12.2 DSP2

For external control four configurable I/O pins have been implemented. Via the I²C-bus these four pins can be independently configured as input or output. The status of these pins can be changed by applying a logic level (input mode). The status is saved in the DSP2 status register. The function of each pin depends on the I²C-bus setting and DSP2 program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.13 I²C-bus control (pins SCL and SDA)

General information about the I²C-bus can be found in *“The I²C-bus and how to use it”*. This document can be ordered using the code 9398 393 40011. For the external control of the SAA7706H device a fast I²C-bus is implemented. This is a 400 kHz bus which is downward-compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multipath etc.)
- Instructions controlling the data flow; such as source selection, IAC control and clock speed.

The detailed description of the I²C-bus and the description of the different bits in the memory map is given in Chapter 9.

8.14 Digital serial inputs/outputs and SPDIF inputs

8.14.1 General description digital serial audio inputs/outputs

For communication with external digital sources a digital serial bus is implemented. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7706H acts as a slave, so the external source is master and supplies the clock.

The digital serial input is capable of handling multiple input formats. The input is capable of handling Philips I^2S-bus and LSB-justified formats of 16, 18, 20 and 24 bits word sizes. The sampling frequency can be either 44.1 or 48 kHz. See Fig.15 for the general waveform formats of all possible formats.

The number of bit clock (BCK) pulses may vary in the application. When the applied word length is smaller than 24 bits (internal resolution of DSP2), the LSB bits will get internally a zero value; when the applied word length exceeds 24 bits then the LSBs are skipped.

It should be noted that:

- Two digital sources can not be used at the same time
- Maximum number of bit clocks per word select (WS) is limited to 64
- The word select (WS) must have a duty cycle of 50%.

8.14.2 General description SPDIF inputs (SPDIF1 and SPDIF2)

For communication with external digital sources also an SPDIF input can be used. The two SPDIF input pins can be connected via an analog multiplexer to the SPDIF receiver. It is a receiver without an analog PLL that samples the incoming SPDIF with a high frequency. In this way the data is recovered synchronously on the applied system clock.

From the SPDIF signal a three wire serial bus (e.g. I^2S-bus) is made, consisting of a word select, data and bit clock line. The sample frequency f_s depends solely on the SPDIF signal input accuracy and both 44.1 and 48 kHz are supported.

This chip does not handle the user data bits, channel status bits and validity bits of the SPDIF stream, but only the audio is given at its outputs. Some rom_codes do take care of the pre-emphasis bit of the SPDIF stream.

The bits in the audio space are always decoded regardless of any status bits e.g. ‘copy protected’, ‘professional mode’ or ‘data mode’. The DAC is not muted in the event of a non-linear PCM audio, however the bit is observable via the I^2C-bus. A few other channel status bits are available. There are 5 control signals available from the SPDIF input stage. These are connected to flags of DSP2. For more details see separate manual.

These 5 control signals are:

- Signals to indicate the sample frequency of the SPDIF signal: 44.1 and 48 kHz (32 kHz is not supported)
- A lock signal indicating if the SPDIF input is in lock
- The pre-emphasis bit of the SPDIF audio stream
- The pcm_audio/non-pcm_audio bit indicating if an audio or data stream is detected. The FSDAC output will not be muted in the event of a non-audio PCM stream. This status bit can be read via the I^2C-bus, the microcontroller can decide to mute the DAC (via pin POM).

The design fulfils the digital audio interface specification *“IEC 60958-1 Ed2, part 1, general part IEC 60958-3 Ed2, part 3, consumer applications”*.

It should be noted that:

- The SPDIF input may only be used in the ‘consumer mode’ specified in the digital audio interface specification
- Only one of the two SPDIF sources can be used (selected) at the same time
- The FSDAC will not (automatically) be muted in the event of a non-audio stream
- Two digital sources can not be used at the same time
- Supported sample frequencies are 44.1 and 48 kHz.

8.14.3 DIGITAL DATA STREAM FORMATS

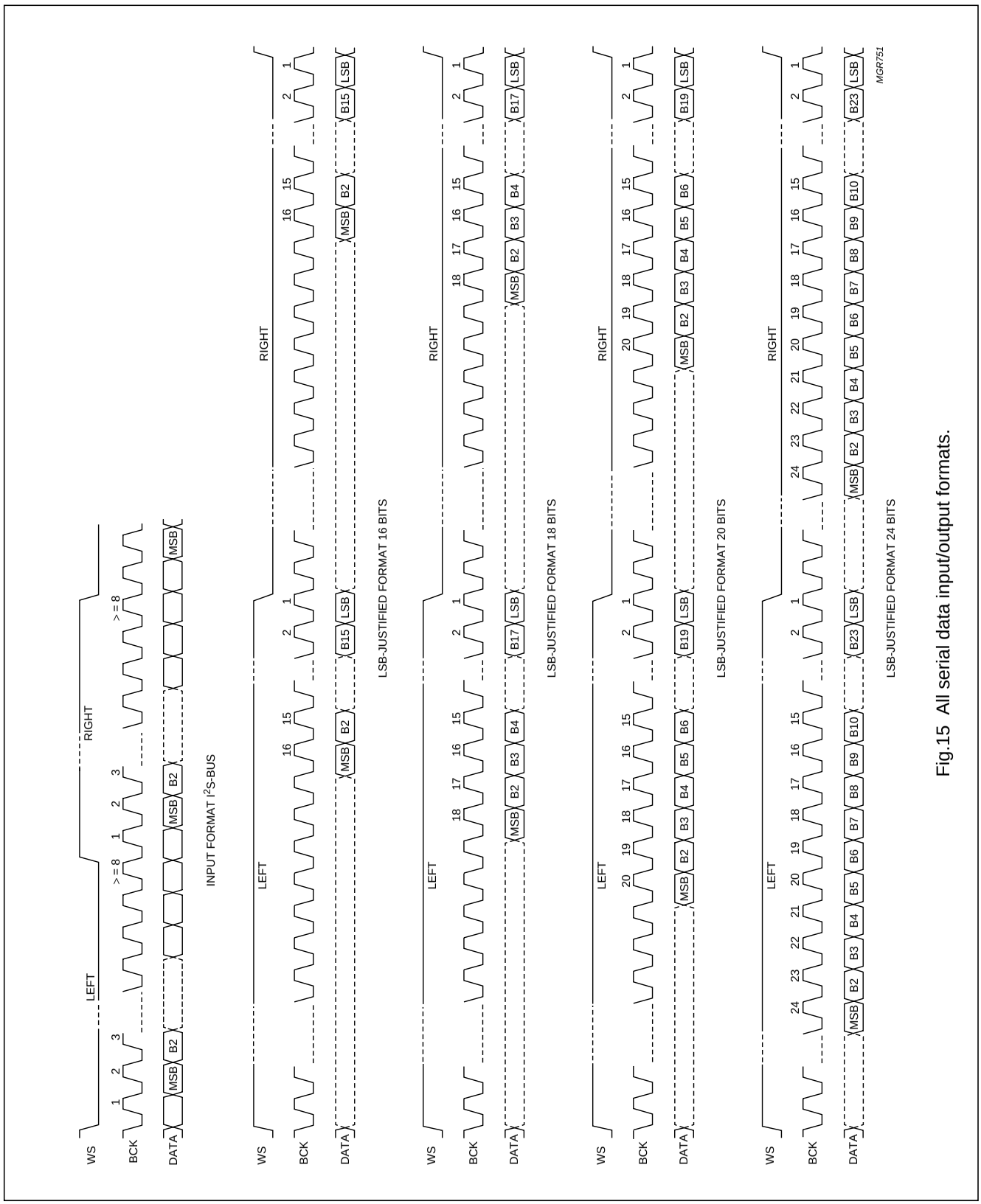


Fig.15 All serial data input/output formats.

8.15 RDS demodulator (pins RDS_CLOCK and RDS_DATA)

The RDS demodulator recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting. The (buffered) data is provided as output for further processing by a suitable decoder. The operational functions of the decoder are in accordance with the EBU specification *"EN 50067"*.

The RDS demodulator has three different functions:

- Clock and data recovery from the MPX signal
- Buffering of 16 bits, if selected
- Interfacing with the microcontroller.

8.15.1 CLOCK AND DATA RECOVERY

The RDS-chain has a separate input. This enables RDS updates during tape play and also the use of a second receiver for monitoring the RDS information of signals from an other transmitter (double tuner concept). It can as such be done without interruption of the audio program. The MPX signal from the main tuner of the car radio can be connected to this RDS input via the built-in source selector. The input selection is controlled by an I^2C-bus bit.

The RDS chain contains a sigma-delta ADC (ADC3), followed by two decimation filters. The first filter passes the multiplex band including the signals around 57 kHz and reduces the sigma-delta noise. The second filter reduces the RDS bandwidth around 57 kHz. The overall filter curve is shown in Fig.16 and a more detailed curve of the RDS 57 kHz band in Fig.17.

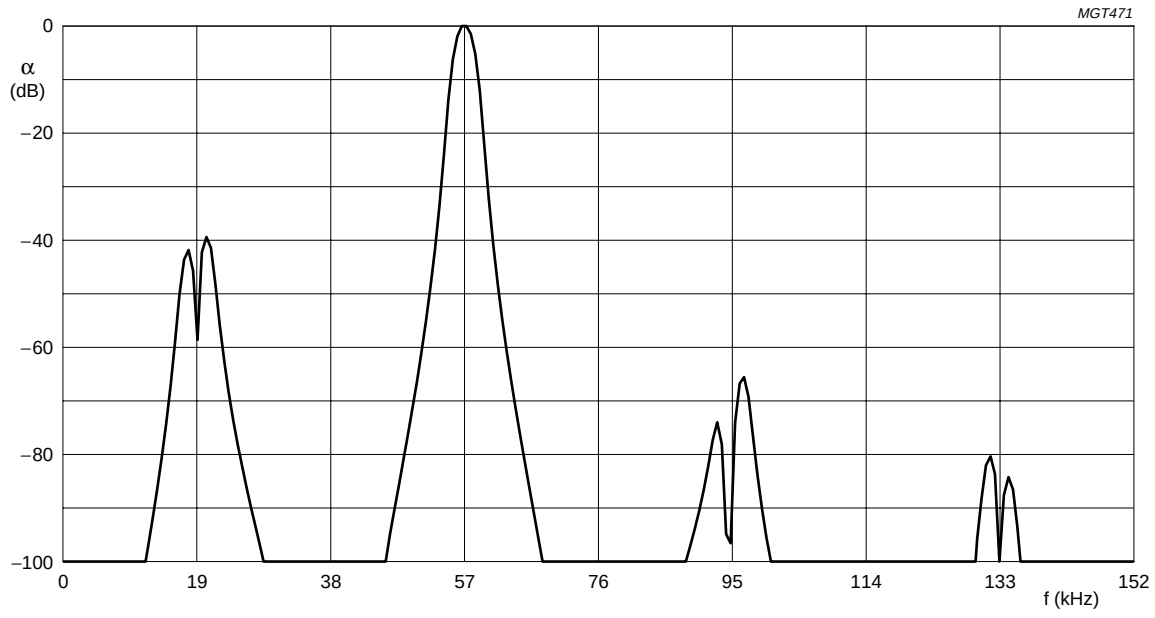


Fig.16 Overall frequency response curve decimation filters.

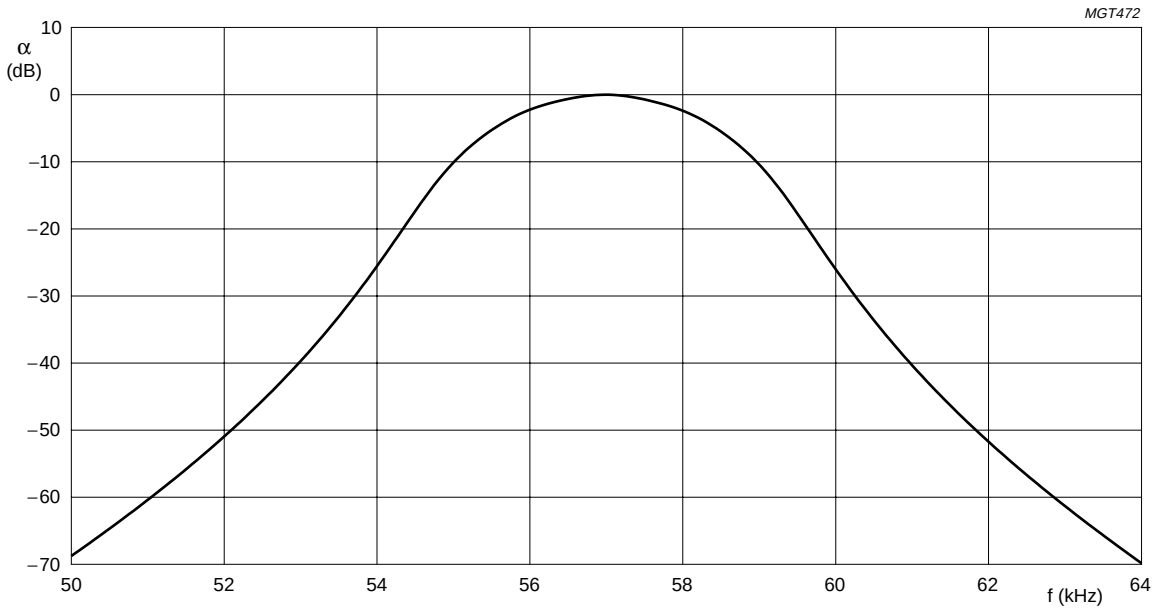


Fig.17 Detailed frequency response curve RDS channel.

The quadrature mixer converts the RDS band to the frequency spectrum around 0 Hz and contains the appropriate Q/I signal filters. The final decoder with CORDIC recovers the clock and data signals. These signals are output on pins RDS_CLOCK and RDS_DATA. In the event of FM-stereo reception the clock of the total chip is locked to the stereo pilot (19 kHz multiple). In the event of FM-mono the DCS loop keeps the DCS clock around the same 19 kHz multiple. In all other cases like AM reception or tape, the DCS circuit has to be set in a preset position by means of an I^2C-bus bit. Under these conditions the RDS system is always clocked by the DCS clock in a 38 kHz (4×9.5 kHz) based sequence.

8.15.2 Timing of clock and data signals

The timing of the clock and data output is derived from the incoming data signal. Under stable conditions the data will remain valid for 400 μs after the clock transition. The timing of the data change is 100 μs before a positive clock change. This timing is suited for positive as well as negative triggered interrupts on a microcontroller. The RDS timing is shown in Fig.18. During poor reception it is possible that faults in phase occur, then the duty cycle of the clock and data signals will vary from minimum 0.5 times to a maximum of 1.5 times the standard clock periods. Normally, faults in phase do not occur on a cyclic basis.

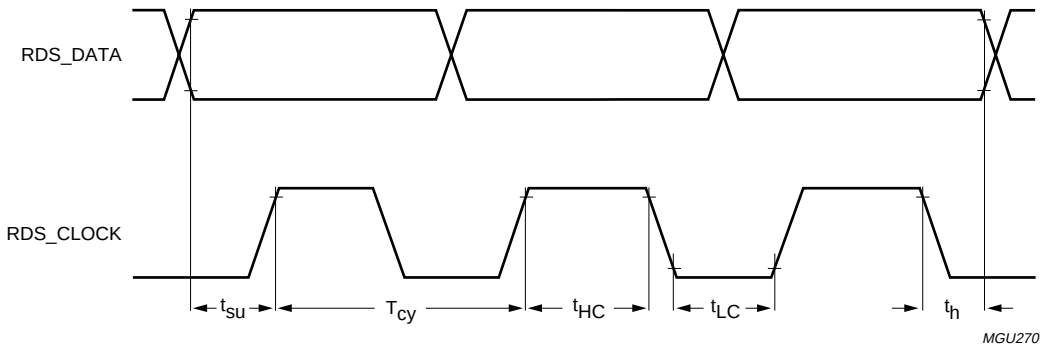


Fig.18 RDS timing in the direct output mode.

8.15.3 Buffering of RDS data

The repetition of the RDS data is around the 1187 Hz. This results in an interrupt on the microcontroller for every 842 μs. In a second mode, the RDS interface has a double 16-bit buffer.

8.15.4 Buffer interface

The RDS interface buffers 16 data bits. Every time 16 bits are received, the data line is pulled down and the buffer is overwritten. The microcontroller has to monitor the data line in at most every 13.5 ms. This mode can be selected via an I^2C-bus.

In Fig.19 the interface signals from the RDS decoder and the microcontroller in buffer mode are shown. When the buffer is filled with 16 bits the data line is pulled down. The data line will remain LOW until reading of the buffer is started by pulling down the clock line. The first bit is clocked out. After 16 clock pulses the reading of the buffer is ready and the data line is set HIGH until the buffer is filled again. The microcontroller stops communication by pulling the line HIGH. The data is written out just after the clock HIGH-to-LOW transition. The data is valid when the clock is HIGH. When a new 16-bit buffer is filled before the other buffer is read, that buffer will be overwritten and the old data is lost.

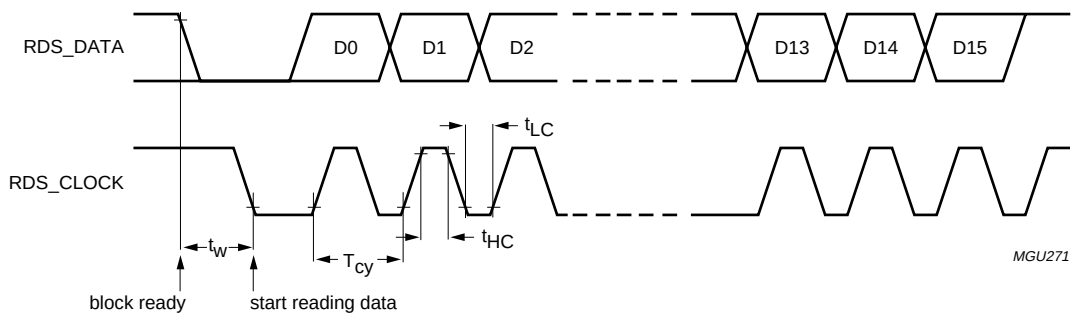


Fig.19 Interface signals RDS decoder and microcontroller (buffer mode).

8.16 DSP reset

Pin DSP_RESET is active LOW and requires an external pull-up resistor. Between this pin and the V_{SSD} ground a capacitor should be connected to allow a proper switch-on of the supply voltage. The capacitor value is such that the chip is in reset as long as the power supply is not stabilized. A more or less fixed relationship between the DSP_RESET (pin) and the POM (pin) time constant is mandatory.

The voltage on pin POM determines the current flowing in the DACs. At 0 V on pin POM the DAC currents are zero and so are the DAC output voltages.

At the V_{DDA2} voltage the DAC currents are at their nominal (maximal) value. Long before the DAC outputs get to their nominal output voltages, the DSP must be in working mode to reset the output register: therefore the DSP time constant must be shorter than the POM time constant. For recommended capacitors see Figs 25 and 26.

The reset has the following function:

- All I^2C-bus bits are set to their default value
- The DSP status registers (DSP1 and DSP2) are reset
- The program counter of both DSPs are set to address 0000H
- The two output flags of DSP1 (DSP1_OUT1 and DSP1_OUT2) are reset to logic 0. All the configurable flags of DSP2 are reset to logic 0, however the four flags available at the output of the chip are default configured as input flags (DSP2_INOUT1, DSP2_INOUT2, DSP2_INOUT3 and DSP2_INOUT4).

When the level on pin DSP_RESET is at HIGH, the DSP program (DSP1 and DSP2) starts to run.

8.17 Test mode connections (pins TSCAN, RTCB and SHTCB)

Pins TSCAN, RTCB and SHTCB are used to put the chip in test mode and to test the internal connections. Each pin has an internal pull-down resistor to ground. In the application these pins can be left open or connected to ground.

9 I²C-BUS FORMAT

For more general information on the I²C-bus protocol, see the Philips I²C-bus specification.

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

9.2 Slave address (pin A0)

The SAA7706H acts as slave receiver or a slave transmitter. Therefore the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The SAA7706H slave address is shown in Table 3.

Table 3 Slave address

MSB							LSB
0	0	1	1	1	0	A0	R/$\overline{W}$

The sub-address bit A0 corresponds to the hardware address pin A0 which allows the device to have 2 different addresses. The A0 input is also used in test mode as a serial input of the test control block.

9.3 Write cycles

The I²C-bus configuration for a write cycle is shown in Fig.20. The write cycle is used to write the bytes to both DSP1 and DSP2 for manipulating the data and coefficients. Depending on which DSP is accessed the data protocol exists out of 2, 3 or 4 bytes. More details can be found in the I²C-bus memory map (see Table 5).

The data length is 2, 3 or 4 bytes depending on the accessed memory. If the Y-memory of DSP1 is addressed the data length is 2 bytes, in the event of the X-memory of DSP1 or X/Y-memory of DSP2 the length is 3 bytes. The slave receiver detects the address and adjusts the number of bytes accordingly. The data length of 4 bytes is not used in the SAA7706H.

9.4 Read cycles

The I²C-bus configuration for a READ cycle is shown in Fig.21. The read cycle is used to read the data values from XRAM or YRAM of both DSPs. The master starts with a START condition S, the SAA7706H address ‘0011100’ and a logic 0 (write) for the R/$\overline{W}$ bit. This is followed by an acknowledge of the SAA7706H.

Then the master writes the high memory address and low memory address where the reading of the memory content of the SAA7706H must start. The SAA7706H acknowledges these addresses both. Then the master generates a repeated START (Sr) and again the SAA7706H address ‘0011100’ but this time followed by a logic 1 (read) of the R/$\overline{W}$ bit.

From this moment on the SAA7706H will send the memory content in groups of 2 (Y-memory DSP1) or 3 (X-memory DSP1, X/Y-memory DSP2 or registers) bytes to the I²C-bus each time acknowledged by the master. The master stops this cycle by generating a negative acknowledge, then the SAA7706H frees the I²C-bus and the master can generate a STOP condition. The data is transferred from the DSP register to the I²C-bus register at execution of the MPI instruction in the DSP2 program. Therefore at least once every DSP routine an MPI instruction should be added. The data length of 4 bytes is not used in the SAA7706H.

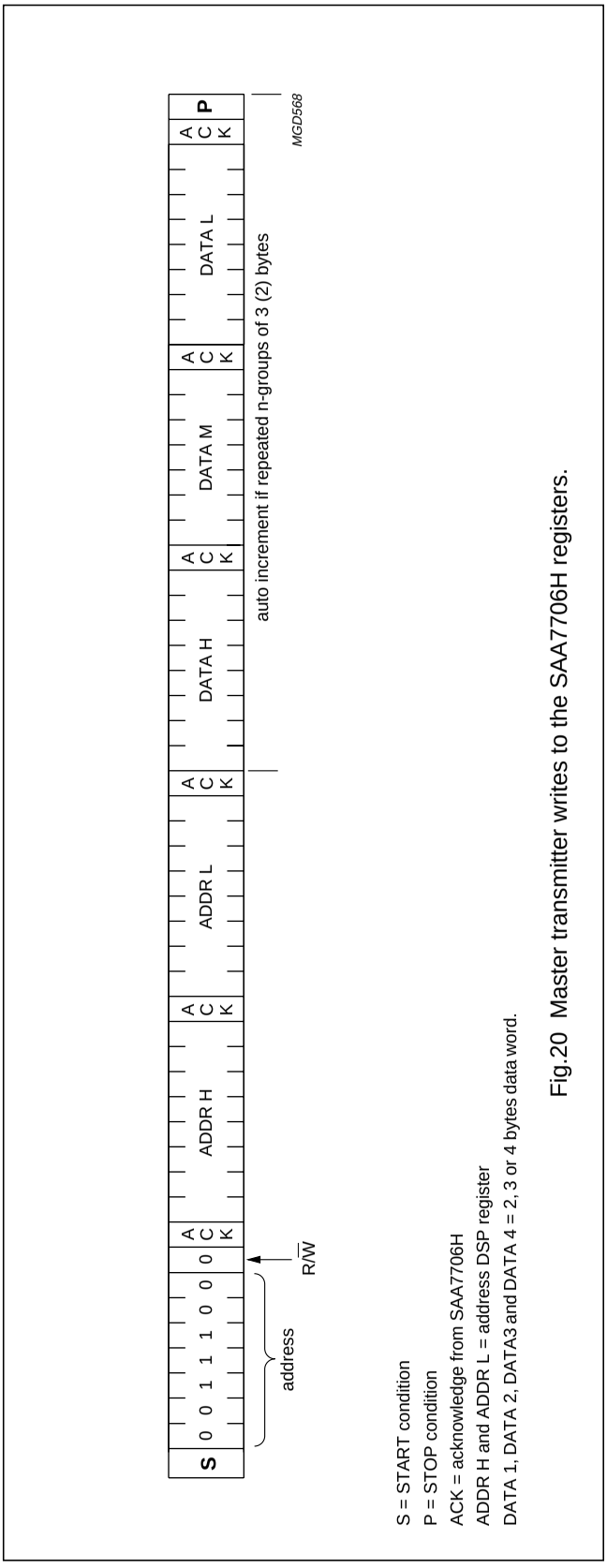
9.5 SAA7706H hardware registers

The write cycle can be used to write the bytes to the hardware registers to control the DCS block, the PLL for the DSP clock generation, the IAC settings, the AD volume control settings, the analog input selection, the format of the I²S-bus and some other settings. It is also possible to read these locations for chip status information. More detail can be found in the I²C-bus memory map, Tables 4 and 5.

9.5.1 SAA7706H DSPs REGISTERS

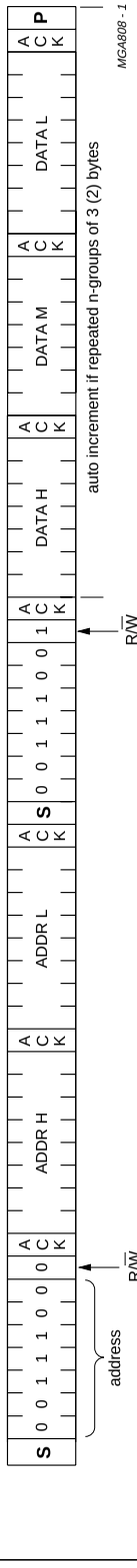
The hardware registers have two different address blocks. One block exists out of hardware register locations which control both DSPs and some major settings such as the PLL division. These locations have a maximum of 16 bits, which means 2 bytes need to be sent to or read from. For the SAA7706H one register is located at the DSPs and general control register (0FFFH).

The second block has an address space of 16 addresses and are all X-memory mapped on DSP2. While this space is 24 bits wide 3 bytes should be sent to or read from. These addresses are DSP2 mapped which means an MPI instruction is needed for accessing those locations and there is no verifying mechanism if all addresses are really mapped to physical registers. Therefore, all those locations will be acknowledged even if the data is not valid. For the SAA7706H several registers are located in this section. A few registers are predefined for DSP2 purposes (see Table 5).



S = START condition
P = STOP condition
ACK = acknowledge from SAA7706H
ADDR H and ADDR L = address DSP register
DATA 1, DATA 2, DATA3 and DATA 4 = 2, 3 or 4 bytes data word.

Fig.20 Master transmitter writes to the SAA7706H registers.



S = START condition
Sr = repeated START condition
P = STOP condition
ACK = acknowledge from SAA7706H (SDA LOW)
R = repeat n-times the 2, 3 or 4 bytes data group
NA = negative acknowledge master (SDA HIGH)
ADDR H and ADDR L = address DSP register
DATA 1, DATA 2, DATA 3 and DATA 4 = 2, 3 or 4 bytes data word.

Fig.21 Master transmitter reads from the SAA7706H registers.

9.6 I²C-bus memory map specification

The I²C-bus memory map contains all defined I²C-bus bits. The map is split up in two different sections, the hardware memory registers and the RAM definitions. In Table 5 the preliminary memory map is depicted. The hardware registers are memory map on the XRAM of DSP2. Table 5 shows the detailed memory map of those locations. All locations are acknowledged by the SAA7706H even if the user tries to write to a reserved space. The data in these sections will be lost. Reading from this locations will result in undefined data words.

Table 4 I²C-bus memory map

ADDRESS	FUNCTION	SIZE
2000H to 21FFH	YRAM (DSP2)	512 × 12 bits
1FF0H to 1FFFH	hardware registers	16 × 24 bits
1000H to 127FH	XRAM (DSP2)	640 × 24 bits
0FFFH	DSP CONTROL	1 × 16 bits
0800H to 097FH	YRAM (DSP1)	384 × 12 bits
0000H to 017FH	XRAM (DSP1)	384 × 18 bits

Table 5 I²C-bus memory map overview of hardware registers

DESCRIPTION	REGISTER
Hardware registers	
Program counter register DSP2	1FFFH
Status register DSP2	1FFEH
I/O configuration register DSP2	1FFDH
Phone, navigation and audio register	1FFCH
FM and RDS sensitivity register	1FFBH
Clock coefficient register	1FFAH
Clock settings register	1FF9H
IAC settings register	1FF8H
Selector register	1FF7H
CL_GEN register 4	1FF6H
CL_GEN register 3	1FF5H
CL_GEN register 2	1FF4H
CL_GEN register 1	1FF3H
Evaluation register	1FF0H
DSP control	
DSPs and general control register	0FFFH

10 LIMITING VALUES

In accordance with the Absolute Maximum Ratings System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+3.6	V
V_n	input voltage on any pin		–0.5	+5.5	V
I_{IK}	DC input clamping diode current	$V_I < –0.5$ V or $V_I > V_{DD} + 0.5$ V	–	±10	mA
I_{OK}	DC output clamping diode current	$V_O < –0.5$ V or $V_O > V_{DD} + 0.5$ V	–	±20	mA
$I_{O(sink/source)}$	DC output source or sink current	$–0.5 \text{ V} < V_O < V_{DD} + 0.5$ V	–	±20	mA
I_{DD},I_{SS}	supply current per supply pin		–	±50	mA
T_{amb}	ambient operating temperature		–40	+85	°C
T_{stg}	storage temperature range		–65	+125	°C
V_{ESD}	ESD voltage				
	human body model	100 pF; 1500 Ω	2000	–	V
	machine model	200 pF; 0.5 μH; 10 Ω	200	–	V
$I_{lu(prot)}$	latch-up protection current	CIC spec/test method	100	–	mA
P_{tot}	total power dissipation		–	890	mW

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board	45	K/W

12 CHARACTERISTICS

V_{DD} = 3 to 3.6 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; T_{amb} = –40 to +85 °C						
V_{DD}	operating supply voltage	all V_{DD} pins with respect to V_{SS}	3.0	3.3	3.6	V
I_{DDD}	supply current of the digital part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	110	150	mA
$I_{DDD(core)}$	supply current of the digital core part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	105	140	mA
$I_{DDD(peri)}$	supply current of the digital periphery part	without external load to ground	–	5	10	mA
I_{DDA}	supply current of the analog part	zero input and output signal	–	40	60	mA
$I_{DDA(ADC)}$	supply current of the ADCs	zero input and output signal	–	15	26	mA
$I_{DDA(DAC)}$	supply current of the DACs	zero input and output signal	–	19	30	mA
$I_{DDA(osc)}$	supply current XTAL oscillator	functional mode	–	2	4	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{tot}	total power dissipation	DSP1 at 50 MHz, DSP2 at 62.9 MHz	–	540	750	mW
Digital I/O; T_{amb} = −40 to +85 °C; V_{DD} = 3 to 3.6 V						
V_{IH}	HIGH-level input voltage for all digital inputs and I/Os		2.0	–	–	V
V_{IL}	LOW-level input voltage for all digital inputs and I/Os		–	–	0.8	V
V_{hys}	Schmitt trigger hysteresis voltage		0.4	–	–	V
V_{OH}	HIGH-level output voltage	standard output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		5 ns slew rate output; I_O = –4 mA	V_{DD} – 0.4	–	–	V
		10 ns slew rate output; I_O = –2 mA	V_{DD} – 0.4	–	–	V
		20 ns slew rate output; I_O = –1 mA	V_{DD} – 0.4	–	–	V
V_{OL}	LOW-level output voltage	standard output; I_O = 4 mA	–	–	0.4	V
		5 ns slew rate output; I_O = 4mA	–	–	0.4	V
		10 ns slew rate output; I_O = 2 mA	–	–	0.4	V
		20 ns slew rate output; I_O = 1 mA	–	–	0.4	V
		I^2C-bus output; I_O = 4 mA	–	–	0.4	V
I_{LO}	output leakage current 3-state outputs	V_O = 0 V or V_{DD}	–	–	±5	µA
R_{pd}	internal pull-down resistor to V_{SS}		24	50	140	kΩ
R_{pu}	internal pull-up resistor to V_{DD}		30	50	100	kΩ
C_i	input capacitance		–	–	3.5	pF
$t_{i(r)}$,$t_{i(f)}$	input rise and fall times	V_{DD} = 3.6 V	–	6	200	ns
$t_{o(t)}$	output transition time	standard output; C_L = 30 pF	–	3.5	–	ns
		5 ns slew rate output; C_L = 30 pF	–	5	–	ns
		10 ns slew rate output; C_L = 30 pF	–	10	–	ns
		20 ns slew rate output; C_L = 30 pF	–	20	–	ns
		I^2C-bus output; C_b = 400 pF	60	–	300	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
DC CHARACTERISTICS						
$\frac{V_{VREFAD}}{V_{VDDA1}}$	common mode reference voltage ADC1, ADC2 and level-ADC	with reference to V_{SSA1}	0.47	0.50	0.53	
$Z_{o(VREFAD)}$	output impedance at pin VREFAD		–	10	–	Ω
V_{VDACP}	positive reference voltage ADC1, 2, 3 and level-ADC		3	3.3	3.6	V
I_{VDACP}	positive reference current ADC1, 2, 3 and level-ADC		–	−200	–	μA
V_{VDACN1}, V_{VDACN2}	negative reference voltage ADC1, 2, 3 and level-ADC		−0.3	0	+0.3	V
I_{VDACN1}, I_{VDACN2}	negative reference current ADC1, 2 and 3		–	200	–	μA
$V_{IO(ADC)}$	input offset voltage ADC1, 2 and 3		–	140	–	mV
AC CHARACTERISTICS						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)					
	CD, TAPE, AM and AUX input signals	THD <1%	0.6	0.66	–	V
	FM_MPX input signal	THD <1%; VOLFM = 00H	0.33	0.368	–	V
R_i	input impedance					
	CD, TAPE, AM and AUX input signals		1	–	–	MΩ
	FM_MPX input signal		48	60	72	kΩ
THD	total harmonic distortion					
	CD, TAPE, AM and AUX input signals	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz; f_s = 44.1 kHz	–	−85	−75	dB
	FM_MPX input signal	input signal 368 mV (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	−70	−65	dB
			–	0.03	0.056	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio					
	CD, TAPE, AM and AUX input signals	input signal at 1 kHz; bandwidth = 20 kHz; 0 dB reference = 0.55 V (RMS); f_s = 44.1 kHz	85	90	–	dB
	FM_MPX input signal mono	input signal at 1 kHz; bandwidth = 19 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H	80	83	–	dB
	FM_MPX input signal stereo	input signal at 1 kHz; bandwidth = 40 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H	75	81	–	dB
α_{19}	carrier and harmonic suppression at the output	pilot signal frequency = 19 kHz	–	81	–	dB
		unmodulated	–	98	–	dB
α_{38}	carrier and harmonic suppression at the output	subcarrier frequency = 38 kHz	–	83	–	dB
		unmodulated	–	91	–	dB
α_{57}	carrier and harmonic suppression for 19 kHz, including notch	subcarrier frequency = 57 kHz	–	83	–	dB
		unmodulated	–	96	–	dB
α_{76}	carrier and harmonic suppression for 19 kHz, including notch	subcarrier frequency = 76 kHz	–	84	–	dB
		unmodulated	–	94	–	dB
$IM_{\alpha 10}$	intermodulation	f_{mod} = 10 kHz; f_{spur} = 1 kHz	77	–	–	dB
$IM_{\alpha 13}$	intermodulation	f_{mod} = 13 kHz; f_{spur} = 1 kHz	76	–	–	dB
$\alpha_{57(VF)}$	traffic radio suppression	f = 57 kHz	–	110	–	dB
$\alpha_{67(SCA)}$	Subsidiary Communication Authority (SCA) suppression	f = 67 kHz	–	110	–	dB
α_{114}	adjacent channel suppression	f = 114 kHz	–	110	–	dB
α_{190}	adjacent channel suppression	f = 190 kHz	–	110	–	dB
$V_{th(pilot)(rms)}$	pilot threshold voltage (RMS value) at pin DSP1_OUT1	stereo on; VOLFM = 07H	–	35.5	–	mV
		stereo off; VOLFM = 07H	–	35.4	–	mV
hys	hysteresis of $V_{th(pilot)(rms)}$		–	0	–	dB
α_{cs1}	channel separation FM-stereo input	f_i = 1 kHz	40	45	–	dB
		f_i = 10 kHz	25	30	–	dB
α_{cs2}	channel separation CD, TAPE, AM and AUX input signals		60	70	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{res}	audio frequency response					
	CD, TAPE, AM and AUX input signals	f_s = 44.1 kHz; at –3 dB	20	–	–	kHz
	FM_MPX input signal	at –3 dB via DSP at DAC output	17	–	–	kHz
ΔG_{L-R}	overall left/right gain unbalance (TAPE, CD, AUX and AM input signals)		–	–	0.5	dB
α_{ct}	crosstalk between inputs	f_i = 1 kHz	65	–	–	dB
		f_i = 15 kHz	50	–	–	dB
$PSRR_{MPX/RDS}$	power supply ripple rejection MPX and RDS ADCs	output via I^2S-bus; ADC input short-circuited; f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak); C_{VREFAD} = 22 µF; C_{VDACP} = 10 µF	35	45	–	dB
$PSRR_{LAD}$	power supply ripple rejection level-ADC	output via DAC; ADC input short-circuited; f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak); C_{VREFAD} = 22 µF	29	39	–	dB
$CMRR_{CD}$	common-mode rejection ratio for CD input mode	$R_{CD\_(L)\_GND}$ = 1 MΩ; resistance of CD player ground cable < 1 kΩ; f_i = 1 kHz	60	–	–	dB
AC characteristics PHONE and NAV inputs; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
THD	total harmonic distortion of PHONE and NAV input signals at maximum input voltage	V_i = 0.75 V (RMS); f_i = 1 kHz; VOLMIX = 30H; measured at FLV and FRV outputs	40	–	–	dB
CMRR	common mode rejection ratio of PHONE and NAV input signals	V_i = 0.75 V(RMS); f_i = 1 kHz; VOLMIX = 30H	25	50	–	dB
R_i	input impedance of PHONE, NAV/AM_L and AM_R input signals		90	120	150	kΩ
$V_{i(max)(rms)}$	maximum input level of PHONE and NAV input signals (RMS value)	f_i = 1 kHz; VOLMIX = 30H	0.75	1	–	V
AC characteristics FM_RDS input; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
$V_{i(con)(max)(rms)}$	maximum conversion level of FM_RDS input (RMS value)	THD < 1%; VOLRDS = 00H	0.33	0.368	–	V
$R_{i(FM\_RDS)}$	input resistance FM_RDS input		40	60	72	kΩ
THD_{FM_RDS}	total harmonic distortion RDS ADC	f_c = 57 kHz	–60	–67	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N_{FMRDS}	signal-to-noise ratio RDS ADC	6 kHz bandwidth; f_c = 57 kHz; 0 dB reference = 0.55 V (RMS); VOLRDS = 00H	54	–	–	dB
α_{pilot}	pilot attenuation RDS		50	–	–	dB
α	nearby selectivity RDS	neighbouring channel at 200 kHz distance	61	–	–	dB
$\alpha_{n(ADC)}$	RDS ADC noise attenuation		70	–	–	dB
$V_{ripple(RDS)}$	ripple voltage RDS pass band	2.4 kHz bandwidth	–	–	0.5	dB
$\alpha_{mux(RDS)}$	multiplex attenuation RDS	mono	70	–	–	dB
		stereo	40	–	–	dB
Δf_{osc}	allowable frequency deviation of the 57 kHz RDS	maximum crystal resonance frequency deviation of 100 ppm	–	–	6	Hz
AC characteristics SPDIF1 and SPDIF2 inputs; T_{amb} = 25 °C; V_{DDA2} = 3.3 V						
$V_{i(p-p)}$	AC input level (peak-to-peak level)		0.2	0.5	3.3	V
R_i	input impedance	at 1 kHz	–	6	–	kΩ
V_{hys}	hysteresis of input voltage		–	40	–	mV
AC characteristics analog LEVEL input; T_{amb} = 25 °C; V_{DDA1} = 3.3 V						
S/N_{LAD}	signal-to-noise ratio of level-ADC	0 to 29 kHz bandwidth; maximum input level; unweighted	48	54	–	dB
R_i	input resistance		1.0	–	2.2	MΩ
$V_{i(fs)(LAD)}$	full-scale level-ADC input voltage		0	–	V_{DDA1}	V
V_{IO}	DC offset voltage		–	–	120	mV
α	decimation filter attenuation		20	–	–	$\frac{dB}{decade}$
$f_{co(PB)}$	pass band cut-off frequency	at –3 dB and DCS clock = 9.728 MHz	–	29	–	kHz
f_{sr}	sample rate frequency after decimation	DCS clock = 9.728 MHz	–	38	–	kHz
Analog DAC outputs on pins FLV, FRV, RLV and RRV; T_{amb} = 25 °C; V_{DDA2} = 3.3 V; f_s = 44.1 kHz; R_L = 5 kΩ; f_i = 1 kHz						
DC CHARACTERISTICS						
$R_{o(ref)}$	reference output resistance	pin VREFDA	–	14	–	kΩ
R_o	DAC output resistance	pins FLV, FRV, RLV and RRV	–	0.13	3.0	Ω
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1%; R_L = 5 kΩ	–	0.22	–	mA
R_L	load resistance		3	–	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_L	load capacitance		–	–	200	pF
AC CHARACTERISTICS						
$V_{o(RMS)}$	output voltage (RMS value)		–	1000	–	mV
ΔV_o	unbalance between channels		–	0.1	–	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio (measured with system one)	at 0 dB	–	–90	–85	dB
		at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio (measured with system one)	code = 0; A-weighted	–	105	–	dB
α_{cs}	channel separation		–	80	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 1%	–	50	–	dB
Oscillator; T_{amb} = 25 °C; $V_{DD(OSC)}$ = 3.3 V						
f_{xtal}	crystal frequency		–	11.2896	–	MHz
V_{xtal}	voltage across the crystal	crystal series resistance R_s < 100 Ω; crystal shunt capacitance C_p < 7 pF; crystal load capacitance C_L = 12 pF; $C_1 = C_2$ = 22 pF (see Fig.13)	1.6	2.6	3.6	V
$I_{DD(OSC)}$	supply current crystal oscillator	at start-up	1.7	3.4	6.4	mA
		at oscillation	–	0.32	–	mA

13 RDS AND I²S-BUS TIMING

T_{amb} = 25 °C; V_{DDD} = 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RDS timing (see Figs 18 and 19)						
f_{RDSCLK}	nominal RDS clock frequency		–	1187.5	–	Hz
t_{su}	clock set-up time	direct output mode	100	–	–	µs
T_{cy}	cycle time	direct output mode	–	842	–	µs
		buffer mode	2	–	–	µs
t_{HC}	clock HIGH time	direct output mode	220	–	640	µs
		buffer mode	1	–	–	µs
t_{LC}	clock LOW time	direct output mode	220	–	640	µs
		buffer mode	1	–	–	µs
t_h	data hold time		100	–	–	µs
t_w	wait time	buffer mode	1	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²S-bus timing (see Fig.23)						
t_r	rise time	T_{cy} = 325 ns	–	–	$0.15T_{cy}$	ns
t_f	fall time	T_{cy} = 325 ns	–	–	$0.15T_{cy}$	ns
T_{cy}	bit clock cycle time		325	–	–	ns
$t_{BCK(H)}$	bit clock time HIGH	T_{cy} = 325 ns	$0.35T_{cy}$	–	–	ns
$t_{BCK(L)}$	bit clock time LOW	T_{cy} = 325 ns	$0.35T_{cy}$	–	–	ns
$t_{su(D)}$	data set-up time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns
$t_{h(D)}$	data hold time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns
$t_{d(D)}$	data delay time	T_{cy} = 325 ns	–	–	$0.15T_{cy}$	ns
$t_{su(WS)}$	word select set-up time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns
$t_{h(WS)}$	word select hold time	T_{cy} = 325 ns	$0.2T_{cy}$	–	–	ns

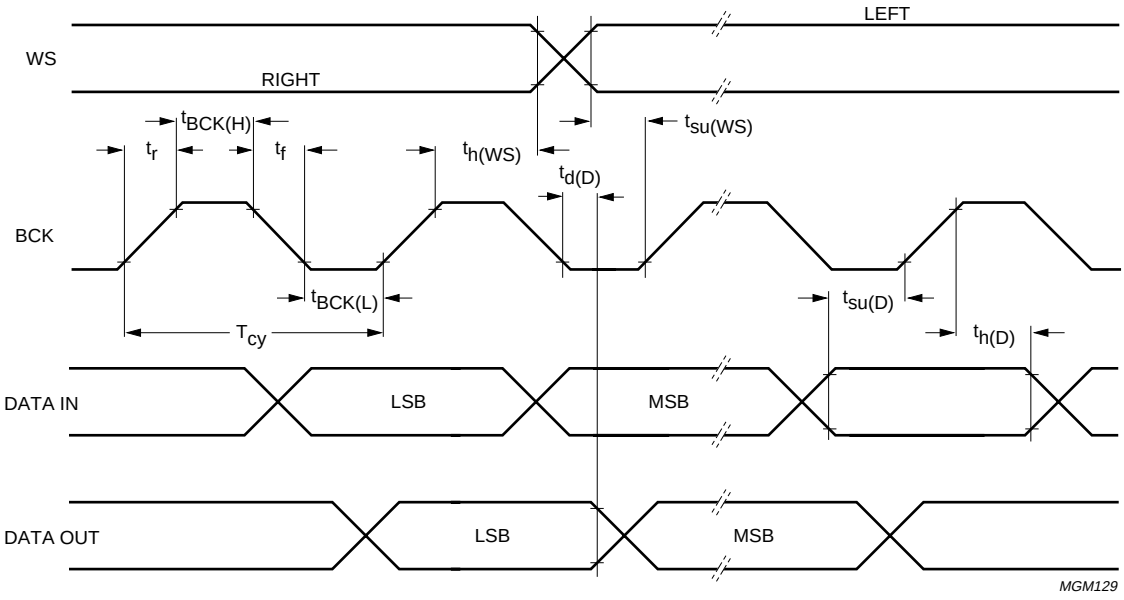


Fig.23 Input timing digital audio data inputs.

14 I²C-BUS TIMING

T_{amb} = 25 °C; V_{DDD} = 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	STANDARD MODE I²C-BUS		FAST MODE I²C-BUS		UNIT
			MIN.	MAX.	MIN.	MAX.	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	1.3	–	µs
$t_{HD;STA}$	hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock		4.7	–	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	–	0.6	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	0.6	–	µs
$t_{HD;DAT}$	data hold time		0	–	0	0.9	µs
$t_{SU;DAT}$	data set-up time		250	–	100	–	ns
t_r	rise time of both SDA and SCL signals	C_b in pF	–	1000	$20 + 0.1C_b$	300	ns
t_f	fall time of both SDA and SCL signals	C_b in pF	–	300	$20 + 0.1C_b$	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	0.6	–	µs
C_b	capacitive load for each bus line		–	400	–	400	pF
t_{SP}	pulse width of spikes to be suppressed by input filter		–	–	0	50	ns

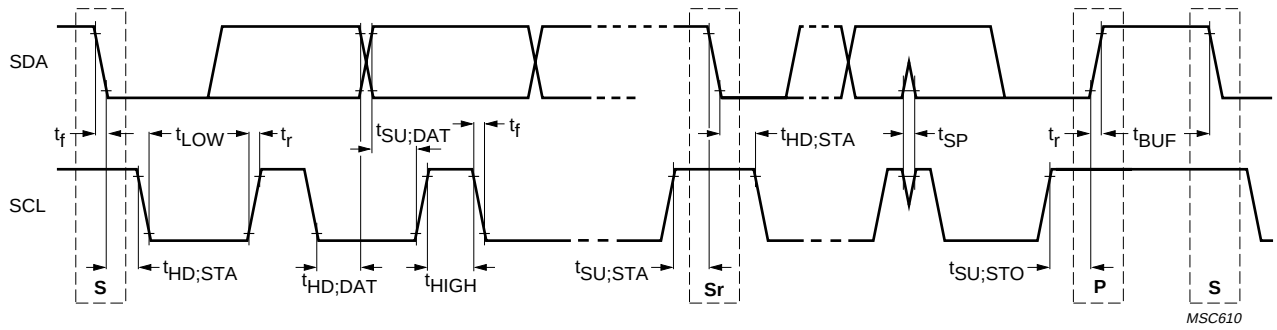


Fig.24 Definition of timing on the I²C-bus.

15 SOFTWARE DESCRIPTION

The use and description of the software features of the SAA7706H will be described in the separate application manual.

16 APPLICATION DIAGRAM

The application diagram shown in Figs 25 and 26 must be considered as one of the examples of a (limited) application of the chip e.g. in this case the I²S-bus inputs of the CD-input are not used. For the real application set-up the information of the application report is necessary.

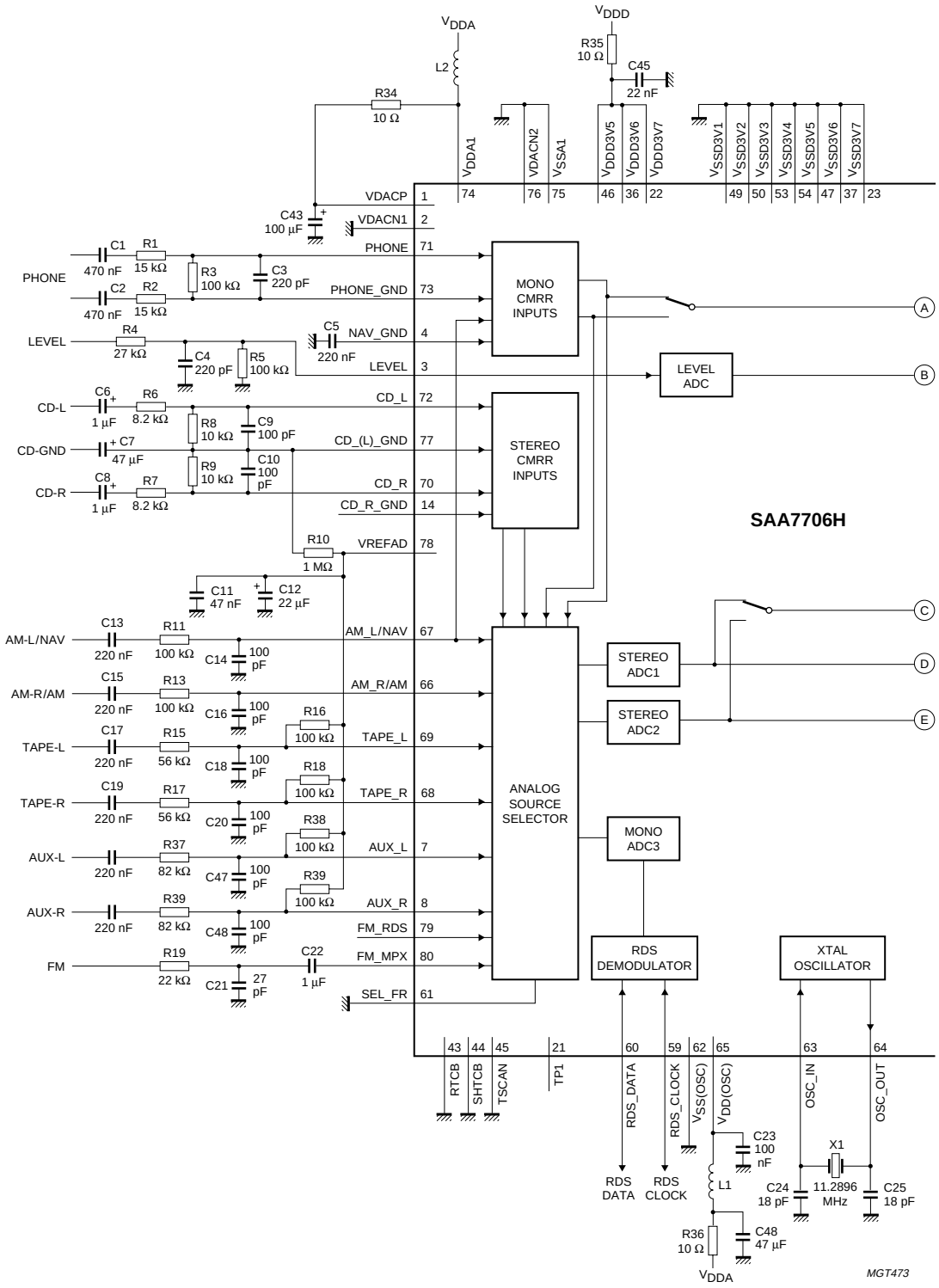


Fig.25 Application diagram (continued in Fig.26).

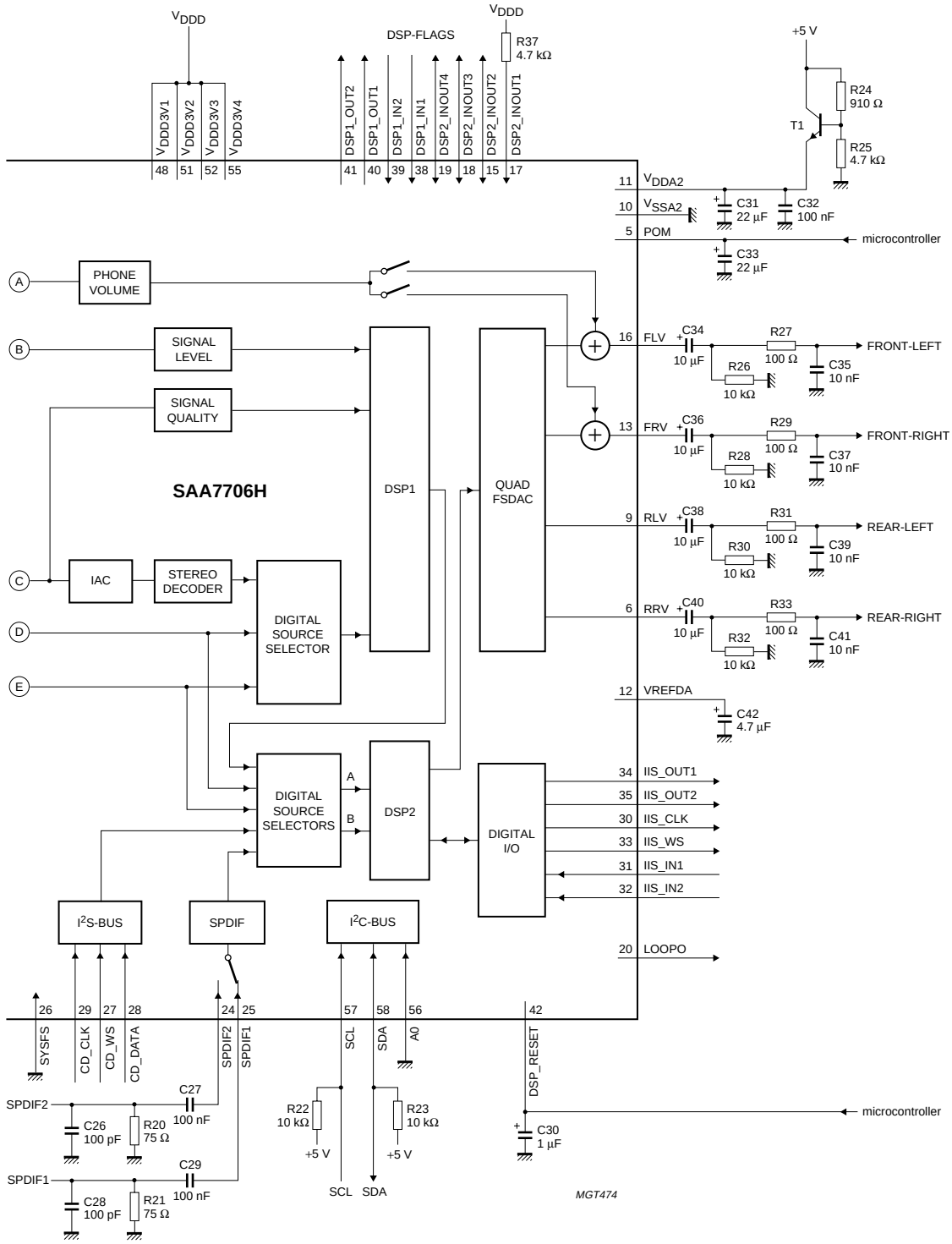
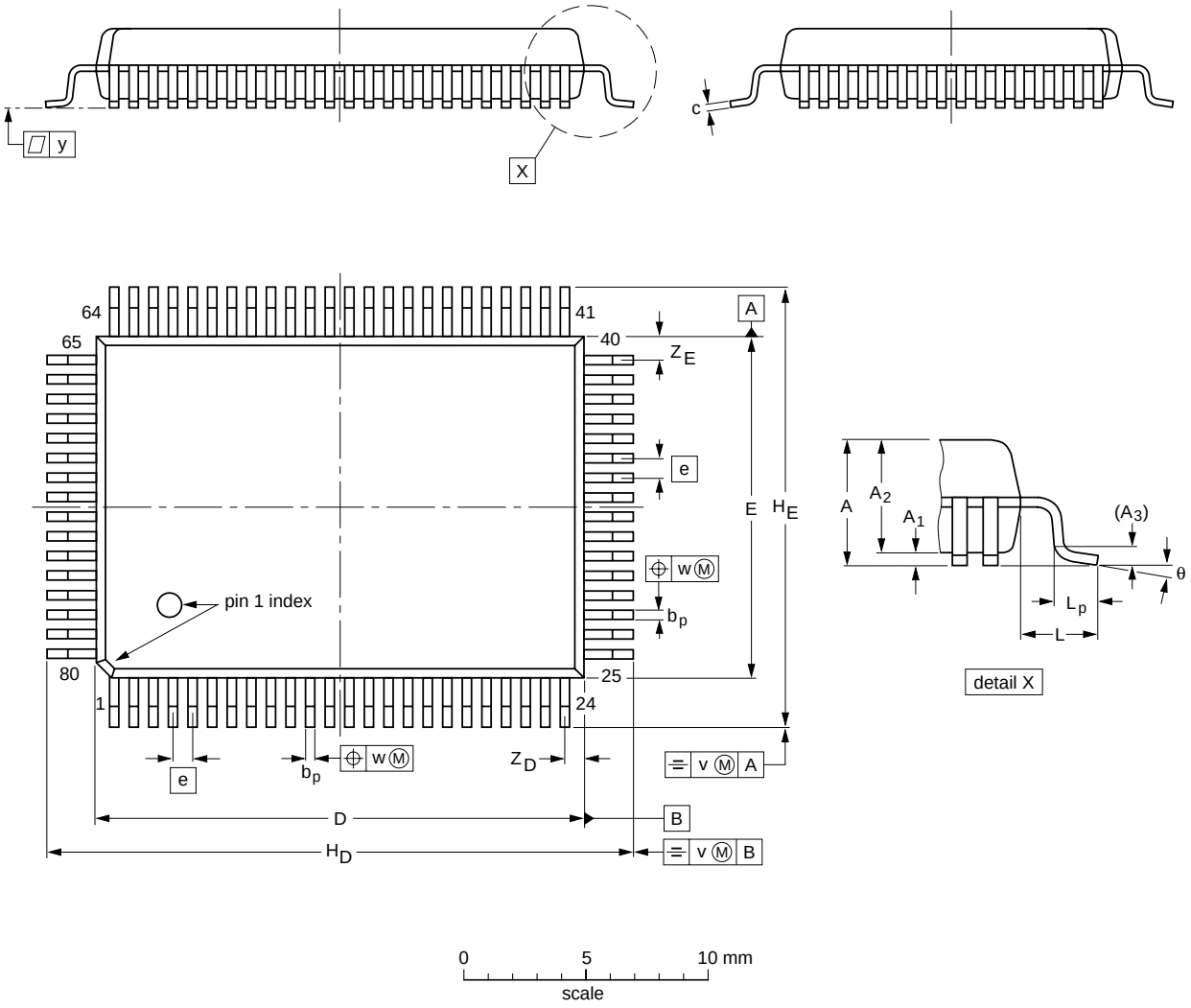


Fig.26 Application diagram (continued from Fig.25).

17 PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2		MO-112				~~97-08-01~~ 99-12-27

18 SOLDERING

18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

19 DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

20 DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: Philips Hungary Ltd., H-1119 Budapest, Fehervari ut 84/A,
Tel: +36 1 382 1700, Fax: +36 1 382 1800

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors,
Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN,
The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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