DATA SHEET

SAA5x9x family
Economy teletext and TV microcontrollers

Preliminary specification
File under Integrated Circuits, IC02

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CONTENTS

1 FEATURES

1.1 General

- Single chip microcontroller with integrated teletext decoder
- Single +5 V power supply
- Single crystal oscillator for teletext decoder, display and microcontroller
- Teletext function can be powered-down independently of microcontroller function for reduced power consumption in stand-by
- Pin compatibility throughout family.

1.2 Microcontroller

- 80C51 microcontroller core
- 16/32/64 kbyte mask programmed ROM
- 256/768/1280 bytes of microcontroller RAM
- Eight 6-bit Pulse Width Modulator (PWM) outputs for control of TV analog signals
- One 14-bit PWM for Voltage Synthesis Tuner control
- Four 8-bit Analog-to-Digital converters
- 2 high current open-drain outputs for directly driving LED's etc.
- I^2C-bus interface
- External ROM and RAM capability on QFP80 package version.

1.3 Teletext acquisition

- 1 page and 10 page Teletext version
- Acquisition of 525-line and 625-line World System Teletext, with automatic selection
- Acquisition and decoding of VPS data (PDC system A)
- Page clearing in under 64 μs (1 TV line)
- Separate storage of extension packets (SAA5296/7, SAA5296/7A and SAA5496/7)
- Inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) and Subtitle Page Table (SPT) (SAA5296/7, SAA5296/7A and SAA5496/7)
- Automatic detection of FASTEXT transmission
- Real-time packet 26 engine for processing accented (and other) characters
- Comprehensive Teletext language coverage
- Video signal quality detector.

1.4 Teletext Display

- 525-line and 625-line display
- 12×10 character matrix
- Double height, width and size On-Screen Display (OSD)
- Definable border colour
- Enhanced display features including meshing and shadowing
- 260 characters in mask programmed ROM
- Automatic FRAME output control with manual override
- RGB push pull output to standard decoder ICs
- Stable display via slave synchronisation to Horizontal Sync and Vertical Sync.

1.5 Additional features of SAA529xA devices

- Wide Screen Signalling (WSS) bit decoding (line 23).

1.6 Additional features of SAA549x devices

- Wide Screen Signalling bit decoding (line 23)
- Quad width OSD capability
- 32 additional OSD characters in mask programmed ROM
- 8 foreground and 8 background colours definable from a palette of 64.

2 GENERAL DESCRIPTION

The SAA529x, SAA529xA and SAA549x family of microcontrollers are a derivative of the Philips' industry-standard 80C51 microcontroller and are intended for use as the central control mechanism in a television receiver. They provide control functions for the television system and include an integrated teletext function.

The teletext hardware has the capability of decoding and displaying both 525-line and 625-line World System Teletext. The same display hardware is used both for Teletext and On-Screen Display, which means that the display features give greater flexibility to differentiate the TV set.

The family offers both 1 page and 10 page Teletext capability, in a range of ROM sizes. Increasing display capability is offered from the SAA5290 to the SAA5497.

3 ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE			PROGRAM MEMORY (ROM)
	NAME	DESCRIPTION	VERSION	
SAA5290PS/nnn	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1	16 kbytes
SAA5291PS/nnn	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1	32 kbytes
SAA5291APS/nnn				
SAA5296PS/nnn				
SAA5296APS/nnn				
SAA5491PS/nnn				
SAA5496PS/nnn				
SAA5291H/nnn	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2	32 kbytes and external
SAA5291AH/nnn				
SAA5296H/nnn				
SAA5296AH/nnn				
SAA5491H/nnn				
SAA5496H/nnn				
SAA5297PS/nnn	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1	64 kbytes
SAA5297APS/nnn				
SAA5497PS/nnn				
SAA5297H/nnn	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2	64 kbytes or external
SAA5297AH/nnn				
SAA5497H/nnn				

Note

1. ‘nnn’ is a three-digit number uniquely referencing the microcontroller program mask and OSD mask.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	supply voltages	4.5	5.0	5.5	V
V_{DDM}					
V_{DDT}					
f_{xtal}	crystal frequency	–	12	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C
I_{DDM}	microcontroller supply current	–	20	35	mA
SAA5290, SAA5291, SAA5291A and SAA5491					
I_{DDA}	analog supply current	–	35	50	mA
I_{DDT}	teletext supply current	–	40	65	mA
SAA5296, SAA5296A, SAA5297, SAA5297A, SAA5496 and SAA5497					
I_{DDA}	analog supply current	–	35	50	mA
I_{DDT}	teletext supply current	–	50	80	mA

5 BLOCK DIAGRAM

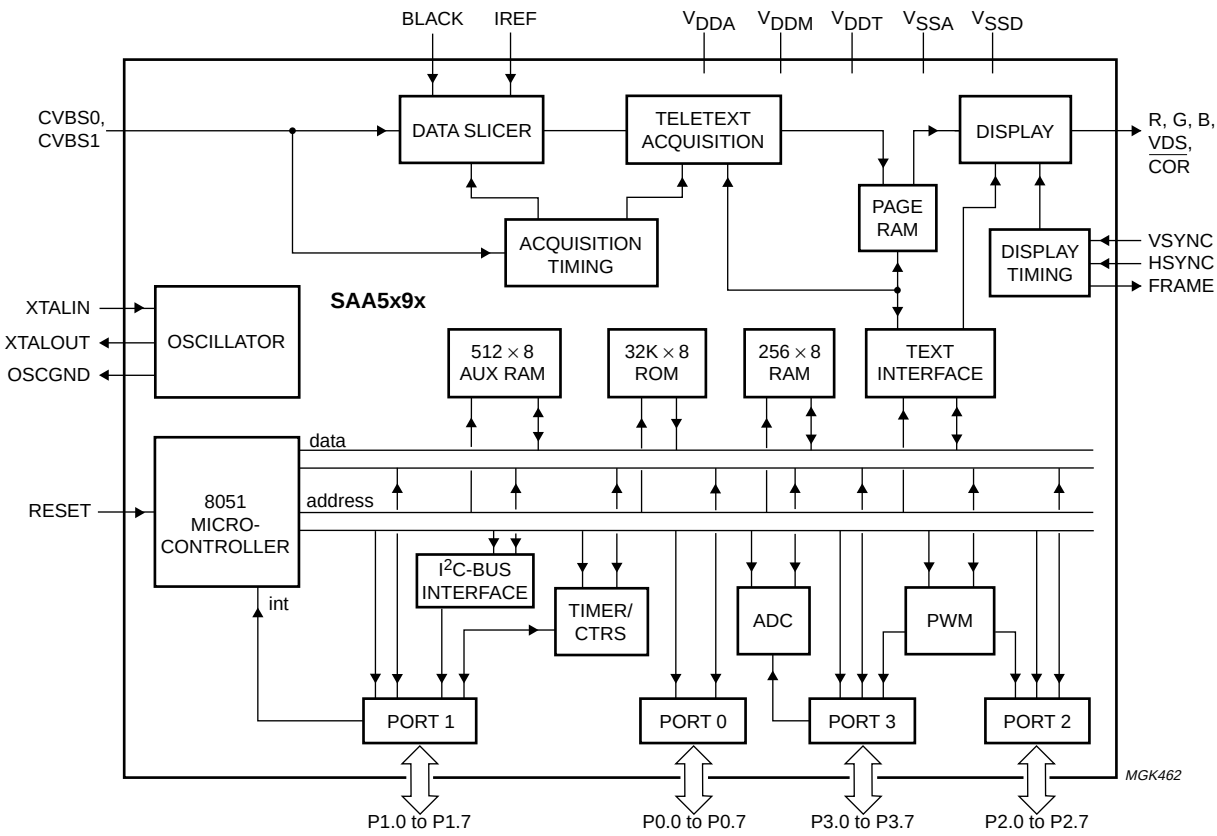


Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning

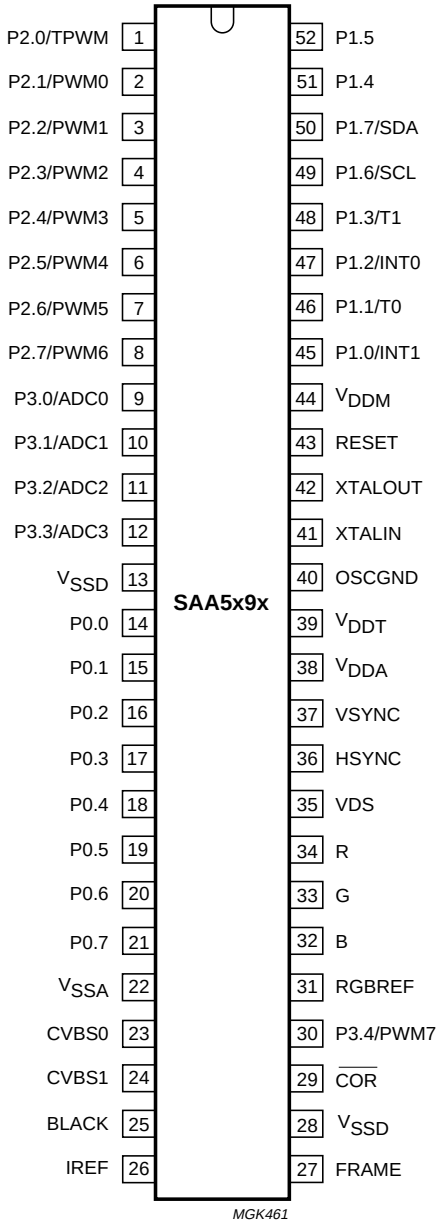


Fig.2 Pin configuration (SDIP52).

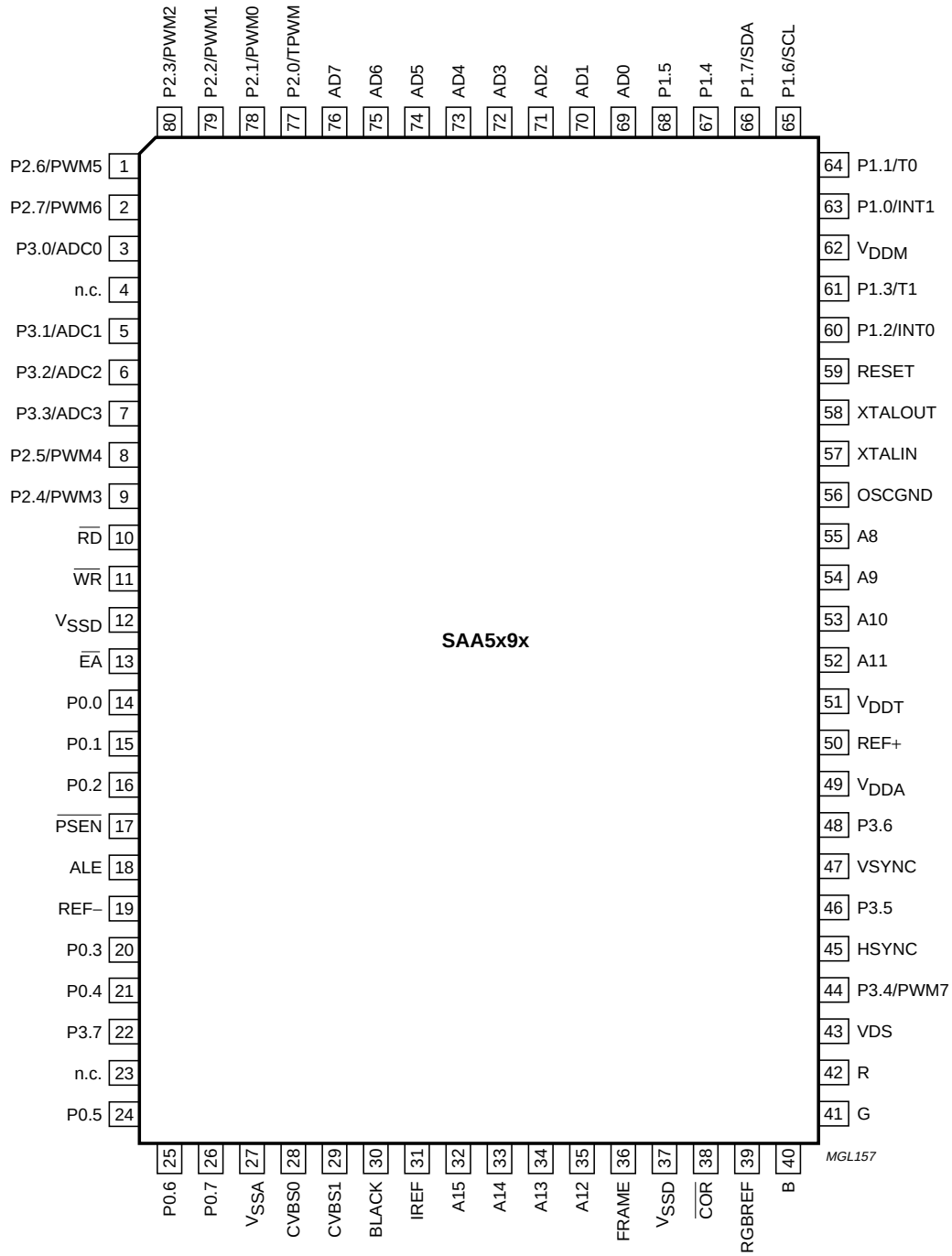


Fig.3 Pin configuration (QFP80).

6.2 Pin description

Table 1 SDIP52 and QFP80 packages

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP80	
P2.0/TPWM	1	77	**Port 2**: 8-bit open-drain bidirectional port with alternative functions. P2.0/TPWM is the output for the 14-bit high precision PWM. P2.1/PWM0 to P2.7/PWM6 are the outputs for the 6-bit PWMs 0 to 6.
P2.1/PWM0	2	78	
P2.2/PWM1	3	79	
P2.3/PWM2	4	80	
P2.4/PWM3	5	9	
P2.5/PWM4	6	8	
P2.6/PWM5	7	1	
P2.7/PWM6	8	2	
P3.0/ADC0	9	3	**Port 3**: 8-bit open-drain bidirectional port with alternative functions. P3.0/ADC0 to P3.3/ADC3 are the inputs for the software ADC facility. P3.4/PWM7 is the output for the 6-bit PWM7.
P3.1/ADC1	10	5	
P3.2/ADC2	11	6	
P3.3/ADC3	12	7	
P3.4/PWM7	30	44	
P3.5	–	46	
P3.6	–	48	
P3.7	–	22	
V_{SSD}	13	12	Digital ground.
P0.0	14	14	**Port 0**: 8-bit open-drain bidirectional port. P0.5 and P0.6 have 10 mA current sinking capability for direct drive of LEDs.
P0.1	15	15	
P0.2	16	16	
P0.3	17	20	
P0.4	18	21	
P0.5	19	24	
P0.6	20	25	
P0.7	21	26	
V_{SSA}	22	27	Analog ground.
CVBS0	23	28	Composite video inputs; a positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor.
CVBS1	24	29	
BLACK	25	30	Video black level storage input: this pin should be connected to V_{SSA} via a 100 nF capacitor.
IREF	26	31	Reference current input for analog circuits, connected to V_{SSA} via a 27 kΩ resistor.
FRAME	27	36	De-interlace output synchronised with the VSYNC pulse to produce a non-interlaced display by adjustment of the vertical deflection circuits.
V_{SSD}	28	37	Internally connected; this pin should be connected to digital ground.
$\overline{COR}$	29	38	Open-drain, active LOW output which allows selective contrast reduction of the TV picture to enhance a mixed mode display.

SYMBOL	PIN		DESCRIPTION
	SDIP52	QFP80	
LRGBREF	31	39	DC input voltage to define the output HIGH level on the RGB pins.
B	32	40	Pixel rate output of the BLUE colour information.
G	33	41	Pixel rate output of the GREEN colour information.
R	34	42	Pixel rate output of the RED colour information.
VDS	35	43	Video/data switch push-pull output for dot rate fast blanking.
HSYNC	36	45	Schmitt trigger input for a TTL level version of the horizontal sync pulse; the polarity of this pulse is programmable by register bit TXT1.H POLARITY.
VSYNC	37	47	Schmitt trigger input for a TTL level version of the vertical sync pulse; the polarity of this pulse is programmable by register bit TXT1.V POLARITY.
V_{DDA}	38	49	+5 V analog power supply.
V_{DDT}	39	51	+5 V teletext power supply.
OSCGND	40	56	Crystal oscillator ground.
XTALIN	41	57	12 MHz crystal oscillator input.
XTALOUT	42	58	12 MHz crystal oscillator output.
RESET	43	59	If the reset input is HIGH for at least 3 machine cycles (36 oscillator periods) while the oscillator is running, the device is reset; this pin should be connected to V_{DDM} via a 2.2 µF capacitor.
V_{DDM}	44	62	+5 V microcontroller power supply.
P1.0/INT1	45	63	**Port** 1: 8-bit open-drain bidirectional port with alternate functions. P1.0/INT1 is external interrupt 1 which can be triggered on the rising and falling edge of the pulse. P1.1/T0 is the counter/timer 0. P1.2/INT0 is external interrupt 0. P1.3/T1 is the counter/timer 1. P1.6/SCL is the serial clock input for the I^2C-bus. P1.7/SDA is the serial data port for the I^2C-bus.
P1.1/T0	46	64	
P1.2/INT0	47	60	
P1.3/INT1	48	61	
P1.6/SCL	49	65	
P1.7/SDA	50	66	
P1.4	51	67	
P1.5	52	68	
REF+	–	50	Positive reference voltage for software driven ADC.
REF–	–	19	Negative reference voltage for software driven ADC.
RD	–	10	Read control signal to external Data Memory.
$\overline{WR}$	–	11	Write control signal to external Data Memory.
$\overline{PSEN}$	–	17	Enable signal for external Program Memory.
ALE	–	18	External latch enable signal; active HIGH.
$\overline{EA}$	–	13	Control signal used to select external (LOW) or internal (HIGH) Program Memory.
AD0 to AD7	–	69 to 76	Address lines A0 to A7 multiplexed with data lines D0 to D7.
A8 to A15	–	55 to 52, 35 to 32	Address lines A8 to A15.

7 FUNCTIONAL DESCRIPTION

7.1 Microcontroller

The functionality of the microcontroller used in this family is described here with reference to the industry-standard 80C51 microcontroller. A full description of its functionality can be found in the *"80C51-Based 8-Bit Microcontrollers; Data Handbook IC20"*. Using the 80C51 as a reference, the changes made to this family fall into two categories:

- Features not supported by the SAA529x, SAA529xA or SAA549x devices
- Features found on the SAA529x, SAA529xA or SAA549x devices but not supported by the 80C51.

7.2 80C51 features not supported

7.2.1 Interrupt priority

The IP SFR is not implemented and all interrupts are treated with the same priority level. The normal prioritisation of interrupts is maintained within the level.

Table 2 Interrupts and vectors address

INTERRUPT SOURCE	VECTOR ADDRESS
Reset	000H
External INT0	003H
Timer 0	00BH
External INT1	013H
Timer 1	01BH
Byte I²C-bus	02BH
Bit I²C-bus; note 1	053H

Note

1. SAA5290, SAA5291, SAA5291A and SAA5491 only.

7.2.2 Off-chip memory

The SDIP52 version does not support the use of off-chip program memory or off-chip data memory.

7.2.3 Idle and Power-down modes

As Idle and Power-down modes are not supported, their respective bits in PCON are not available.

7.2.4 UART Function

The 80C51 UART is not available. As a consequence the SCON and SBUF SFRs are removed and the ES bit in the IE SFR is unavailable.

7.3 Additional features

The following features are provided in addition to the standard 80C51 features.

7.3.1 Interrupts

The external INT1 interrupt is modified to generate an interrupt on both the rising and falling edges of the INT1 pin, when EX1 bit is set. This facility allows for software pulse width measurement for handling of a remote control.

7.3.2 Bit level I²C-bus interface

For reasons of compatibility with SAA5290, the SAA5291, SAA5291A and SAA5491 contain a bit level serial I/O which supports the I²C-bus. P1.6/SCL and P1.7/SDA are the serial I/O pins. These two pins meet the I²C-bus specification *"The I²C-bus and how to use it (including specifications)"* concerning the input levels and output drive capability. Consequently, these two pins have an open-drain output configuration. All the four following modes of the I²C-bus are supported.

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

Three SFRs support the function of the bit-level I²C-bus hardware: S1INT, S1BIT and S1SCS and are enabled by setting register bit TXT8.I²C SELECT to logic 0.

7.3.3 Byte level I²C-bus interface

The byte level serial I/O supports the I²C-bus protocol. P1.6/SCL and P1.7/SDA are the serial I/O pins. These two pins meet the I²C-bus specification concerning the input levels and output drive capability. Consequently, these two pins have an open-drain output configuration.

The byte level I²C-bus serial port is identical to the I²C-bus serial port on the 8xC552. The operation of the subsystem is described in detail in the 8xC552 data sheet found in *"80C51-Based 8-Bit Microcontrollers; Data Handbook IC20"*.

Four SFRs support the function of the byte level I²C-bus hardware, they are S1CON, S1STA, S1DAT and S1ADR and are enabled by setting register bit TXT8.I²C SELECT to logic 1.

7.3.4 LED support

Port pins P0.5 and P0.6 have a 10 mA current sinking capability to enable LEDs to be driven directly.

7.3.5 6-BIT PWM DACS

Eight 6-bit DACs are available to allow direct control of analog parts of the television.

Each low resolution 6-bit DAC is controlled by its associated Special Function Register (PWM0 to PWM7). The PWM outputs are alternative functions of Port 2 and Port 3.4. The PWE bit in the SFR for the port corresponding to the PWM should be set to logic 1 for correct operation of the PWM, e.g. if PWM0 is to be used, P2.1 should be set to logic 1 setting the port pin to high-impedance.

7.3.5.1 Pulse Width Modulator Registers (PWM0 to PWM7)

Table 3 Pulse Width Modulator Registers (see Table 10 for addresses)

7	6	5	4	3	2	1	0
PWE	–	PV5	PV4	PV3	PV2	PV1	PV0

Table 4 Description of PWMn bits (n = 0 to 7)

BIT	SYMBOL	DESCRIPTION
7	PWE	If PWE is set to a logic 1, the corresponding PWM is active and controls its assigned port pin. If PWE is set to a logic 0, the port pin is controlled by the corresponding bit in the port SFR.
6	–	Not used.
5	PV5	The output of the PWM is a pulse of period 21.33 μs with a pulse HIGH time determined by the binary value of these 6-bits multiplied by 0.33 μs. PV5 is the most significant bit.
4	PV4	
3	PV3	
2	PV2	
1	PV1	
0	PV0	

7.3.6 14-BIT PWM DAC

One 14-bit DAC is available to allow direct control of analog sections of the television. The 14-bit PWM is controlled using Special Function Registers TDACL and TDACH.

The output of the TPWM is a pulse of period 42.66 μs. The 7 most significant bits, TDACH.TD13 (MSB) to TDACH.TD8 and TDACL.TD7, alter the pulse width between 0 and 42.33 μs, in much the same way as in the 6-bit PWMs. The 7 least significant bits, TDACL.TD6 to TDACL.TD0 (LSB), extend certain pulses by a further 0.33 μs, e.g. if the 7 least significant bits are given the value 01H, then 1 in 128 cycles is extended. If the 7 least significant bits are given the value 02H, then 2 in 128 cycles is extended, and so forth.

The TPWM will not start to output a new value until after writing a value to TDACH. Therefore, if the value is to be changed, TDACL should be written to before TDACH.

7.3.6.1 TPWM High Byte Register (TDACH)

Table 5 TPWM High Byte Register (SFR address D3H)

7	6	5	4	3	2	1	0
PWE	–	TD13	TD12	TD11	TD10	TD9	TD8

Table 6 Description of TDACH bits

BIT	SYMBOL	DESCRIPTION
7	PWE	If PWE is set to a logic 1, the TPWM is active and controls port line P2.0. If PWE is set to a logic 0, the port pin is controlled by the corresponding bit in the port SFR.
6	–	Not used.
5	TD13	These 6-bits along with bit TD7 in the TDACL register control the pulse width period. TD13 is the most significant bit.
4	TD12	
3	TD11	
2	TD10	
1	TD9	
0	TD8	

7.3.6.2 TPWM Low Byte Register (TDACL)

Table 7 TPWM Low Byte Register (SFR address D2H)

7	6	5	4	3	2	1	0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Table 8 Description of TDACL bits

BIT	SYMBOL	DESCRIPTION
7	TD7	This bit is used with bits TD13 to TD8 in the TDACH register to control the pulse width period.
6 to 0	TD6 to TD0	These 7-bits extend certain pulses by a further 0.33 μs.

7.3.7 SOFTWARE ADC

Up to 4 successive approximation ADCs can be implemented in software by making use of the on-chip 8-bit DAC and multiplexed voltage comparator. The software ADC uses 4 analog inputs which are multiplexed with P3.0 to P3.3.

Table 9 ADC input channel selection

CH1	CH0	INPUT PIN
0	0	P3.3/ADC3
0	1	P3.0/ADC0
1	0	P3.1/ADC1
1	1	P3.2/ADC2

The control of the ADC is achieved using the Special Function Registers SAD and SADB.

SAD.CH1 and SAD.CH0 select one of the four inputs to pass to the comparator. The other comparator input comes from the DAC, whose value is set by SAD.SAD7 (MSB) to SAD.SAD4 and SADB.SAD3 to SADB.SAD0 (LSB). The setting of the value SAD.SAD7 to SAD.SAD4 must be performed at least 1 instruction cycle before the setting of SAD.ST to ensure comparison is made using the correct SAD.SAD7 to SAD.SAD4 value.

The output of the comparator is SAD.VHI, and is valid after 1 instruction cycle following the setting of SAD.ST to a logic 1.

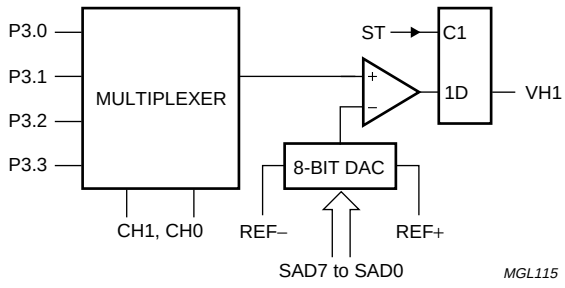


Fig.4 SAD block diagram.

7.4 Microcontroller interfacing

The 80C51 communicates with the peripheral functions using Special Function Registers (SFRs) which are addressed as RAM locations. The registers in the teletext decoder appear as normal SFRs in the microcontroller memory map, but are written to using an internal serial bus. The SFR map is given in Table 10.

7.4.1 Special Function Register map

Table 10 Special Function Register map; note 1

SYMBOL	NAME	DIRECT ADDR. (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			7	6	5	4	3	2	1	0	
ACC[2]	Accumulator	E0	E7	E6	E5	E4	E3	E2	E1	E0	00
			–	–	–	–	–	–	–	–	
B[2]	B register	F0	F7	F6	F5	F4	F3	F2	F1	F0	00
			–	–	–	–	–	–	–	–	
DPTR	Data Pointer (2 bytes)										
DPH	High byte	83	–	–	–	–	–	–	–	–	00
DPL	Low byte	82	–	–	–	–	–	–	–	–	00
IE[2][3]	Interrupt Enable	A8	AF	AE	AD	AC	AB	AA	A9	A8	00
			EA	ES1	ES2	*	ET1	EX1	ET0	EX0	
P0[2]	Port 0	80	87	86	85	84	83	82	81	80	FF
			–	–	–	–	–	–	–	–	
P1[2]	Port 1	90	97	96	95	94	93	92	91	90	FF
			–	–	–	–	–	–	–	–	
P2[2]	Port 2	A0	A7	A6	A5	A4	A3	A2	A1	A0	FF
			–	–	–	–	–	–	–	–	
P3[2][3]	Port 3	B0	B7	B6	B5	B4	B3	B2	B1	B0	FF
			–	–	–	–	–	–	–	–	
PCON[3]	Power Control	87	–	ARD	–	*	GF1	GF0	–	–	10

SYMBOL	NAME	DIRECT ADDR. (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			7	6	5	4	3	2	1	0	
PSW[2]	Program Status Word	D0	D7	D6	D5	D4	D3	D2	D1	D0	00
			CY	AC	F0	RS1	RS0	OV	*	P	
PWM0[3]	Pulse Width Modulator 0	D5	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM1[3]	Pulse Width Modulator 1	D6	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM2[3]	Pulse Width Modulator 2	D7	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM3[3]	Pulse Width Modulator 3	DC	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM4[3]	Pulse Width Modulator 4	DD	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM5[3]	Pulse Width Modulator 5	DE	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM6[3]	Pulse Width Modulator 6	DF	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM7[3]	Pulse Width Modulator 7	D4	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
S1ADR[3]	Serial I^2C-bus address	DB	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	GC	00
S1CON [2][3][4]	Serial I^2C-bus control	D8	DF	DE	DD	DC	DB	DA	D9	D8	
			CR2	ENSI	STA	STO	SI	AA	CR1	CR0	00
S1SCS [2][3][5]	Serial I^2C-bus control	D8	DF	DE	DD	DC	DB	DA	D9	D8	
			SDI	SCI	CLH	BB	RBF	WBF	STR	ENS	E0
S1DAT [3][4]	Serial I^2C-bus data	DA	DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0	00
S1INT [3][5]	Serial I^2C-bus Interrupt	DA	SI	–	–	–	–	–	–	–	7F

SYMBOL	NAME	DIRECT ADDR. (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			7	6	5	4	3	2	1	0	
S1STA (3)(4)	Serial I²C-bus status	D9	STAT4	STAT3	STAT2	STAT1	STAT0	0	0	0	F8
S1BIT (3)(5)	Serial I²C-bus data	D9	SDO/SDI	–	–	–	–	–	–	–	7F
SAD (2)(3)	Software ADC (MSB)	E8	EF	EE	ED	EC	EB	EA	E9	E8	00
			VHI	CH1	CH0	ST	SAD7	SAD6	SAD5	SAD4	
SADB (2)(3)	Software ADC (LSB)	98	9F	9E	9D	9C	9B	9A	99	98	00
			–	–	–	–	SAD3	SAD2	SAD1	SAD0	
SP	Stack Pointer	81	8F	8E	8D	8C	8B	8A	89	88	07
TCON(2)	Timer/counter control	88	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00
TDACH	TPWM High byte	D3	PWE	*	TD13	TD12	TD11	TD10	TD9	TD8	40
TDACL	TPWM Low byte	D2	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	00
TH0	Timer 0 High byte	8C	TH07	TH06	TH05	TH04	TH03	TH02	TH01	TH00	00
TH1	Timer 1 High byte	8D	TH17	TH16	TH15	TH14	TH13	TH12	TH11	TH10	00
TL0	Timer 0 Low byte	8A	TL07	TL06	TL05	TL04	TL03	TL02	TL01	TL00	00
TL1	Timer 1 Low byte	8B	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10	00
TMOD	Timer/counter mode	89	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00
			Timer 1				Timer 0				
TXT0(3)	Teletext Register 0	C0	X24 POSN	DISPLAY X24	AUTO FRAME	DISABLE HDR ROLL	DISPLAY STATUS ROW ONLY	DISABLE FRAME	VPS ON	INV ON	00
TXT1(3)	Teletext Register 1	C1	EXT PKT OFF	8–BIT	ACQ OFF	X26 OFF	FULL FIELD	FIELD POLARITY	H POLARITY	V POLARITY	00

SYMBOL	NAME	DIRECT ADDR. (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			7	6	5	4	3	2	1	0	
TXT2(3)	Teletext Register 2	C2	*	REQ3	REQ2	REQ1	REQ0	SC2	SC1	SC0	00
TXT3(3)	Teletext Register 3	C3	*	*	*	PRD4	PRD3	PRD2	PRD1	PRD0	00
TXT4(3)	Teletext Register 4	C4	OSD BANK ENABLE	QUAD WIDTH ENABLE	EAST/$\overline{\text{WEST}}$	DISABLE DBL HT	B MESH ENABLE	C MESH ENABLE	TRANS ENABLE	SHADOW ENABLE	00
TXT5(3)	Teletext Register 5	C5	BKGND OUT	BKGND IN	$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03
TXT6(3)	Teletext Register 6	C6	BKGND OUT	BKGND IN	$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03
TXT7(3)	Teletext Register 7	C7	STATUS ROW TOP	CURSOR ON	REVEAL	$\overline{\text{TOP}}$/ BOTTOM	DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	00
TXT8(3)	Teletext Register 8	C8	I^2C SELECT	IDS ENABLE	*	DISABLE SPANISH	PKT26 RECEIVED	WSS RECEIVED	WSS ON	$\overline{\text{CVBS0}}$/ CVBS1	00
TXT9(3)	Teletext Register 9	C9	CURSOR FREEZE	CLEAR MEMORY.	A0	R4	R3	R2	R1	R0	00
TXT10(3)	Teletext Register 10	CA	*	*	C5	C4	C3	C2	C1	C0	00
TXT11(3)	Teletext Register 11	CB	D7	D6	D5	D4	D3	D2	D1	D0	00
TXT12(3)	Teletext Register 12	CC	$\overline{625}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TXT ON	VIDEO SIGNAL QUALITY	0XXXX X00B
TXT13 (2)(3)	Teletext Register 13	B8	BF	BE	BD	BC	BB	BA	B9	B8	00
			VPS RECEIVED	PAGE CLEARING	525 DISPLAY	525 TEXT	625 TEXT	PKT 8/30	FASTEXT	TIB	
TXT14(3)	Teletext Register 14	CD	–	–		–	PAGE3	PAGE2	PAGE1	PAGE0	00

SYMBOL	NAME	DIRECT ADDR. (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			7	6	5	4	3	2	1	0	
TXT15(3)	Teletext Register 15	CE	–	–	–	–	BLOCK3	BLOCK2	BLOCK1	BLOCK0	00
TXT16(3)	Teletext Register 16	CF	–	Y2	Y1	Y0	–	–	X1	X0	00
TXT17(3)	Teletext Register 17	B9	–	FORCE ACQ 1	FORCE ACQ 0	FORCE 625	FORCE 525	SCREEN COL2	SCREEN COL1	SCREEN COL0	00
WSS1(3)	WSS Register 1	BA	–	–	–	WSS0 to WSS3 ERROR	WSS3	WSS2	WSS1	WSS0	00
WSS2(3)	WSS Register 2	BB	–	–	–	WSS4 to WSS7 ERROR	WSS7	WSS6	WSS5	WSS4	00
WSS3(3)	WSS Register 3	BC	WSS11 to WSS13 ERROR	WSS13	WSS12	WSS11	WSS8 to WSS10 ERROR	WSS10	WSS9	WSS8	00
CLUT(3)	CLUT Register	BD	CLUT ENABLE	CLUT ADDRESS	B1 or –	B0 or –	G1 or ENTRY 3	G0 or ENTRY 2	R1 or ENTRY 1	R0 or ENTRY 0	00

Notes

1. The asterisk (*) indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. SFRs are bit addressable.
3. SFRs are modified or added to the 80C51 SFRs.
4. This register used for Byte Orientated I^2C-bus, TXT8.I^2C SELECT = 1.
5. This register used for Bit Orientated I^2C-bus, TXT8.I^2C SELECT = 0.

7.4.2 Special Function Registers bit descriptions

Table 11 SFRs bit description

REGISTER	FUNCTION
Interrupt Enable Register (IE)	
EA	disable all interrupts (logic 0) or use individual interrupt enable bits (logic 1)
ES1	bit I^2C-bus interrupt enable (logic 1)
ES2	byte I^2C-bus interrupt enable (logic 1)
ET1	enable timer 1 overflow interrupt (logic 1)
EX1	enable external interrupt 1 (logic 1)
ET0	enable timer 0 overflow interrupt (logic 1)
EX0	enable external interrupt 0 (logic 1)
Power Control Register (PCON)	
ARD	AUX-RAM disable bit. Disables the 512 bytes of internal AUX-RAM (logic 1); all MOVX-instructions access the external data memory
GF1	general purpose flag 1
GF0	general purpose flag 0
Program Status Word (PSW)	
CY	carry flag
AC	auxiliary carry flag
F0	flag 0
RS1,RS0	register bank select control bits
OV	overflow flag
P	parity flag
6-bit Pulse Width Modulator Control Registers (PWM0 to PWM7)	
PWE	activate this PWM and take control of respective port pin (logic 1)
PV5 to PV0	binary value sets high time of PWM output
Serial Interface Slave Address Register (S1ADR); note 1	
ADR6 to ADR0	I^2C-bus slave address to which the device will respond
GC	enables response to the I^2C-bus general call address
Serial Interface Control Register (S1CON); note 1	
CR2 to CR0	clock rate bits
ENSI	I^2C-bus interface enable
STA	start condition flag
STO	stop condition flag
SI	interrupt flag
AA	assert acknowledge flag

REGISTER	FUNCTION
Serial Interface Data Register (S1DAT); note 1	
DAT7 to DAT0	I^2C-bus data
Serial Interface Status Register (S1STA) - READ only; note 1	
STAT4 to STAT0	I^2C-bus interface status
Serial Interface Data Register (S1BIT) - READ; note 2	
SDI	I^2C-bus data bit input
Serial Interface Data Register (S1BIT) - WRITE; note 2	
SDO	I^2C-bus data bit output
Serial Interface Interrupt Register (S1INT); note 2	
SI	I^2C-bus interrupt flag
Serial Interface Control Register (S1SCS) - READ; note 2	
SDI	serial data input at SDA
SCI	serial clock input at SCL
CLH	clock LOW-to-HIGH transition flag
BB	bus busy flag
RBF	read bit finished flag
WBF	write bit finished flag
STR	clock stretching enable (logic 1)
ENS	enable serial I/O (logic 1)
Serial Interface Control Register (S1SCS) - WRITE; note 2	
SDO	serial data output at SDA
SCO	serial clock output at SCL
CLH	clock LOW-to-HIGH transition flag
STR	clock stretching enable (logic 1)
ENS	enable serial I/O (logic 1)
Software ADC Control Register (SAD)	
VHI	comparator output indicating that analog input voltage greater than DAC voltage (logic 1)
CH1 and CH0	ADC input channel selection bits; see Table 11
ST	initiate voltage comparison (logic 1); this bit is automatically reset to logic 0
SAD7 to SAD4	4 MSB’s of DAC input value

REGISTER	FUNCTION
Software ADC Control Register (SADB)	
SAD3 to SAD0	4 LSB's of DAC input value
Timer/Counter Control Register (TCON)	
TF1	timer 1 overflow flag
TR1	timer 1 run control bit
TF0	timer 0 overflow flag
TR0	timer 0 run control bit
IE1	interrupt 1 edge flag
IT1	interrupt 1 type control bit
IE0	interrupt 0 edge flag
IT0	interrupt 0 type control bit
14-bit PWM MSB Register (TDACH)	
PWE	activate this 14-bit PWM and take over port pin (logic 1)
TD13 to TD8	6 MSBs of 14-bit number to be output by the 14-bit PWM
14-bit PWM LSB Register (TDACL)	
TD7 to TD0	8 LSBs of 14-bit number to be output by the 14-bit PWM
Timer 0 High byte (TH0)	
TH07 to TH00	8 MSBs of Timer 0 16-bit counter
Timer 1 High byte (TH1)	
TH17 to TH10	8 MSBs of Timer 1 16-bit counter
Timer 0 Low byte (TL0)	
TL07 to TL00	8 LSBs of Timer 0 16-bit counter
Timer 1 Low byte (TL1)	
TL17 to TL10	8 LSBs of Timer 1 16-bit counter
Timer/Counter Mode Control Register (TMOD)	
GATE	gating control
C/$\overline{T}$	counter or timer selector
M1, M0	mode control bits

REGISTER	FUNCTION
Teletext Register 0 (TXT0) - WRITE only	
X24 POSN	store packet 24 in extension packet memory (logic 0) or page memory (logic 1)
DISPLAY X24	display X24 from page memory (logic 0) or extension packet memory (logic 1)
AUTO FRAME	FRAME output switched off automatically if any video displayed (logic 1)
DISABLE HDR ROLL	disable writing of rolling headers and time into memory (logic 1)
DISPLAY STATUS ROW ONLY	display row 24 only (logic 1)
DISABLE FRAME	FRAME output always LOW (logic 1)
VPS ON	enable capture of VPS data (logic 1)
INV ON[3]	enable capture of inventory page in block 8 (logic 1)
Teletext Register 1 (TXT1) - WRITE only	
EXT PKT OFF[3]	disable decoding of extension packets (logic 1)
8-BIT	data in packets 0 to 24 written into memory without error checking (logic 1)
ACQ OFF	prevent teletext acquisition section writing to memory (logic 1)
X26 OFF	disable automatic processing of packet 26 data (logic 1)
FULL FIELD	decode teletext on VBI lines only (logic 0) or decode teletext on any line (logic 1)
FIELD POLARITY	VSYNC in first half of the line (logic 0) or second half of the line (logic 1) at start of even field
H POLARITY	HSYNC input positive-going (logic 0) or negative-going (logic 1)
V POLARITY	VSYNC input positive-going (logic 0) or negative-going (logic 1)
Teletext Register 2 (TXT2) - WRITE only	
REQ3 to REQ0[3]	selects which page is modified by TXT3 page request data
SC2 to SC0	start column at which page request data written to TXT3, page request data is placed
Teletext Register 3 (TXT3) - WRITE only	
PRD4 to PRD0	page request data
Teletext Register 4 (TXT4) - WRITE only	
OSD BANK ENABLE[4]	bank switching of OSD enabled (logic 1)
QUAD WIDTH ENABLE[4]	enable quad width characters (logic 1)
EAST/ $\overline{\text{WEST}}$	western languages selected (logic 0) or Eastern languages selected (logic 1)
DISABLE DBL HGHT	disable display of double height teletext control codes (logic 1) in OSD boxes
B MESH ENABLE	enable meshing of area with black background (logic 1)
C MESH ENABLE	enable meshing of area with other background colours (logic 1)
TRANS ENABLE	set black background to transparent i.e. video is displayed (logic 1)
SHADOW ENABLE	enable south-east shadowing (logic 1)

REGISTER	FUNCTION
Teletext Register 5 (TXT5) - WRITE only	
BKGND OUT	background colour displayed outside teletext boxes (logic 1)
BKGND IN	background colour displayed inside teletext boxes (logic 1)
$\overline{\text{COR}}$ OUT	COR output active outside teletext boxes (logic 1)
$\overline{\text{COR}}$ IN	COR output active inside teletext boxes (logic 1)
TEXT OUT	text displayed outside teletext boxes (logic 1)
TEXT IN	text displayed inside teletext boxes (logic 1)
PICTURE ON OUT	video picture displayed outside teletext boxes (logic 1)
PICTURE ON IN	video picture displayed inside teletext boxes (logic 1)
Teletext Register 6 (TXT6) - WRITE only	
See TXT5	this register has the same meaning as TXT5 but is only invoked if either newsflash (C5) or subtitle (C6) bit in row 25 of the basic page memory is set
Teletext Register 7 (TXT7) - WRITE only	
STATUS ROW TOP	display row 24 below (logic 0) or above (logic 1) teletext page
CURSOR ON	display cursor at location pointed to by TXT9 and TXT10 (logic 1)
REVEAL	display characters in areas with the conceal attribute set (logic 1)
$\overline{\text{TOP}}$/BOTTOM	display rows 0 to 11 (logic 0) or 12 to 23 (logic 1) when the double height bit is set
DOUBLE HEIGHT	display each character as twice normal height (logic 1)
BOX ON 24	enable teletext boxes in memory row 24 (logic 1)
BOX ON 1-23	enable teletext boxes in memory rows 1 to 23 (logic 1)
BOX ON 0	enable teletext boxes in memory row 0 (logic 1)
Teletext Register 8 (TXT8)	
I^2C SELECT[2]	select bit I^2C-bus (logic 0) or byte I^2C-bus (logic 1)
IDS ENABLE[2]	capture teletext Independent Date Services (logic 1)
DISABLE SPANISH[2]	disable special treatment of Spanish packet 26 decoding
PKT 26 RECEIVED	set to logic 1 when packet 26 teletext data processed
WSS RECEIVED[5]	set to logic 1 when wide screen signalling data received
WSS ON[5]	enable acquisition of wide screen signalling data
$\overline{\text{CVBS0}}$/CVBS1	select CVBS0 (logic 0) or CVBS1 (logic 1) input to the device
Teletext Register 9 (TXT9) - WRITE only	
CURSOR FREEZE	locks current cursor position (logic 1)
CLEAR MEMORY	write 20H into every location in teletext memory (logic 1)
A0	TXT11 accesses the basic page memory, selected by TXT15 on the 10 page device, (logic 0) or extension packet memory (logic 1)
R4 to R0	memory row to be accessed by TXT11

REGISTER	FUNCTION
Teletext Register 10 (TXT10) - WRITE only	
C5 to C0	memory column to be accessed by TXT11
Teletext Register 11 (TXT11)	
D7 to D0	data byte written to, or read from teletext memory
Teletext Register 12 (TXT12) - READ only	
$\overline{625}$/525 SYNC	a 625-line CVBS signal (logic 0), or a 525-line CVBS signal (logic 1) is being input
ROM VER R4 to R0	mask programmable identification for character set
TXT ON	power has been applied to the teletext hardware (logic 1)
VIDEO SIGNAL QUALITY	CVBS input can be locked on by the teletext decoder (logic 1)
Teletext Register 13 (TXT13)	
VPS RECEIVED	set to logic 1 when VPS data is received
PAGE CLEARING	set when software requested page clear in progress
525 DISPLAY	set to logic 1 when 525-line syncs are driving the display
525 TEXT	set to logic 1 when 525-line teletext is received
625 TEXT	set to logic 1 when 625-line teletext is received
PKT 8/30	set to logic 1 when packet 8/30 is detected
FASTEXT	set to logic 1 when packet X27/0 is detected
TIB	text interface busy; logic 1 indicates that TXT registers 0 to 16 cannot currently be accessed
Teletext Register 14 (TXT 14) - WRITE only; note 3	
PAGE3 to PAGE0	selects which page to display
Teletext Register 15 (TXT15) - WRITE only; note 3	
BLOCK3 to BLOCK0	selects which memory block accessed by TXT9, 10 and 11
Teletext Register 16 (TXT16) - WRITE only	
Y2 to Y0	sets vertical position of display area
X1 to X0	sets horizontal position of display area
Teletext Register 17 (TXT17) - Write only	
FORCE ACQ0,1	force acquisition mode
FORCE 625	force display to 625-line mode
FORCE 525	force display to 525-line mode
SCREEN COL 2 to 0	defines colour displayed instead of TV picture and black background

REGISTER	FUNCTION
Wide Screen Signalling Register 1 (WSS1) - READ only; note 5	
WSS 0-3 ERROR	error flag for bits WSS0 to WSS3
WSS3 to WSS0	signalling bits to define aspect ratio (group 1)
Wide Screen Signalling Register 2 (WSS2) - READ only; note 5	
WSS 4-7 ERROR	error flag for bits WSS4 to WSS7
WSS7 to WSS4	signalling bits to define enhanced services (group 2)
Wide Screen Signalling Register 3 (WSS3) - READ only; note 5	
WSS11-13 ERROR	error flag for bits WSS11 to WSS13
WSS13 to WSS11	signalling bits to define reserved elements (group 4)
WSS8-10 ERROR	error flag for bits WSS8 to WSS10
WSS10 to WSS8	signalling bits to define subtitles (group 3)
Colour Look-Up Table Register (CLUT) - WRITE only; note 4	
CLUT ENABLE	enable the colour look-up table (logic 1)
CLUT ADDRESS	load CLUT address (logic 1) or CLUT data (logic 0)
B1	most significant BLUE component data
B0	least significant BLUE component data
G1 or ENTRY3	most significant GREEN component data or most significant bit of CLUT address
G0 or ENTRY2	least significant GREEN component data or CLUT address
R1 or ENTRY1	most significant RED component data or CLUT address
R0 or ENTRY0	least significant RED component data or least significant bit of CLUT address

Notes

1. Available on SAA5296, SAA5296A, SAA5297, SAA5297A, SAA5496, SAA5497 permanently and SAA5290, SAA5291, SAA5291A, SAA5491 when TXT8.I^{2}C SELECT set to logic 1.
2. Available on SAA5290, SAA5291, SAA5291A and SAA5491.
3. Available on SAA5296, SAA5296A, SAA5297, SAA5297A, SAA5496, SAA5497.
4. Available on SAA5491, SAA5496, SAA5497.
5. Available on SAA5291A, SAA5296A, SAA5297A, SAA5491, SAA5496, SAA5497.

8 TELETEXT DECODER

8.1 Data slicer

The data slicer extracts the digital teletext data from the incoming analog waveform. This is performed by sampling the CVBS waveform and processing the samples to extract the teletext data and clock.

8.2 Acquisition timing

The acquisition timing is generated from a logic level positive-going composite sync signal VCS. This signal is generated by a sync separator circuit which adaptively slices the sync pulses. The acquisition clocking and timing are locked to the VCS signal using a digital phase-locked-loop. The phase error in the acquisition phase-locked-loop is detected by a signal quality circuit which disables acquisition if poor signal quality is detected.

8.3 Teletext acquisition

This family is capable of acquiring 625-line and 525-line World System Teletext see *"World System Teletext and Data Broadcasting System"*. Teletext pages are identified by seven numbers: magazine (page hundreds), page tens, page units, hours tens, hours units, minutes tens and minutes units. The last four digits, hours and minutes, are known as the subcode, and were originally intended to be time related, hence their names. A page is requested by writing a series of bytes into the TXT3 SFR which corresponds to the number of the page required.

The bytes written into TXT3 are put into a small RAM with an auto-incrementing address. The start address for the RAM is set using the TXT2 SFR. Table 12 shows the contents of the page request RAM.

TXT2.REQ0 to TXT2.REQ3 determine which of the 10 page requests is being modified for a 10 page teletext decoder. If TXT2.REQ is given a value greater than 09H, then data written into TXT3 is ignored.

Up to 10 pages of teletext can be acquired on the 10 page device, when TXT1.EXT PKT OFF is set to logic 1, and up to 9 pages can be acquired when this bit is set to logic 0.

If the 'DO CARE' bit for part of the page number is set to a logic 0 then that part of the page number is ignored when the teletext decoder is deciding whether a page being received off air should be stored or not. For example, if the 'DO CARE' bits for the 4 subcode digits are all set to logic 0s then every subcode version of the page will be captured.

When the HOLD bit is set to a logic 0 the teletext decoder will not recognise any page as having the correct page number and no pages will be captured. In addition to providing the user requested hold function this bit should be used to prevent the inadvertent capture of an unwanted page when a new page request is being made. For example, if the previous page request was for page 100 and this was being changed to page 234, it would be possible to capture page 200 if this arrived after only the requested magazine number had been changed.

The E1 and E0 bits control the error checking which should be carried out on packets 1 to 23 when the page being requested is captured. This is described in more detail in Section 8.5.

For the ten page device, each packet can only be written into one place in the teletext RAM so if a page matches more than one of the page requests the data is written into the area of memory corresponding to the lowest numbered matching page request.

At power-up each page request defaults to any page, hold on and error check Mode 0.

Table 12 The contents of the Page request RAM

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	DO CARE Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	DO CARE Page Tens	PT3	PT2	PT1	PT0
2	DO CARE Page Units	PU3	PU2	PU1	PU0
3	DO CARE Hours Tens	X	X	HT1	HT0
4	DO CARE Hours Units	HU3	HU2	HU1	HU0
5	DO CARE Minutes Tens	X	MT2	MT1	MT0
6	DO CARE Minutes Units	MU3	MU2	MU1	MU0
7	X	X	X	E1	E0

Table 13 Notation used in Table 12

MNEMONIC	DESCRIPTION
MAG	Magazine
PT	Page Tens
PU	Page Units
HT	Hours Tens
HU	Hours Units
MT	Minutes Tens
MU	Minutes Units
E	Error check mode

8.4 Rolling headers and time

When a new page has been requested it is conventional for the decoder to turn the header row of the display green and to display each page header as it arrives until the correct page has been found.

When a page request is changed (i.e. when the TXT3 SFR is written to) a flag (PBLF) is written into bit 5, column 9, row 25 of the corresponding block of the page memory. The state of the flag for each block is updated every TV line, if it is set for the current display block, the acquisition section writes all valid page headers which arrive into the display block and automatically writes an alphanumeric green character into column 7 of row 0 of the display block every TV line.

When a requested page header is acquired for the first time, rows 1 to 23 of the relevant memory block are cleared to space, i.e. have 20H written into every column, before the rest of the page arrives. Row 24 is also cleared if the TXT0.X24 POSN bit is set. If the TXT1.EXT PKT OFF bit is set the extension packets corresponding to the page are also cleared.

The last 8 characters of the page header are used to provide a time display and are always extracted from every valid page header as it arrives and written into the display block.

The TXT0.DISABLE HEADER ROLL bit prevents any data being written into row 0 of the page memory except when a page is acquired off air i.e. rolling headers and time are not written into the memory. The TXT1.ACQ OFF bit prevents any data being written into the memory by the teletext acquisition section.

When a parallel magazine mode transmission is being received only headers in the magazine of the page requested are considered valid for the purposes of rolling headers and time. Only one magazine is used even if don't care magazine is requested. When a serial magazine mode transmission is being received all page headers are considered to be valid.

8.5 Error checking

Before teletext packets are written into the page memory they are error checked. The error checking carried out depends on the packet number, the byte number, the error check mode bits in the page request data and the TXT1.8 BIT bit.

If an uncorrectable error occurs in one of the Hamming checked addressing and control bytes in the page header or in the Hamming checked bytes in packet 8/30, bit 4 of the byte written into the memory is set, to act as an error flag to the software. If uncorrectable errors are detected in any other Hamming checked data the byte is not written into the memory.

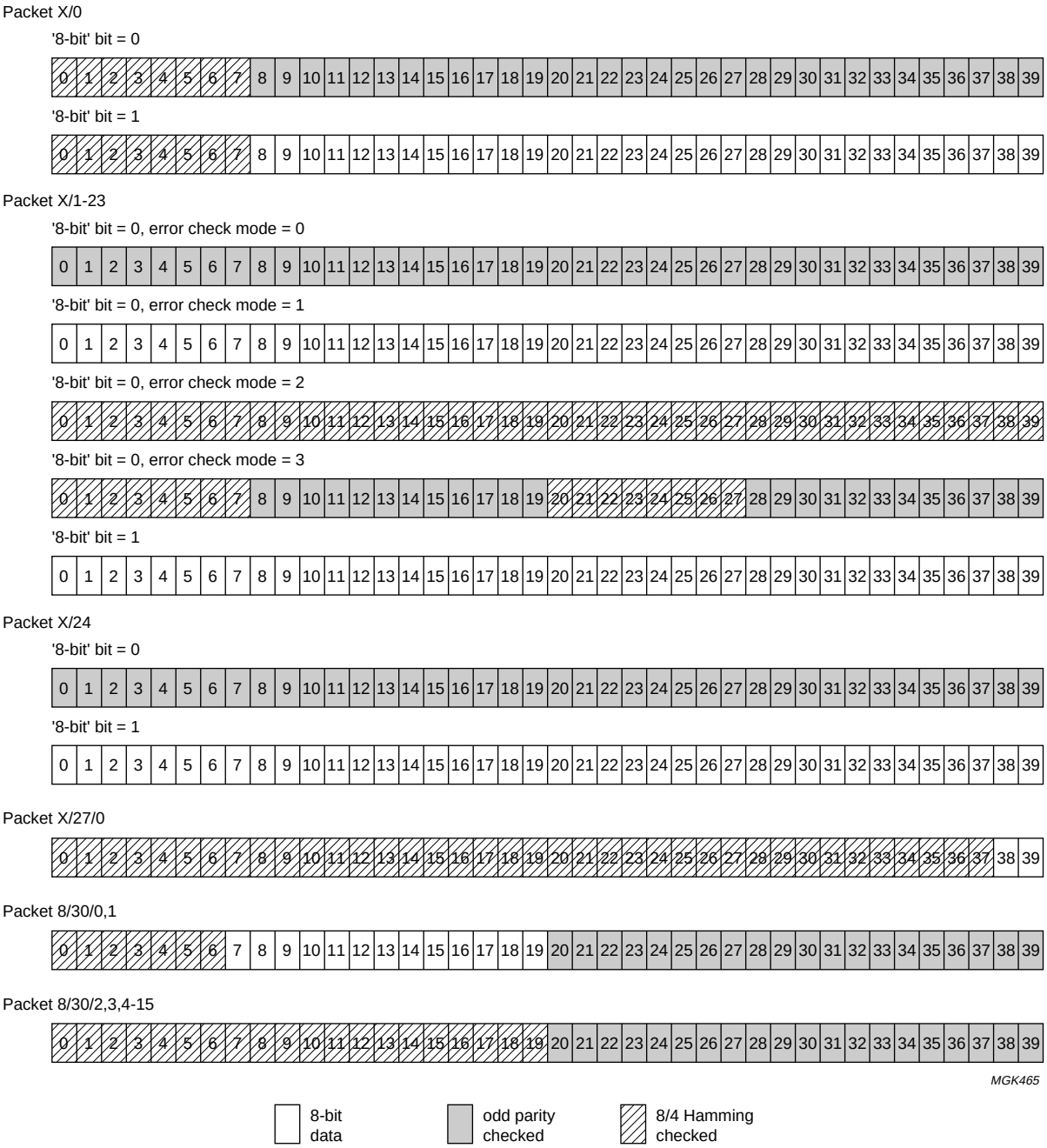


Fig.5 Error checking.

8.6 Memory organisation of SAA5296/7, SAA5296/7A and SAA5496/7

The teletext memory is divided into 10 blocks. Normally, when the TXT1.EXT PKT OFF bit is logic 0, each of blocks 0 to 8 contains a teletext page arranged in the same way as the basic page memory (see Fig.6) of the page device and block 9 contains extension packets (see Fig.7).

When the TXT1.EXT PKT OFF bit is logic 1, no extension packets are captured and block 9 of the memory is used to store another page.

The number of the memory block into which a page is written corresponds to the page request number which resulted in the capture of the page.

Packet 0, the page header, is split into 2 parts when it is written into the text memory. The first 8 bytes of the header contain control and addressing information. They are Hamming decoded and written into columns 0 to 7 of row 25 (see Table 15). Row 25 also contains the magazine number of the acquired page and the PBLF flag but the last 14 bytes are unused and may be used by the software, if necessary. The Hamming error flags are set if the on-board 8/4 Hamming checker detects that there has been an uncorrectable (2 bit) error in the associated byte.

It is possible for the page to still be acquired if some of the page address information contains uncorrectable errors if that part of the page request was a ‘don’t care’. There is no error flag for the magazine number as an uncorrectable error in this information prevents the page being acquired.

The interrupted sequence (C9) bit is automatically dealt with by the acquisition section so that rolling headers do not contain discontinuities in the page number sequence.

The magazine serial (C11) bit indicates whether the transmission is a serial or a parallel magazine transmission. This affects the way the acquisition section operates and is dealt with automatically.

The newsflash (C5), subtitle (C6), suppress header (C7), inhibit display (C10) and language control (C12 to 14) bits are dealt with automatically by the display section, described below.

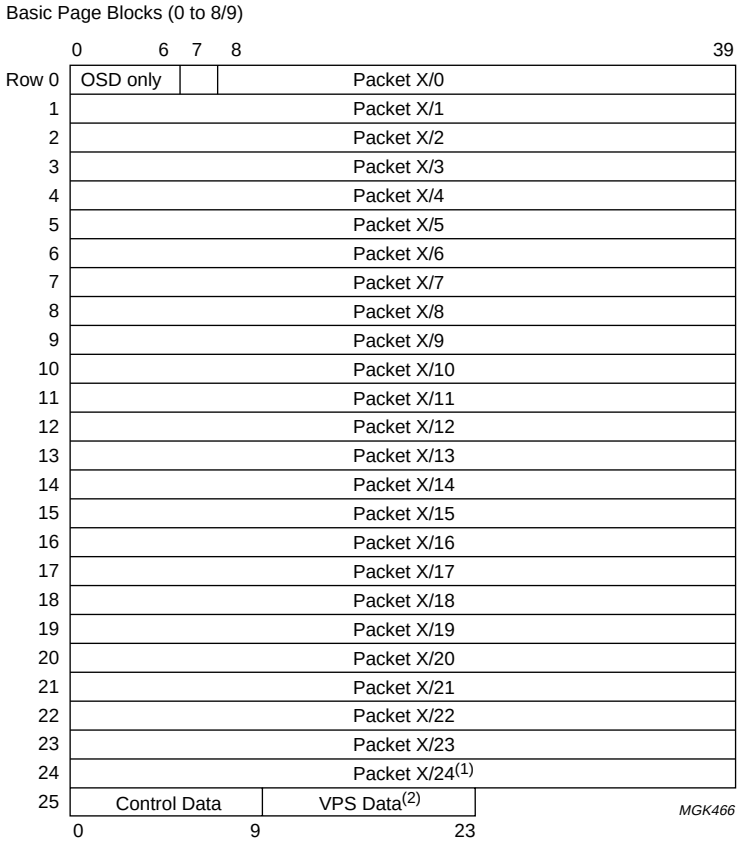
The update (C8) bit has no effect on the hardware. The remaining 32 bytes of the page header are parity checked and written into columns 8 to 39 of row 0. Bytes which pass the parity check have the MSB set to a logic 0 and are written into the page memory. Bytes with parity errors are not written into the memory.

Table 14 Notation used in Table 15

MNEMONIC	DESCRIPTION
MAG	Magazine
PT	Page Tens
PU	Page Units
HT	Hours Tens
HU	Hours Units
MT	Minutes Tens
MU	Minutes Units

Table 15 The data in row 25 of the basic page memory

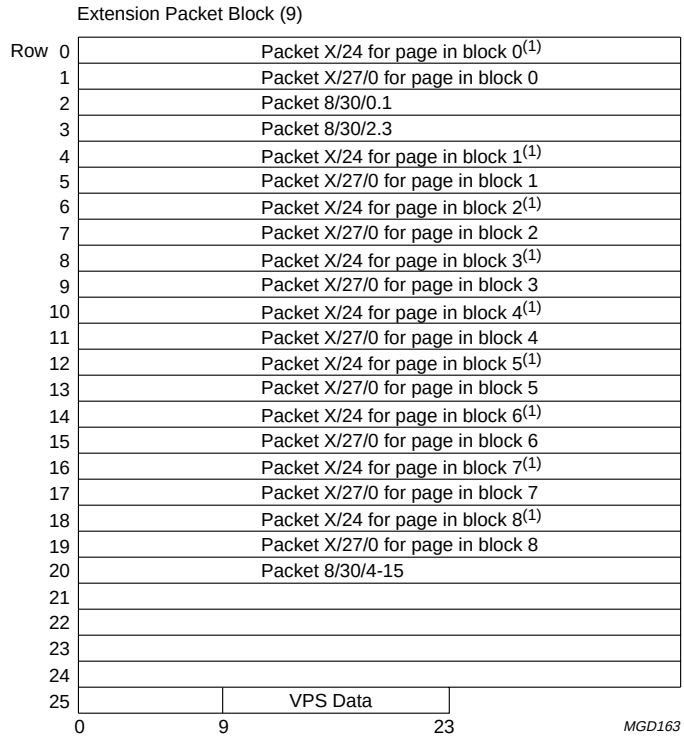
COL	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	Hamming error	PU3	PU2	PU1	PU0
1	0	0	0	Hamming error	PT3	PT2	PT1	PT0
2	0	0	0	Hamming error	MU3	MU2	MU1	MU0
3	0	0	0	Hamming error	C4	MT2	MT1	MT0
4	0	0	0	Hamming error	HU3	HU2	HU1	HU0
5	0	0	0	Hamming error	C6	C5	HT1	HT0
6	0	0	0	Hamming error	C10	C9	C8	C7
7	0	0	0	Hamming error	C14	C13	C12	C11
8	0	0	0	$\overline{\text{FOUND}}$	0	MAG2	MAG1	MAG0
9	0	0	PBLF	0	0	0	0	0
10 to 23	–	–	–	unused	–	–	–	–



(1) If ‘X24 Posn’ bit = 1.

(2) VPS data block 9, unused in blocks 0 to 8.

Fig.6 Packet storage locations.



(1) If ‘X24 Position’ bit = 0.

Fig.7 Extension packet storage locations.

8.7 Inventory page

If the TXT0.INV ON bit is a logic 1, memory block 8 is used as an inventory page.The inventory page consists of two tables: the Transmitted Page Table (TPT) and the Subtitle Page Table (SPT).

In each table, every possible combination of the page tens and units digit, 00H to FFH, is represented by a byte. Each bit of these bytes corresponds to a magazine number so each page number, from 100 to 8FF, is represented by a bit in the table.

The bit for a particular page in the TPT is set when a page header is received for that page. The bit in the SPT is set when a page header for the page is received which has the ‘subtitle’ page header control bit (C6) set.

Before the inventory page is enabled the software must ensure that page request 8 is put on hold.

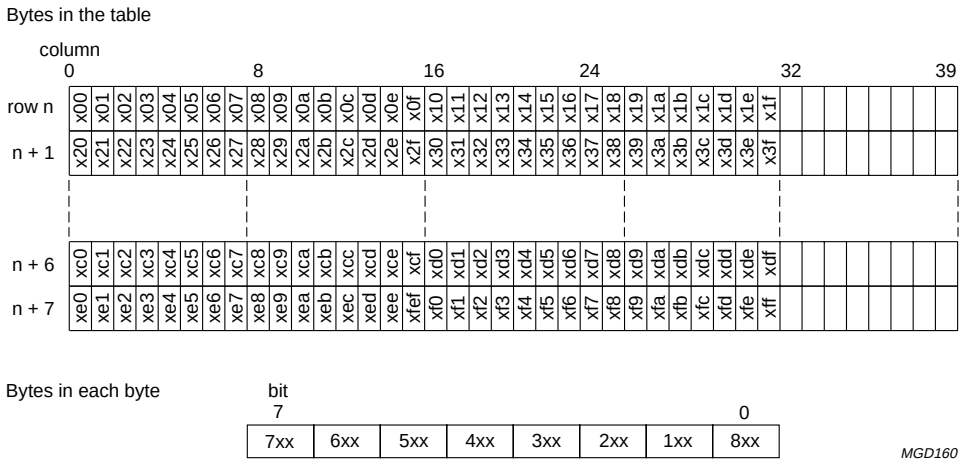


Fig.8 Table organisation.

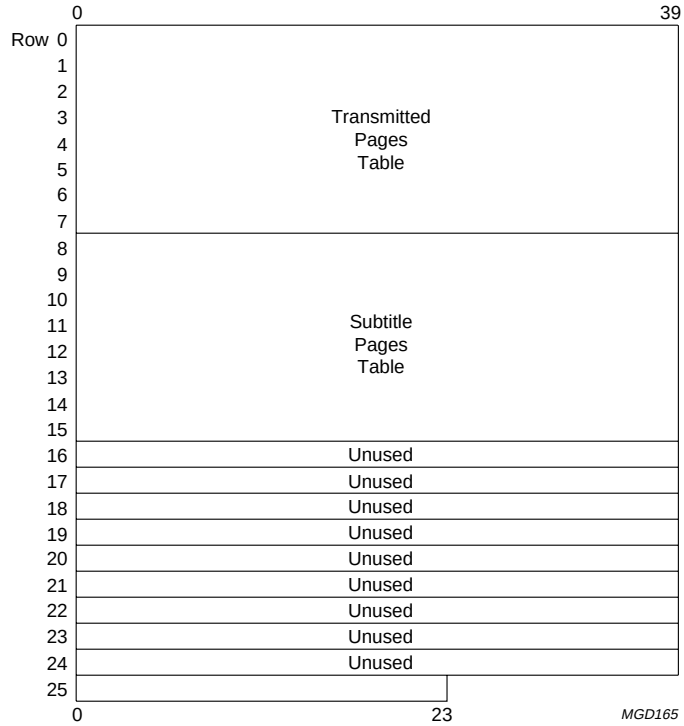
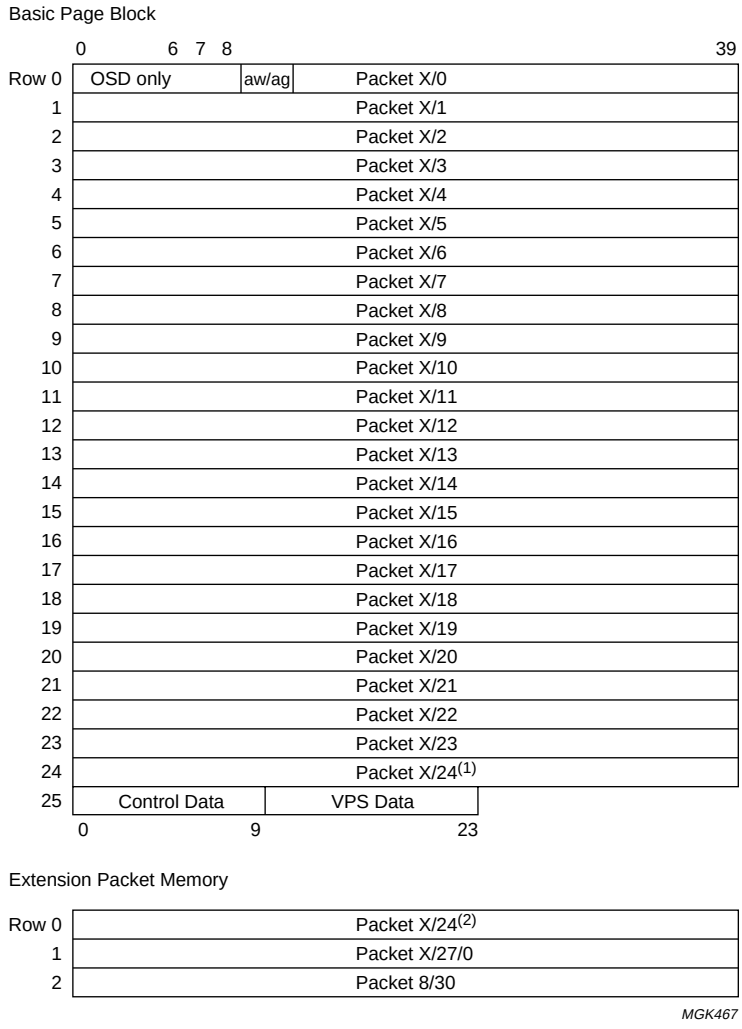


Fig.9 Inventory page organisation.

8.8 Memory Organisation of SAA5290, SAA5291, SAA5291A and SAA5491

Teletext packets each contain 40 bytes of data and one packet is stored in each row of the text memory, the row used being dependent on the packet number.

Packet 0, the page header, is split into 2 parts when it is written into the text memory. The first 8 bytes of the header contain control and addressing information. They are Hamming decoded and written into columns 0 to 7 of row 25.



(1) If X24 Position bit = 1.

(2) If X24 Position bit = 0.

Fig.10 Packet storage locations.

8.9 Packet 26 processing

One of the uses of packet 26 is to transmit characters which are not in the basic teletext character set. The family automatically decodes packet 26 data and, if a character corresponding to that being transmitted is available in the character set, automatically writes the appropriate character code into the correct location in the teletext memory. This is not a full implementation of the packet 26 specification allowed for in level 2 teletext, and so is often referred to as level 1.5.

By convention, the packets 26 for a page are transmitted before the normal packets. To prevent the default character data overwriting the packet 26 data the device incorporates a mechanism which prevents packet 26 data from being overwritten. On the SAA5291,SAA5291A and SAA5491 devices this mechanism is disabled when the Spanish national option is detected as the Spanish transmission system sends even parity (i.e. incorrect) characters in the basic page locations corresponding to the characters sent via packet 26 and these will not overwrite the packet 26 characters anyway. The special treatment of Spanish national option is prevented if TXT12.ROM VER R4 is logic 0 or if the TXT8.DISABLE SPANISH is set.

Packet 26 data is processed regardless of the TXT1.EXT PKT OFF bit, but setting theTXT1.X26 OFF disables packet 26 processing.

The TXT8.Pkt 26 received bit is set by the hardware whenever a character is written into the page memory by the packet 26 decoding hardware. The flag can be reset by writing a logic 0 into the SFR bit.

8.10 VPS

When the TXT0. VPS ON bit is set, any VPS data present on line 16, field 0 of the CVBS signal at the input of the teletext decoder is error checked and stored in row 25, block 0 for SAA5291, SAA5291A, SAA5491 and row 25, block 9 for SAA5296/7, SAA5296/7A, SAA5496/7 of the basic page memory. The device automatically detects whether teletext or VPS is being transmitted on this line and decodes the data appropriately.

Each VPS byte in the memory consists of 4 bi-phase decoded data bits (bits 0 to 3), a bi-phase error flag (bit 4) and three 0s (bits 5 to 7).

The TXT13.VPS Received bit is set by the hardware whenever VPS data is acquired. The flag can be reset by writing a logic 0 into the SFR bit. Full details of the VPS system can be found in *“Specification of the Domestic Video Programme Delivery Control System (PDC); EBU Tech. 3262-E”*.

Table 16 VPS data storage

ROW	COLUMN							
	0 TO 9	**10 TO 11**	**12 TO 13**	**14 TO 15**	**16 TO 17**	**18 TO 19**	**20 TO 21**	**22 TO 23**
Row 25	Teletext page header data	VPS byte 11	VPS byte 12	VPS byte 13	VPS byte 14	VPS byte 15	VPS byte 4	VPS byte 5

8.11 Wide Screen Signalling (SAA529xA and SAA549x only)

The Wide Screen Signalling data transmitted on line 23 gives information on the aspect ratio and display position of the transmitted picture, the position of subtitles and on the camera/film mode. Some additional bits are reserved for future use. A total of 14 data bits are transmitted.

All of the available data bits transmitted by the Wide Screen Signalling signal are captured by the appropriate device in the family and stored in SFRs WSS1, WSS2 and WSS3. The bits are stored as groups of related bits and an error flag is provided for each group to indicate when a transmission error has been detected in one or more of the bits in the group.

Wide screen signalling data is only acquired when the TXT8.WSS ON bit is set.

The TXT8.WSS RECEIVED bit is set by the hardware whenever wide screen signalling data is acquired. The flag can be reset by writing a logic 0 into the SFR bit.

8.12 525-line world system teletext

As well as the 625-line teletext format described previously, the family can acquire teletext in the 525-line WST (World System Teletext) format.

The 525-line format is similar to the 625-line format but the data rate is lower and there are less data bytes per packet (32 rather than 40). There are still 40 characters per display row so extra packets are sent each of which contains the last 8 characters for four rows. These packets can be identified by looking at the ‘tabulation bit’ (T), which replaces one of the magazine bits in 525-line teletext. When an ordinary packet with T = 1 is received, the decoder puts the data into the four rows starting with that corresponding to the packet number, but with the 2 LSB’s set to logic 0. For example, a packet 9 with T = 1 (packet X/1/9) contains data for rows 8, 9, 10 and 11. The error checking carried out on data from packets with T = 1 depends on the setting of the TXT1. 8 BIT bit and the error checking control bits in the page request data and is the same as that applied to the data written into the same memory location in the 625-line format.

The rolling time display (the last 8 characters in row 0) is taken from any packets X/1/1, 2 or 3 received. In parallel magazine mode only packets in the correct magazine are used for rolling time. Packet number X/1/0 is ignored.

The tabulation bit is also used with extension packets.

The first 8 data bytes of packet X/1/24 are used to extend the Fastext prompt row to 40 characters. These characters are written into whichever part of the memory the packet 24 is being written into (determined by the ‘X24 Posn’ bit).

Packets X/0/27/0 contain 5 Fastext page links and the link control byte and are captured, Hamming checked and stored by in the same way as are packets X/27/0 in 625-line text. Packets X/1/27/0 are not captured.

Because there are only 2 magazine bits in 525-line text, packets with the magazine bits all set to a logic 0 are referred to as being in magazine 4. Therefore, the broadcast service data packet is packet 4/30, rather than packet 8/30. As in 625 line text, the first 20 bytes of packet 4/30 contain encoded data which is decoded in the same way as that in packet 8/30. The last 12 bytes of the packet contains half of the parity encoded status message. Packet 4/0/30 contains the first half of the message and packet 4/1/30 contains the second half. The last 4 bytes of the message are not written into memory. The first 20 bytes of the each version of the packet are the same so they are stored whenever either version of the packet is acquired.

In 525-line text each packet 26 only contains ten 24/18 Hamming encoded data triplets, rather than the 13 found in 625-line text. The tabulation bit is used as an extra bit (the MSB) of the designation code, allowing 32 packet 26s to be transmitted for each page. The last byte of each packet 26 is ignored.

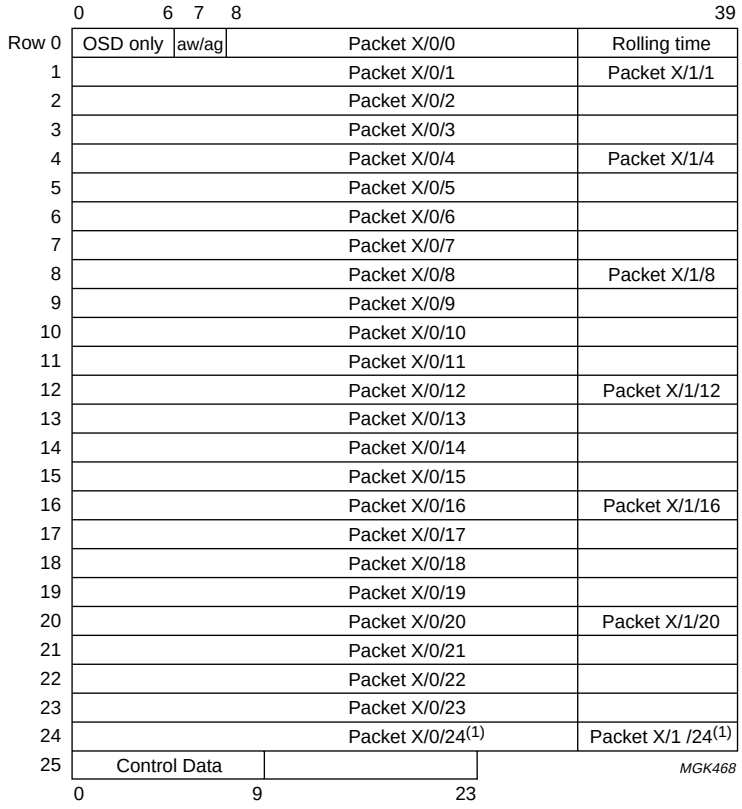
The device automatically detects whether 525 or 625-line teletext is being received by checking whether teletext packets are being recognised, and switching to the other system if they aren’t.

The TXT13.625 TXT bit is set if the device has decided, using the algorithm above, that 625-line text is being received. The TXT13.525 Text bit is set if the device has decided that 525-line text is being received. If the device has not decided which type of text is being received then neither flag is set.

The ‘FORCE ACQ0’ and ‘FORCE ACQ1’ bits in TXT17 can be used to override the automatic detection and selection mechanism; see Table 17.

Table 17 Acquisition selection table

FORCE ACQ1	FORCE ACQ0	TIMING	TELETEXT STANDARD
0	0	automatic	automatic
0	1	525-line	525-line
1	0	625-line	625-line
1	1	625-line	525-line



(1) If X24 Position bit = 1.

Fig.11 Ordinary packet storage locations, 525-line.

8.13 Fastext detection

When a packet 27, designation code 0 is detected, whether or not it is acquired, the TXT13.FASTEXT bit is set. If the device is receiving 525-line teletext, a packet X/0/27/0 is required to set the flag. The flag can be reset by writing a logic 0 into the SFR bit.

When a packet 8/30 is detected, or a packet 4/30 when the device is receiving a 525-line transmission, the TXT13.Pkt 8/30 is set. The flag can be reset by writing a logic 0 into the SFR bit.

8.14 Page clearing

When a page header is acquired for the first time after a new page request or a page header is acquired with the erase (C4) bit set the page memory is ‘cleared’ to spaces before the rest of the page arrives.

When this occurs, the space code (20H) is written into every location of rows 1 to 23 of the basic page memory, row 1 of the extension packet memory and the row where teletext packet 24 is written. This last row is either row 24 of the basic page memory, if the TXT0.X24 POSN bit is set, or row 0 of the extension packet memory, if the bit is not set. Page clearing takes place before the end of the TV line in which the header arrived which initiated the page clear. This means that the 1 field gap between the page header and the rest of the page which is necessary for many teletext decoders is not required.

The software can also initiate a page clear, by setting the TXT9.CLEAR MEMORY bit. When it does so, every location in the memory is cleared. The CLEAR MEMORY bit is not latched so the software does not have to reset it after it has been set.

Only one page can be cleared in a TV line so if the software requests a page clear it will be carried out on the next TV line on which the hardware does not force the page to be cleared. A flag, TXT13.PAGE CLEARING, is provided to indicate that a software requested page clear is being carried out. The flag is set when a logic 1 is written into the TXT9.CLEAR MEMORY bit and is reset when the page clear has been completed.

At power-on and reset the whole of the page memory is cleared and theTXT13.PAGE CLEARING bit will be set.

8.15 Full channel operation

If the TXT1.FULL FIELD bit is set the device will acquire data transmitted on any TV line, not just during the vertical blanking interval.

This allows the device to be used with teletext transmissions occupying the entire TV channel and with data extracted from different TV broadcast standards (e.g.: MAC packet teletext).

8.16 Independent data services (SAA5291, SAA5291A, SAA5491 only)

When the TXT8.IDS ENABLE bit is set, SAA5291 becomes a receiver for teletext ‘Independent Data Services’. These services use teletext packet numbers 30 and 31 to transmit data from a central database to a large number of distributed receivers.

Unlike normal teletext data, IDS data is not organised into pages but into ‘data channels’.

There are 16 data channels, identified by the magazine number and the LSB of the packet number (actually, the second byte of the magazine and packet number group). Data channel 0 is the familiar packet 8/30, used to transmit broadcast related information.

The data channel to be captured by the device is selected by writing to column 0 of the page request RAM.

Only IDS packets from the selected data channel are captured and rows 0 to 23 of the basic page memory are used to store the last 24 packets acquired. The first IDS packet acquired after theTXT8.IDS ENABLE bit is set is written into row 0, the next into row 1 and so on until 24 packets have been acquired. The internal packet counter then rolls over and the 25th packet is written into row 0. The hardware never initiates a page clear in IDS mode but if the software initiates one the packet counter is reset to 0 after the memory is cleared.

The data bytes in the IDS packers are not error checked in any way.

The software must keep track of which of the IDS packets in the memory it has processed and detect newly arrived packets. It can do this by writing a value which cannot be produced by the 8/4 Hamming checker (such as FFH) into column 0 of each row and detecting when it is over written.

The 24 packet buffer is sufficient to ensure that the device will not be overwhelmed by IDS data sent in the vertical blanking interval, but it may not be able to cope with full channel IDS data.

IDS data is dealt with in the same way for both the 525 and 625-line teletext standards.

Table 18 Page request RAM for IDS data

COL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	X	X	X	X	Data Ch 3	Data Ch 2	Data Ch 1	Data Ch 0
1 to 7	X	X	X	X	X	X	X	X

9 THE DISPLAY

9.1 Introduction

The capabilities of the display are based on the requirements of level 1 teletext, with some enhancements for use with locally generated on screen displays.

The display consists of 25 rows each of 40 characters, with the characters displayed being those from rows 0 to 24 of the basic page memory. If the TXT7.STATUS ROW TOP bit is set row 24 is displayed at the top of the screen, followed by row 0, but normally memory rows are displayed in numerical order.

The teletext memory stores 8 bit character codes which correspond to a number of displayable characters and control characters, which are normally displayed as spaces. The character set of the device is described in more detail below.

9.2 Character matrix

Each character is defined by a matrix 12 pixels wide and 10 pixels high. When displayed, each pixel is $^1/_{12}$ µs wide and 1 TV line, in each field, high.

9.3 East/$\overline{\text{West}}$ selection

In common with their predecessors, these devices store teletext pages as a series of 8 bit character codes which are interpreted as either control codes (to change colour, invoke flashing etc.) or displayable characters. When the control characters are excluded, this gives an addressable set of 212 characters at any given time.

More characters than this were required to give the language coverage required from the first version of the device, so the TXT4.East/$\overline{\text{West}}$ bit was introduced to allow the meanings of character codes D0H to FFH to be changed, depending on where in Europe the device was to be used.

This bit is still used with the other language variants, although the name East/$\overline{\text{West}}$ may not make much sense.

9.4 National option characters

The meanings of some character codes between 20H and 7FH depend on the C12 to C14 language control bits from the teletext page header.

The interpretation of the C12 to C14 language control bits is dependent on the East/$\overline{\text{West}}$ bit.

9.5 The twist attribute

In many of the character sets, the ‘twist’ serial attribute (code 1BH) can be used to switch to an alternate basic character code table, e.g. to change from the Hebrew alphabet to the Arabic alphabet on an Arab/Hebrew device. For some national option languages the alternate code table is the default, and a twist control character will switch to the first code table.

The display hardware on the devices allows one language to invoke the alternate code table by default when the East/$\overline{\text{West}}$ register bit is a logic 0 and another when the bit is a logic 1. In all of the character sets defined so far, the language which invokes the alternate code table is the same for either setting of the East/$\overline{\text{West}}$ bit.

9.6 On Screen Display symbols

In the character sets character codes 80H to 9FH are OSD symbols not addressed by the teletext decoding hardware. An editor is available to allow these characters to be redefined by the customer.

The SAA549x allows another 32 OSD symbols. These are selected using the ‘graphics’ serial attribute.

9.7 Language group identification

The devices have a readable register TXT12 which contains a 5 bit identification code TXT12.ROM VER R4 to TXT12.ROM VER R0 which is intended for use in identifying which character set the device is using.

9.8 525-line operation

When used with 525-line display syncs, the devices modify their displays such that the bottom line is omitted from each character cell. The character sets have been designed to be readable under these circumstances and anyone designing OSD symbols is advised to consider this mode of operation.

9.9 On Screen Display characters

Character codes 80H to 9FH are not addressed by the hardware and can be redefined by the customer, as OSD characters if necessary.

The alternative character shapes in columns 8a and 9a (SAA549x only) can be displayed when the ‘graphics’ serial attribute is set. This increases the number of customer definable characters to 64.

To ensure compatibility with devices only having 32 OSD characters, the additional OSD characters are only accessible when the TXT4.OSD BANK ENABLE bit is set. If this bit is not set, the characters in columns 8 and 9 will be displayed in both alphanumeric and graphics modes.

9.10 Control characters

Character codes 00H to 1FH, B0H to B7H and BCH to BFH are interpreted as control characters which can be used to change the colour of the characters, the background colour, the size of characters, and various other features. All control characters are normally displayed as spaces.

The alphanumerical colour control characters (00H to 07H) are used to change colour of the characters displayed.

The graphics control characters (10H to 17H) change the colour of the characters and switch the display into a mode where the codes in columns 2, 3, 6 and 7 of the character table (see the character table above) are displayed as the block mosaic characters in columns 2a, 3a, 6a and 7a. The display of mosaics is switched off using one of the alphanumerics colour control characters.

The ‘new background’ character (1DH) the background colour of the display, sets the background colour equal to the current foreground colour. The ‘black background’ character (1CH) changes the background colour to black independently of the current foreground colour. The background colour control characters in the upper half of the code table (B0H to B7H) are additions to the normal teletext control characters which allow the background colour to be changed to any colour with a single control character and independently of the foreground colour. The background colour is changed from the position of the background colour control character.

Displayable characters between a ‘flash’ (08H) and a ‘steady’ (09H) control character will flash on and off.

Displayable characters between a ‘conceal display’ (18H) character and an alphanumerics or graphics control character are displayed as spaces, unless the TXT7.REVEAL bit is set.

The ‘contiguous graphics’ (19H) and ‘separated graphics’ (1AH) characters control the way in which mosaic shapes are displayed. The difference between the two is shown in Fig.12.

Control characters encountered between a ‘hold graphics’ (1EH) control character and a ‘release graphics’ (1FH) control character are displayed as the last character displayed in graphics mode, rather than as spaces. From the hold graphics character until the first character displayed in graphics mode the held character is a space.

The ‘start box’ (0BH) and ‘end box’ (0AH) characters are used to define teletext boxes. Two start box characters are required to begin a teletext box, with the box starting between the 2 characters. The box ends after an end box character has been encountered. The display can be set up so that different display modes are invoked inside and outside teletext boxes e.g. text inside boxes but TV outside. This is described in Section 9.13.

The ‘normal size’ (0CH), ‘double height’ (0DH), ‘double width’ (0EH) and ‘double size’ (0FH) control characters are used to change the size of the characters displayed. If any double height (or double size) characters are displayed on a row the whole of the next row is displayed as spaces. Double height display is not possible on either row 23 or row 24.

The character in the position occupied by the right hand half of a double width (or double size) character is ignored, unless it is a control character in which case it takes effect on the next character displayed. This allows double width to be used to produce a display in which blank spaces do not appear when character attributes are changed.

The size implying OSD (BCH to BFH) control characters are not standard teletext control characters and have been included in this device to allow OSD messages to be generated with the minimum disruption to the teletext page stored in the memory. These characters are described in full later in this document.

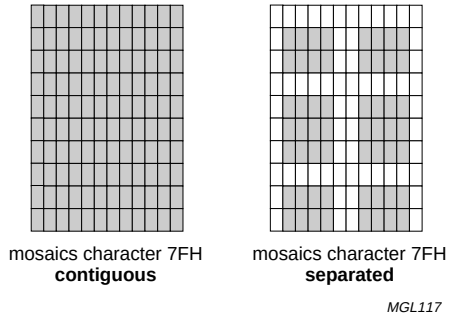


Fig.12 Contiguous and separated mosaics.

9.11 Quadruple width display (SAA549x)

Two successive double width control characters will invoke quadruple width display. Quad width display is terminated by another size control character.

Any combination of two of the four controls which invoke double width display (double width, double size, double width OSD and double size OSD) can invoke quad width display. If a double size control character is part of the sequence, characters will be displayed in quad width and double height.

To ensure that broadcast teletext pages can be displayed correctly, quadruple width will only be displayed if the TXT4.QUAD WIDTH ENABLE bit is set. If this bit is not set, two successive double width characters will invoke double width display.

If quadruple width characters are to be used within OSD boxes (see later section) then the first of the width characters must be either ‘double width’ (OEH) or ‘double size’ (OFH).

This is because if two consecutive size implying OSD control characters are used, the first starts the OSD box and the second finishes the OSD box, and therefore no OSD box is defined.

Quadruple width characters must not start in columns 37, 38 or 39 of the display since the whole of the character cannot be displayed.

9.12 Page attributes

Row 25 of the basic page memory contains control data from the page header of the page stored in the memory. The bits which affect the display are the newsflash (C5), subtitle (C6), suppress header (C7), inhibit display (C10) and language control (C12 to 14) bits.

If either the newsflash or the subtitle bit is set a different SFR is used to define the display mode, as described in Section 9.13.

The suppress header bit causes the header row (row 0) to be displayed as if every character was a space and the inhibit display bit has this effect on every display row.

The language control bits cause certain character codes to be interpreted differently, as described above.

9.13 Display modes

The device signals the TVs display circuits to display the R, G and B outputs of the device, rather than the video picture, by outputting a logic 1 on the VDS output. The way in which this signal is switched is controlled by the bits in the TXT5 and TXT6 SFRs. There are 3 control functions - text on, background on and picture on. Separate sets of bits are used inside and outside teletext boxes so that different display modes can be invoked. Also, different SFRs are used depending on whether the newsflash (C5) or subtitle (C6) bits in row 25 of the basic page memory are set (SFR TXT6) or not (SFR TXT5). This allows the software to set up the type of display required on newsflash and subtitle pages (e.g. text inside boxes, TV picture outside) this will be invoked without any further software intervention when such a page is acquired.

When teletext box control characters are present in the page memory, whichever is relevant of the ‘Boxes On Row 0’, ‘Boxes On Row 1 to 23’ and ‘Boxes On Row 24’ SFR bits in TXT17 must be set if the display mode is to change in the box. These bits are present to allow boxes in certain areas of the screen to be disabled so that teletext boxes can be used for the display of OSD messages without the danger of subtitles in boxes, which may also be in the page memory, being displayed. The use of teletext boxes for OSD messages has been superseded in this device by the OSD box concept, described later, but these bits remain to allow teletext boxes to be used, if required.

The $\overline{\text{COR}}$ bits in the TXT5 and TXT6 SFRs control when the $\overline{\text{COR}}$ output of the device is activated (i.e. pulled down). This output is intended to act on the TV’s display circuits to reduce the contrast of the video display when it is active. The result of contrast reduction is to improve the readability of the text in a mixed text and video display.

The bits in the TXT5 and TXT6 SFRs allow the display to be set up so that, for example, the areas inside teletext boxes will be contrast reduced when a subtitle is being displayed but that the rest of the screen will be displayed as normal video.

Setting the shadow TXT4.SHADOW ENABLE bit will add a ‘south east’ shadow to the text, significantly enhancing its readability in mix mode. Shadowing is illustrated in Fig.13.

The readability of text can also be enhanced using ‘meshing’. Meshing causes the VDS signal to switch so that when the text background colour should be displayed every other pixel is displayed from the video picture. Text foreground pixels are always displayed.

The TXT4.BMESH bit enables meshing on areas of the screen within the text display area with black as the background colour. The TXT4.CMESH bit has the same effect on areas with other background colours. Meshing can only be invoked in areas displayed in text mode i.e. where the TXT5.TEXT IN and TXT5.BKGND IN bits are both set to logic 1s, and in OSD boxes. Meshed text can also be shadowed. Meshing is illustrated in Fig.13.

The TXT4.TRANS bit causes areas of black background colour to become transparent i.e. video is displayed instead of black background. Black background transparency can also only be invoked in areas displayed in text mode i.e. where the TXT5.TEXT IN and TXT5.BKGND IN bits are both set to a logic 1, and in OSD boxes.

Table 19 Display control bits

PICTURE ON	TEXT ON	BACKGROUND ON	EFFECT
0	0	X	text mode, black screen
0	1	0	text mode, background always black
0	1	1	text mode
1	0	X	TV mode
1	1	0	mixed text and TV mode
1	1	1	text mode, TV picture outside text area

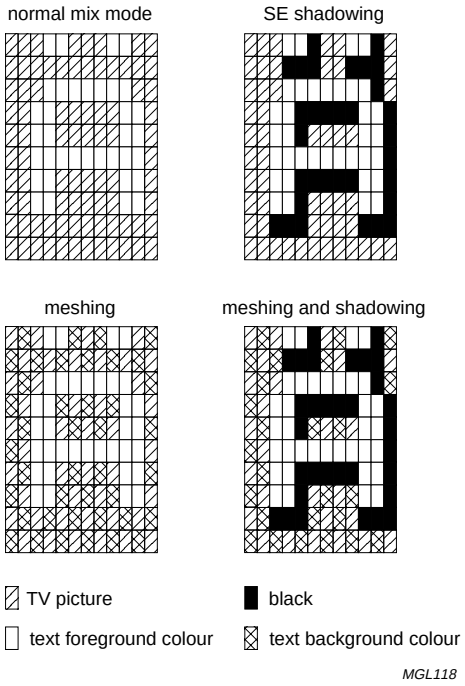


Fig.13 Meshing and shadowing.

Table 20 Enhanced display mode selection

SHADOW	TRANS	BMESH	CMESH	DISPLAY
0	0	0	0	normal, unshadowed, unmeshed text
0	0	0	1	text with coloured backgrounds meshed, black background solid
0	0	1	0	text with coloured backgrounds solid, black background meshed
0	0	1	1	text with all backgrounds meshed
0	1	X	0	text with coloured backgrounds solid, black background transparent
0	1	X	1	text with coloured backgrounds meshed, black background transparent
1	0	0	1	shadowed text with coloured backgrounds meshed, black background solid
1	0	1	0	shadowed text with coloured backgrounds solid, black background meshed
1	0	1	1	shadowed text with all backgrounds meshed
1	1	X	0	shadowed text with coloured backgrounds solid, black background transparent
1	1	X	1	shadowed text with coloured backgrounds meshed, black background transparent

9.14 On Screen Display boxes

The size implying OSD control characters (BCH to BFH) are intended to allow OSD messages to be displayed with the minimum disruption to the teletext page stored in the page memory. OSD boxes are not the same as teletext boxes created using the teletext boxing control characters (0AH and 0BH).

When one of these characters occurs the display size changes appropriately (to normal size for BCH, double height for BDH, double width for BEH and double size for BFH) and an OSD box starts from the next character position (‘set after’). The OSD box ends either at the end of the row of text or at the next size implying OSD character. When an OSD box is ended using another size implying OSD character the box ends at the position of the control character (‘set at’). This arrangement allows displays to be created without blank spaces at the ends of the OSD boxes.

To prevent control characters from the teletext page affecting the display of the OSD message the flash, teletext box, conceal, separated graphics, twist and hold graphics functions are all reset at the start of an OSD box, as they are at the start of the row. In order to allow the most commonly used display attributes to be set up before the box starts the foreground colour, background colour and mosaics on/off attributes are not reset.

The text within an OSD box is always displayed in text mode i.e. as if the Text On and Bkgnd On bits are both set to a logic 1. The type of display produced inside an OSD box is, therefore, dependent on the states of the TXT4.SHADOW ENABLE, TXT4.TRANS ENABLE, TXT4.BMESH ENABLE and TXT4.CMESH ENABLE register bits, as described previously. OSD boxes can only be displayed in TV mode i.e. when the Picture On SFR bit is a logic 1 and the Text On SFR bit is a logic 0, both inside and outside text boxes and for both normal and newsflash/subtitle pages.

The display of OSD boxes is not affected by the C7, suppress header, and C10, inhibit display, control bits stored in row 25 of the page memory.

9.15 Screen colour

The register bits TXT17.SCREEN COL2 to COL0 can be used to define a colour to be displayed in place of TV picture and the black background colour. If the bits are all set to logic 0s, the screen colour is defined as ‘transparent’ and the TV picture and background colour are displayed as normal.

Screen colour is displayed from 10.5 to 62.5 μs after the active edge of the HSync input and on TV lines 23 to 310 inclusive, for a 625-line display, and lines 17 to 260 inclusive for a 525-line display.

When the screen colour has been redefined, no TV picture is displayed so the FRAME de-interlace output can be activated, if the SFR bits controlling FRAME are set up to allow this.

Table 21 Screen colours

SCREEN COL 2	SCREEN COL 1	SCREEN COL 0	SCREEN COLOUR
0	0	0	transparent
0	0	1	red
0	1	0	green
0	1	1	yellow
1	0	0	blue
1	0	1	magenta
1	1	0	cyan
1	1	1	white

9.16 Redefinable Colours (SAA549x)

The CLUT SFR can be used to load a colour look-up table (CLUT) which allows the 8 foreground colours and 8 background colours to be redefined. Each entry has 6 bits, 2 for each colour component, giving a total palette of 64 colours from which to choose.

When the CLUT.CLUT ENABLE bit is a logic 0 the CLUT is disabled and the device will display the normal, full intensity, teletext colours.

The meaning of the least significant 6 bits of the CLUT SFR depends on the setting of the CLUT.CLUT ADDRESS bit when the register is written to. If the CLUT.CLUT ADDRESS bit is a logic 1, the 4 LSB’s of the SFR contain the address of the entry in the CLUT which will be modified by subsequent writes to the CLUT SFR. If the CLUT.CLUT ADDRESS bit is a logic 0, the 6 LSB’s of the SFR define a colour which will be written into the CLUT at the address defined by a previous write to the CLUT SFR. An entry is written into the CLUT whenever the CLUT SFR is written to, unless the CLUT.CLUT ADDRESS bit is set.

Table 22 shows which CLUT entry corresponds to which full intensity colour. The contents of the CLUT are not reset at power-up and should be defined by the software before the CLUT is enabled.

Table 22 CLUT Address

CLUT ADDRESS	FULL INTENSITY EQUIVALENT
0	black foreground
1	red foreground
2	green Foreground
3	yellow foreground
4	blue foreground
5	magenta foreground
6	cyan foreground
7	white foreground
8	black background
9	red background
A	green background
B	yellow background
C	blue background
D	magenta background
E	cyan background
F	white background

9.17 Cursor

If the TXT7.CURSOR ON bit is set, a cursor is displayed. The cursor operates by reversing the background and foreground colours in the character position pointed to by the active row and column bits in the TXT9 and TXT10 SFRs.

Setting the TXT9.CURSOR FREEZE bit, causes the cursor to stay in its current position, no matter what happens to the active row and column positions. This means that the software can read data from the memory (e.g. TOP table information) without affecting the position of the cursor.

9.18 Other display features

Setting the TXT7.DOUBLE HEIGHT bit causes the normal height of all display characters to be doubled and the whole of the display area to be occupied by half of the display rows. Characters normally displayed double height will be displayed quadruple height when this bit is set. Rows 12 to 24 can be enlarged, rather then rows 0 to 11, by setting the TXT7.$\overline{\text{TOP}}$/BOTTOM bit.

This feature can be used for either a user controlled ‘enlarge’ facility or to provide very large characters for OSD.

The display of rows 0 to 23 can be disabled by setting the TXT0.DISLAY STATUS ROW ONLY bit.

The Fastext prompt row (packet 24) can be displayed from the extension packet memory by setting the TXT0.DISPLAY X/24 bit. When this bit is set the data displayed on display row 24 is taken from row 0 in the extension packet memory.

When the display from extension packet block option is enabled, the display will revert to row 24 of the basic page memory if bit 3 of the link control byte in packet 27 is set.

9.19 Display timing

The display synchronises to the device’s HSync and VSync inputs. A typical configuration is shown in Fig.14.

The HSync and VSync signals are derived from the signals driving the deflection coils of the TV. The CVBS input is only used to extract teletext from. Locking the display to the signals from the scan circuits allows the device give a stable display under almost all signal conditions.

The polarity of the input signals which the device is expecting can be set using the TXT1.H polarity and TXT1.V polarity bits. If the polarity bit is a logic 0, a positive going signal is expected and if it is a logic 1, a negative going signal is expected.

9.20 Horizontal timing

Every time an HSync pulse is received the display resynchronizes to its leading edge. To get maximum display stability, the HSync input must have fast edges, free of noise to ensure that there is no uncertainty in the timing of the signal to which the display synchronisation circuits must lock.

The display area starts 17.2 µs into the line and lasts for 40 µs. The display area will be in the centre of the screen if the HSync pulse is aligned with line flyback signal. Therefore, it is better to derive HSync directly from the line flyback or from an output of the line output transformer than from, say, slicing the sandcastle signal as this would introduce delays which would shift the display to the right.

9.21 Vertical timing

The vertical display timing also resynchronizes to every sync pulse received. This means that the device can produce a stable display on both 625 and 525-line screens. Display starts on the 41st line of each field and continues for 250 lines, or until the end of the field.

Normally, television displays are interlaced, i.e. only every other TV line is displayed on each field. It is normal to de-interlace teletext displays to prevent the displayed characters flickering up and down. In many TV designs this

is achieved by modulating the vertical deflection current in such a way that odd fields are shifted up and even fields are shifted down on the screen so that lines 1 and 314, 2 and 315 etc. are overlaid. The FRAME output is provided to facilitate this.

If the active edge of Vsync occurs in the first half of a TV line this is an even field and the FRAME output should be a logic 0 for this field. Similarly, if VSync is in the second half of the line this is an odd field and FRAME should be a logic1. The algorithm used to derive Frame is such that a consistent output will be obtained no matter where the VSync signal is relative to the HSync signal, even if VSync occurs at the start and mid points of a line.

Setting the TXT0.DISABLE FRAME bit forces the FRAME output to a logic 0. Setting the TXT0.AUTO FRAME bit causes the FRAME output to be active when just text is being displayed but to be forced to a logic 0 when any video is being displayed. This allows the de-interlacing function to take place with virtually no software intervention.

Some TV architectures do not use the FRAME output but accomplish the de-interlacing function in the vertical deflection IC, under software control, by delaying the start of the scan for one field by half a line, so that lines in this field are moved up by one TV line. In such TVs, VSync may occur in the first half of the line at the start of an odd field and in the second half of the line at the start of an even field. In order to obtain correct de-interlacing in these circumstances, the TXT1.FIELD POLARITY must be set to reverse the assumptions made by the vertical timing circuits on the timing of VSync in each field. The start of the display may be delayed by a line. The ‘Field Polarity’ bit does not affect the FRAME output.

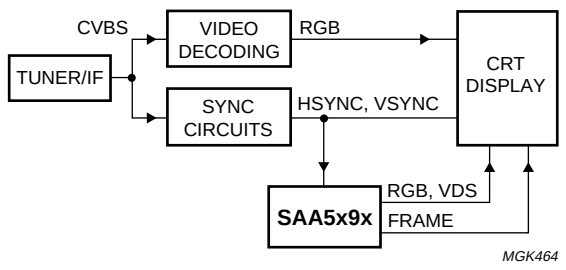


Fig.14 Timing configuration.

9.22 Display position

The position of the display relative to the HSync and VSync inputs can be varied over a limited range to allow for optimum TV set-up.

The horizontal position is controlled by the X0 and X1 bits in TXT16. Table 23 gives the time from the active edge of the HSync to the start of the display area for each setting of X0 and X1.

Table 23 Display horizontal position

X1	X0	Hsync TO DISPLAY (µs)
0	0	17.2
0	1	16.2
1	0	15.2
1	1	14.2

The line on which the display area starts depends on whether the display is 625-line or 525-line and on the setting of the Y0 to Y2 bits in TXT16. Table 24 gives the first display line for each setting of Y0 to Y2, for both 625 and 525-line display.

On the other field, the display starts on the equivalent line.

Table 24 Display vertical position

Y2	Y1	Y0	FIRST LINE FOR DISPLAY	
			625-LINE	525-LINE
0	0	0	42	28
0	0	1	44	30
0	1	0	46	32
0	1	1	48	34
1	0	0	34	20
1	0	1	36	22
1	1	0	38	24
1	1	1	40	26

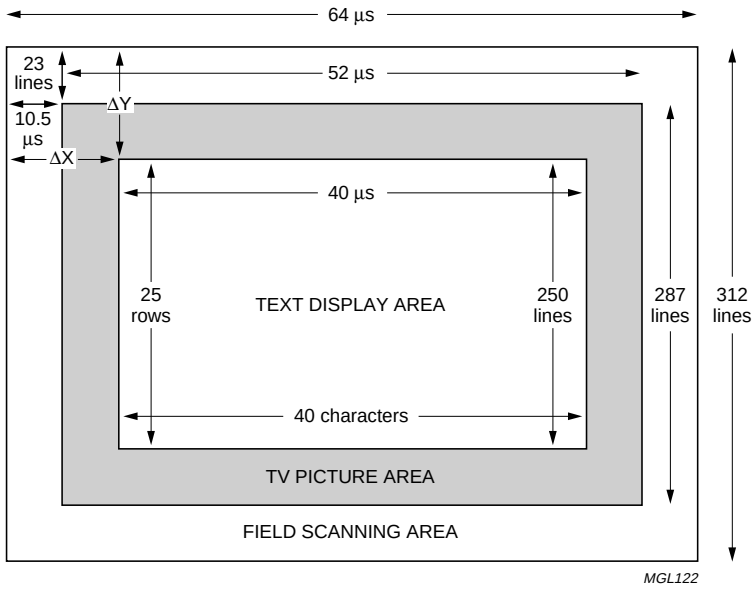


Fig.15 625-line display format.

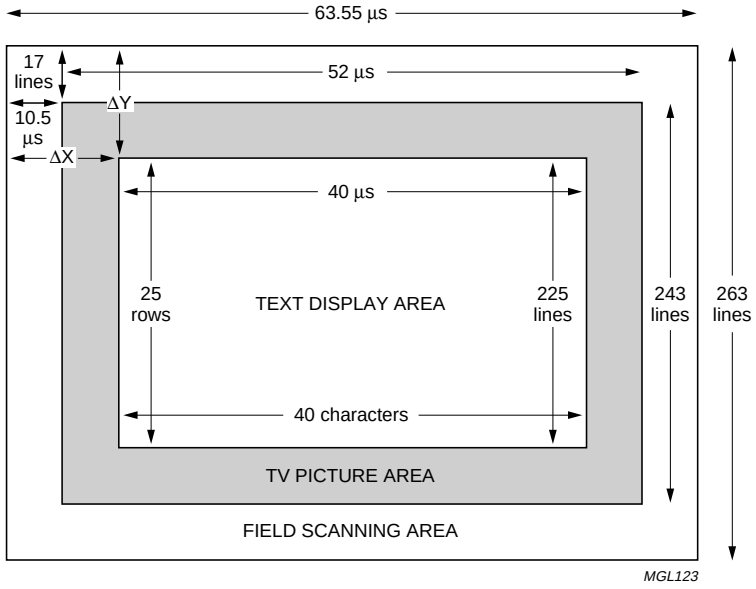
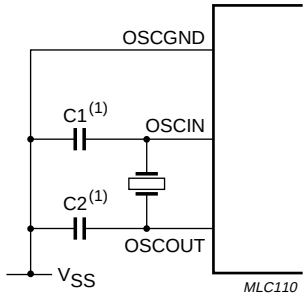


Fig.16 525-line display format.

9.23 Clock generator

The oscillator circuit is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between OSCIN and OSCOUT is basically an inverter biased to the transfer point. A crystal must be used as the feedback element to complete the oscillator circuitry. It is operated in parallel resonance. OSCIN is the high gain amplifier input and OSCOUT is the output. To drive the device externally OSCIN is driven from an external source and OSCOUT is left open-circuit.



(1) The values of C1 and C2 depend on the crystal specification: $C1 = C2 = 2C_L$.

Fig.17 Oscillator circuit.

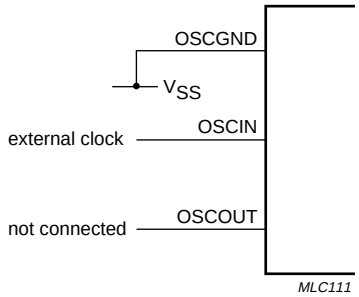


Fig.18 Oscillator circuit driven from external source.

10 CHARACTER SETS

The two Pan-European character sets are shown in Figs 20 and 21. The character sets for Russian, Greek/Turkish, Arabic/English/French, Thai and Arabic/Hebrew are available on request.

10.1 Pan-European

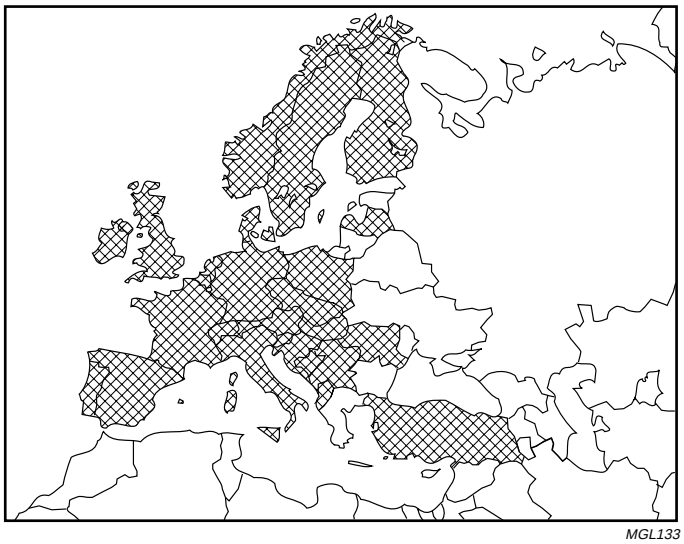


Fig.19 Pan-European geographical coverage.

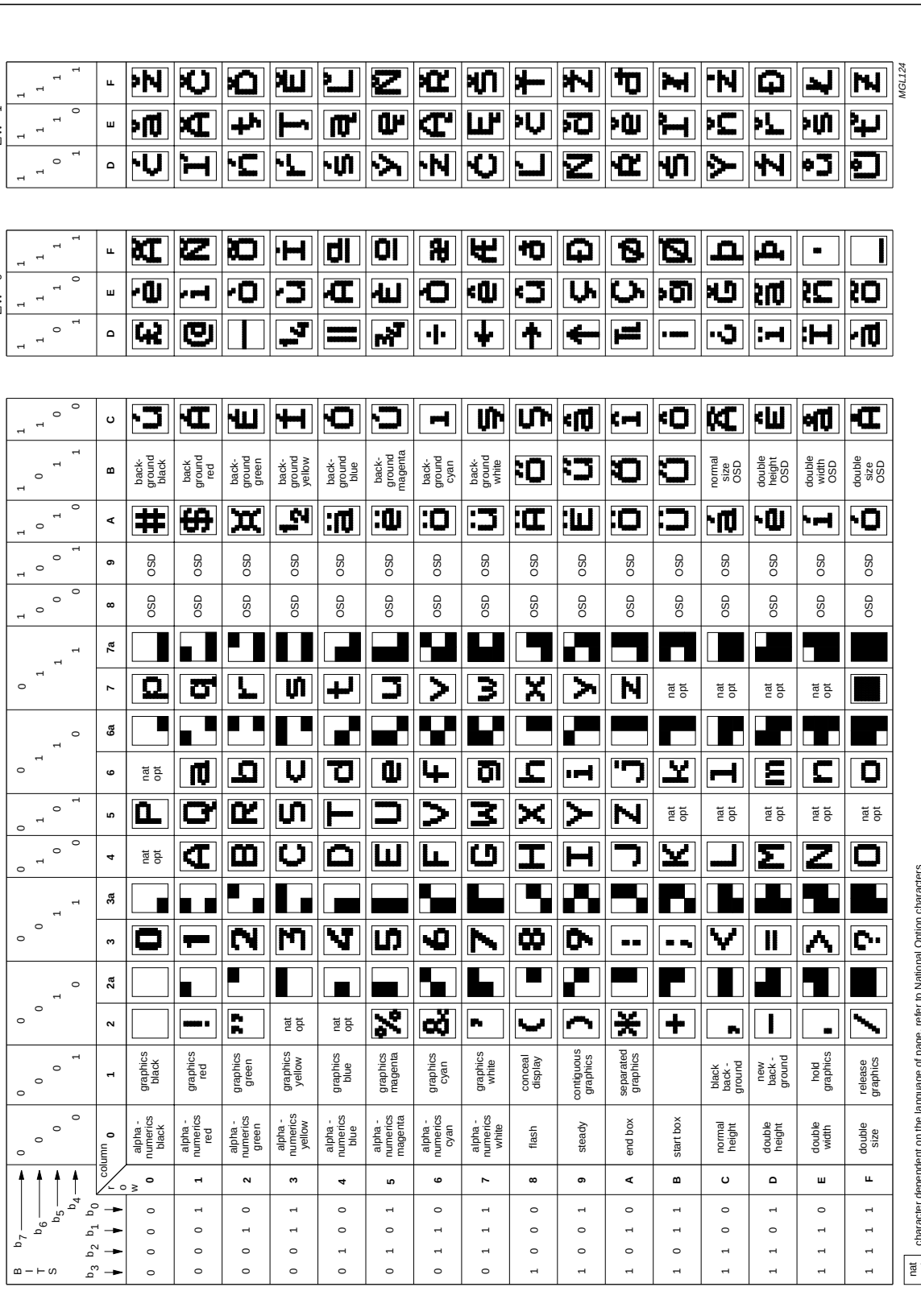


Fig.20 Pan-European basic character set.

LANGUAGE	E/W	C12	C13	C14	CHARACTER												
					23	24	40	5B	5C	5D	5E	5F	60	7B	7C	7D	7E
ENGLISH(1)	**0**	**0**	**0**	**0**	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN(1)	**0**	**0**	**0**	**1**	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH(1)	**0**	**0**	**1**	**0**	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN(1)	**0**	**0**	**1**	**1**	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH(1)	**0**	**1**	**0**	**0**	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH(1)	**0**	**1**	**0**	**1**	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à
TURKISH(1)	**0**	**1**	**1**	**0**	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ENGLISH(2)	**0**	**1**	**1**	**1**	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
POLISH(1)	**1**	**0**	**0**	**0**	#	ń	ą	Ż	ś	ł	ć	ó	ę	ż	ś	ł	ź
GERMAN(1)	**1**	**0**	**0**	**1**	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
ESTONIAN(1)	**1**	**0**	**1**	**0**	#	õ	Š	Ä	Ö	Ž	Ü	Õ	š	ä	ö	ž	ü
GERMAN(2)	**1**	**0**	**1**	**1**	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
GERMAN(2)	**1**	**1**	**0**	**0**	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SERBO-CROAT(1)	**1**	**1**	**0**	**1**	#	Ë	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECH(1)	**1**	**1**	**1**	**0**	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN(1)	**1**	**1**	**1**	**1**	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MGL125

(1) Languages in bold typeface conform to the EBU document SP492 or where superseded ETSI document pr ETS 300 706 with respect to C12/C13/C14 definition.

(2) Languages in italic typeface are included for backward compatibility with previous generation of Philips teletext decoders.

Fig.21 National option characters.

10.2 Russian

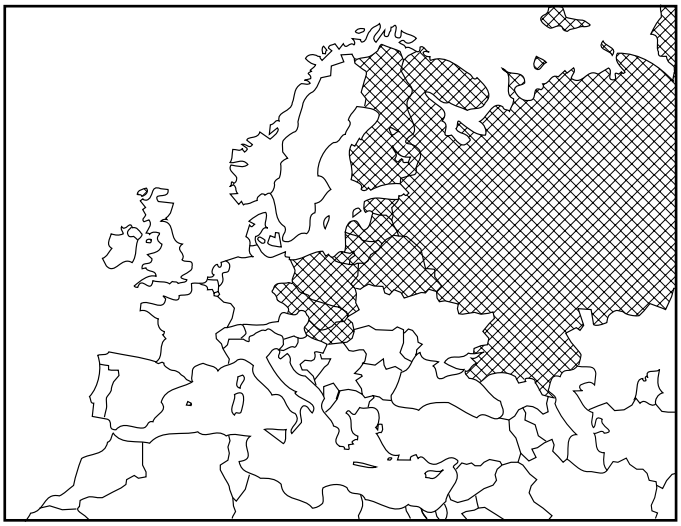


Fig.22 Russian geographical coverage.

10.3 Greek/Turkish

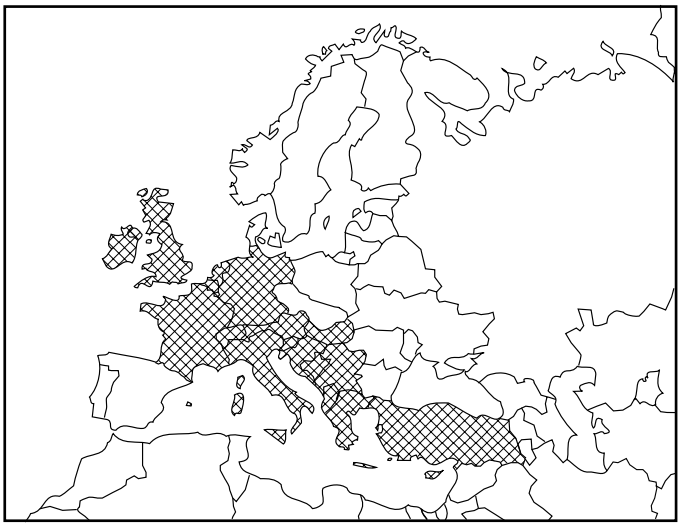


Fig.23 Greek/Turkish geographical coverage.

10.4 Arabic/English/French

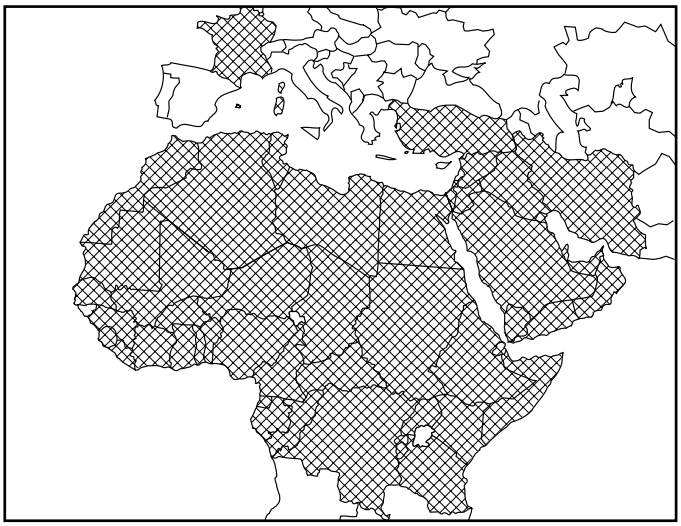


Fig.24 Arabic/English/French geographical coverage.

10.5 Thai

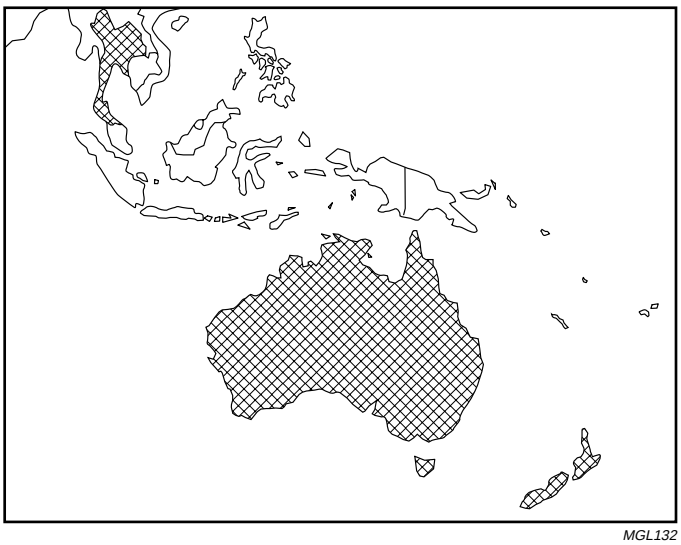


Fig.25 Thai geographical coverage.

10.6 Arabic/Hebrew

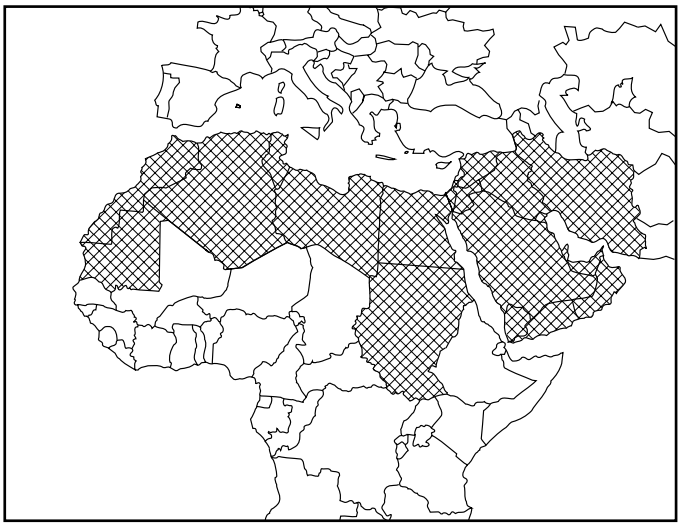


Fig.26 Arabic/Hebrew geographical coverage.

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)		–0.3	+6.5	V
V_I	input voltage (any input)	note 1	–0.3	V_{DD} + 0.5	V
V_O	output voltage (any output)	note 1	–0.3	V_{DD} + 0.5	V
I_O	output current (each output)		–	±10	mA
I_{IOK}	DC input or output diode current		–	±20	mA
T_{amb}	operating ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. This value has an absolute maximum of 6.5 V independent of V_{DD}.

12 CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = –20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage (V_{DD} to V_{SS})		4.5	5.0	5.5	V
I_{DDM}	microcontroller supply current		–	25	40	mA
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DDM}	microcontroller supply current		–	20	35	mA
I_{DDA}	analog supply current		–	35	50	mA
I_{DDT}	teletext supply current SAA5290, SAA5291, SAA5291A, SAA5491		–	40	65	mA
I_{DDT}	teletext supply current SAA5296/7, SAA5296/7A, SAA5496/7		–	50	80	mA
Digital inputs						
RESET, $\overline{EA}$						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DD}$ – 0.1	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	4	pF
HSYNC AND VSYNC						
V_{thf}	switching threshold falling		$0.2V_{DD}$	–	–	V
V_{thr}	switching threshold rising		–	–	$0.8V_{DD}$	V
V_{HYS}	hysteresis voltage		–	$0.33V_{DD}$	–	V
C_I	input capacitance		–	–	4	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs						
R, G AND B; NOTE 1						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	V_{RGBREF} – 0.3	V_{RGBREF}	V_{RGBREF} + 0.4	V
$\|Z_O\|$	output impedance		–	–	150	Ω
C_L	load capacitance		–	–	50	pF
I_O	DC output current		–	–	–4	mA
t_r	output rise time	between 10 and 90%; C_L = 50 pF	–	–	20	ns
t_f	output fall time	between 90 and 10%; C_L = 50 pF	–	–	20	ns
VDS						
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1.6 mA	V_{DD} – 0.3	–	V_{DD} + 0.4	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10 and 90%; C_L = 50 pF	–	–	20	ns
t_f	output fall time	between 90 and 10%; C_L = 50 pF	–	–	20	ns
R, G, B AND VDS						
t_{skew}	skew delay between any two pins		–	–	20	ns
$\overline{COR}$ (OPEN-DRAIN OUTPUT)						
V_{OH}	HIGH-level pull-up output voltage		–	–	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.5	V
I_{OL}	LOW-level output current		–	–	2	mA
C_L	load capacitance		–	–	25	pF
FRAME, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{PSEN}$, AD0 TO AD7, A8 TO A15						
V_{OH}	HIGH-level output voltage	I_{OL} = 8 mA	0	–	0.5	V
V_{OL}	LOW-level output voltage	I_{OL} = –8 mA	V_{DD} – 0.5	–	V_{DD}	V
I_{OL}	LOW-level output current		–8	–	+8	mA
C_L	load capacitance		–	–	100	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input/outputs						
P0.0 TO P0.4, P0.7, P1.0 TO P1.5, P2.0 TO P2.7 AND P3.0 TO P3.4						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DD} - 0.1$	V
V_{IH}	HIGH-level input voltage		$0.2V_{DD} + 0.9$	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	4	pF
V_{OL}	LOW-level output voltage	I_{OL} = 3.2 mA	0	–	0.45	V
C_L	load capacitance		–	–	50	pF
P0.5 AND P0.6						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DD} - 0.1$	V
V_{IH}	HIGH-level input voltage		$0.2V_{DD} + 0.9$	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	4	pF
V_{OL}	LOW-level output voltage	I_{OL} = 10 mA	0	–	0.45	V
C_L	load capacitance		–	–	50	pF
P1.6 AND P1.7						
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	5	pF
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	0	–	0.5	V
C_L	load capacitance		–	–	400	pF
t_f	output fall time	between 3 and 1 V	–	–	200	ns
Analog inputs						
CVBS0 AND CVBS1						
V_{sync}	sync voltage amplitude		0.1	0.3	0.6	V
$V_{vid(p-p)}$	video input voltage amplitude (peak-to-peak value)		0.7	1.0	1.4	V
Z_{source}	source impedance		–	–	250	Ω
V_{IH}	HIGH level input voltage		3.0	–	$V_{DD} + 0.3$	V
$\lvert Z_I \rvert$	input impedance		2.5	5.0	–	kΩ
C_I	input capacitance		–	–	10	pF
IREF						
R_{gnd}	resistor to ground		–	27	–	kΩ
RGBREF; NOTE 1						
V_I	input voltage		–0.3	–	V_{DD}	V
I_I	DC input current		–	–	12	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REF+, REF–						
V_{IH}	HIGH level input voltage		3.0	–	V_{DD} + 0.3	V
$\|Z_I\|$	input impedance		2.5	5.0	–	kΩ
C_I	input capacitance		–	–	10	pF
ADC0, ADC1 and ADC2						
V_{IL}	LOW-level input voltage		–0.3	–	V_{DD}	V
Analog input/output						
BLACK						
C_{BLACK}	storage capacitor to ground		–	100	–	nF
V_{BLACK}	black level voltage for nominal sync amplitude		1.8	2.15	2.5	V
I_{LI}	input leakage current		-10	–	+10	μA
Crystal oscillator						
OSCIN						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DD}$ – 0.1	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
C_I	input capacitance		–	–	10	pF
OSCOUT						
C_O	output capacitance		–	–	10	pF
CRYSTAL SPECIFICATION; NOTE 2						
f_{xtal}	nominal frequency		–	12	–	MHz
C_L	load capacitance		–	32	–	pF
C1	series capacitance	T_{amb} = 25 °C	–	18.5	–	fF
C0	parallel capacitance	T_{amb} = 25 °C	–	4.9	–	pF
R_r	resonance resistance	T_{amb} = 25 °C	–	35	–	Ω
T_{xtal}	temperature range		-20	+25	+70	°C
X_j	adjustment tolerance	T_{amb} = 25 °C	–	–	$\pm 50 \times 10^{-6}$	
X_d	drift		–	–	$\pm 30 \times 10^{-6}$	

Notes

1. All RGB current is sourced from the RGBREF pin. The maximum effective series resistance between RGBREF and the R, G and B pins is 150 Ω.
2. Crystal order number 4322 143 05561.

13 CHARACTERISTICS FOR THE I²C-BUS INTERFACE

SYMBOL	PARAMETER	INPUT	OUTPUT	I²C-BUS SPECIFICATION
SCL timing				
$t_{HD;STA}$	START condition hold time	≥4.0 μs	note 1	≥4.0 μs
t_{LOW}	SCL LOW time	≥4.7 μs	note 1	≥4.7 μs
t_{HIGH}	SCL HIGH time	≥4.0 μs	≥4.0 μs; note 2	≥4.0 μs
t_{rC}	SCL rise time	≤1.0 μs	note 3	≤1.0 μs
t_{fC}	SCL fall time	≤0.3 μs	≤0.3 μs; note 4	≤0.3 μs
SDA timing				
$t_{SU;DAT1}$	data set-up time	≥250 ns	note 1	≥250 ns
$t_{HD;DAT}$	data hold time	≥0 ns	note 1	≥0 ns
$t_{SU;STA}$	repeated START set-up time	≥4.7 μs	note 1	≥4.7 μs
$t_{SU;STO}$	STOP condition set-up time	≥4.0 μs	note 1	≥4.0 μs
t_{BUF}	bus free time	≥4.7 μs	note 1	≥4.7 μs
t_{rD}	SDA rise time	≤1.0 μs	note 3	≤1.0 μs
t_{fD}	SDA fall time	≤0.3 μs	≤0.3 μs; note 4	≤0.3 μs

Notes

1. This parameter is determined by the user software. It must comply with the I²C-bus specification.
2. This value gives the auto-clock pulse length which meets the I²C-bus specification for the special crystal frequency. Alternatively, the SCL pulse must be timed by software.
3. The rise time is determined by the external bus line capacitance and pull-up resistor. It must be less than 1 μs.
4. The maximum capacitance on bus lines SDA and SCL is 400 pF.

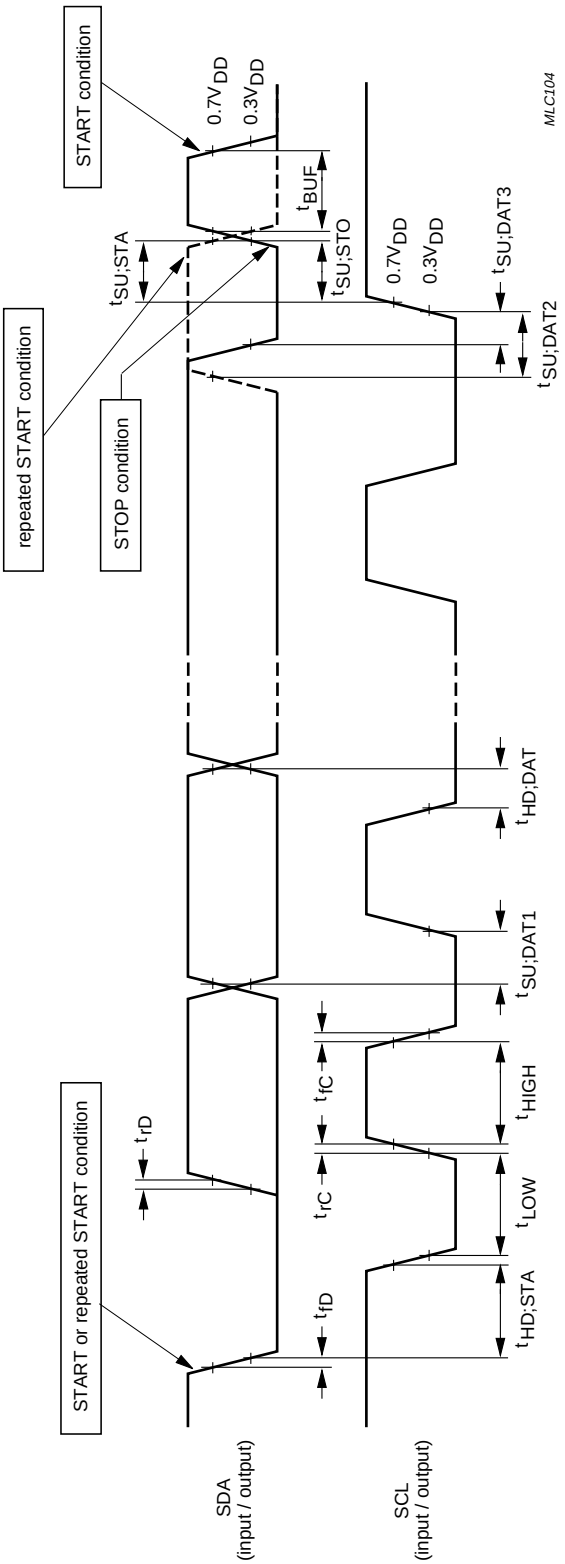


Fig.27 I²C-bus interface timing.

14 QUALITY SPECIFICATIONS

This device will meet Philips Semiconductors General Quality Specification for Business group *"Consumer Integrated Circuits SNW-FQ-611-Part E"*; *"Quality Reference Handbook, order number 9398 510 63011"*. The principal requirements are shown in Table 25 to 28.

Table 25 Acceptance tests per lot; note 1

TEST	REQUIREMENTS
Mechanical	cumulative target: <80 ppm
Electrical	cumulative target: <80 ppm

Table 26 Processability tests (by package family); note 2

TEST	REQUIREMENTS
solderability	<7% LTPD
mechanical	<15% LTPD
solder heat resistance	<15% LTPD

Table 27 Reliability tests (by process family); note 3

TEST	CONDITIONS	REQUIREMENTS
operational life	168 hours at T_j = 150 °C	<1000 FPM at T_j = 70 °C
humidity life	temperature, humidity, bias 1000 hours, 85 °C, 85% RH (or equivalent test)	<2000 FPM
temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Table 28 Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS
ESD and latch-up	ESD Human body model 100 pF, 1.5 kΩ	2000 V
	ESD Machine model 200 pF, 0 Ω	200 V
	latch-up	100 mA, $1.5 \times V_{DD}$ (absolute maximum)

Notes to Tables 25, 26 and 27

1. ppm = fraction of defective devices, in parts per million.
2. LTPD = Lot Tolerance Percent Defective.
3. FPM = fraction of devices failing at test condition, in failures per million.

15 APPLICATION INFORMATION

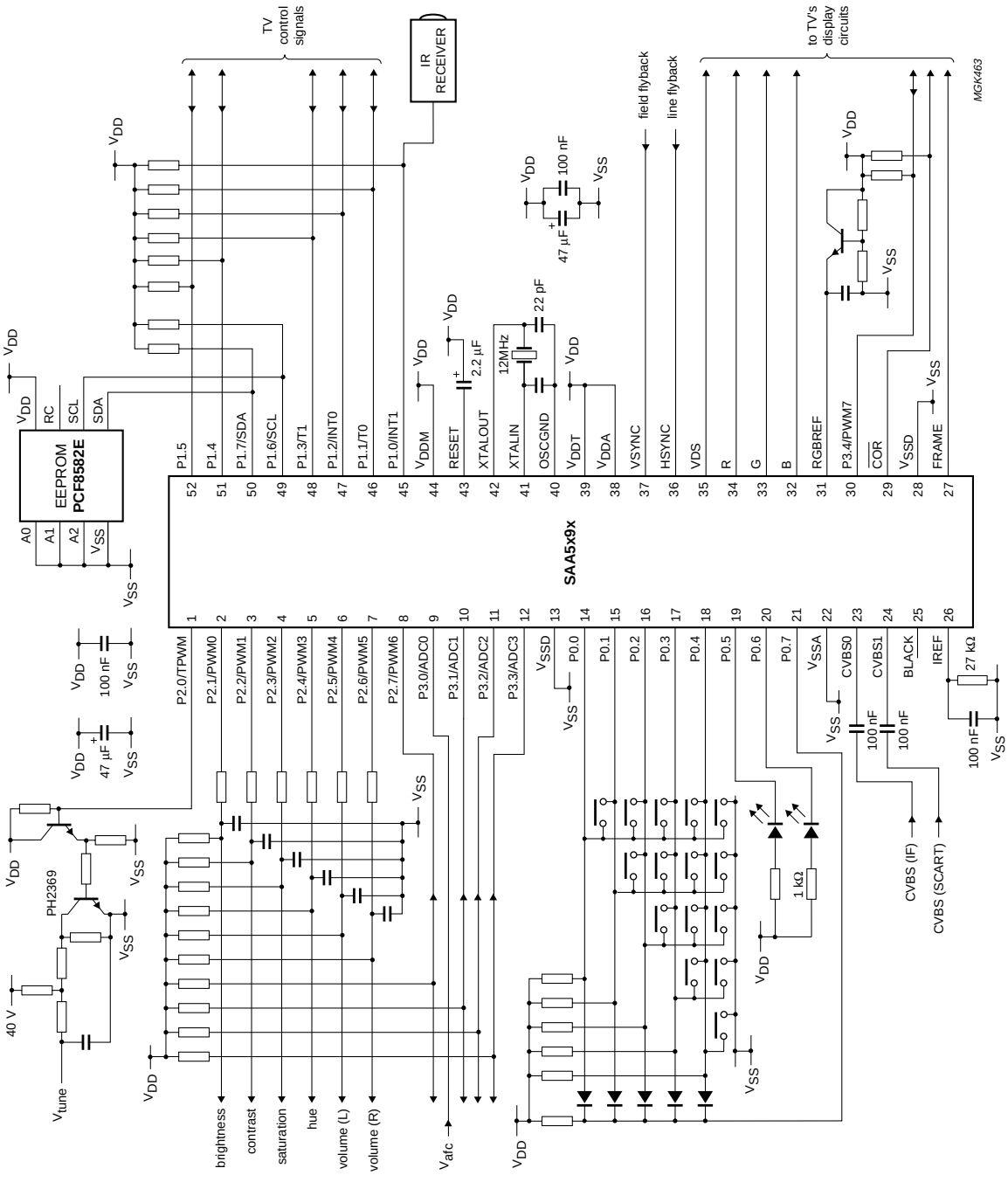


Fig.28 Application diagram.

16 EMC GUIDELINES

If possible, a ground plane under the whole IC should be present, i.e. no signal tracks running underneath the IC as shown in Fig.29.

The ground plane under the IC should be connected by the widest possible connection back to the ground connection of the PCB, and electrolytic decoupling capacitor. It should preferably not connect to other grounds on the way and no wire links should be present in this connection. The use of wire links increases ground bounce by introducing inductance into the ground, thereby reducing the electrolytic capacitor's decoupling efficiency.

The supply pins should be decoupled at the pin, to the ground plane under the IC. This is easily accomplished when using SM capacitors (which are also most effective at high frequencies). Each supply pin should be connected separately to the power connection of the PCB, preferably via at least one wire link which:

1. May be replaced by a ferrite or inductor at a later point if necessary
2. Will introduce a small amount of inductance.

Signals connected to the +5 V supply e.g. via a pull-up resistors, should be connected to the +5 V supply before the wire link to the IC (i.e. not the IC side). This will prevent if from being polluted and conduct or radiate noise onto signal lines, which may then radiate themselves.

OSCGND should connect only to the crystal load capacitors (and not GND).

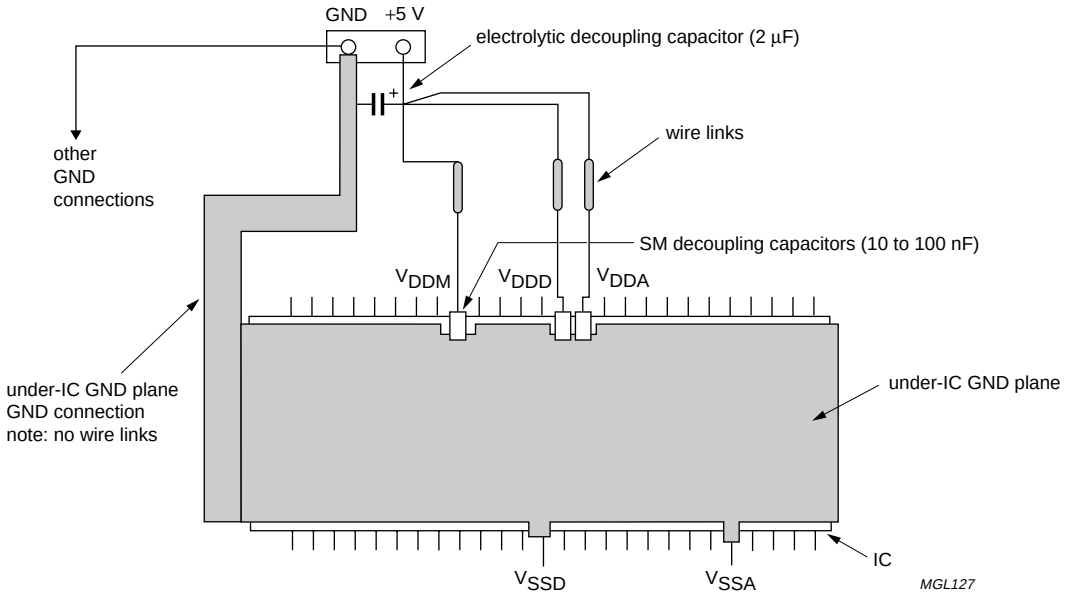
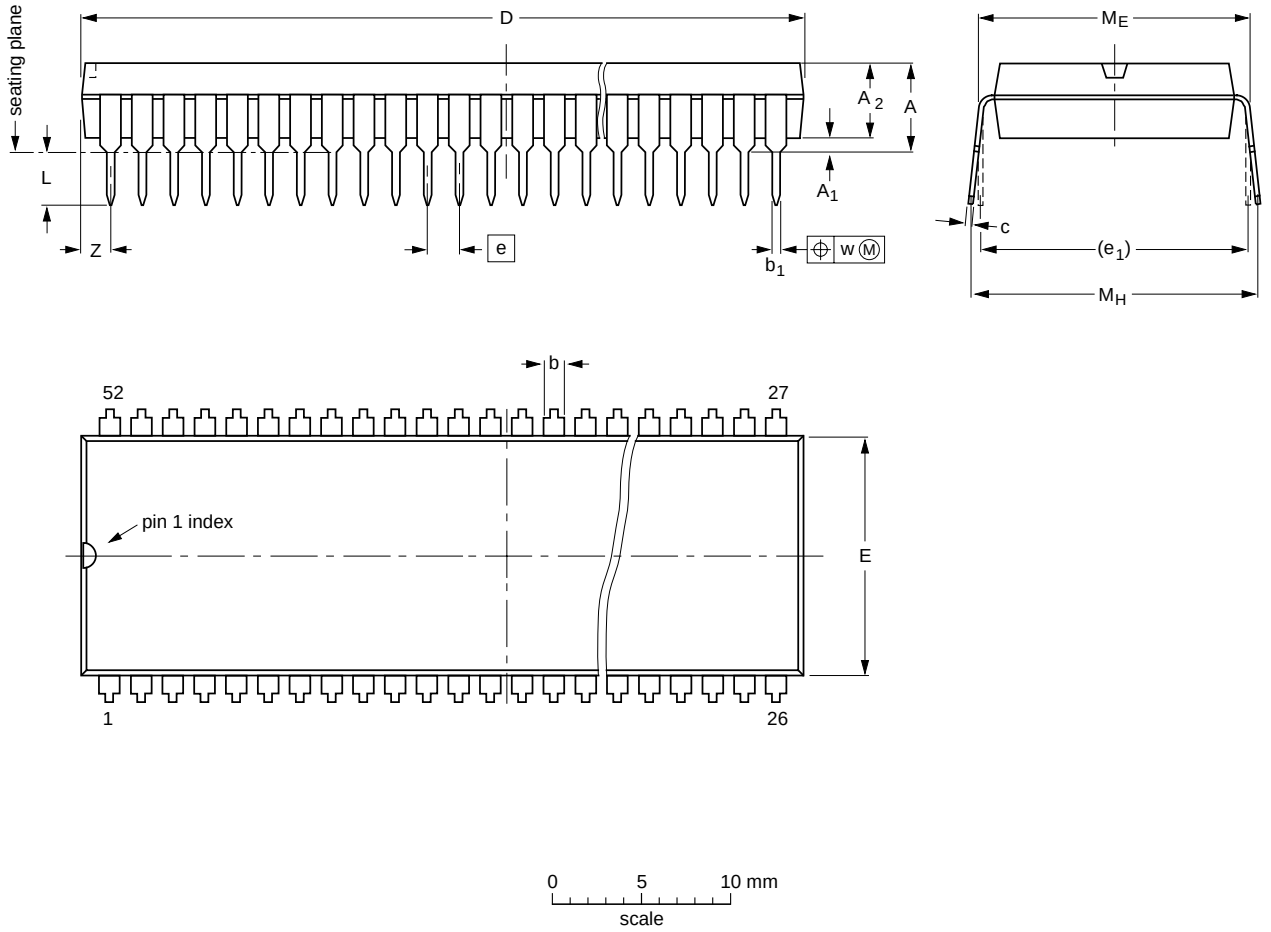


Fig.29 Power supply and GND connections for SOT247-1.

17 PACKAGE OUTLINES

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

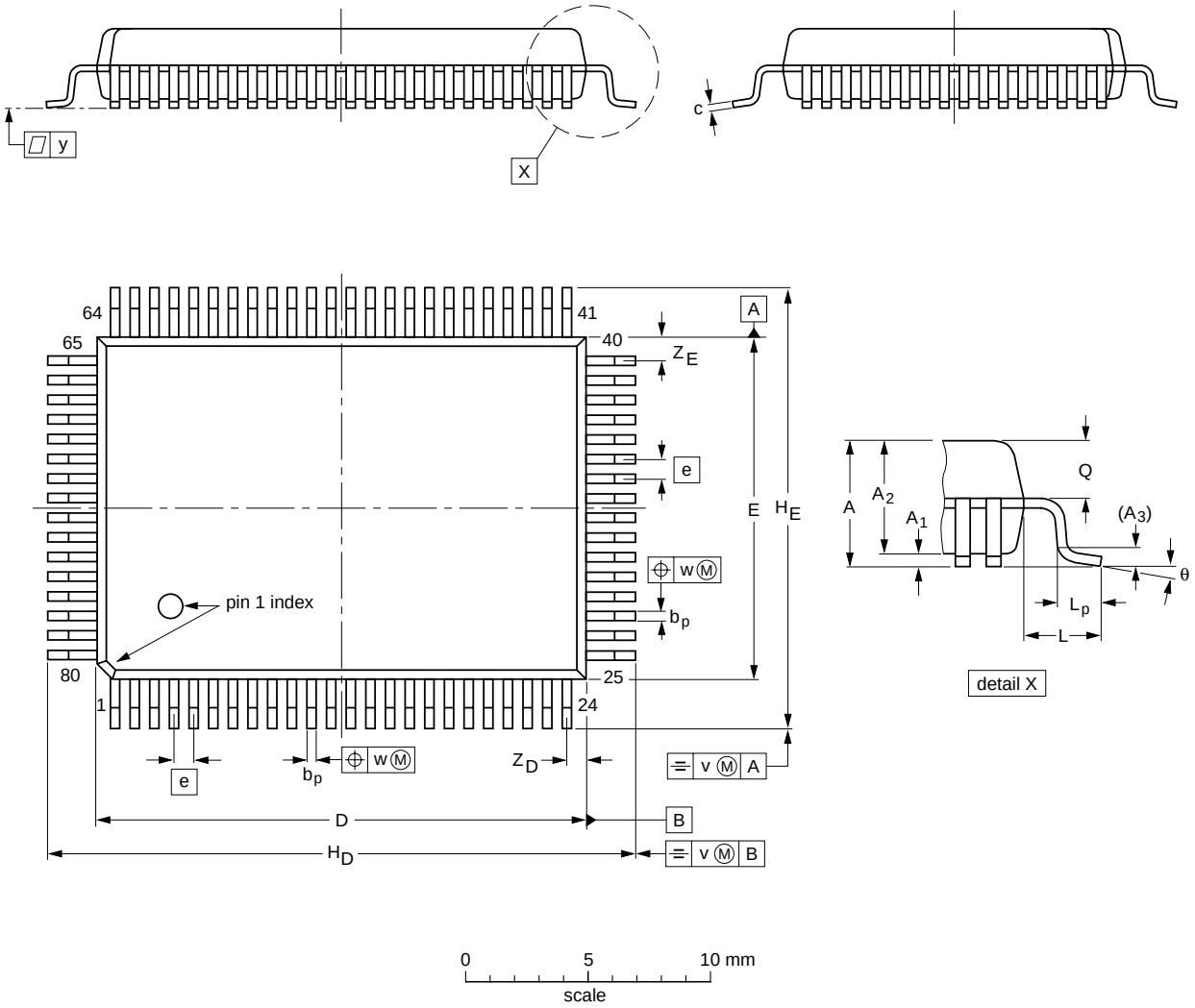
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT318-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2						~~92-12-15~~ 95-02-04

18 SOLDERING

18.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

18.2 SDIP

18.2.1 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

18.2.2 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

18.3 QFP

18.3.1 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

18.3.2 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.3.3 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

20 LIFE SUPPORT APPLICATIONS

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

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Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
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Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

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Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

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