

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT164**

8-bit serial-in/parallel-out shift register

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-bit serial-in/parallel-out shift register

## 74HC/HCT164

## FEATURES

- Gated serial data inputs
- Asynchronous master reset
- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT164 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages.

Data is entered serially through one of two inputs ( $D_{sa}$  or  $D_{sb}$ ); either input can be used as an active HIGH enable for data entry through the other input.

Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into  $Q_0$ , which is the logical AND of the two data inputs ( $D_{sa}, D_{sb}$ ) that existed one set-up time prior to the rising clock edge.

A LOW level on the master reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$ MR to $Q_n$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	12	14	ns
			11	16	ns
$f_{max}$	maximum clock frequency		78	61	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	40	40	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

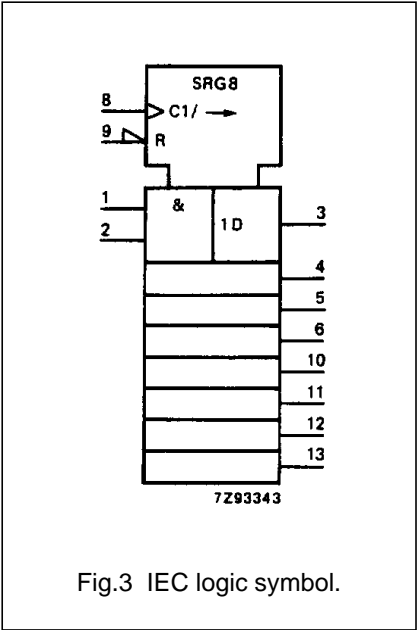
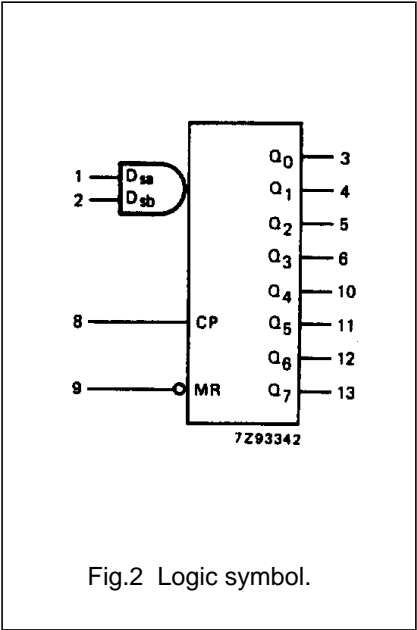
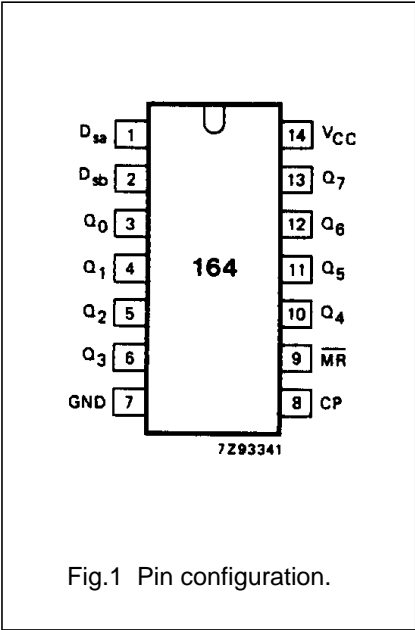
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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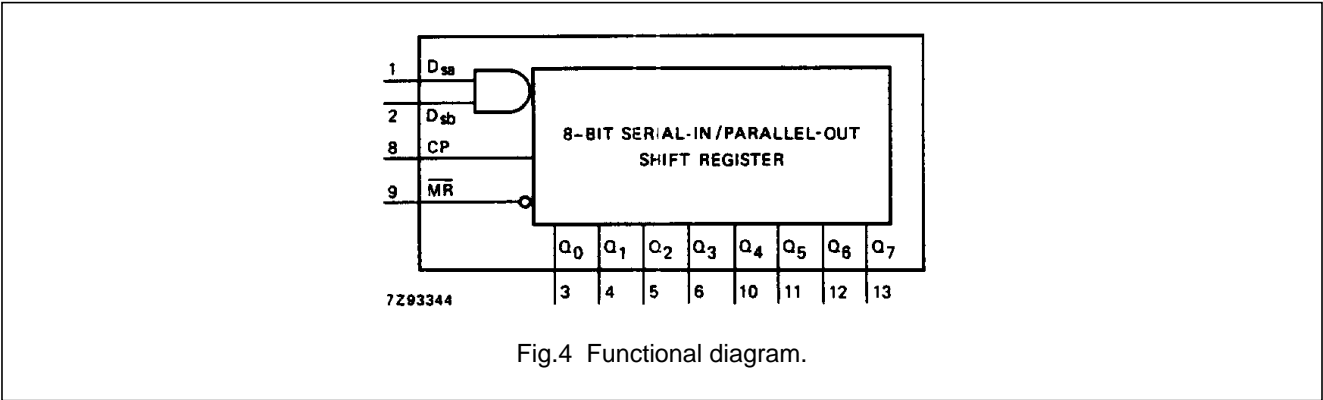
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	$D_{sa}, D_{sb}$	data inputs
3, 4, 5, 6, 10, 11, 12, 13	$Q_0$ to $Q_7$	outputs
7	GND	ground (0 V)
8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	master reset input (active LOW)
14	$V_{CC}$	positive supply voltage



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APPLICATIONS

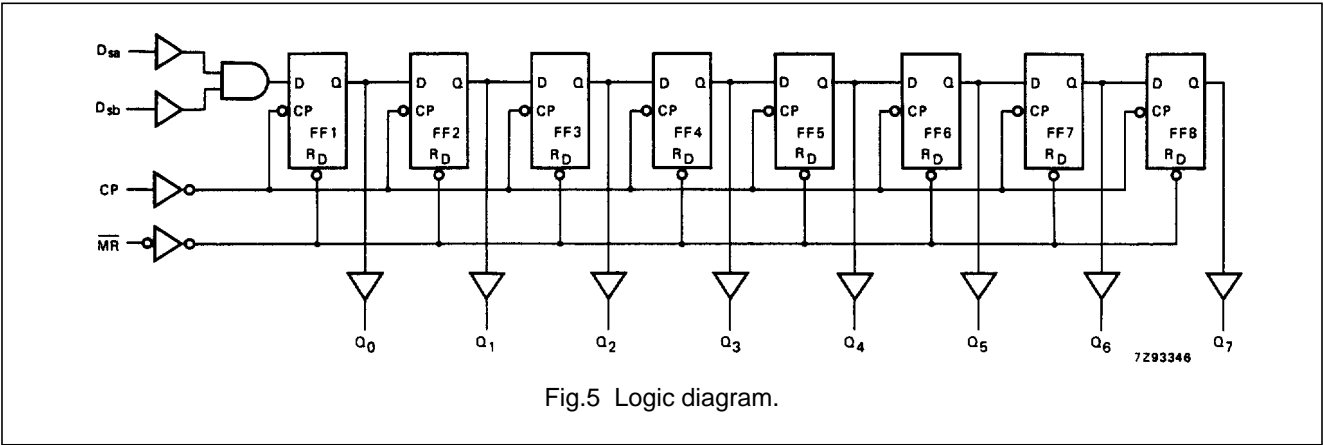
- Serial data transfer

FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{\text{MR}}$	CP	D <sub>sa</sub>	D <sub>sb</sub>	Q <sub>0</sub>	Q <sub>1</sub> – Q <sub>7</sub>
reset (clear)	L	X	X	X	L	L – L
shift	H	↑	l	l	L	q <sub>0</sub> – q <sub>6</sub>
	H	↑	l	h	L	q <sub>0</sub> – q <sub>6</sub>
	H	↑	h	l	L	q <sub>0</sub> – q <sub>6</sub>
	H	↑	h	h	H	q <sub>0</sub> – q <sub>6</sub>

Note

- H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition  
q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition  
↑ = LOW-to-HIGH clock transition



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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		41 15 12	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	master reset pulse width; LOW	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.6
t <sub>rem</sub>	removal time MR to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.6
t <sub>su</sub>	set-up time D <sub>sa</sub> , D <sub>sb</sub> to CP	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.6
t <sub>h</sub>	hold time D <sub>sa</sub> , D <sub>sb</sub> to CP	4 4 4	−6 −2 −2		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig.6
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	23 71 85		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig.6

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>sa</sub> , D <sub>sb</sub>	0.25
CP	0.60
MR	0.90

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		17	36		45		54	ns	4.5	Fig.6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		19	38		48		57	ns	4.5	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	18	7		23		27		ns	4.5	Fig.6
t <sub>W</sub>	master reset pulse width; LOW	18	10		23		27		ns	4.5	Fig.6
t <sub>rem</sub>	removal time MR to CP	16	7		20		24		ns	4.5	Fig.6
t <sub>su</sub>	set-up time D <sub>sa</sub> , D <sub>sb</sub> to CP	12	6		15		18		ns	4.5	Fig.6
t <sub>h</sub>	hold time D <sub>sa</sub> , D <sub>sb</sub> to CP	4	−2		4		4		ns	4.5	Fig.6
f <sub>max</sub>	maximum clock pulse frequency	27	55		22		18		MHz	4.5	Fig.6

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## AC WAVEFORMS

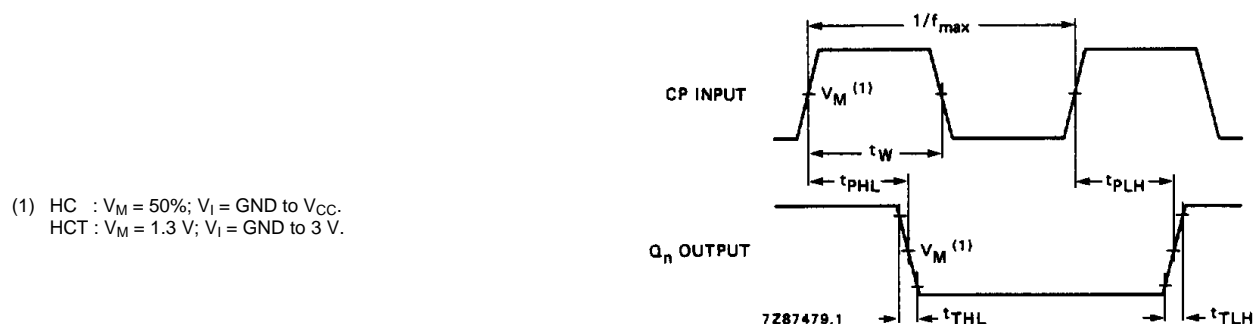


Fig.6 Waveforms showing the clock (CP) to output ( $Q_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

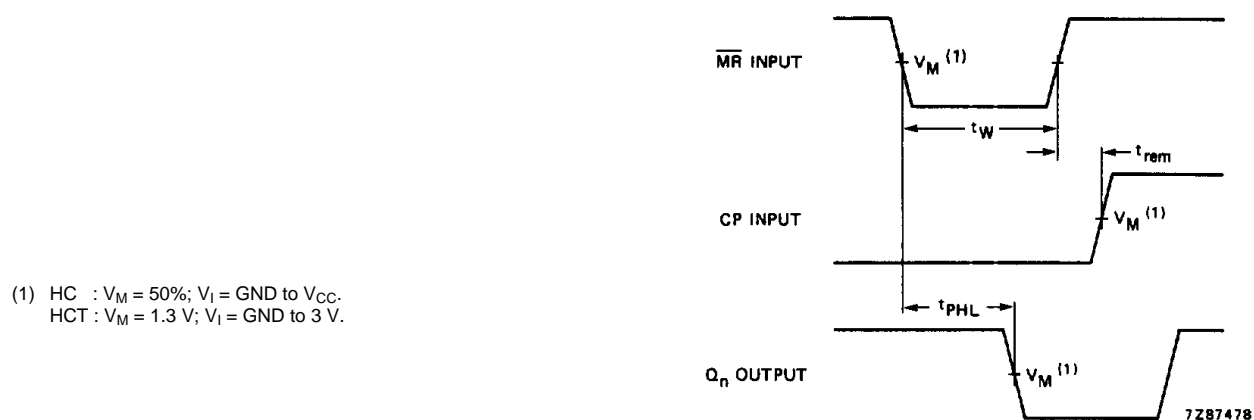


Fig.7 Waveforms showing the master reset ( $\overline{MR}$ ) pulse width, the master reset to output ( $Q_n$ ) propagation delays and the master reset to clock (CP) removal time.

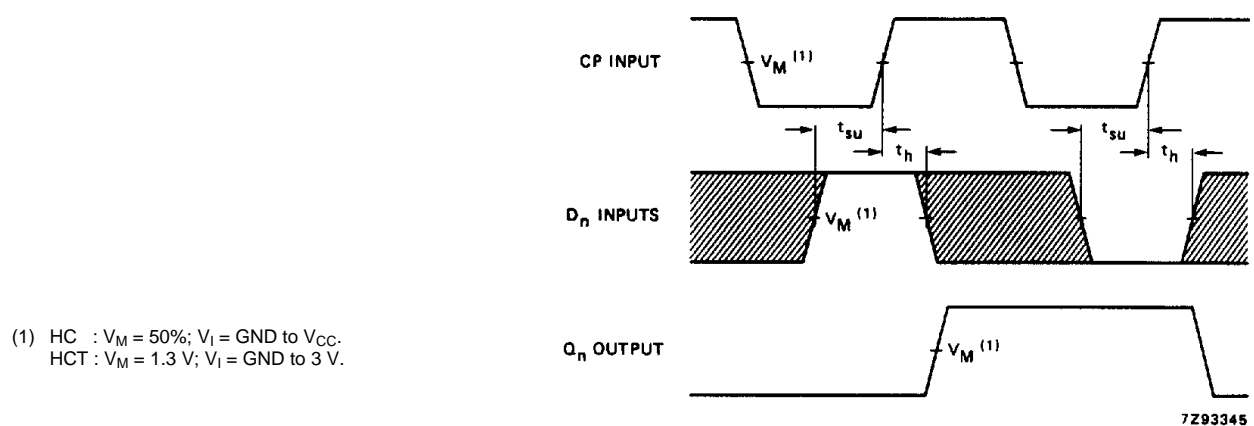


Fig.8 Waveforms showing the data set-up and hold times for  $D_n$  inputs.

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**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.