

# DATA SHEET

## **74AHC138; 74AHCT138** 3-to-8 line decoder/demultiplexer; inverting

Product specification  
Supersedes data of 1999 Mar 31  
File under Integrated Circuits, IC06

1999 Sep 27

**3-to-8 line decoder/demultiplexer; inverting****74AHC138;  
74AHCT138****FEATURES**

- ESD protection:  
HBM EIA/JESD22-A114-A  
exceeds 2000 V  
MM EIA/JESD22-A115-A  
exceeds 200 V  
CDM EIA/JESD22-C101  
exceeds 1000 V
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Inputs accept voltages higher than  $V_{CC}$
- For AHC only:  
operates with CMOS input levels
- For AHCT only:  
operates with TTL input levels
- Specified from  
-40 to +85 and +125 °C.

**DESCRIPTION**

The 74AHC/AHCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC/AHCT138 decoders accept three binary weighted address inputs ( $A_0$ ,  $A_1$  and  $A_2$ ) and when enabled, provide 8 mutually exclusive active LOW outputs ( $\bar{Y}_0$  to  $\bar{Y}_7$ ).

The '138' features three enable inputs: two active LOW ( $\bar{E}_1$  and  $\bar{E}_2$ ) and one active HIGH ( $E_3$ ). Every output will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and  $E_3$  is HIGH.

This multiple enable function allows easy parallel expansion of the '138' to a 1-of-32 (5 to 32 lines) decoder with just four '138' ICs and one inverter.

The '138' can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The '138' is identical to the '238' but has inverting outputs.

**QUICK REFERENCE DATA**

GND = 0 V;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f \leq 3.0\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $\bar{Y}_n$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	4.4	4.4	ns
	propagation delay $E_3$ to $\bar{Y}_n$ ; $\bar{E}_n$ to $\bar{Y}_n$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	4.2	4.3	ns
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
$C_O$	output capacitance		4.0	4.0	pF
$C_{PD}$	power dissipation capacitance	$C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ; notes 1 and 2	18	23	pF

**Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

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## FUNCTION TABLE

See note 1.

INPUT						OUTPUT							
$\bar{E}_1$	$\bar{E}_2$	$E_3$	$A_0$	$A_1$	$A_2$	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

## Note

1. H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care.

## ORDERING INFORMATION

OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGES			
		PINS	PACKAGE	MATERIAL	CODE
74AHC138D	74AHC138D	16	SO	plastic	SOT109-1
74AHC138PW	74AHC138PW DH	16	TSSOP	plastic	SOT403-1
74AHCT138D	74AHCT138D	16	SO	plastic	SOT109-1
74AHCT138PW	74AHCT138PW DH	16	TSSOP	plastic	SOT403-1

## PINNING

PIN	SYMBOL	DESCRIPTION
1, 2 and 3	$A_0$ , $A_1$ and $A_2$	address inputs
4 and 5	$\bar{E}_1$ and $\bar{E}_2$	enable inputs (active LOW)
6	$E_3$	enable input (active HIGH)
7, 9, 10 11, 12, 13, 14 and 15	$\bar{Y}_7$ to $\bar{Y}_0$	outputs (active LOW)
8	GND	ground (0 V)
16	$V_{CC}$	DC supply voltage

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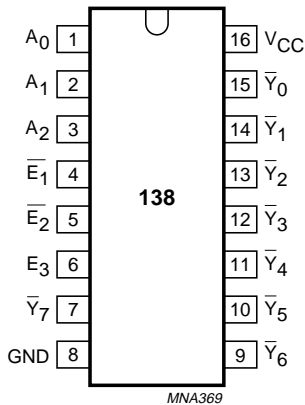


Fig.1 Pin configuration.

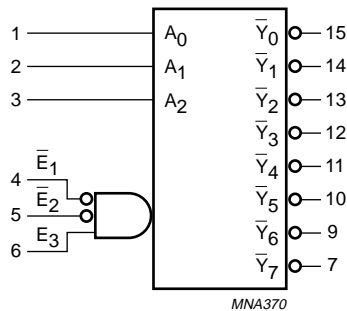


Fig.2 Logic symbol.

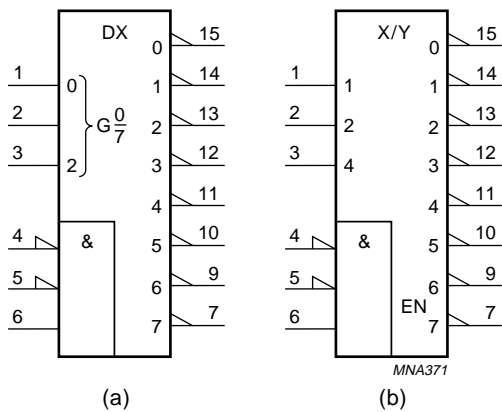


Fig.3 IEC logic symbol.

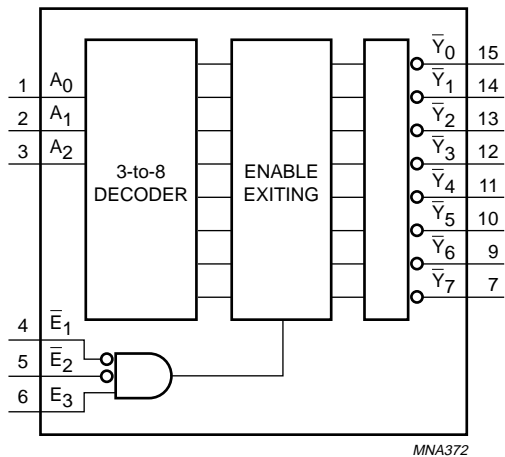


Fig.4 Functional diagram.

## 3-to-8 line decoder/demultiplexer; inverting

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	5.5	0	–	5.5	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature range	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
$t_r, t_f (\Delta t/\Delta f)$	input rise and fall rates	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	–	–	100	–	–	–	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	–	–	20	–	–	20	

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	DC supply voltage		–0.5	+7.0	V
$V_I$	input voltage range		–0.5	+7.0	V
$I_{IK}$	DC input diode current	$V_I < -0.5 \text{ V}$ ; note 1	–	–20	mA
$I_{OK}$	DC output diode current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$ ; note 1	–	$\pm 20$	mA
$I_O$	DC output source or sink current	$-0.5 \text{ V} < V_O < V_{CC} + 0.5 \text{ V}$	–	$\pm 25$	mA
$I_{CC}$	DC $V_{CC}$ or GND current		–	$\pm 75$	mA
$T_{stg}$	storage temperature range		–65	+150	°C
$P_D$	power dissipation per package	for temperature range: –40 to +125 °C; note 2	–	500	mW

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO packages: above 70 °C the value of  $P_D$  derates linearly with 8 mW/K.  
For TSSOP packages: above 60 °C the value of  $P_D$  derates linearly with 5.5 mW/K.

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## DC CHARACTERISTICS

## 74AHC family

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)							UNIT
		OTHER	V <sub>CC</sub> (V)	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	
			5.5	3.85	–	–	3.85	–	3.85	–	
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	
			5.5	–	–	1.65	–	1.65	–	1.65	
V <sub>OH</sub>	HIGH-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –50 μA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	2.9	–	
			4.5	4.4	4.5	–	4.4	–	4.4	–	
	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –4.0 mA	3.0	2.58	–	–	2.48	–	2.40	–	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –8.0 mA	4.5	3.94	–	–	3.8	–	3.70	–	
V <sub>OL</sub>	LOW-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 50 μA	2.0	–	0	0.1	–	0.1	–	0.1	V
			3.0	–	0	0.1	–	0.1	–	0.1	
			4.5	–	0	0.1	–	0.1	–	0.1	
	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4 mA	3.0	–	–	0.36	–	0.44	–	0.55	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8 mA	4.5	–	–	0.36	–	0.44	–	0.55	
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	0.1	–	1.0	–	2.0	μA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±0.25	–	±2.5	–	±10.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	4.0	–	40	–	80	μA
C <sub>I</sub>	input capacitance		–	–	3	10	–	10	–	10	pF

## 3-to-8 line decoder/demultiplexer; inverting

74AHC138;  
74AHCT138**74AHCT family**

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)							UNIT
		OTHER	V <sub>CC</sub> (V)	25			–40 to +85		–40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –50 μA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –8.0 mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V <sub>OL</sub>	LOW-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 50 μA	4.5	–	0	0.1	–	0.1	–	0.1	V
	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8 mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	0.1	–	1.0	–	2.0	μA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	±0.25	–	±2.5	–	±10.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	4.0	–	40	–	80	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	4.5 to 5.5	–	–	1.35	–	1.5	–	1.5	mA
C <sub>I</sub>	input capacitance		–	–	3	10	–	10	–	10	pF

## 3-to-8 line decoder/demultiplexer; inverting

74AHC138;  
74AHCT138

## AC CHARACTERISTICS

## Type 74AHC138

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)								UNIT
		WAVEFORMS	C <sub>L</sub>	25			−40 to +85		−40 to +125			
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V <sub>CC</sub> = 3.0 to 3.6 V; note 1												
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Y}_n$	see Figs 5 and 7	15 pF	–	6.0	11.4	1.0	13.0	1.0	14.5	ns	
	propagation delay E <sub>3</sub> to $\bar{Y}_n$			–	5.8	12.8	1.0	15.0	1.0	16.0	ns	
	propagation delay $\bar{E}_1, \bar{E}_2$ to $\bar{Y}_n$	see Figs 6 and 7	–	5.7	11.4	1.0	13.5	1.0	14.5	ns		
	propagation delay A <sub>n</sub> to $\bar{Y}_n$	see Figs 5 and 7	50 pF	–	8.6	15.8	1.0	18.0	1.0	20.0	ns	
	propagation delay E <sub>3</sub> to $\bar{Y}_n$			–	8.2	16.3	1.0	18.5	1.0	20.5	ns	
	propagation delay E <sub>1</sub> , E <sub>2</sub> to $\bar{Y}_n$	see Figs 6 and 7	–	8.2	14.9	1.0	17.0	1.0	19.0	ns		
V <sub>CC</sub> = 4.5 to 5.5 V; note 2												
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay A <sub>n</sub> to $\bar{Y}_n$	see Figs 5 and 7	15 pF	–	4.4	8.1	1.0	9.5	1.0	10.5	ns	
	propagation delay E <sub>3</sub> to $\bar{Y}_n$			–	4.2	8.1	1.0	9.5	1.0	10.5	ns	
	propagation delay $\bar{E}_1, \bar{E}_2$ to $\bar{Y}_n$	see Figs 6 and 7	–	4.2	8.1	1.0	9.5	1.0	10.5	ns		
	propagation delay A <sub>n</sub> to $\bar{Y}_n$	see Figs 5 and 7	50 pF	–	6.3	10.1	1.0	11.5	1.0	13.0	ns	
	propagation delay E <sub>3</sub> to $\bar{Y}_n$			–	6.0	10.1	1.0	11.5	1.0	13.0	ns	
	propagation delay $\bar{E}_1, \bar{E}_2$ to $\bar{Y}_n$	see Figs 6 and 7	–	6.0	10.1	1.0	11.5	1.0	13.0	ns		

## Notes

1. Typical values at  $V_{CC} = 3.3$  V.
2. Typical values at  $V_{CC} = 5.0$  V.



## 3-to-8 line decoder/demultiplexer; inverting

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## Type 74AHCT138

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)							UNIT	
		WAVEFORMS	C <sub>L</sub>	25			−40 to +85		−40 to +125			
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.		
V <sub>CC</sub> = 4.5 to 5.5 V; note 1												
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay A <sub>n</sub> to Y <sub>n</sub>	see Figs 5 and 7	15 pF	–	4.4	10.4	1.0	12.0	1.0	13.0	ns	
	propagation delay E <sub>3</sub> to Y <sub>n</sub>			–	4.3	9.1	1.0	10.5	1.0	11.5	ns	
	propagation delay E <sub>1</sub> , E <sub>2</sub> to Y <sub>n</sub>	see Figs 6 and 7	–	4.3	9.6	1.0	11.0	1.0	12.0	ns		
	propagation delay A <sub>n</sub> to Y <sub>n</sub>	see Figs 5 and 7	50 pF	–	6.2	11.4	1.0	13.0	1.0	14.5	ns	
	propagation delay E <sub>3</sub> to Y <sub>n</sub>			–	6.2	10.1	1.0	11.5	1.0	13.0	ns	
	propagation delay E <sub>1</sub> , E <sub>2</sub> to Y <sub>n</sub>	see Figs 6 and 7	–	6.2	10.6	1.0	12.0	1.0	13.5	ns		

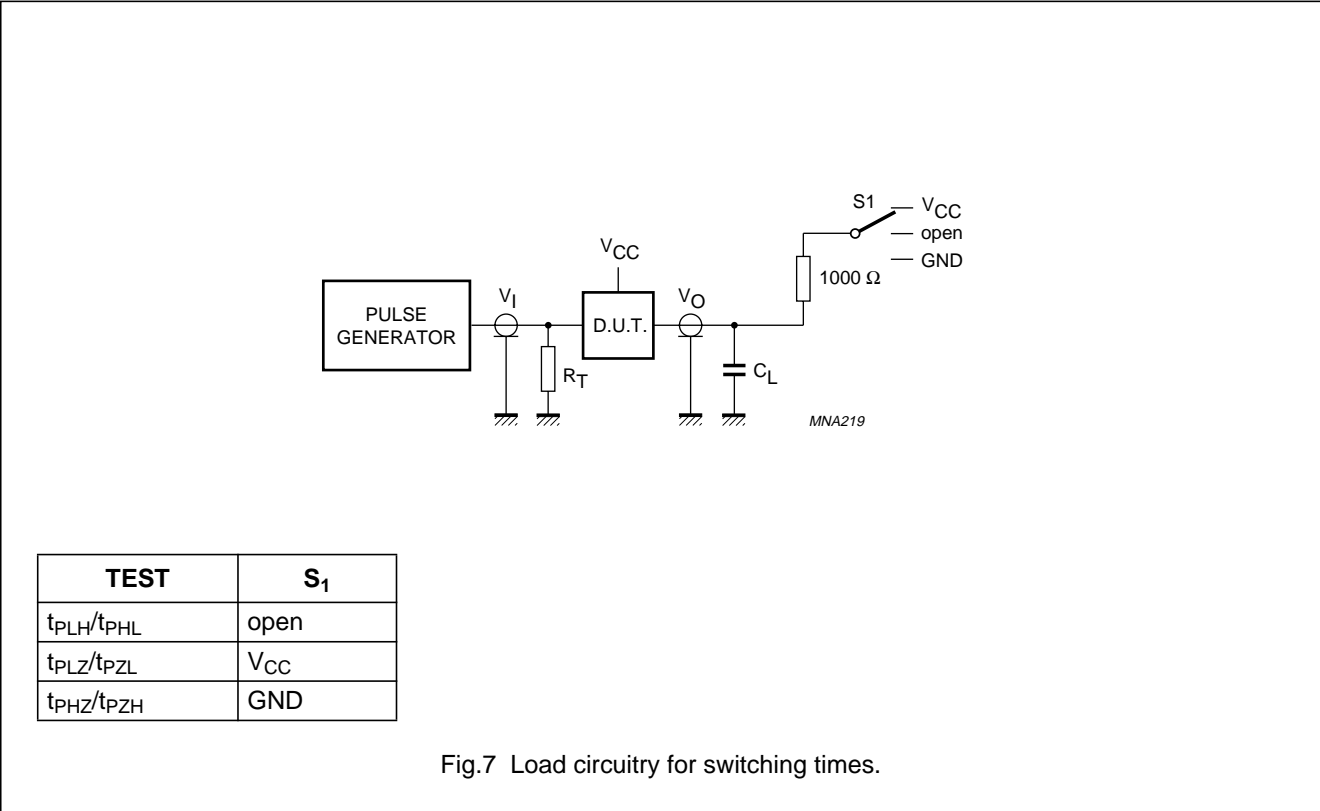
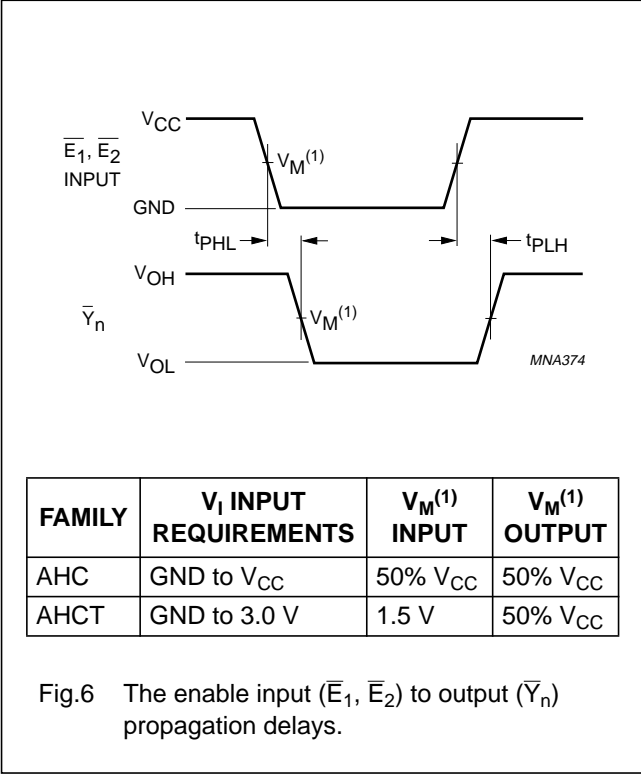
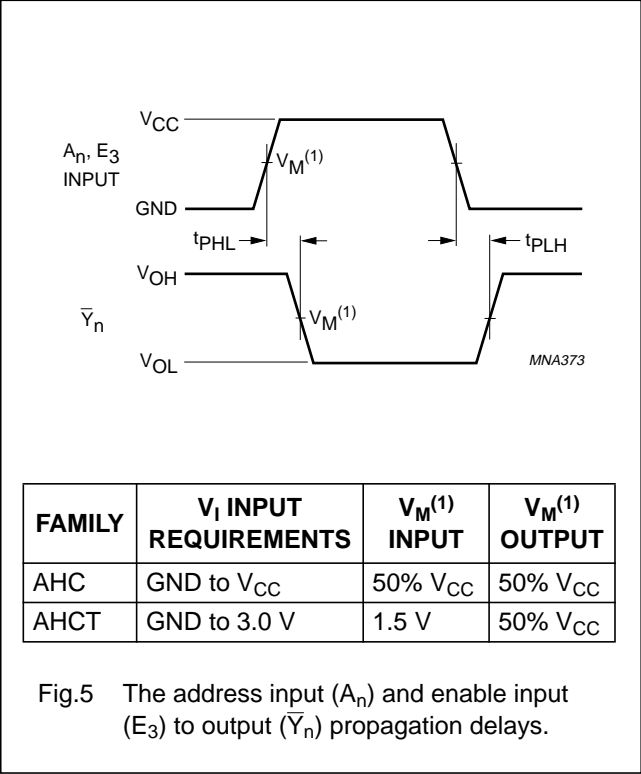
## Note

1. Typical values at  $V_{CC} = 5.0$  V.

3-to-8 line decoder/demultiplexer; inverting

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AC WAVEFORMS



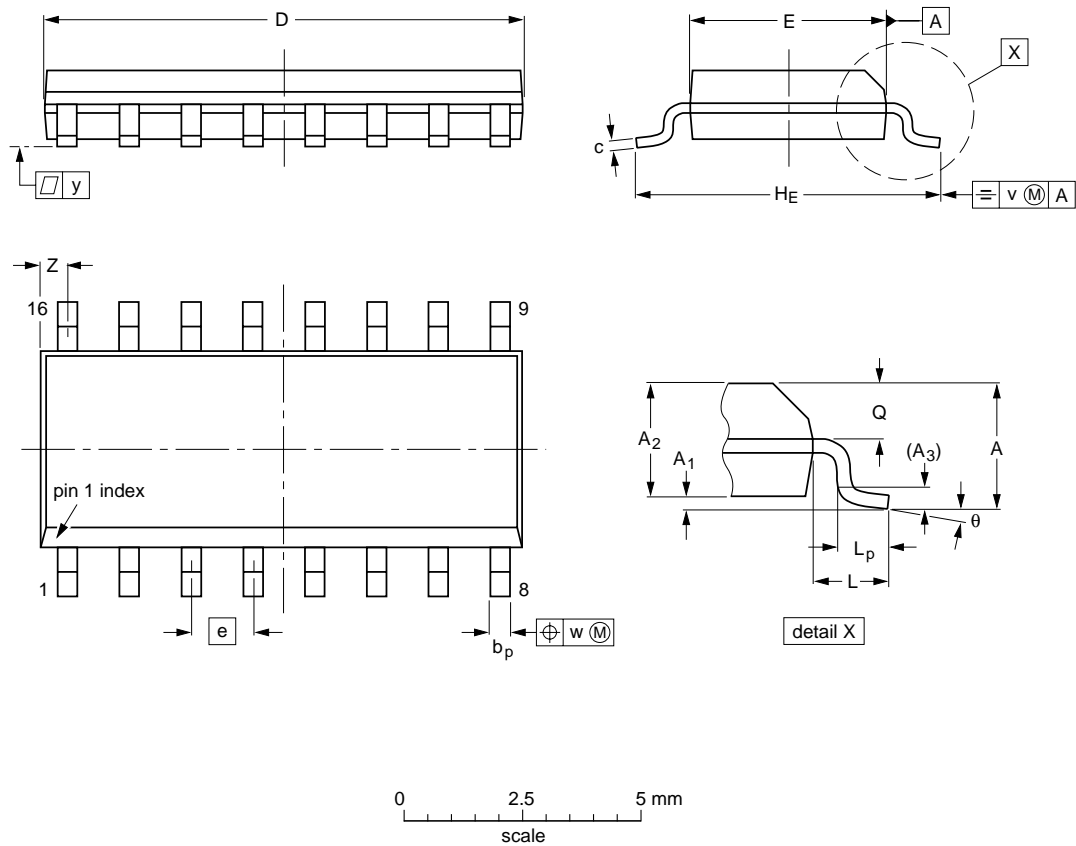
3-to-8 line decoder/demultiplexer; inverting

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74AHCT138

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

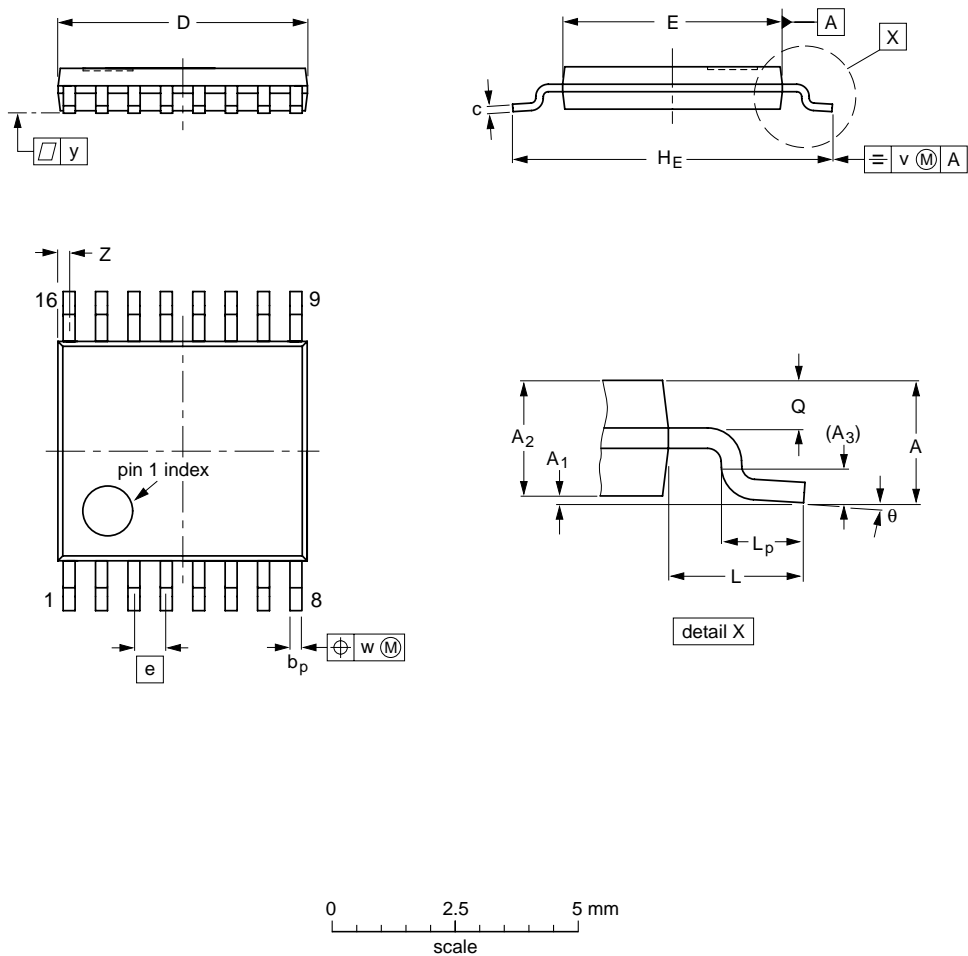
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23- 97-05-22

3-to-8 line decoder/demultiplexer; inverting

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				-94-07-12- 95-04-04

## 3-to-8 line decoder/demultiplexer; inverting

74AHC138;  
74AHCT138

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

## Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

245002/02/pp16

Date of release: 1999 Sep 27

Document order number: 9397 750 06295

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