

# 2SA0885 (2SA885)

## Silicon PNP epitaxial planar type

For low-frequency power amplification

Complementary to 2SC1846

### ■ Features

- Output of 3 W can be obtained by a complementary pair with 2SC1846
- TO-126B package which requires no insulation plate for installation to the heat sink

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	-45	V
Collector-emitter voltage (Base open)	$V_{CEO}$	-35	V
Emitter-base voltage (Collector open)	$V_{EBO}$	-5	V
Collector current	$I_C$	-1	A
Peak collector current	$I_{CP}$	-1.5	A
Collector power dissipation	$P_C$	1.2	W
		5.0 *	
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Note) \*: With a  $100 \times 100 \times 2$  mm Al heat sink

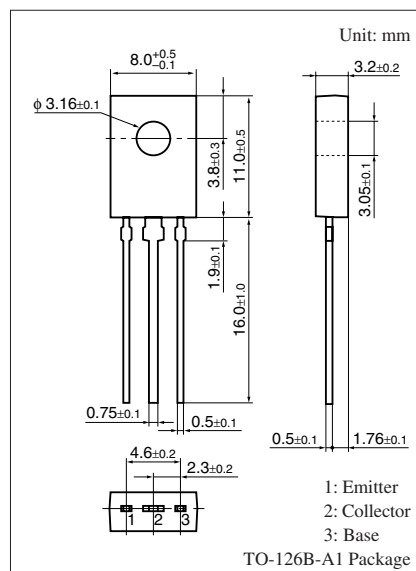
### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = -10 \mu\text{A}$ , $I_E = 0$	-45			V
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = -2 \text{ mA}$ , $I_B = 0$	-35			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = -20 \text{ V}$ , $I_E = 0$			- 0.1	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	$I_{CEO}$	$V_{CE} = -20 \text{ V}$ , $I_B = 0$			-100	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = -5 \text{ V}$ , $I_C = 0$			-10	$\mu\text{A}$
Forward current transfer ratio	$h_{FE1}$ *	$V_{CE} = -10 \text{ V}$ , $I_C = -500 \text{ mA}$	85		340	—
	$h_{FE2}$	$V_{CE} = -5 \text{ V}$ , $I_C = -1 \text{ A}$	50			—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -500 \text{ mA}$ , $I_B = -50 \text{ mA}$			- 0.5	V
Transition frequency	$f_T$	$V_{CE} = -10 \text{ V}$ , $I_E = 50 \text{ mA}$ , $f = 200 \text{ MHz}$		200		MHz
Collector output capacitance (Common base, input open circuited)	$C_{ob}$	$V_{CB} = -10 \text{ V}$ , $I_E = 0$ , $f = 1 \text{ MHz}$		20	30	pF

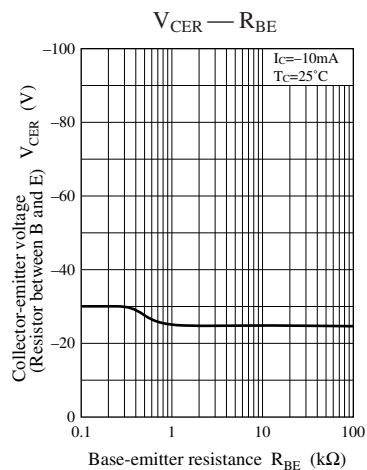
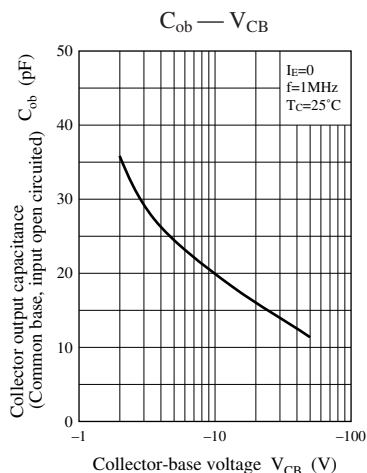
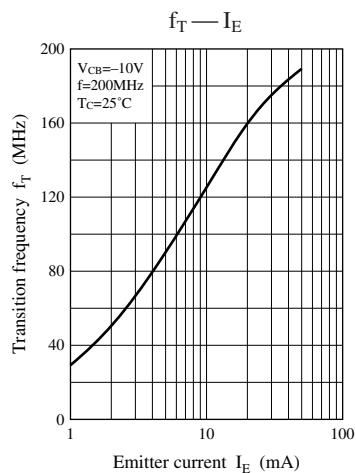
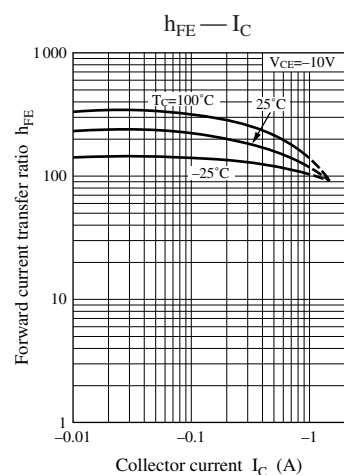
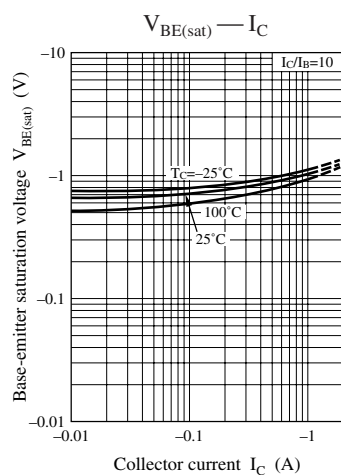
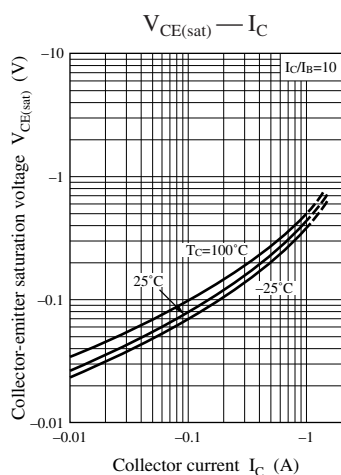
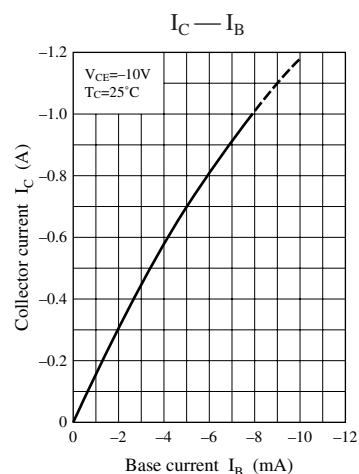
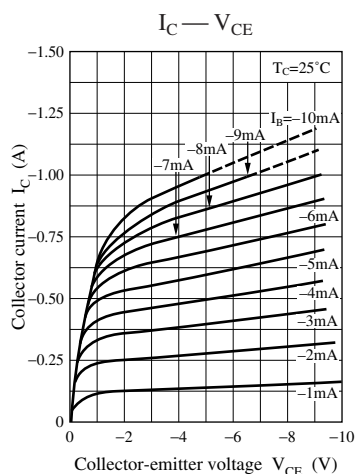
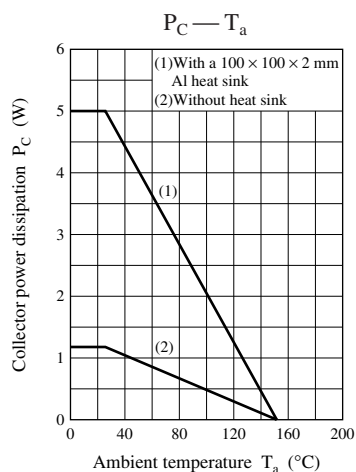
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

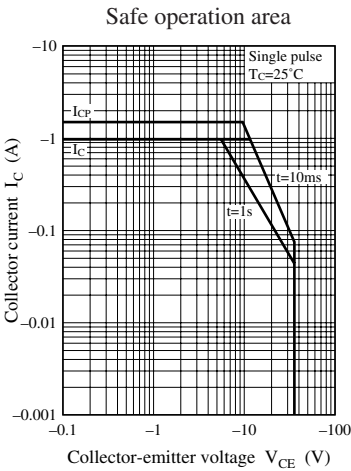
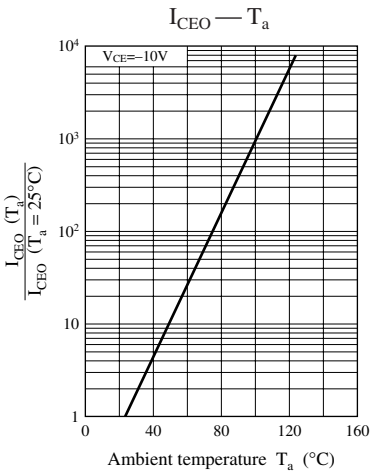
2. \*: Rank classification

Rank	Q	R	S
$h_{FE1}$	85 to 170	120 to 240	170 to 340



Note) The part number in the parenthesis shows conventional part number.





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