

NTTS2P03R2

Power MOSFET -2.48 Amps, -30 Volts P-Channel Enhancement Mode Single Micro8™ Package

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature Micro8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided

Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-30	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Thermal Resistance – Junction-to-Ambient (Note 1.)	$R_{\theta JA}$	160	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.78	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-2.48	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	-1.98	A
Thermal Resistance – Junction-to-Ambient (Note 2.)	$R_{\theta JA}$	70	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.78	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-3.75	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	-3.0	A
Thermal Resistance – Junction-to-Ambient (Note 3.)	$R_{\theta JA}$	210	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.60	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-2.10	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	-1.67	A
Pulsed Drain Current (Note 5.)	I_{DM}	-17	A
Thermal Resistance – Junction-to-Ambient (Note 4.)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.25	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	-3.02	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	-2.42	A
Pulsed Drain Current (Note 5.)	I_{DM}	-24	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. Minimum FR-4 or G-10 PCB, Time ≤ 10 Seconds.
2. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), Time ≤ 10 Seconds.
3. Minimum FR-4 or G-10 PCB, Steady State.
4. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz Cu 0.06" thick single sided), Steady State.
5. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

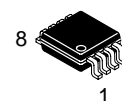
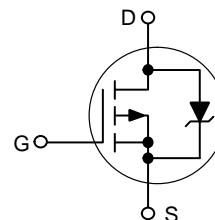


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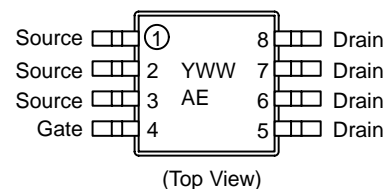
**-2.48 AMPERES
-30 VOLTS
85 m Ω @ $V_{GS} = -10$ V**

Single P-Channel



Micro8
CASE 846A
STYLE 1

MARKING DIAGRAM & PIN ASSIGNMENT



(Top View)

Y = Year
WW = Work Week
AE = Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTTS2P03R2	Micro8	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTTS2P03R2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) (continued)

Rating	Symbol	Value	Unit
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = -30 Vdc, V _{GS} = -10 Vdc, Peak I _L = -3.0 Apk, L = 65 mH, R _G = 25 Ω)	E _{AS}	292.5	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T _L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 6.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = -250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	-30 –	– -30	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{GS} = 0 Vdc, V _{DS} = -30 Vdc, T _J = 25°C) (V _{GS} = 0 Vdc, V _{DS} = -30 Vdc, T _J = 125°C)	I _{DSS}	– –	– –	-1.0 -25	μAdc
Gate-Body Leakage Current (V _{GS} = -20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	-100	nAdc
Gate-Body Leakage Current (V _{GS} = +20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = -250 μAdc) Temperature Coefficient (Negative)	V _{GS(th)}	-1.0 –	-1.7 3.6	-3.0 –	Vdc
Static Drain-to-Source On-State Resistance (V _{GS} = -10 Vdc, I _D = -2.48 Adc) (V _{GS} = -4.5 Vdc, I _D = -1.24 Adc)	R _{DS(on)}	– –	0.063 0.100	0.085 0.135	Ω
Forward Transconductance (V _{DS} = -15 Vdc, I _D = -1.24 Adc)	g _{FS}	–	3.1	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = -24 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	500	–	pF
Output Capacitance		C _{oss}	–	160	–	
Reverse Transfer Capacitance		C _{rss}	–	65	–	

SWITCHING CHARACTERISTICS (Notes 7. & 8.)

Turn-On Delay Time	(V _{DD} = -24 Vdc, I _D = -2.48 Adc, V _{GS} = -10 Vdc, R _G = 6.0 Ω)	t _{d(on)}	–	10	–	ns
Rise Time		t _r	–	20	–	
Turn-Off Delay Time		t _{d(off)}	–	40	–	
Fall Time		t _f	–	35	–	
Turn-On Delay Time	(V _{DD} = -24 Vdc, I _D = -1.24 Adc, V _{GS} = -4.5 Vdc, R _G = 6.0 Ω)	t _{d(on)}	–	16	–	ns
Rise Time		t _r	–	40	–	
Turn-Off Delay Time		t _{d(off)}	–	30	–	
Fall Time		t _f	–	30	–	
Total Gate Charge	(V _{DS} = -24 Vdc, V _{GS} = -4.5 Vdc, I _D = -2.48 Adc)	Q _{tot}	–	15	22	nC
Gate-Source Charge		Q _{gs}	–	3.2	–	
Gate-Drain Charge		Q _{gd}	–	4.0	–	

BODY-DRAIN DIODE RATINGS (Note 7.)

Diode Forward On-Voltage	(I _S = -2.48 Adc, V _{GS} = 0 Vdc) (I _S = -2.48 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	– –	-0.92 -0.72	-1.3 –	Vdc
Reverse Recovery Time	(I _S = -1.45 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs)	t _{rr}	–	38	–	ns
		t _a	–	20	–	
		t _b	–	18	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.04	–	μC

6. Handling precautions to protect against electrostatic discharge is mandatory.
7. Indicates Pulse Test: Pulse Width = 300 μsec max, Duty Cycle = 2%.
8. Switching characteristics are independent of operating junction temperature.

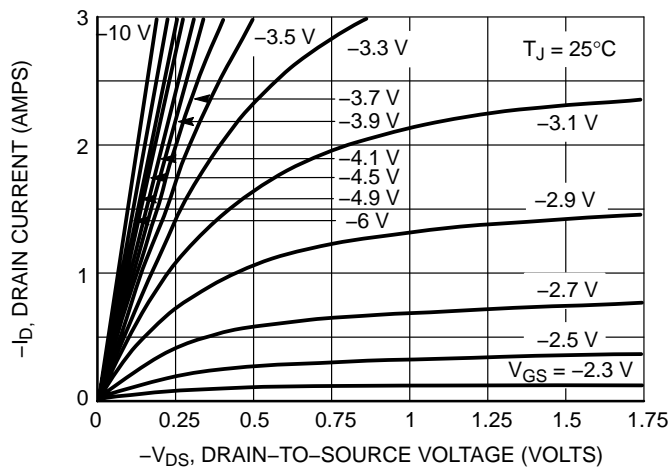


Figure 1. On-Region Characteristics

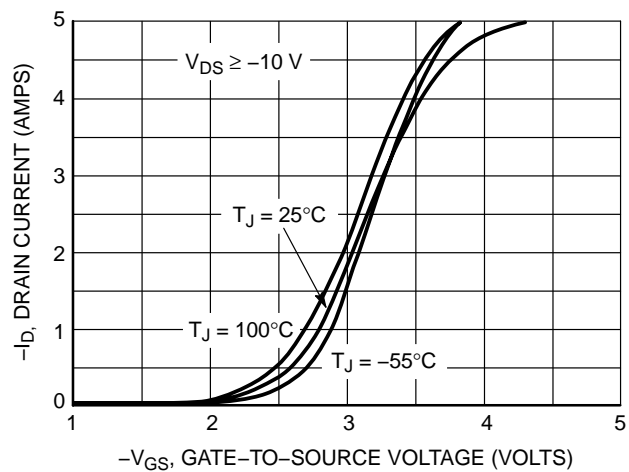


Figure 2. Transfer Characteristics

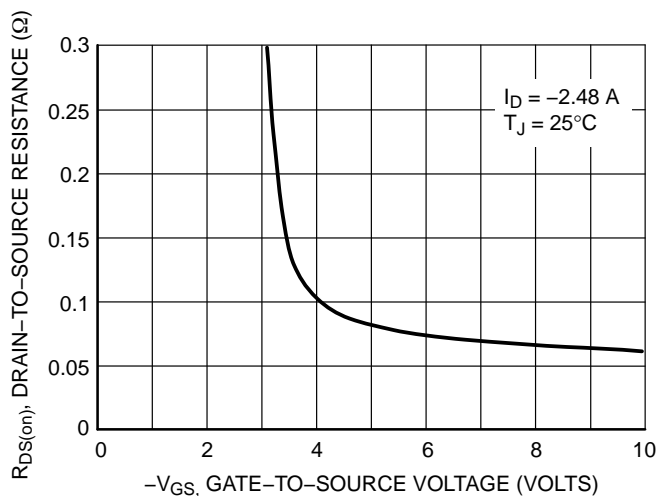


Figure 3. On-Resistance versus Gate-to-Source Voltage

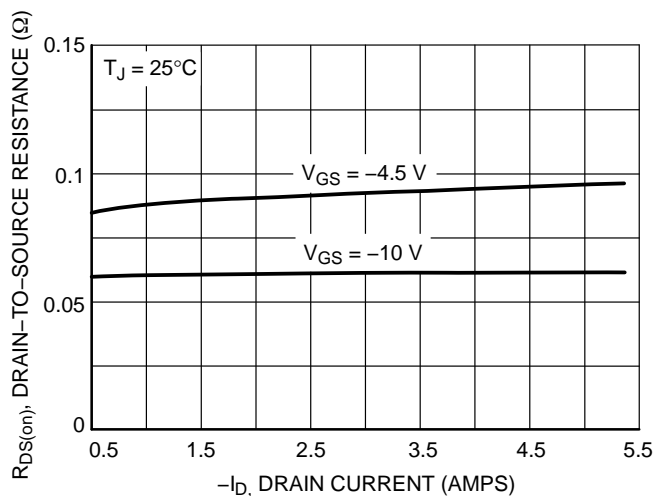


Figure 4. On-Resistance versus Drain Current and Gate Voltage

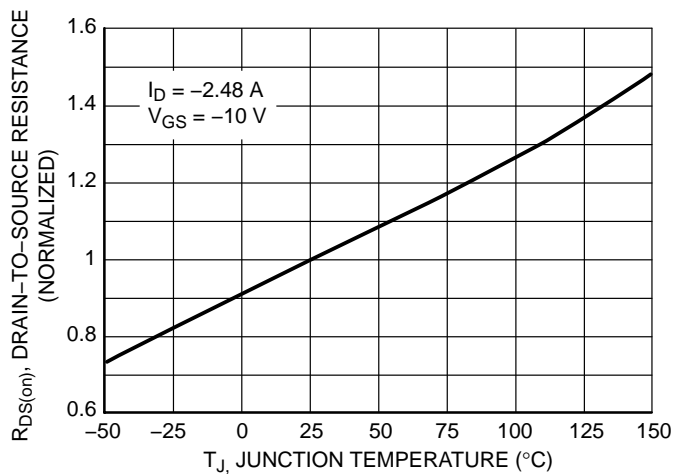


Figure 5. On-Resistance Variation with Temperature

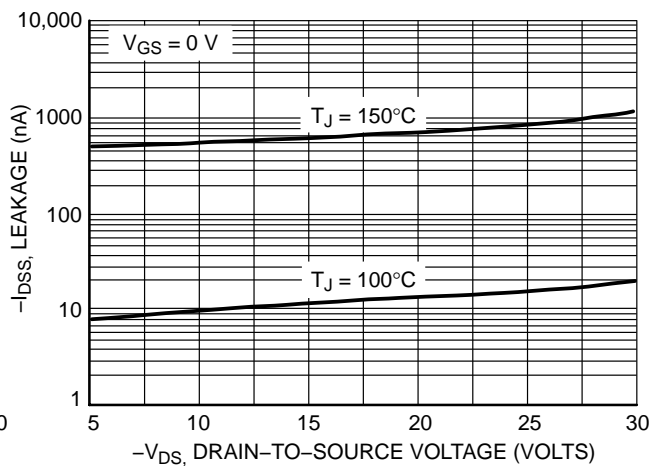


Figure 6. Drain-to-Source Leakage Current versus Voltage

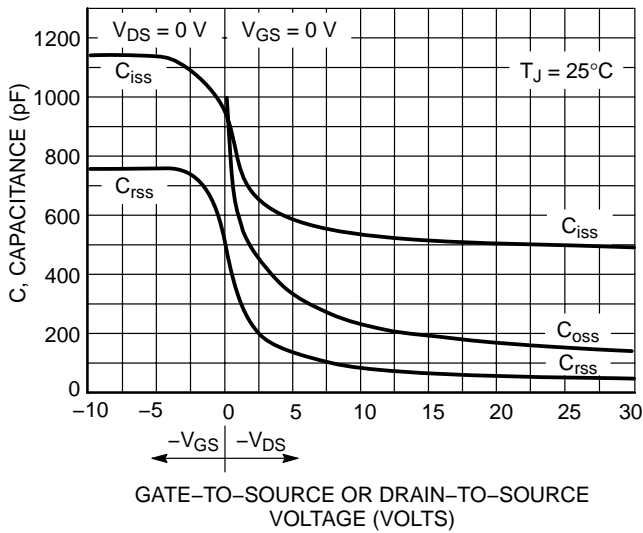


Figure 7. Capacitance Variation

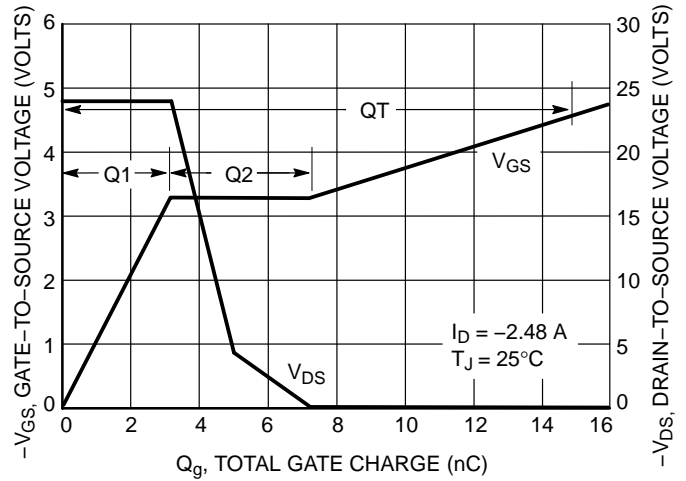


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

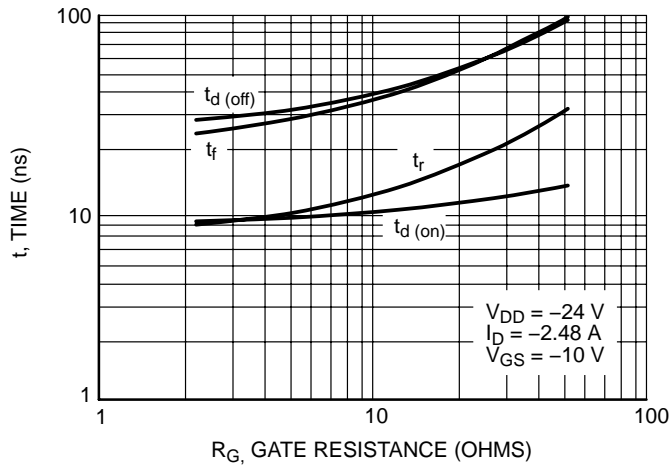


Figure 9. Resistive Switching Time Variation versus Gate Resistance

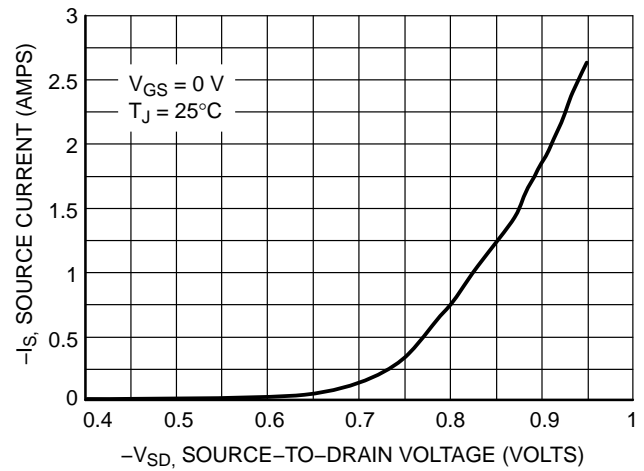


Figure 10. Diode Forward Voltage versus Current

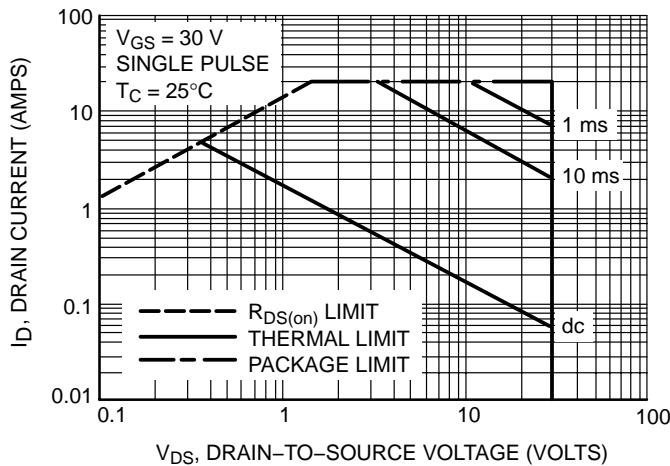


Figure 11. Maximum Rated Forward Biased Safe Operating Area

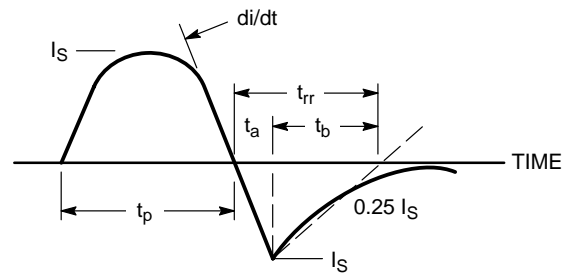


Figure 12. Diode Reverse Recovery Waveform

TYPICAL ELECTRICAL CHARACTERISTICS

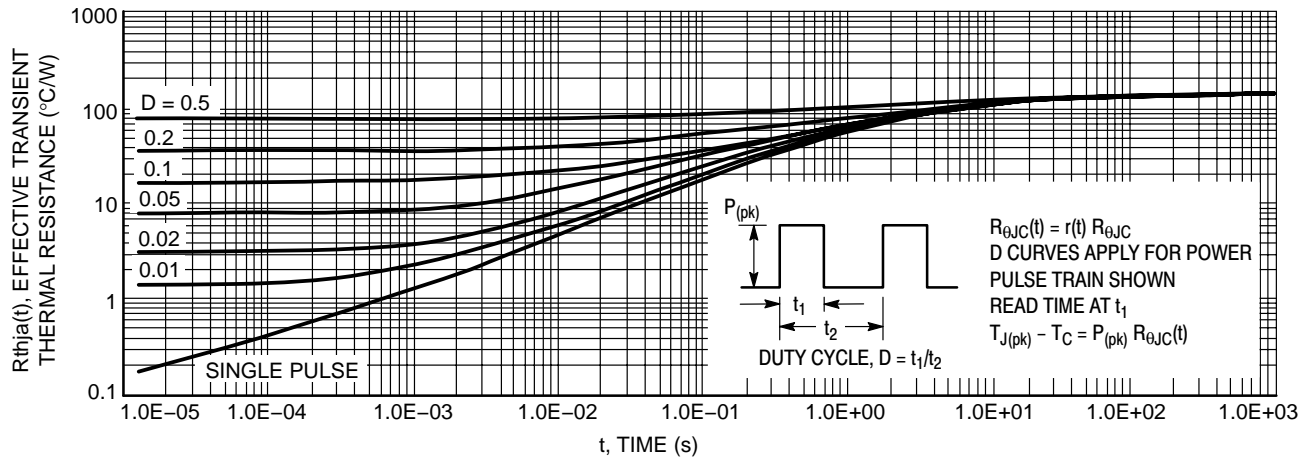
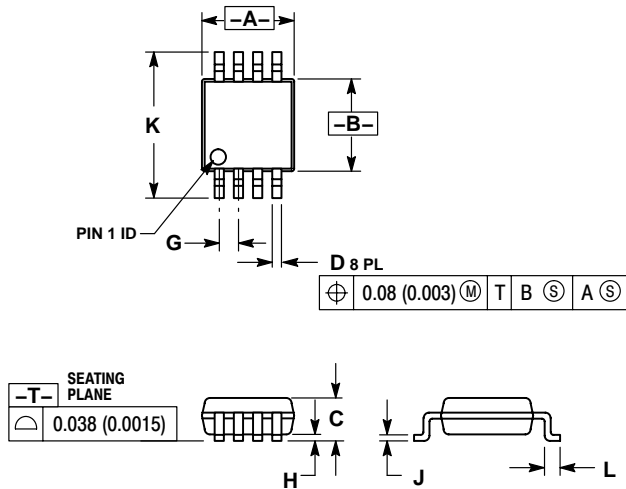


Figure 13. Thermal Response

NTTS2P03R2

PACKAGE DIMENSIONS

Micro8
CASE 846A-02
ISSUE F

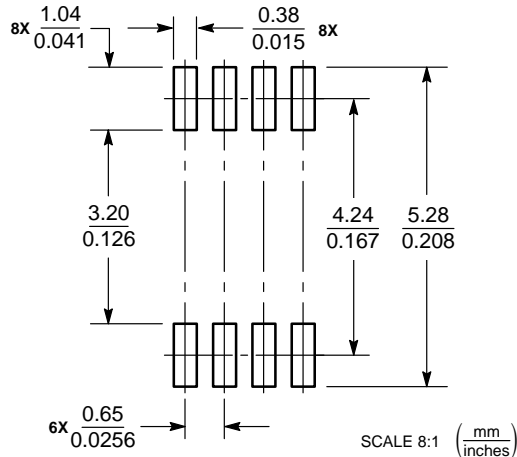


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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