OKI Semiconductor

FEDL2250DIGEST-01
Issue Date: Oct. 15, 2002

ML2252/54-XXX, ML22Q54

2-Channel Mixing Oki ADPCM Algorithm-Based Speech Synthesis LSI

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

GENERAL DESCRIPTION

The ML2250 family is a 2-channel mixing speech synthesis device with an on-chip voice data (i.e., phrases) storing mask ROM and a flash memory. Besides playing the built-in voice data, this device can output voice data that is input from outside the device. This ML2250 family allows to select the playback method from the 8-bit PCM, non-linear 8-bit PCM, 16-bit PCM, 2-bit ADPCM2, and 4-bit ADPCM2 algorithms. And the sound volume is adjustable as well.
The ML2250 family incorporates a 14-bit D/A converter, low-pass filter, and 1-bit DAC (PWM output).
It is easy to configure a speech synthesizer by externally connecting a power amplifier and a CPU to the ML2250 family.
The ML2250 family line-up includes 2 types of products: with on-chip mask ROM, and with on-chip flash memory.

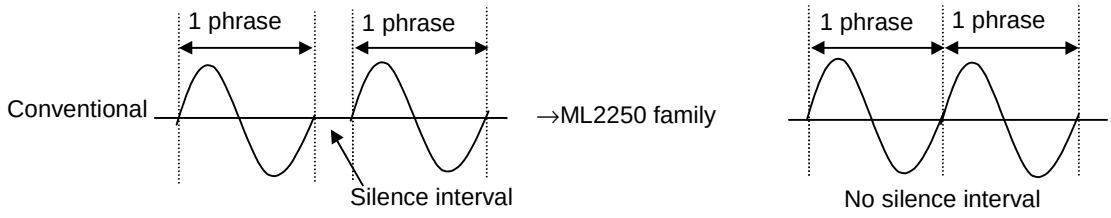
- ML2252/54-XXX
  This is a CMOS single chip speech synthesis device with an on-chip mask ROM. Products with 2 types of mask ROMs are available in the ML2250 family depending upon the total playback time length.

- ML22Q54
  The ML22Q54 is a speech synthesis device with a 4-Mbit flash memory built in. The voice data can be easily written to the flash memory using a special tool. The on-chip flash memory product is suitable for the diversified low volume production or short delivery time applications that the on-chip mask ROM product cannot support. The ML22Q54 is most suitable for evaluation because the circuit configuration is the same as the on-chip mask ROM product.
  A combination of fixed and variable messages can be written because it is easy to write to the built-in flash memory. It is also possible to store and read data, other than voice, to/from an area in the flash memory not used as voice data.

Table below summarizes the points of difference between the ML2250 family and currently manufactured products with a ROM built in.

	ML2250 family	MSM6650 family	MSM9800 family	ML2210 family
Interface	Parallel or serial	Parallel, serial or stand-alone	Parallel or stand-alone	Serial
Playback method	2-bit ADPCM2 4-bit ADPCM2 8-bit PCM 8-bit non-linear PCM 16-bit PCM	4-bit ADPCM 8-bit PCM	8-bit PCM 8-bit non-linear PCM	4-bit ADPCM 8-bit PCM 8-bit non-linear PCM
Max. number of phrases	256	127	63	247
Sampling frequency (kHz)	4.0/5.3/6.4/8.0/10.7/ 12.8/16.0/21.3/25.6/ 32.0/42.7/48.0	4.0/5.3/6.4/8.0/10.7/ 12.8/16.0/32.0	4.0/5.3/6.4/8.0/10.7/ 12.8/16.0	4.0/5.3/6.4/8.0/10.7/ 12.8/16.0
Clock frequency	4.096 MHz	256 kHz (CR oscillation) 4.096 MHz (XT)	256 kHz (CR oscillation) 4.096 MHz (XT)	4.096 MHz
D/A converter	1-bit DAC PWM Voltage type: 14 bits	Voltage type: 12 bits	Current type: 10 bits	Current type: 12 bits
Low-pass filter	FIR type interpolation filter	Secondary comb filter	Primary comb filter	Secondary comb filter
Number of channels	2 channels	2 channels	1 channel	1 channel
Phrase control table	Both 2 channels without user definable phrase restrictions	Can edit 8 phrases (1 channel only)	Can edit 8 phrases	None
Volume adjustment	29 steps (–2 dB/–5 dB steps)	4 steps (–6 dB steps)	Set at VREF.	Set at VREF.
Repeat function	No limit	4 types	None	None
STOP	Each channel independent	Simultaneous channels 1 and 2	Available	Available
Seam silence interval in continuous playback	0 (Note)	4 sampling cycles	3 sampling cycles	4 sampling cycles
Others	External data input possible	—	—	—

Note: Continuous playback shown in the figure below is possible.



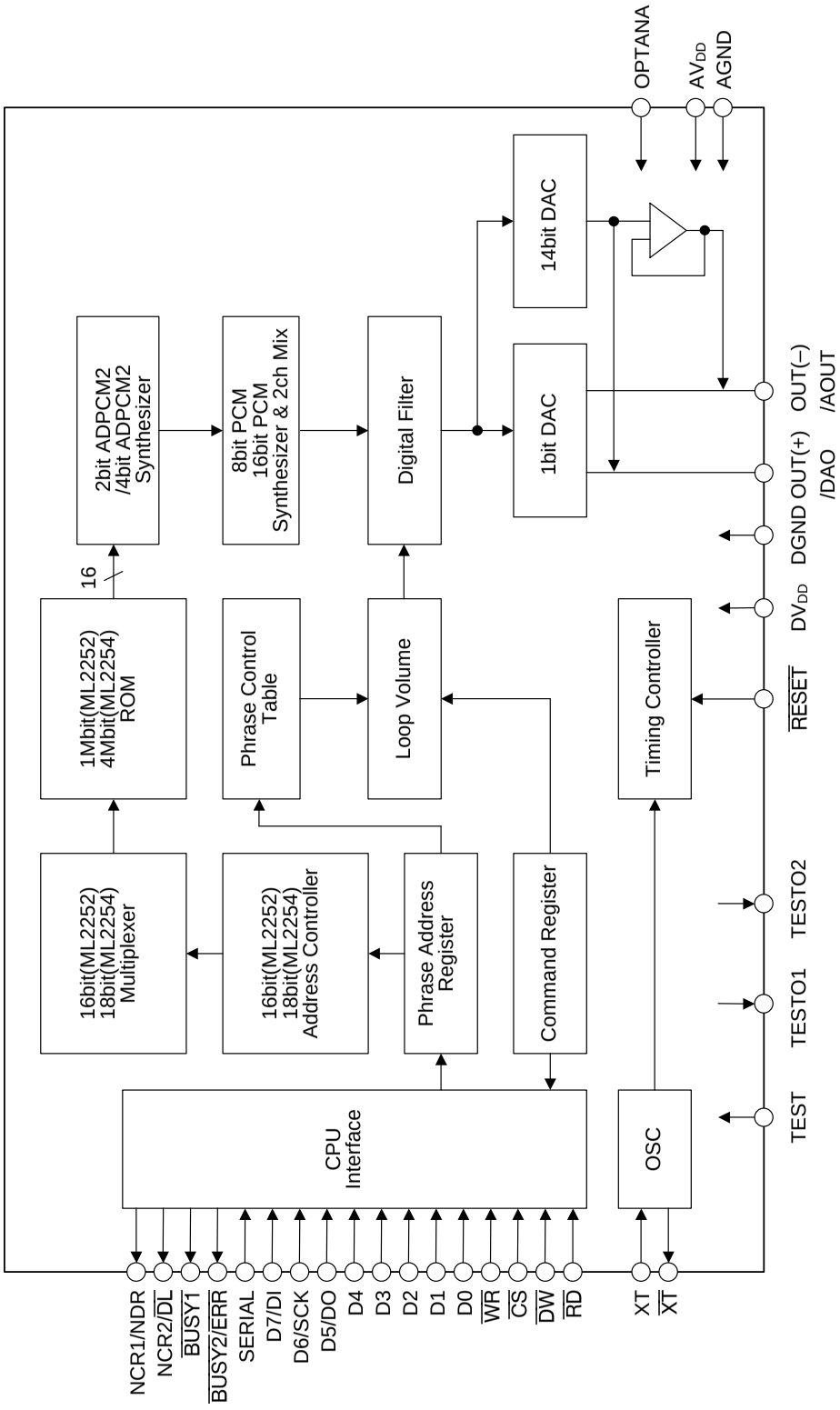
FEATURES

Type	ROM capacity	Maximum playback time length (sec) (In 4-bit ADPCM2)				
		F_{SAM} = 4.0 kHz	F_{SAM} = 6.4 kHz	F_{SAM} = 8.0 kHz	F_{SAM} = 16 kHz	F_{SAM} = 32 kHz
ML2252	1 Mbit	64.5	40.3	32.2	16.1	8.0
ML2254	4 Mbit	261.1	163.2	130.5	65.2	32.6
ML22Q54	4 Mbit	261.1	163.2	130.5	65.2	32.6

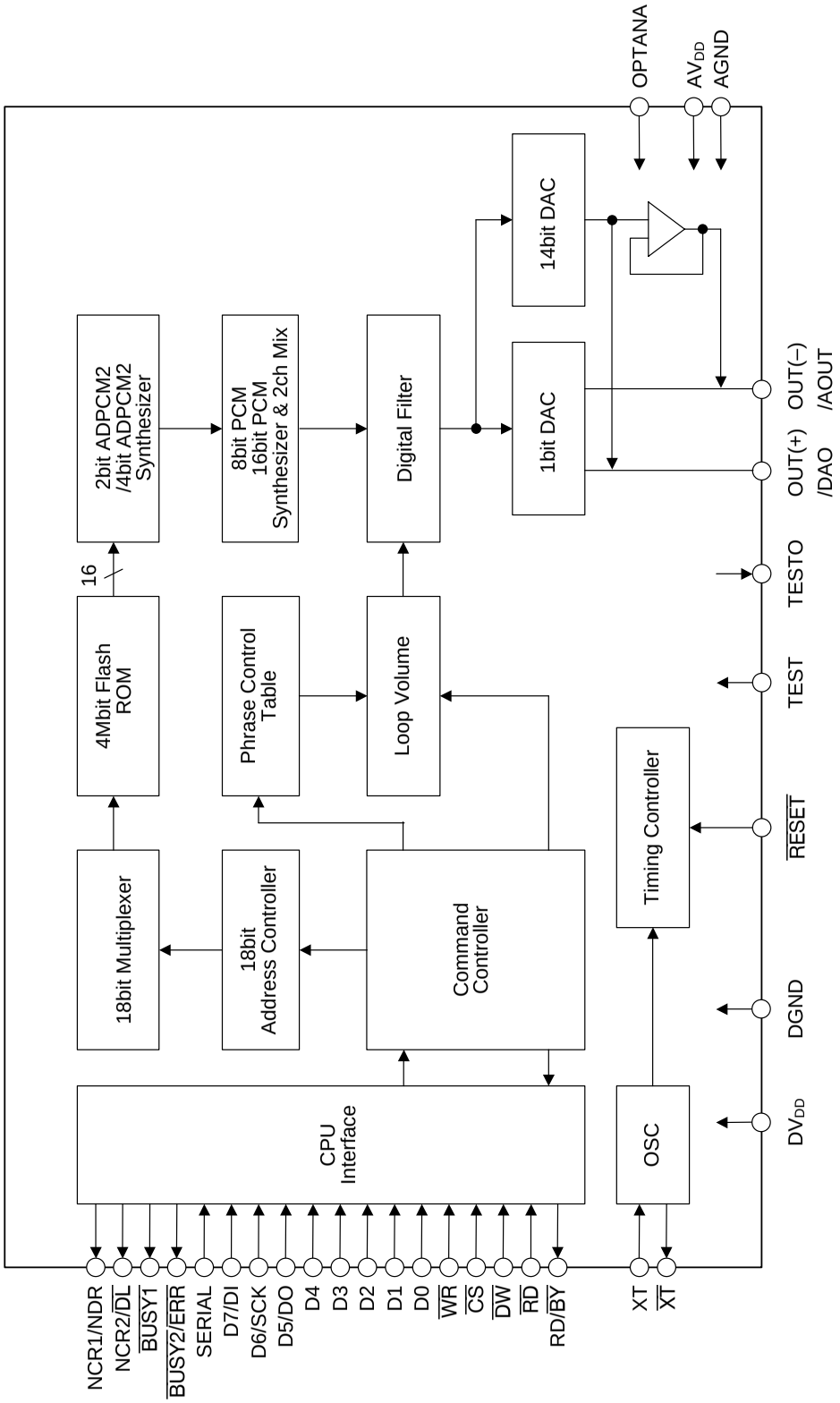
- Non-linear 8-bit PCM, 8-bit PCM, 16-bit PCM, 2-bit ADPCM2, and 4-bit ADPCM2 algorithms
- Serial input/parallel input selectable
- Phrase control table function i.e., user definable phrase control table function
- 2 channels mixing function
- Master clock frequency: 4.096 MHz
- Sampling frequency: 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.7 kHz, 12.8 kHz, 16.0 kHz, 21.3 kHz, 25.6 kHz, 32.0 kHz, 42.7 kHz, 48 kHz
- Maximum number of phrases: 256 phrases
- Sound volume adjustment function built in (2 sounds independently adjustable in 29 steps)
- External voice data can be input
- 1-bit D/A converter, and14-bit D/A converter built in
- Built-in low-pass filter: Digital filter
- Package: 44-pin plastic QFP (QFP44-P-910-0.80-2K)
  (ML2252-XXXGA/ML2254-XXXGA/ML22Q54GA-MC)

BLOCK DIAGRAM

ML2252/54-XXX



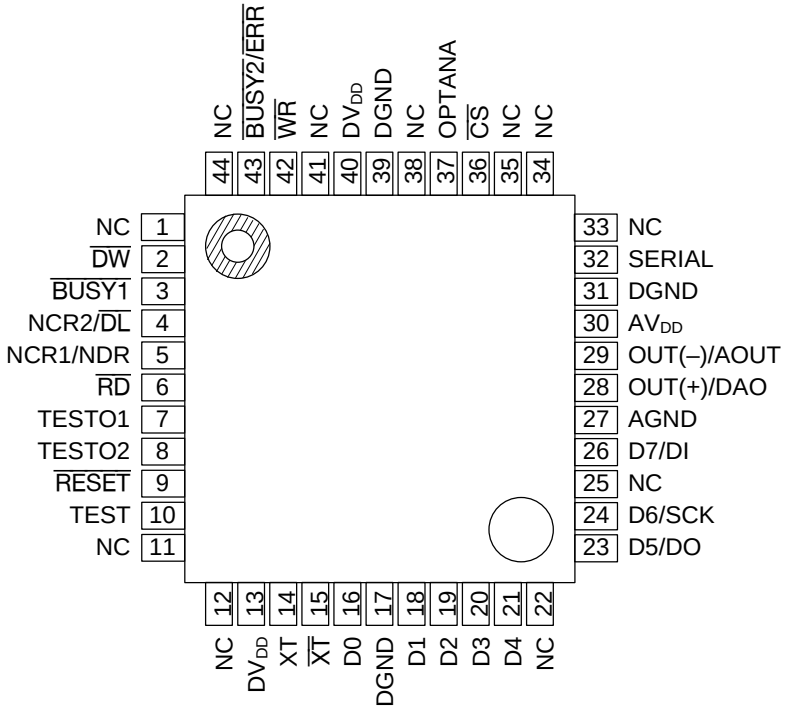
ML22Q54


OPTANA
AVDD
AGND
14bit DAC
1bit DAC
2bit ADPCM2
/4bit ADPCM2
Synthesizer
8bit PCM
16bit PCM
Synthesizer & 2ch Mix
Digital Filter
16
4Mbit Flash
ROM
Phrase Control
Table
Loop Volume
18bit Multiplexer
18bit
Address Controller
Command
Controller
Timing Controller
CPU
Interface
OSC
OUT(–)
/AOUT
OUT(+)
/DAO
TESTO
TEST
RESET
DGND
DVDD
NCR1/NDR
NCR2/DL
BUSY1
BUSY2/ERR
SERIAL
D7/DI
D6/SCK
D5/DO
D4
D3
D2
D1
D0
WR
CS
DW
RD
RD/BY
XT
XT

PIN CONFIGURATION (TOP VIEW)

ML2252/54-XXX

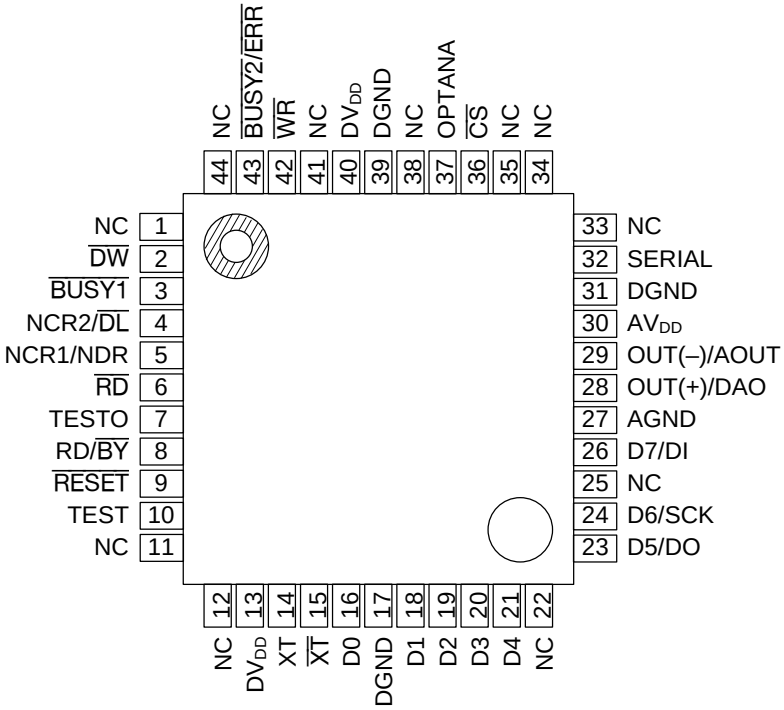
44-pin plastic QFP



NC: No Connection

ML22Q54

44-pin plastic QFP



NC: No Connection

PIN DESCRIPTIONS-1

ML2252/54-XXX Common Pins
44-pin plastic QFP

Pin	Symbol	Type	Description
43	$\overline{\text{BUSY2}}/\overline{\text{ERR}}$	O	When using the built-in ROM for voice output, this pin outputs "L" level while channel 2 side processes a command and while plays back voice. Works as $\overline{\text{ERR}}$ pin when using the EXT command for voice output. If an abnormality occurred in the transfer of data, the pin will output "L" level and the voice output may become noisy. "H" level at power on.
3	$\overline{\text{BUSY1}}$	O	Outputs "L" level while the channel 1 side processes a command and plays back voice. "H" level at power on.
4	NCR2/$\overline{\text{DL}}$	O	The command input of channel 2 side is valid at "H" level when using the built-in ROM for voice output. Works as $\overline{\text{DL}}$ pin when using EXT command for the voice output. This pin outputs the signal that captures voice data to inside. The data is captured inside on the rising edge of $\overline{\text{DL}}$. "H" level at power on.
5	NCR1/NDR	O	The command input of channel 1 side is valid at "H" level when using the built-in ROM for voice output. Works as NDR pin when using EXT command for the voice output. The voice data input is valid at "H" level. "H" level at power on.
9	$\overline{\text{RESET}}$	I	At "L" level input, the device enters the initial state; the oscillation stops, and AOUT output and DAQ output are GND level at this time.
10	TEST	I	Test pin for the device. Input "L" level to this pin. This pin has a pull-down resistor built in.
14	XT	I	Wired to a crystal or ceramic oscillator. A feedback resistor of around 1 MΩ is built in between this XT pin and $\overline{\text{XT}}$ pin (pin 15). When using an external clock, input the clock from this pin.
15	$\overline{\text{XT}}$	O	Wired to a ceramic or crystal oscillator. When using an external clock, keep this pin open.
16, 18, 19, 20	D3 D2 D1 D0	I/O	CPU interface data bus pins in the parallel input interface. Channel status output pins at $\overline{\text{RD}}$ pin = "L" level. In the serial input interface, keep these pins at "L" level.
21	D4	I/O	CPU interface data bus pin in the parallel input interface. When $\overline{\text{RD}}$ pin is at "L" level, this pin D4 usually outputs "L" level. In the serial input interface, keep this pin at "L" level.
23	D5/DO	I/O	CPU interface data bus pin in the parallel input interface. When $\overline{\text{RD}}$ pin is at "L" level, this D5/DO pin usually outputs "L" level. Works as channel status output pin in the serial interface. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pins are "L" level, the status of each channel is output serially from this D5/DO pin in synchronization with SCK clock.

Pin	Symbol	Type	Description
24	D6/SCK	I/O	CPU interface data bus pin in the parallel input interface. Usually outputs "L" level when $\overline{RD}$ = "L" level. Works as serial clock input pin in the serial input interface. When the SCK input is at "L" level on the falling edge of $\overline{CS}$, the DI input is captured in the device on the rising edge of SCK clock. And when the SCK input is at "H" level on the falling edge of $\overline{CS}$, the DI input is captured on the falling edge of SCK clock.
26	D7/DI	I/O	CPU interface data bus pin in the parallel input interface. Usually output "L" level when $\overline{RD}$ is at "L" level. Works as serial data input pin in the serial input interface.
28	OUT(+)/DAO	O	When OPTANA pin is at "H" level, this OUT(+)/DAO pin outputs PWM (positive phase) of 1-bit DAC. When OPTANA pin is at "L" level, the OUT(+)/DAO pin outputs analog signal of 14-bit DAC.
29	OUT(–)/AOUT	O	When OPTANA pin is at "H" level, this OUT(–)/AOUT pin outputs PWM (reverse phase) of 1-bit DAC. When OPTANA pin is at "L" level, the OUT(–)/AOUT pin usually outputs the analog signal of 14-bit DAC via voltage follower.
32	SERIAL	I	CPU interface switching pin. Serial input interface at "H" level. And parallel input interface at "L" level.
36	$\overline{CS}$	I	CPU interface chip select pin. When $\overline{CS}$ pin is at "H" level, the $\overline{WR}$, $\overline{DW}$, and $\overline{RD}$ signals cannot be input to the device.
37	OPTANA	I	Analog output/PWM output select signal. When OPTANA pin is at "H" level, the PWM of 1-bit DAC outputs from OUT(+)/DAO and OUT(–)/AOUT pins. When OPTANA pin is at "L" level, the analog signal of 14-bit DAC is output from OUT(+)/DAO pin and from OUT(–)/AOUT pin via voltage follower.
42	$\overline{WR}$	I	CPU interface write signal. When $\overline{CS}$ pin is at "H" level, the $\overline{WR}$ signal cannot be input to the device.
2	$\overline{DW}$	I	Data write signal when using EXT command for the voice output. Set the pin to "H" level when not using EXT command. When $\overline{CS}$ pin is at "H" level, the $\overline{DW}$ signal cannot be input to the device. This pin has a pull-up resistor built in.
6	$\overline{RD}$	I	CPU interface read signal. When $\overline{CS}$ pin is at "H" level, the $\overline{RD}$ signal cannot be input to the device. This pin has a pull-up resistor built in.
7, 8	TESTO1 TESTO2	O	Output pin for testing. Keep this pin open.
30	AV_{DD}	—	Analog power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and AGND pin.
13, 40	DV_{DD}	—	Digital power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and DGND pin.
27	AGND	—	Analog ground pin.
17, 31, 39	DGND	—	Digital ground pin.

PIN DESCRIPTIONS-2

ML22Q54 Pins
44-pin plastic QFP

Pin	Symbol	Type	Description
43	$\overline{\text{BUSY2}}/\overline{\text{ERR}}$	O	When using the built-in ROM for voice output, this pin outputs "L" level while channel 2 side processes a command and while plays back voice. Works as $\overline{\text{ERR}}$ pin when using EXT command for the voice output. If an abnormality occurred in the transfer of data, the $\overline{\text{ERR}}$ pin outputs "L" level and the voice output may become noisy. "H" level at power on.
3	$\overline{\text{BUSY1}}$	O	Outputs "L" level while the channel 1 side processes a command and while plays back voice. "H" level at power on.
4	NCR2/$\overline{\text{DL}}$	O	The input command of channel 2 is valid at "H" level when using the built-in ROM for voice output. $\overline{\text{DL}}$ pin when using EXT command for the voice output. It outputs the voice data capture signal. The data is captured on the rising edge of $\overline{\text{DL}}$. "H" level at power on.
5	NCR1/NDR	O	The command input of channel 1 side is valid at "H" level when using the built-in ROM for voice output. NDR pin when using EXT command for the voice output. The voice data input is effective at "H" level. "H" level at power on.
9	$\overline{\text{RESET}}$	I	When "L" level is input to this pin, the device is reset, the oscillation stops, and AOUT and DAQ outputs go into GND level.
10	TEST	I	Test pin for the device. Input "L" level to this pin. This pin has a pull-down resistor built in.
14	XT	I	Wired to a crystal or ceramic oscillator. A feedback resistor of around 1 MΩ is built in between this XT pin and $\overline{\text{XT}}$ pin (pin 15). When using an external clock, input the clock from this pin.
15	$\overline{\text{XT}}$	O	Wired to a ceramic or crystal oscillator. When using an external clock, keep this pin open.
16, 18, 19, 20	D3 D2 D1 D0	I/O	CPU interface data bus pins in the parallel input interface. Channel status output pins when $\overline{\text{RD}}$ is at "L" level. The pins output the flash memory data when reading the built-in flash memory data. In the serial input interface, keep these pins at "L" level.
21	D4	I/O	CPU interface data bus pin in the parallel input interface. The pin outputs flash memory data when reading the built-in flash memory data. When $\overline{\text{RD}}$ is at "L" level other than when reading the flash memory data, this pin usually outputs "L" level. In the serial input interface, keep this pin at "L" level.
23	D5/DO	I/O	CPU interface data bus pin in the parallel input interface. The pin outputs flash memory data when reading the built-in flash memory data. When $\overline{\text{RD}}$ is at "L" level other than when reading the flash memory data, this pin usually outputs "L" level. Channel status output pin in the serial input interface. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are at "L" level, this D5/DO pin serially outputs the status of each channel in synchronization with SCK clock. When reading data of the built-in flash memory, the pin will output serially the flash memory data.

Pin	Symbol	Type	Description
24	D6/SCK	I/O	Works as CPU interface data bus pin in parallel input interface. Works as flash memory data output pin when reading the built-in flash memory data. When $\overline{RD}$ is at "L" level other than when reading the flash memory data, this D6/SCK pin usually outputs "L" level. Works as serial clock input pin in the serial input interface. When the SCK input is at "L" level on the falling edge of $\overline{CS}$, the DI input is captured in device on the rising edge of SCK clock. And when the SCK input is at "H" level on the falling edge of $\overline{CS}$, the DI input is captured on the falling edge of SCK clock.
26	D7/DI	I/O	Works as CPU interface data bus pin in the parallel input interface. Works as flash data output pin when reading the built-in flash memory data. When $\overline{RD}$ is at "L" level at times other than reading the flash memory data, this D7/DI pin usually outputs "L" level. Works as serial data input pin in the serial input interface.
28	OUT(+)/DAO	O	When OPTANA pin is at "H" level, this OUT(+)/DAO pin outputs PWM (positive phase) of 1-bit DAC. And when OPTANA pin is at "L" level, the OUT(+)/DAO pin outputs the 14-bit DAC analog signal.
29	OUT(–)/AOUT	O	When OPTANA pin is at "H" level, this OUT(–)/AOUT pin outputs PWM (reverse phase) of 1-bit DAC. And when OPTANA pin is at "L" level, the OUT(–)/AOUT pin outputs the 14-bit DAC analog signal via voltage follower.
32	SERIAL	I	CPU interface switching pin. At "H" level: Serial input interface. At "L" level: Parallel input interface.
36	$\overline{CS}$	I	CPU interface chip select pin. When $\overline{CS}$ pin is at "H" level, the $\overline{WR}$, $\overline{DW}$, and $\overline{RD}$ signals cannot be input to the device.
37	OPTANA	I	Analog output/PWM output select signal. At OPTANA pin = "H" level, PWM of 1-bit DAC is output from OUT(+)/DAO and OUT(–)/AOUT pins. At OPTANA pin = "L" level, 14-bit DAC analog signal is output from OUT(+)/DAO pin and 14-bit DAC analog signal is output from OUT(–)/AOUT pin via the voltage follower.
42	$\overline{WR}$	I	CPU interface write signal. When $\overline{CS}$ pin is at "H" level, the $\overline{WR}$ signal cannot be input to the device.
2	$\overline{DW}$	I	Data write signal at EXT command and Flash I/F command. When the EXT and Flash I/F commands are not used, keep this pin at "H" level. When $\overline{CS}$ pin is at "H" level, the $\overline{DW}$ signal cannot be input to the device. This pin has a pull-up resistor built in.
6	$\overline{RD}$	I	CPU interface read signal. This pin is used when reading the status signal of each channel or when reading data of the built-in flash memory. When not in use, keep this pin to "H" level. This pin has a pull-up resistor built in.
7	TESTO	O	Output pin for testing. Keep this pin open.
8	RD/BY	O	Output pin to indicate the automatic erase/write status of the built-in flash memory. Outputs "L" level during erase or programming cycle to indicate the busy state. Goes to "H" level at the end of the erase or programming cycle and enters into the ready state.

Pin	Symbol	Type	Description
30	AV_{DD}	—	Analog power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and AGND pin.
13, 40	DV_{DD}	—	Digital power supply pin. Insert a 0.1 μF or larger bypass capacitor between this pin and DGND pin.
27	AGND	—	Analog ground pin.
17, 31, 39	DGND	—	Digital ground pin.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (3 V)

ML2252/54-XXX, ML22Q54

(GND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	—	2.7 to 3.6			V
Operating temperature	T_{OP}	ML2252/54-XXX	–40 to +85			°C
		ML22Q54	0 to +70			
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

RECOMMENDED OPERATING CONDITIONS (5 V)

ML2252/54-XXX

(GND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	—	4.5 to 5.5			V
Operating temperature	T_{OP}	—	–40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	

ELECTRICAL CHARACTERISTICS

DC Characteristics (3 V)

ML2252/54-XXX, ML22Q54

ML2252/54-XXX: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C
ML22Q54: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	0.86 × V_{DD}	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.14 × V_{DD}	V
"H" output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} –0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	V_{IH} = V_{DD}	—	—	10	µA
"H" input current 2 (Note 1)	I_{IH2}	V_{IH} = V_{DD}	0.3	2.0	15	µA
"H" input current 3 (Note 2)	I_{IH3}	V_{IH} = V_{DD} Pull-down resistor built in pin	8	40	130	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (Note 3)	I_{IL2}	V_{IL} = GND Pull-up resistor built in pin	–120	–40	–10	µA
"L" input current 3 (Note 1)	I_{IL3}	V_{IL} = GND	–15	–2.0	–0.3	µA
Playback Operating current consumption 1	I_{DD1}	f_{OSC} = 4.096 MHz at no load OPTANA = "L"	—	9	35	mA
Playback Operating current consumption 2	I_{DD2}	f_{OSC} = 4.096 MHz at no load OPTANA = "H"	—	10	35	mA
Buit-in Flash memory access Operating current consumption 1	I_{DD2}	f_{OSC} = 4.096 MHz at no load Read Operation (ML22Q54)	—	10	35	mA
Buit-in Flash memory access Operating current consumption 2	I_{DD2}	f_{OSC} = 4.096 MHz at no load Write and Erase Operation (ML22Q54)	—	20	60	mA
Standby current consumption	I_{DDS}	Ta = –40 to +70°C	—	—	15	µA
		Ta = –40 to +85°C	—	—	50	µA
		Ta = 0 to +70°C (ML22Q54)	—	—	55	µA

Notes: 1. Applies to XT pin.
2. Applies to TEST pin.
3. Applies to $\overline{RD}$ and $\overline{DW}$ pins.

DC Characteristics (5 V)
ML2252/54-XXX

DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.8 \times V_{DD}$	—	—	V
"L" input voltage	V_{IL}	—	—	—	$0.2 \times V_{DD}$	V
"H" output voltage	V_{OH}	I_{OH} = –1 mA	V_{DD} –0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" input current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" input current 2 (Note 1)	I_{IH2}	$V_{IH} = V_{DD}$	0.8	5.0	20	µA
"H" input current 3 (Note 2)	I_{IH3}	$V_{IH} = V_{DD}$ Pull-down resistor built in pin	30	—	350	µA
"L" input current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" input current 2 (Note 3)	I_{IL2}	V_{IL} = GND Pull-up resistor built in pin	–230	—	–60	µA
"L" input current 3 (Note 1)	I_{IL3}	V_{IL} = GND	–20	–5.0	–0.8	µA
Operating current consumption 1	I_{DD1}	f_{OSC} = 4.096 MHz at no load OPTANA = "L"	—	19	40	mA
Operating current consumption 2	I_{DD2}	f_{OSC} = 4.096 MHz at no load OPTANA = "H"	—	23	40	mA
Standby current consumption	I_{DDS}	Ta = –40 to +70°C	—	—	15	µA
		Ta = –40 to +85°C	—	—	100	µA

Notes: 1. Applies to XT pin.
2. Applies to $\overline{\text{TEST}}$ pin.
3. Applies to $\overline{\text{RD}}$ and $\overline{\text{DW}}$ pins.

Analog Section Characteristics (3 V)
ML2252/54-XXX, ML22Q54

ML2252/54-XXX: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C
ML22Q54: DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = 0 to +70°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LAO}	—	50	—	—	kΩ
AOUT output voltage range	V_{AOUT}	No output load	0.5	—	AV_{DD} –0.5	V
DAO output impedance	R_{DAO}	—	30	43	60	kΩ
OUT(+), OUT(–) "H" level output voltage	V_{PWMH}	I_{OH} = –2 mA	AV_{DD} –0.4	—	—	V
OUT(+), OUT(–) "L" level output voltage	V_{PWML}	I_{OH} = 2 mA	—	—	0.4	V
Analog output maximum amplitude when PWM output is selected.	V_{PWMO}	20 kHz LPF used when OPTANA pin = "H".	—	—	$AV_{DD} \times 0.5$	V_{P-P}

Analog Section Characteristics (5 V)
ML2252/54-XXX

DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AOUT output load resistance	R_{LAO}	—	50	—	—	kΩ
AOUT output voltage range	V_{AOUT}	No output load	0.5	—	AV_{DD} –0.5	V
DAO output impedance	R_{DAO}	—	30	43	60	kΩ
OUT(+), OUT(–) "H" level output voltage	V_{PWMH}	I_{OH} = –2 mA	AV_{DD} –0.4	—	—	V
OUT(+), OUT(–) "L" level output voltage	V_{PWML}	I_{OH} = 2 mA	—	—	0.4	V
Analog output maximum amplitude when PWM output is selected.	V_{PWMO}	20 kHz LPF used when OPTANA pin = "H".	—	—	$AV_{DD} \times 0.5$	V_{P-P}

FUNCTIONAL DESCRIPTION

Micro-computer Interface

The micro-computer interface in the ML2250 family has 2 types of interface circuits built in: Parallel interface and serial interface. The interface setting can be changed with the SERIAL pin.

SERIAL pin = "H" level: Serial interface

SERIAL pin = "L" level: Parallel interface

Table below shows the SERIAL pin status in the serial and parallel interfaces.

SERIAL = "L"		SERIAL = "H"	
Parallel interface		Serial interface	
D7 (I/O)	Data input/output pins	D (I)	Serial data input pin
D6 (I/O)		SCK (I)	Serial clock input pin
D5 (I/O)		DO (O)	Serial data output pin
D4 (I/O)		D4 (I)	Not used. (Input "L" level.)
D3 (I/O)		D3 (I)	Not used. (Input "L" level.)
D2 (I/O)		D2 (I)	Not used. (Input "L" level.)
D1 (I/O)		D1 (I)	Not used. (Input "L" level.)
D0 (I/O)		D0 (I)	Not used. (Input "L" level.)

1. Parallel Interface

   When selecting the parallel interface, the I/O pins $\overline{CS}$, $\overline{WR}$, $\overline{DW}$, D7 to D0, and $\overline{RD}$ are used as input pins to input various commands and data, and as output pins to read out the status of the commands and data input.

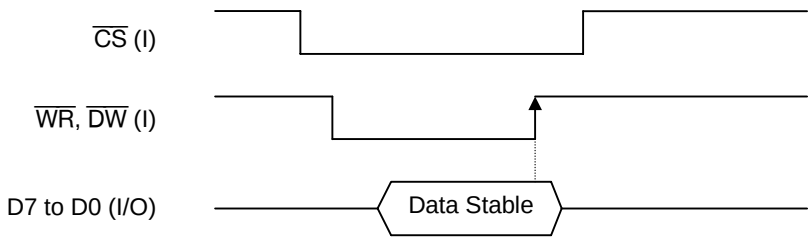
   The micro-computer interface becomes effective when the $\overline{CS}$ pin is set to "L" level.

   When a command or data is input, the input data to D7 through D0 pins is captured inside the device on the rising edge of the $\overline{WR}$ pin.

   The $\overline{DW}$ pin is used to input data after having input the EXT or Flash I/F command. The method to input data to the $\overline{DW}$ pin is the same as the method to input command from the $\overline{WR}$ pin.

   To read the channels status, pins $\overline{CS}$ and $\overline{RD}$ are made "L" level. By doing so, the status signals (NCR1, NCR2, $\overline{BUSY1}$, $\overline{BUSY2}$) of each channel are output to D3 through D0 pins. D7 to D4 pins usually output "L" level.

Command and Data Input Timing



Status Read Timing

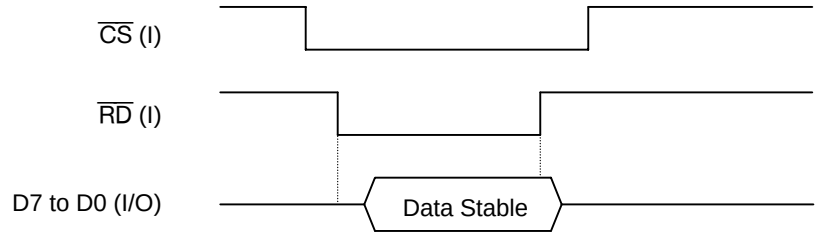


Table below shows the contents of each data output when reading the status of the channels.

Pin	Output status signal
D7	"L" level
D6	"L" level
D5	"L" level
D4	"L" level
D3	Channel 2 busy output ($\overline{\text{BUSY2}}$)
D2	Channel 1 busy output ($\overline{\text{BUSY1}}$)
D1	Channel 2 NCR output (NCR2)
D0	Channel 1 NCR output (NCR1)

The $\overline{\text{BUSY}}$ signal outputs "L" level when either a command is being processed or the playback of a pertinent channel is going on. In other states, the $\overline{\text{BUSY}}$ signal outputs "H" level.
The NCR signal outputs "L" level when either a command is being processed or a pertinent channel is in standby for playback. In other states, the NCR signal outputs "H" level.

2. Serial Interface

When selecting the serial interface, the I/O pins $\overline{CS}$, $\overline{WR}$, $\overline{DW}$, DI, SCK, $\overline{RD}$, and DO are used as input pins to input various commands and data, and as output pins to read out the status of the commands and data.

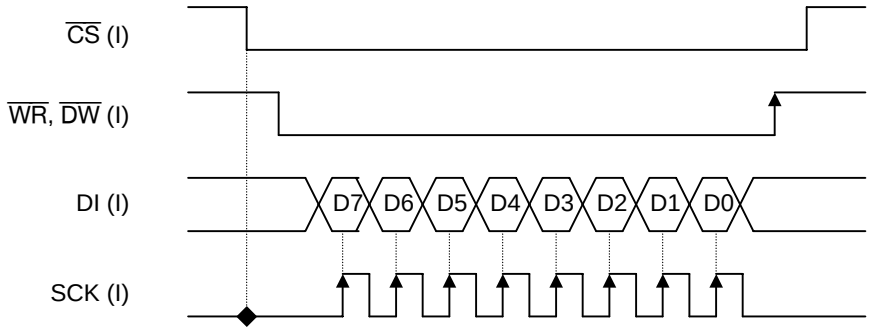
The micro-computer interface becomes effective when $\overline{CS}$ pin is set to “L” level.

To input the commands and data, “L” level is input to $\overline{CS}$ and $\overline{WR}$ pins followed by, from MSB, to DI pin in synchronization with the input clock signal at SCK pin. Data at DI pin is captured inside the device on the rising or falling edge of the clock at SCK pin. And the command is executed on the rising edge of the $\overline{WR}$ pin. The selection of rising/falling edge of SCK clock is determined by the input level of the SCK pin on the falling edge of the $\overline{CS}$ pin. If the SCK pin on the falling edge of the $\overline{CS}$ pin is at “L” level, the DI pin data is captured inside the device on the rising edge of SCK clock. Conversely, if the SCK pin on the falling edge of the $\overline{CS}$ pin is at “H” level, then the DI pin data is captured on the falling edge of SCK clock.

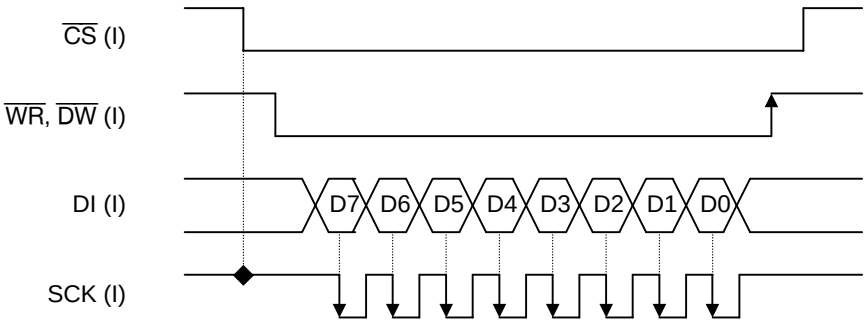
Use the $\overline{DW}$ pin to input various data after having input the EXT or Flash I/F command. The data input method is the same as to input data from the $\overline{WR}$ pin.

Command and Data Input Timings

- SCK Rising Edge Operation



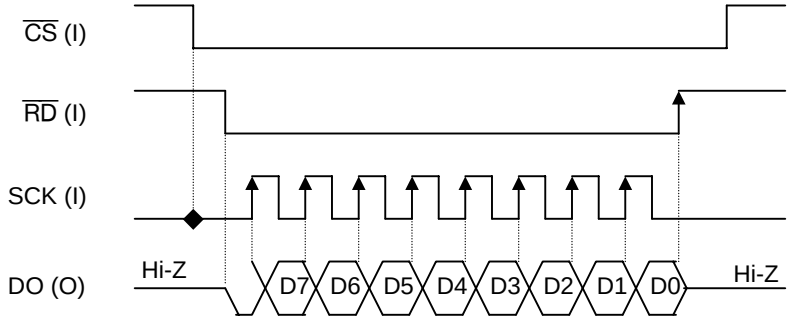
- SCK falling Edge Operation



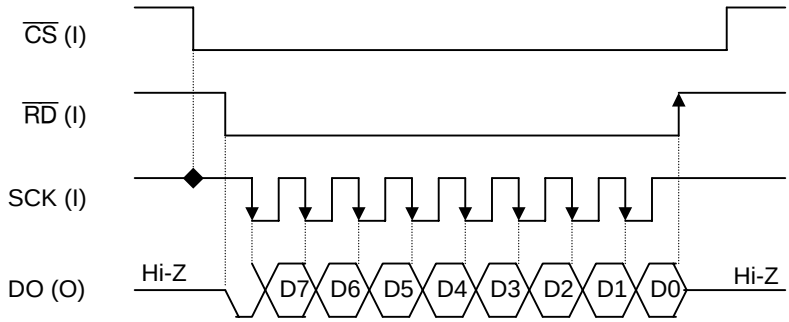
To read the channel status, input “L” level to $\overline{CS}$ and $\overline{RD}$ pins. DQ pin will output the channel status in synchronization with SCK clock.
The selection of rising/falling edge of SCK clock, similar to when inputting the commands and data, is determined by the level at SCK pin at the falling edge of $\overline{CS}$ pin.
The status signals in the parallel interface are output to D7 to D0 pins sequentially from D7.

Status Read Timing

- SCK Rising Edge Operation



- SCK Falling Edge Operation



Commands List

Each command is 1-byte (8 bits) input. PLAY, MUON, and FLASH I/F only are 2 bytes input.

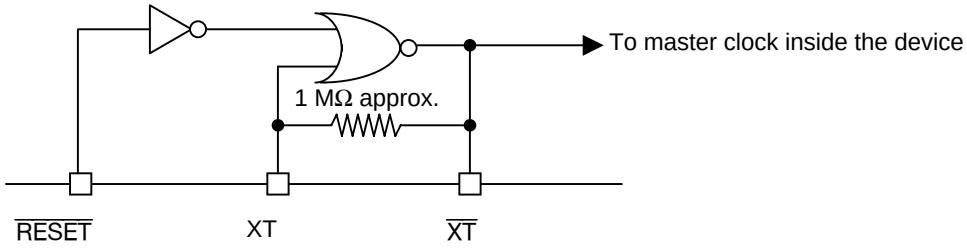
Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP1	0	0	0	0	0	0	0	0	Instantly shifts the power down device to the command standby state.
PUP2	0	0	0	1	0	0	0	0	Suppresses pop noise and shifts the power down device to the command standby state.
PDWN1	0	0	1	0	0	0	0	0	Instantly shifts the device from the command standby state to the power down state.
PDWN2	0	0	1	1	0	0	0	0	Suppresses pop noise and shifts the device from the command standby state to power down state.
PLAY	0	1	0	0	0	0	C1	C0	Inputs the phrase after the playback channel is specified, and then starts the playback.
	F7	F6	F5	F4	F3	F2	F1	F0	
START	0	1	0	1	0	0	C1	C0	Playback start command with phrase specification. Inputs the phrase after the playback channel is specified, and then starts the playback. Playback start command without phrase specification. Inputs the phrase with the FADR command and starts the playback on multiple channels at the same time.
FADR	0	1	1	0	0	0	C1	C0	Phrase specification command. With this command, specifies the playback phrase for each channel.
	M7	M6	M5	M4	M3	M2	M1	M0	
STOP	0	1	1	1	0	0	C1	C0	Specifies the finish channel and ends the voice.
MUON	1	0	0	0	0	0	C1	C0	Inserts silence time after specifying the channel to insert silence, and then inserts silence.
	M7	M6	M5	M4	M3	M2	M1	M0	
SLOOP	1	0	0	1	0	0	C1	C0	Repeats the playback mode setting command. Effective only for the channel being used for playback.
CLOOP	1	0	1	0	0	0	C1	C0	Repeat playback mode releasing command. Inputting the STOP command releases repeat playback mode automatically.
VOL	1	0	1	1	0	0	C1	C2	Specifies the channel whose sound volume is to be set, and then sets the volume of that channel.
	V7	V6	V5	V4	V3	V2	V1	V0	
EXT	1	1	0	0	0	0	0	0	Inputs voice data from the CPU I/F to play it back.
Flash I/F	1	1	0	1	BE	SE	WR	RD	Performs data read/write/erase of the built-in flash memory. This command cannot be used while the playback is going on. (Applicable to the ML22Q54.)

C1, C0: Channel specification (C0 = “1”: Channel 1; CH = “1”: Channel 2; C0, C1 = “1”: Channel 1, Channel 2)
F7 to F0: Phrase address
M7 to M0: Silence time length
X0: Releases the repeated playback
V4 to V0: Sound volume
RD, WR, SE, BE: Mode (RD = “1”: Read data; WR = “1”: Write data; SE = “1”: Erase sector; BE = “1”: Erase block)

Power Down Function

In power down state, the power down function in the device stops the internal operation and oscillation, sets AOUT to GND, and minimizes the static Idd.
When an external clock is in use, input "L" level to the XT pin, so that current does not flow into the oscillation circuit.

Figure below shows the equivalent circuit of $\overline{XT}$ and XT pins.



Channel Status

Channel status is of 2 types: NCRn and $\overline{BUSYn}$.

Channel	Channel status	
CH1	NCR1	$\overline{BUSY1}$
CH2	NCR2	$\overline{BUSY2}$

NCRn = "H" indicates that it is possible to input the PLAY, START and MUON commands for the phrase to be played back next for channel n.

$\overline{BUSYn}$ = "H" indicates a state in which channel n has not performed voice processing. $\overline{BUSYn}$ = "L" indicates a state in which channel n is performing voice processing.
Meanwhile, after a command is input, the NCR and $\overline{BUSY}$ signals of all channels are at "L" level during the processing of the command.

Voice Synthesis Algorithm

The ML2250 family contains 5 algorithm types to match the characteristic of playback voice: 2-bit ADPCM 2 algorithm, 4-bit ADPCM 2 algorithm, 8-bit PCM algorithm, 8-bit non-linear PCM algorithm, and 16-bit PCM algorithm.
Key feature of each algorithm is described in the table below.

Voice synthesis algorithm	Applied waveform	Feature
Oki 2-bit ADPCM2	Normal voice waveform	Oki's specific speech synthesis algorithm of low bit rate with improved 2-bit ADPCM.
Oki 4-bit ADPCM2	Normal voice waveform	Oki's specific speech synthesis algorithm of improved waveform follow-up with improved 4-bit ADPCM.
Oki 8-bit Nonlinear PCM	High-frequency components inclusive sound effect etc.	Algorithm which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM	High-frequency components inclusive sound effect etc.	Normal 8-bit PCM algorithm
16-bit PCM	High-frequency components inclusive sound effect etc.	Normal 16-bit PCM algorithm

Memory Allocation and Creating Voice Data

The ROM is partitioned into 4 data areas: voice (i.e., phrase) control area, test area, voice area, and phrase control table area.
The voice control area manages the ROM's voice data. It controls the start/end addresses of voice data, usage/not usage of the phrase control table function and so on. The voice control area stores voice control data for 256 phrases.
The test area stores the data for testing.
The voice area stores the actual waveform data.
The phrase control table area stores data for effective use of voice data. As for the details, please refer to the Phrase Control Table Function.
There is no phrase control table area if the phrase control table is not used.

The ROM data is created using a development tool.

ROM Addresses (ML2252)

0x00000 0x007FF	Voice control area (16 Kbit Fixed)
0x00800 0x00807	Test area
0x00808 max: 0x1FFFF	Voice area
max: 0x1FFFF	Phrase Control Table area Depends on creation of ROM data.

Built-in ROM Usage Prohibited Area
(Applies to ML2252/54-XXX, ML22Q54)

The 8 bytes between the voice control area and the voice area in the ROM is the prohibited area for use.
The voice data are stored automatically behind 00808(HEX) address by using the development tool (AR762, AR203, AR204) when creating the ROM data.
Table below lists the addresses prohibited for use in every ROM model.

Model	Voice data area	Usage prohibited area
ML2252	00808 to 1FFFF	00800 to 00807
ML2254, 22Q54	00808 to 7FFFF	00800 to 00807

Note: The addresses are indicated in hexadecimal notation.

Playback Time and Memory Capacity

The playback time depends upon the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.

$$\text{Playback time [sec]} = \frac{1.024 \times (\text{Memory capacity} - 16)\ (\text{Kbit})}{\text{Sampling frequency (kHz)} \times \text{Bit length}}$$

(Bit length is ADPCM, ADPCM 2 = 4 bits; PCM = 8 bits.)

Example: Let the sampling frequency be 16 kHz and 4-bit ADPCM algorithm. If one 8 Mbits ROM is used, then the playback time is obtained as follows:

$$\text{Playback time} = \frac{1.024 \times (8192 - 16)\ (\text{Kbit})}{16\ (\text{kHz}) \times 4\ (\text{bit})} \cong 131\ (\text{sec})$$

The above equation gives the playback time when the phrase control table function is not used.

Mixing Function

The ML2250 family can perform simultaneous mixing of 2 channels. It is possible to specify PLAY and STOP for each channel separately.

- Precautions for Waveform Clamp at the Time of Channels Mixing
  When mixing of channels is done, the clamp occurrence possibility increases from the mixing calculation point of view. If it is known beforehand that the clamp will occur, then adjust the sound volume by VOL command.

- Mixing of Different Sampling Frequency
  It is not possible to perform analog mixing by a different sampling frequency.
  When performing analog mixing, the sampling frequency group of the first playback channel is selected. Therefore, please note that if analog mixing is performed by a sampling frequency group other than the selected sampling frequency group, then the playback will not be of constant speed: some times faster and at other times slower.
  The available sampling groups for analog mixing by a different sampling frequency are listed below.
  4.0 kHz, 8.0 kHz, 16.0 kHz, 32.0 kHz ··· (Group 1)
  5.3 kHz, 10.6 kHz, 21.3 kHz, 42.7 kHz ··· (Group 2)
  6.4 kHz, 12.8 kHz, 25.6 kHz ··· (Group 3)

Figures below show a case when a sampling frequency group played back a different sampling frequency group.

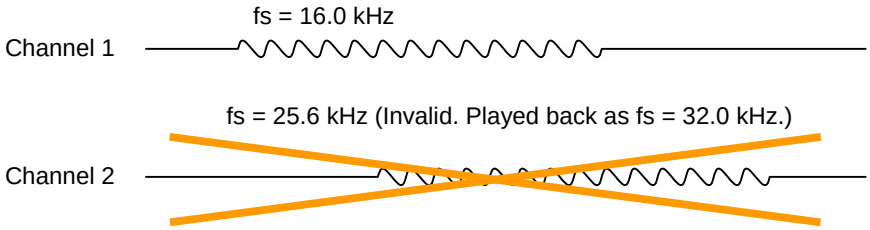


Figure 1 In Case a Different Sampling Frequency Played Back during Playback of the Other Channel Playback

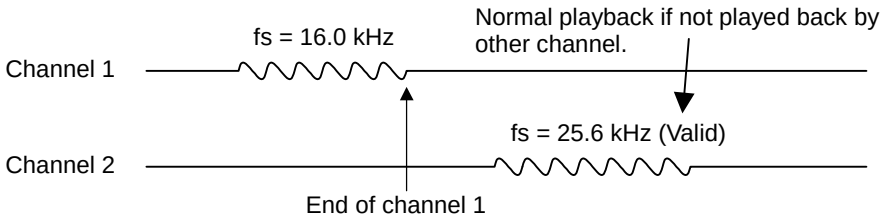


Figure 2 In Case a Different Sampling Frequency Played Back after the End of the Other Channel

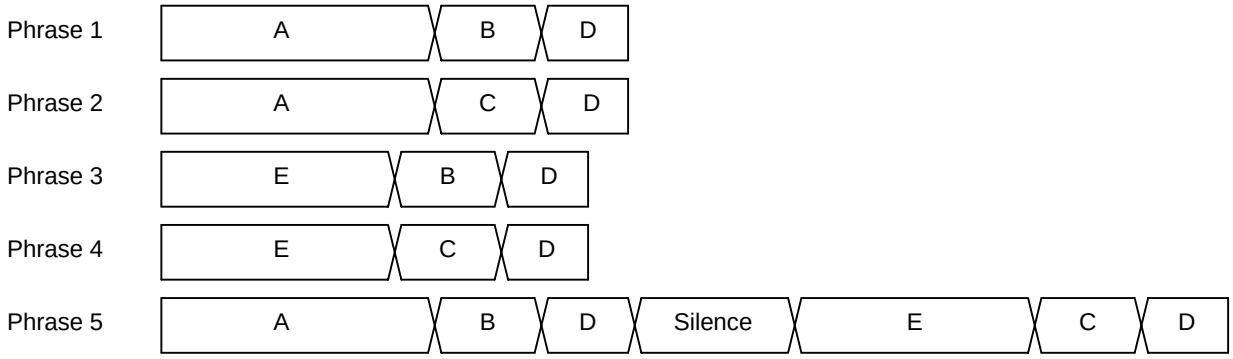
Phrase Control Table Function

The phrase control table function makes it possible to play back multiple phrases in succession. The following functions are set using the phrase control table function:

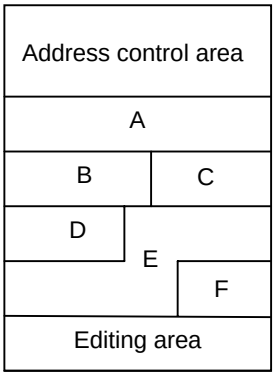
- Continuous playback: There is no limit to the number of times a continuous playback can be specified. It depends on the memory capacity only.
- Silence insertion function: 4 to 1024 ms

Using the phrase control table function enables to effectively use the memory capacity of voice ROM.
Below is an example of the ROM configuration in the case of using the phrase control table function.

Example 1: Phrases Using the Phrase Control Table Function



Example 2: Example of ROM Data in case Example 1 Converted to ROM

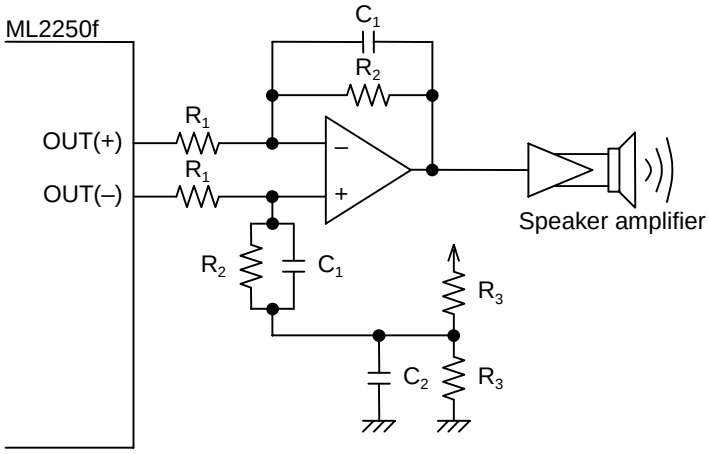


Converting PWM Signal to Analog Signal

Examples of circuits that convert the PWM output signal to an Analog signal when PWM output is selected (OPTANA pin = "H") are given below.

1. Example Using Active LPF

The LPF primary side is configured as below using an OP amplifier.

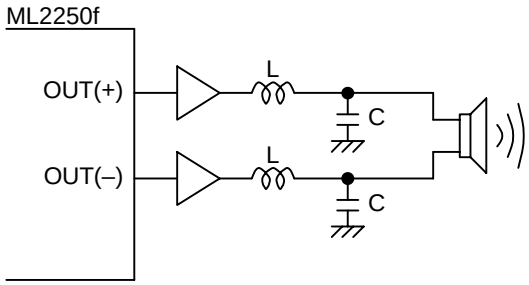


LPC cutoff frequency, f_C, is determined by $f_C = \frac{1}{2\pi R_2 C_1}$

Ratio of resistors R_1 to R_2 determines the voltage amplification factor. To set the amplification factor 2 times of the OP amplifier, set R_1:R_2 = 1:2.

2. Example Using LC Filter

Secondary LPF is configured using a coil (L) and a capacitor (C). This configuration can directly drive a speaker. However, a buffer is required between the PWM output and the LC filter.



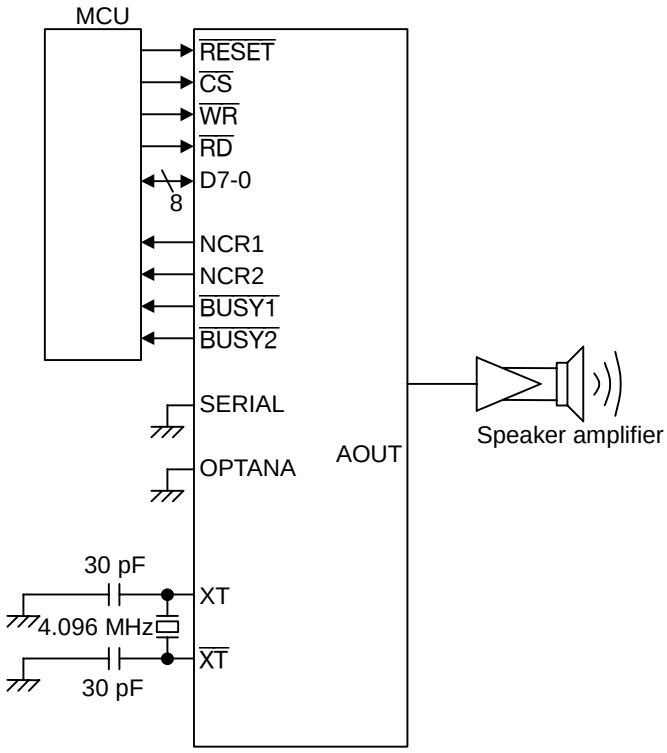
LPF cutoff frequency, f_C, is determined by $f_C = \frac{1}{2\pi\sqrt{LC}}$.

In the case of secondary Butterworth type LC filter, the constants are obtained by the following equations:

$$L = 1.4142 \times \frac{1}{2\pi f_C} \qquad C = \frac{1}{1.412 \times R_L \times (2\pi f_C)}$$

Here, R_L stands for the output load resistance and f_C stands for cutoff frequency of LC filter.

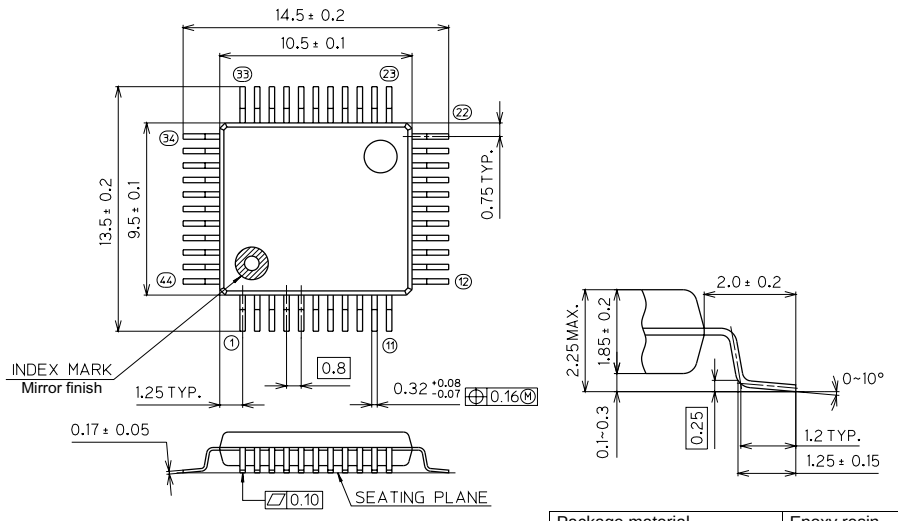
APPLICATION CIRCUIT EXAMPLE (ML2252/54-XXX, ML22Q54)



PACKAGE DIMENSIONS

(Unit: mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL2250DIGEST-01	Oct. 15, 2002	–	–	Final edition 1

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.
   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

Copyright 2002 Oki Electric Industry Co., Ltd.