NT3883

Dot Matrix LCD 80-Channel Driver

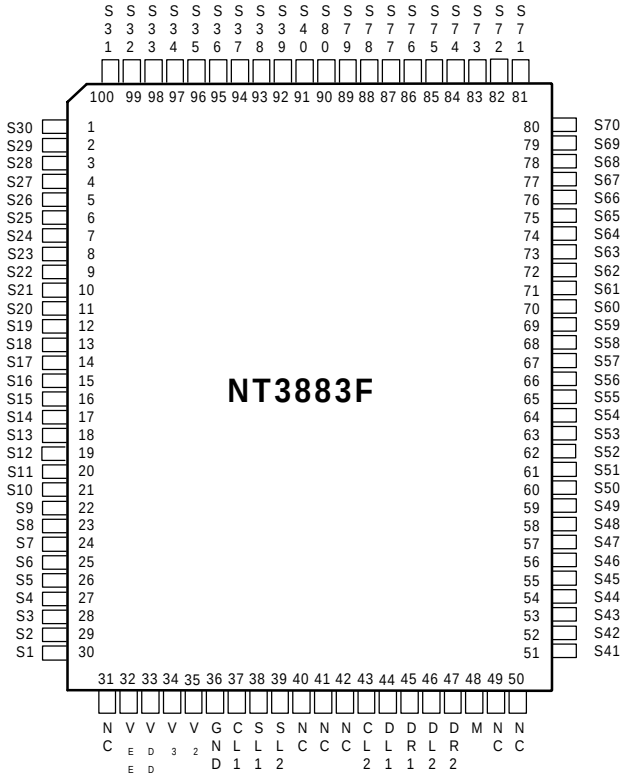
Features

- Provides 80-channel LCD driver
- Internal serial to parallel conversion circuits:
  - 40-bit bi-direction shift register × 2
  - 80-bit latch × 1
  - 80-bit 4-level driver × 1
- Logic circuit supply voltage range: 4.5V - 5.5V
- LCD driving voltage range (V_{DD} - V_{EE}): 3.5V to 11V
- Applicable LCD duty cycle: 1/2 to 1/16
- Interfaces with a NT3881B/C/D LCD controller
- LCD bias voltage can be supplied externally
- Available in 100-pin QFP and in CHIP FORM

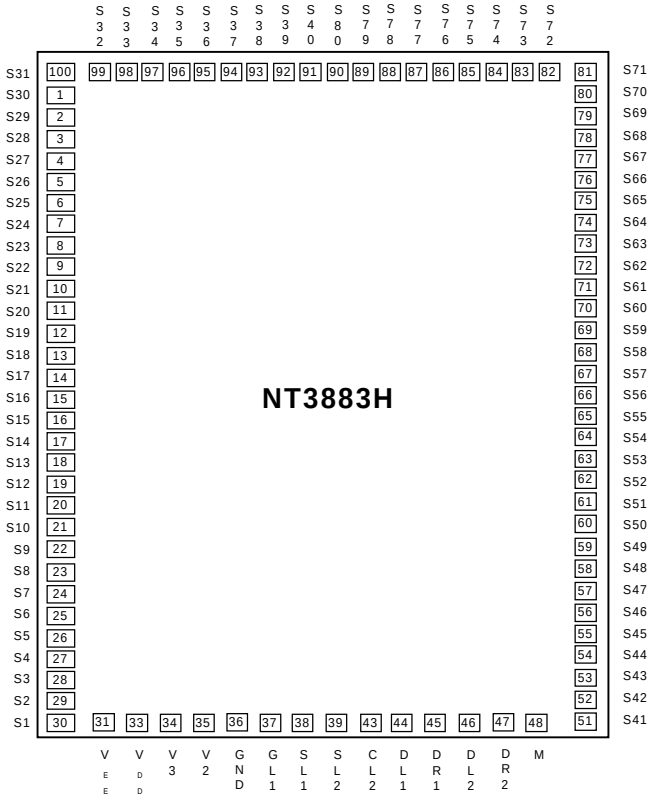
General Description

The NT3883 is a dot matrix LCD 80-channel driver fabricated by low power CMOS technology. This IC consists of two 40-bit bi-directional shift registers, 80-bit latch and 80-bit 4-level LCD driver. The NT3883 converts serial data that are received from the LCD controller, such as NT3881B/C/D, to parallel data and outputs LCD driving waveforms to drive LCD. Expansion of character-type liquid crystal display can be easily obtained according to the number and structure of characters.

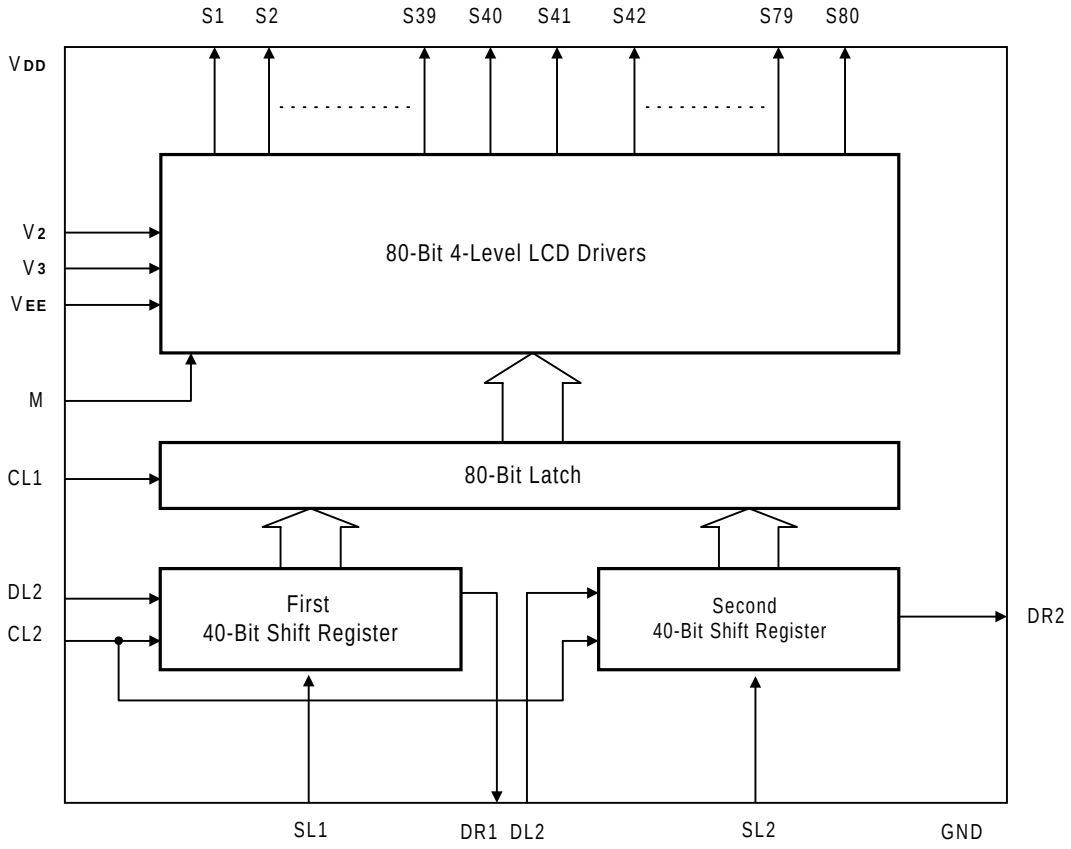
Pin Configuration



Pad Configuration



Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage (V_{DD}-GND) . . . . . -0.3V to 7.0V
Power Supply Voltage (V_{DD}-V_{EE}) . . . . . .
. . . . . .V_{DD} - 13.5V to V_{DD} + 0.3V
Input Voltage . . . . . -0.3V to V_{DD} + 0.3V
Operating Temperature . . . . . -20°C to + 75°C
Storage Temperature . . . . . -55°C to + 125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 5.0V, GND = 0V, V_{EE} = 0V, T_A = 25°C)

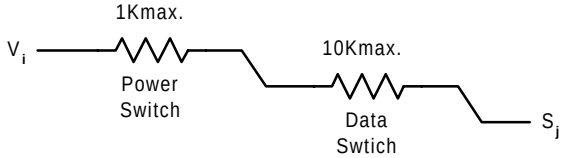
Parameter	Symbol	Terminal	Min.	Typ.	Max.	Unit	Conditions
Input Voltage	V_{IH}	CL1, CL2, DL1, DL2 *1	0.7 V_{DD}	-	V_{DD}	V	
	V_{IL}		0	-	0.3 V_{DD}	V	
Output Voltage	V_{OH}	DR1, DR2 *1	V_{DD} - 0.4	-	-	V	I_{OH} = -0.4mA
	V_{OL}		-	-	0.4	V	I_{OL} = +0.4mA
Vi - Sj Voltage	V_{D1}	*2	-	-	1.1	V	I_{ON} = 0.1mA for one of Sj
Descending	V_{D2}		-	-	1.5	V	I_{ON} = 0.05mA for each of Sj
Input Leakage Current	I_{IL}	CL1, CL2 DL1, DL2*1	-5	-	5	μA	V_{IN} = 0 or V_{DD}
Vi Leakage Current	I_{VL}	V_2, V_3, V_{EE}	-10	-	10	μA	S1 to S80 open
Power Supply Current	I_{DD}	*3	-	-	500	μA	f_{CL1} = 1KHz f_{CL2} = 1MHz

Note *1: SL1 and SL2 determine The Input or Output of DL1, DL2, DR1 and DR2 and the configuration is as follows.

Terminal	SL1 = High	SL1 = Low	SL2 = High	SL2 = Low
DL1	Output	Input	-	-
DR1	Input	Output	-	-
DL2	-	-	Output	Input
DR2	-	-	Input	Output

*2: V_i – S_j (V_i = V_{DD}, V_2, V_3, V_{EE}; j = 1 to 80) equivalent circuit (for reference)

*3: Input/output current is excluded. When the input is at the intermediate level with CMOS, some excessive

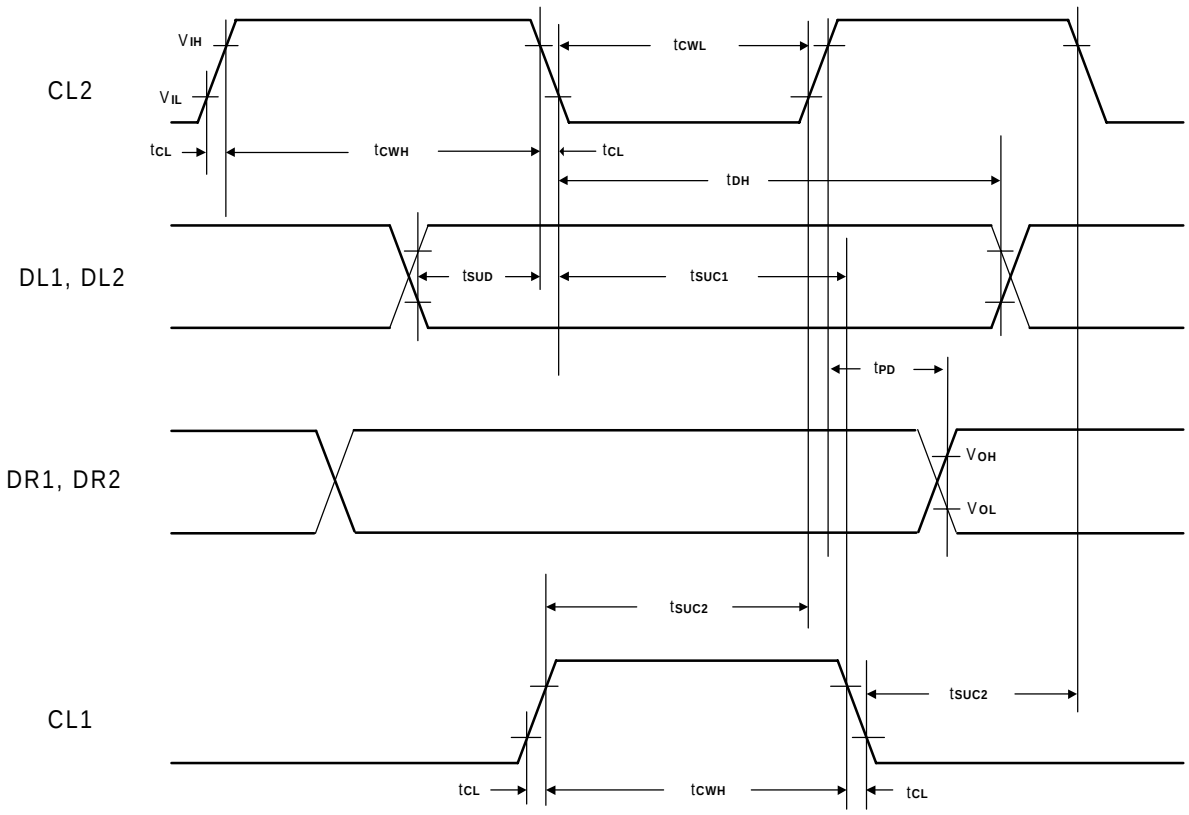


Current will flow through the input circuit to power supply. To avoid this, the input level must be fixed at high or low state.

AC Characteristics (V_{DD} = 5.0V, GND = 0V, V_{EE} = 0V, T_A = 25°C)

Parameter		Symbol	Terminal	Min.	Typ.	Max.	Unit
Data Shift Frequency		f_{CL2}	CL2	-	-	400	KHz
Clock Width	High	t_{CWH}	CL1, CL2	800	-	-	ns
	Low	t_{CWL}	CL2	800	-	-	ns
Data Hold Time		t_{DH}	DL1~2, DR1~2	300	-	-	ns
Data Set-up Time		t_{SUD}	DL1~2, DR1~2	300	-	-	ns
Clock Set-up Time(CL2→CL1)		t_{SUC1}	CL1, CL2	500	-	-	ns
Clock Set-up Time(CL1→CL2)		t_{SUC2}	CL1, CL2	500	-	-	ns
Clock Rise/Fall Time		t_{CL}	CL1, CL2	-	-	200	ns
Data Delay Time		t_{PD}	-	-	-	500	ns

Timing Waveforms



Pin and Pad Descriptions

Pin No.	Pad No.	Designation	I/O	External Connection	Description
1~30, 51~100	1~30, 51~100	S1~S30, S80~S31	O	LCD panel	Segment signal output pins
33	33	V_{DD}	P	Power supply	Power for logic circuits
36	36	GND	P	Power supply	0V
37	37	CL1	I	Controller	Clock to latch serial data
38	38	SL1	I	MPU	Shift left control for 1st 40-bit shift register (see NOTE*4)
39	39	SL2	I	MPU	Shift left control for 1st 40-bit shift register (see NOTE*4)
43	43	CL2	I	Controller	Clock to shift serial data
44	44	DL1	I/O	Controller or NT3882A/NT3883	Data input/output of 1st 40-bit shift register (see NOTE*4)
45	45	DR1	I/O	Controller or NT3882A/NT3883	Data input/output of 1st 40-bit shift register (see NOTE*4)
46	46	DL2	I/O	Controller or NT3882A/NT3883	Data input/output of 2nd 40-bit shift register (see NOTE*4)
47	47	DR2	I/O	Controller or NT3882A/NT3883	Data input/output of 2nd 40-bit shift register (see NOTE*4)
48	48	M	I	Controller	Alternate signal for LCD drivers
31, 34, 35	31, 34, 35	V_{EE}, V_3, V_2	P	Power supply	Power for LCD drivers
32, 40, 41, 42, 49,50	-	NC	-	-	No connection

NOTE *4: Relation of SL1, SL2, DL1, DR1, DL2 and DR2

SL1	SL2	Shift Direction	DL1	DR1	DL2	DR2
1(High)	-	Left(S40 to S1)	Output	Input	-	-
0(Low)	-	Right(S1 to S40)	Input	Output	-	-
-	1(High)	Left(S80 to S41)	-	-	Output	Input
-	0(Low)	Right(S41 to S80)	-	-	Input	Output

Functional Description

NT3883 is a dot matrix LCD segment driver LSI. It operates with the controller, such as NT3881B/C/D, and/or another segment driver LSI NT3882A/3883. NT3883 receives serial data from the controller or another NT3883, converts it to parallel data and then supplies the LCD driving waveforms to the LCD panel.

1. CL1

This signal is used for latching the shift register contents. When CL1 is set at high, the shift register contents are transferred to the 80-bit 4level LCD driver. When CL1 is set at low, the last display output data (S1 to S80) is held.

2. CL2

Clock pulse inputs for the two 40-bit shift registers. The data is shifted to an 80-bit latch at the falling edge of CL2. The clock signal CL2 must be active when operating to refresh shift registers' contents.

3. DL1

Data input/output of the 1^{st} - 40^{th} register. When SL1 is connected to GND or open, the data from LCD controller is fed into the 1^{st} - 40^{th} register through DL1 serially. If SL1 is connected to V_{DD}, the DL1 becomes the output of the 1^{st} - 40^{th} register.

4. DR1

Data input/output of the 1^{st} - 40^{th} register. When SL1 is connected to GND, the 20^{th} bit of the 1^{st} - 40^{th} register output from DR1. By connecting DR1 to DL2, two 40-bit shift registers cascaded to one 80-bit shift register. If SL1 is connected to V_{DD}, the DR1 becomes the input of the 1^{st} - 40^{th} register, in this case, the data may come from DL2.

5. DL2

Data input/output of the 41^{st} - 80^{th} register. When SL2 is connected to GND, the data from LCD controller is fed into the 41^{st} - 80^{th} register through DL2 serially. If SL2 is connected to V_{DD}, the DL2 becomes the output of the 41^{st} - 80^{th} register.

6. DR2

Data input/output of the 41^{st} - 80^{th} register. When SL2 is connected to GND, the 80^{th} bit of the 41^{st} - 80^{th} register output from DR2. By connecting DR2 to DL1 of next NT3882A/3883, the cascade structure is obtained to drive a wider LCD panel. If SL2 is connected to V_{DD}, the DR2 becomes the input of the 41^{st} - 80^{th} register, in this case, the data may come from the next NT3882A/3883.

7. SL1

The shift direction of S1 to S40, i.e. 1^{st} to 40^{th} shift register, is selected by SL1. The detail function description is listed in Note*4 of Page5.

8. SL2

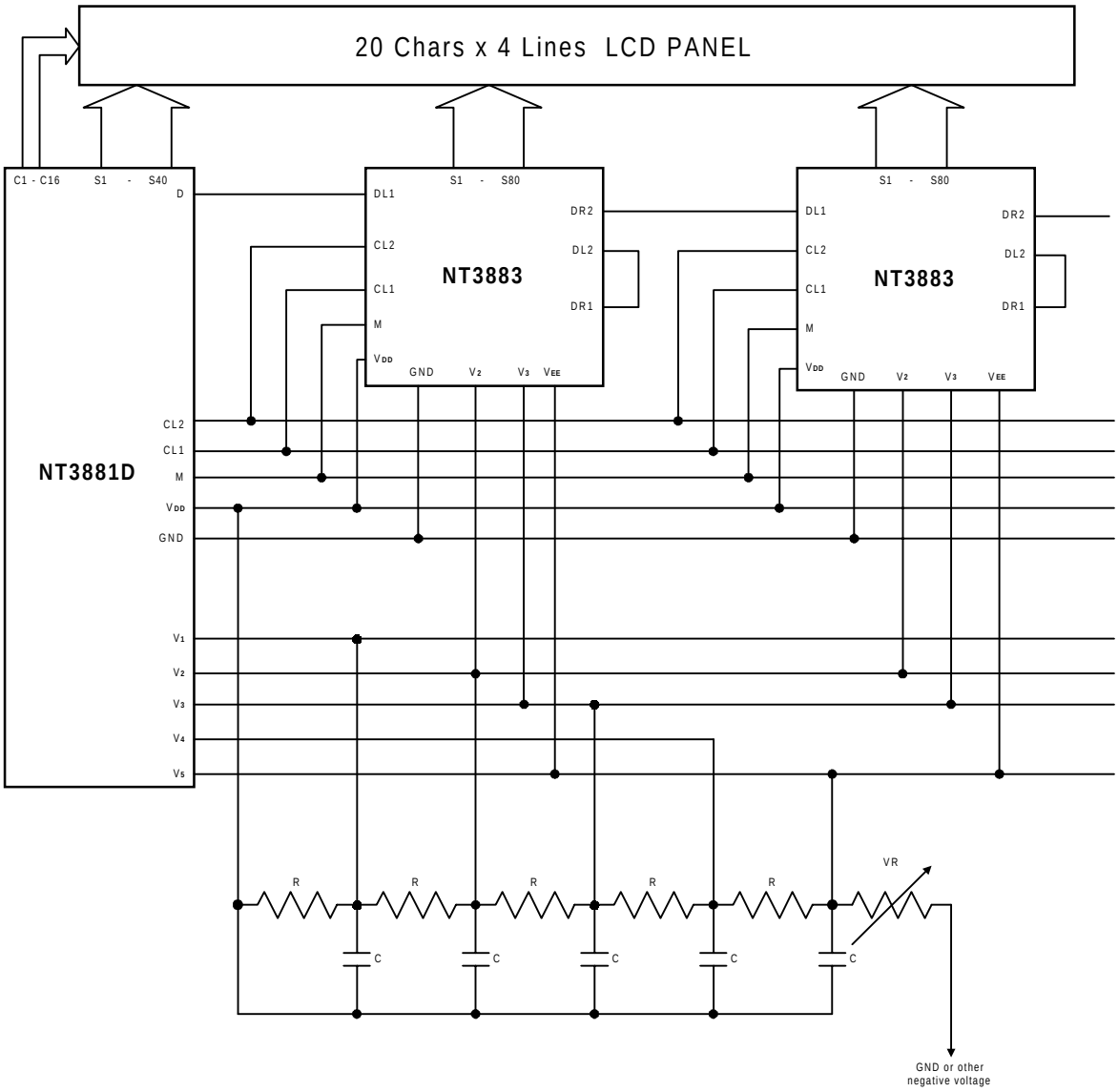
The shift direction of S41 to S80, i.e. 41^{st} to 80^{th} shift register, is selected by SL2. The detail function description is listed in Note*4 of Page5.

9. S1 to S80

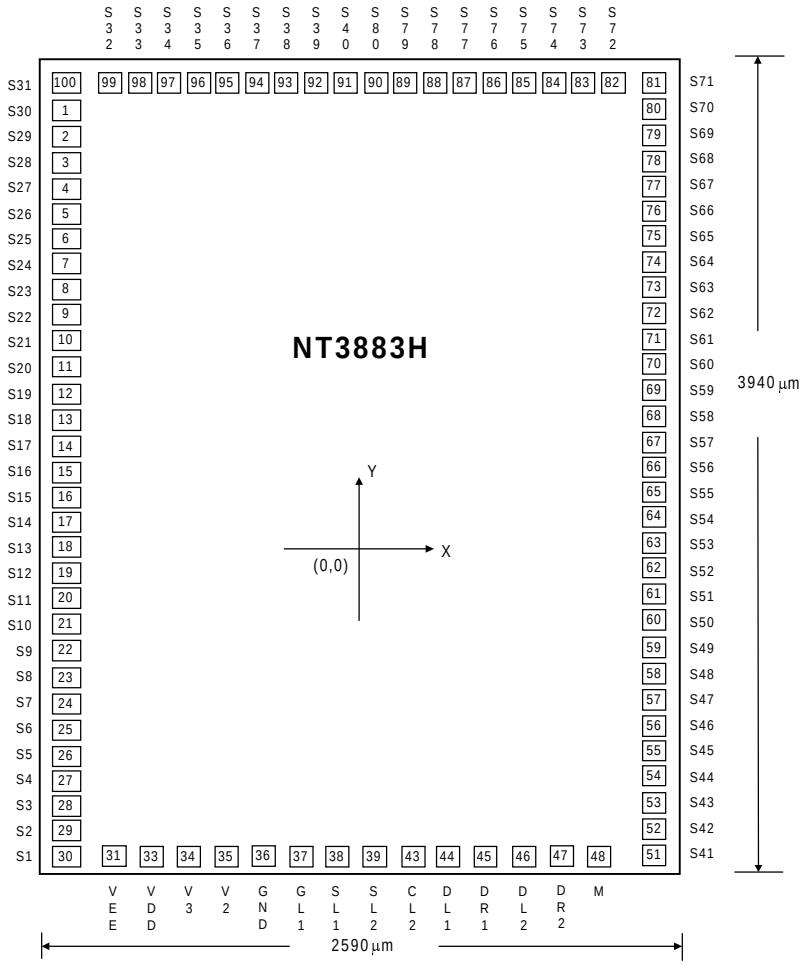
LCD driver output pins. These 80 bits represent the 80 data bits in the 80-bit latch and one of V_{DD}, V_2, V_3 and V_{EE} is selected as a LCD driving voltage source according to the combination of latched data level and the alternate signal (M). The truth table is listed as follows:

Latched Data	M	Output Level of S1 to S80
1(High)	1(High)	V_{EE}
(Selected)	0(Low)	V_{DD}
0(Low)	1(High)	V_3
(Non-selected)	0(Low)	V_2

Application Circuit (for reference only)



Bonding Diagram



* Connecting IC substrate to V_{DD} or keeping floating is recommended.

* Pad window area 100μm × 100μm.

Bonding Dimensions

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	S30	-1194	1677	54	S44	1195	-1442
2	S29	-1194	1557	55	S45	1195	-1311
3	S28	-1194	1437	56	S46	1195	-1202
4	S27	-1194	1317	57	S47	1195	-1082
5	S26	-1194	1197	58	S48	1195	-962
6	S25	-1194	1077	59	S49	1195	-842
7	S24	-1194	957	60	S50	1195	-722
8	S23	-1194	837	61	S51	1195	-602
9	S22	-1194	717	62	S52	1195	-482
10	S21	-1194	597	63	S53	1195	-362
11	S20	-1194	477	64	S54	1195	-242
12	S19	-1194	357	65	S55	1195	-122
13	S18	-1194	237	66	S56	1195	-2
14	S17	-1194	117	67	S57	1195	117
15	S16	-1194	-2	68	S58	1195	237
16	S15	-1194	-122	69	S59	1195	357
17	S14	-1194	-242	70	S60	1195	477
18	S13	-1194	-362	71	S61	1195	597
19	S12	-1194	-482	72	S62	1195	717
20	S11	-1194	-602	73	S63	1195	837
21	S10	-1194	-722	74	S64	1195	957
22	S9	-1194	-842	75	S65	1195	1077
23	S8	-1194	-962	76	S66	1195	1197
24	S7	-1194	-1082	77	S67	1195	1317
25	S6	-1194	-1202	78	S68	1195	1437
26	S5	-1194	-1322	79	S69	1195	1557
27	S4	-1194	-1442	80	S70	1195	1677
28	S3	-1194	-1562	81	S71	1185	1811
29	S2	-1194	-1682	82	S72	995	1821
30	S1	-1184	-1812	83	S73	875	1821
31	VEE	-945	-1822	84	S74	755	1821
33	VDD	-807	-1822	85	S75	635	1821
34	V3	-670	-1822	86	S76	515	1821
35	V2	-520	-1822	87	S77	395	1821
36	GND	-353	-1822	88	S78	275	1821
37	CL1	-204	-1822	89	S79	155	1821
38	SL1	-54	-1822	90	S80	35	1821
39	SL2	95	-1822	91	S40	-84	1821
43	CL2	245	-1822	92	S39	-204	1821
44	DL1	395	-1822	93	S38	-324	1821
45	DR1	545	-1822	94	S37	-444	1821
46	DL2	695	-1822	95	S36	-564	1821
47	DR2	845	-1822	96	S35	-684	1821
48	M	995	-1822	97	S34	-805	1821
51	S41	1185	-1812	98	S33	-925	1821
52	S42	1195	-1682	99	S32	-1045	1821
53	S43	1195	-1562	100	S31	-1184	1811

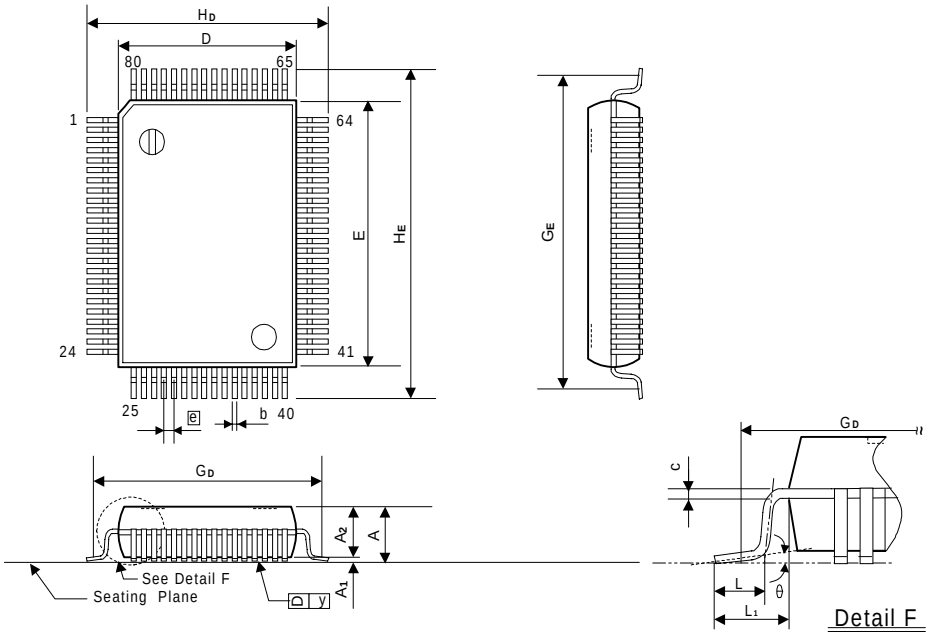
Ordering Information

Part No.	Package
NT3883H	CHIP FORM
NT3883F	100L QFP

Package Information

QFP 100L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.130 Max.	3.30 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.112±0.005	2.85±0.13
b	0.014 +0.004 -0.002	0.35 +0.10 -0.05
c	0.006 +0.004 -0.002	0.15 +0.10 -0.05
D	0.551±0.005	14.00±0.13
E	0.787±0.005	20.00±0.13
e	0.031±0.006	0.80±0.15
G_D	0.693 NOM.	17.60 NOM.
G_E	0.929 NOM.	23.60 NOM.
H_D	0.740±0.012	18.80±0.31
H_E	0.976±0.012	24.79±0.31
L	0.047±0.008	1.19±0.20
L_1	0.095±0.008	2.41±0.20
y	0.006 Max.	0.15 Max.
θ	0° ~ 12°	0° ~ 12°

Notes:

1. Dimensions D & E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only