

MEDIUM POWER AMPLIFIER GaAs MMIC

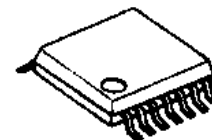
■GENERAL DESCRIPTION

NJG1302V is a GaAs MMIC designed mainly for the final stage power amplifier of Japanese PHS handset, but suitable digital wireless phone and wireless LAN.

This amplifier has wide variable gain capability of 20dB dynamic range.

NJG1302V has input and output matching circuits internally and features low voltage and high efficiency operation. The output power of 21dBm is easily available with very low distortion.

■PACKAGE OUTLINE



NJG1302V

■FEATURES

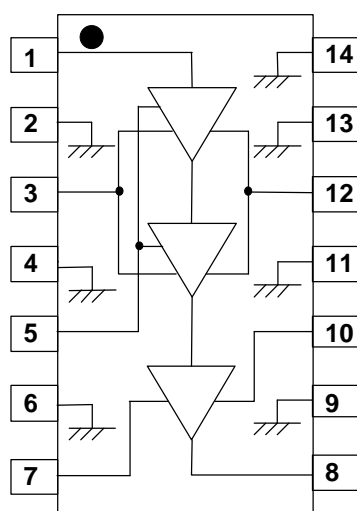
- Voltage gain under low distortion
- Low voltage operation
- Low current consumption
- High gain
- Low distortion(ACP)
- Reduction of Parasitic oscillation
- Input and output internal matching circuit
- Package

+3.0V typ.
195mA typ. @f= 1.9GHz, P_{out} = 21dBm
32dB
-60dBc typ. @f= 1.9GHz, P_{OUT} = 21dBm

SSOP14

■PIN CONFIGURATION

V Type
(Top View)



Pin Connection

| | |
|---------------|---------------|
| 1. RF_{IN} | 8. RF_{OUT} |
| 2. GND | 9. GND |
| 3. V_{GG1} | 10. V_{DD1} |
| 4. GND | 11. GND |
| 5. V_{CONT} | 12. V_{DD1} |
| 6. GND | 13. GND |
| 7. V_{GG2} | 14. GND |

NJG1302V

■ABSOLUTE MAXIMUM RATINGS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_i=50\Omega$)

| PARAMETER | SYMBOL | CONDITIONS | RATINGS | UNITS |
|-----------------------|--------------------|---|------------|--------------------|
| Drain Voltage | V_{DD1}, V_{DD2} | $V_{GG1}, V_{GG2}=-0.9\text{V}$ | 6 | V |
| Gate Voltage | V_{GG1}, V_{GG2} | $V_{DD1}, V_{DD2}=-3.0\text{V}$ | -4 | V |
| Gain Control Voltage | V_{CONT} | $V_{DD1}, V_{DD2}=-3.0\text{V}$ | -4 | V |
| Input Power | P_{in} | $V_{DD1}, V_{DD2}=-3.0\text{V}$, $V_{GG1}, V_{GG2}=-0.9\text{V}$ | 3 | dBm |
| Power Dissipation | P_D | At on PCB board | 600 | mW |
| Operating Temperature | T_{opr} | | -30 ~ +85 | $^{\circ}\text{C}$ |
| Storage Temperature | T_{stg} | | -40 ~ +150 | $^{\circ}\text{C}$ |

■ELECTRICAL CHARACTERISTICS

($T_a=+25^{\circ}\text{C}$, $Z_s=Z_i=50\Omega$)

| PARAMETER | SYMBOL | CONDITONS | MIN | TYP | MAX | UNITS |
|----------------------------------|-------------------|---|---|------|------|---------------|
| Operating Frequency | freq | $V_{DD1,2}=3.0\text{V}$ | 1.89 | - | 1.92 | GHz |
| Drain Voltage | $V_{DD1,2}$ | | 2.9 | 3.0 | 5.0 | V |
| Gate Voltage | $V_{GG1,2}$ | $V_{DD1,2}=3.0\text{V}$, $I_{\text{idle}}=180\text{mA}$ | -1.25 | -0.9 | -0.6 | V |
| Idle Current *1 | I_{idle} | $V_{DD1,2}=3.0\text{V}$, No RF Signal | 175 | 180 | 185 | mA |
| Operating Current *1 | I_{DD} | $V_{DD1,2}=3.0\text{V}$, $P_{\text{out}}=21\text{dBm}$ | 180 | 195 | 205 | mA |
| Gate Current *2 | I_{GG} | $V_{DD1,2}=3.0\text{V}$, $P_{\text{out}}=21\text{dBm}$ | -150 | -70 | - | μA |
| Gain Control Terminal Current | I_{CONT} | $V_{DD1,2}=3.0\text{V}$, $P_{\text{out}}=21\text{dBm}$ $-2.0 < V_{\text{CONT}} < 0.0\text{V}$ | -5 | -2 | - | μA |
| Gain Control Voltage | V_{CONT} | | -2.0 | - | 0 | V |
| Small Signal Gain | Gain | $V_{DD1,2}=3.0\text{V}$, $I_{\text{idle}}=180\text{mA}$ | 29 | 32 | 35 | dB |
| Gain Flatness | G_{flat} | $V_{DD1,2}=3.0\text{V}$, $I_{\text{idle}}=180\text{mA}$ | 0 | 0.5 | 1.0 | dB |
| Gain Control Range | G_{CONT} | $V_{\text{CONT}}=-2\sim 0\text{V}$, $V_{DD1,2}=3.0\text{V}$ $I_{\text{idle}}=180\text{mA}$ | 18 | 20 | 23 | dB |
| Pout at 1dB Compression point | $P_{-1\text{dB}}$ | $V_{DD1,2}=3.0\text{V}$ | 22 | 23 | - | dBm |
| Adjacent Channel Leakage Power 1 | $P_{\text{acp}1}$ | $V_{DD1,2}=3.0\text{V}$, $P_{\text{out}}=21\text{dBm}$ offset=600kHz, $P_{\text{in}}; \pi/4$ DQPSK | - | -60 | -55 | dBc |
| Adjacent Channel Leakage Power 2 | $P_{\text{acp}2}$ | $V_{DD1,2}=3.0\text{V}$, $P_{\text{out}}=21\text{dBm}$ offset=900kHz, $P_{\text{in}}; \pi/4$ DQPSK | - | -65 | -60 | dBc |
| Harmonics | P_{SP} | $V_{DD1,2}=3.0\text{V}$, $P_{\text{out}}=21\text{dBm}$ | - | -35 | -30 | dBc |
| Input VSWR | VSWR_i | $V_{DD1,2}=3.0\text{V}$ | - | - | 2.2 | |
| Load VSWR Tolerance | - | $V_{DD1,2}=3.0\text{V}$, $P_{\text{out}}=21\text{dBm}$ Load VSWR=4:1, All Phase | Parasitic Oscillation for Fundamental Signal Level $\leq -60\text{dBc}$ | | | |

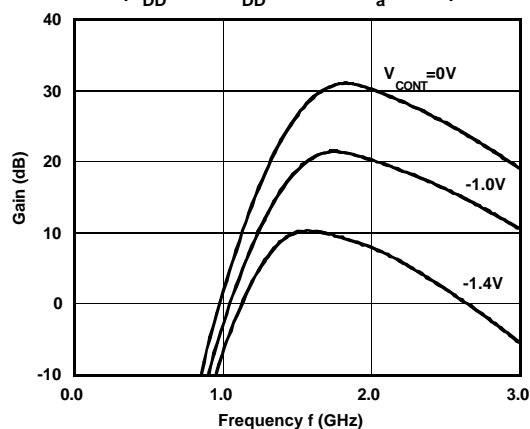
*1: V_{DD1} Terminal V_{DD2} Terminal Total Current

*2: V_{GG1} Terminal V_{GG2} Terminal Total Current

TYPICAL CHARACTERISTICS

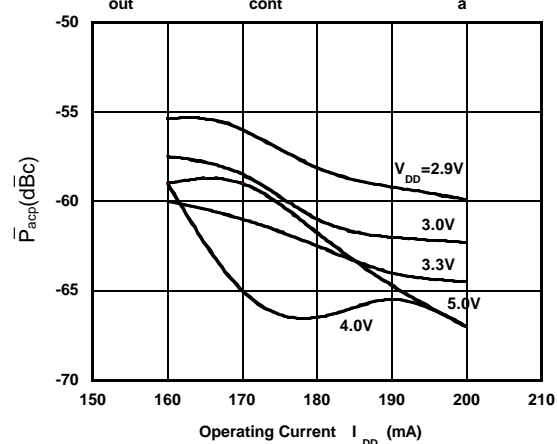
Gain vs. Frequency vs. Control Voltage

($V_{DD}=3.0V$, $I_{DD}=180mA$, $T_a=25^\circ C$)



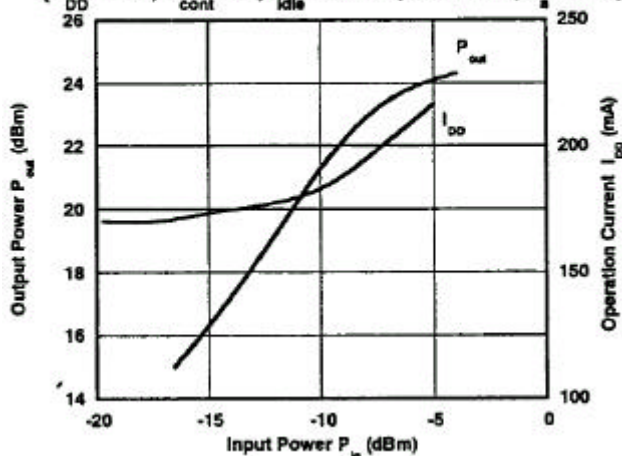
P_{acp} vs. Operating Current vs. V_{DD}

($P_{out}=21dBm$, $V_{cont}=0V$, $f=1.9GHz$, $T_a=25^\circ C$)



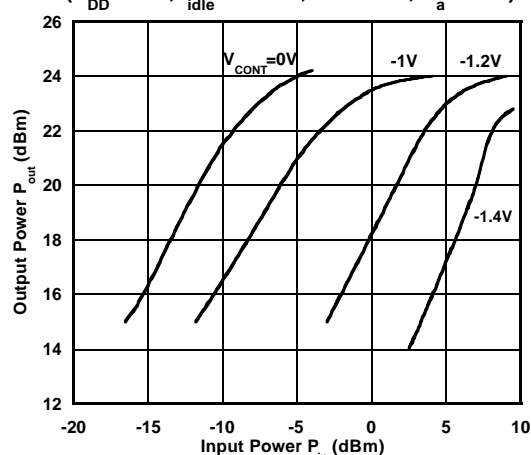
Output Power, Operating Current vs. Input Power

($V_{DD}=3.0V$, $V_{cont}=0V$, $I_{idle}=180mA$, $f=1.9GHz$, $T_a=25^\circ C$)



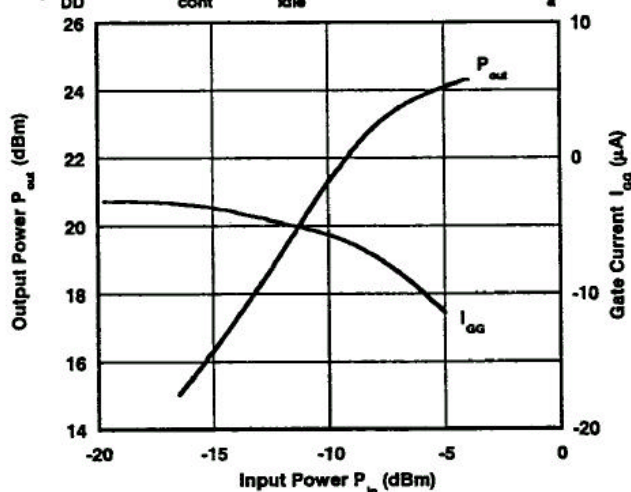
Output Power vs. Input Power vs. Control Voltage

($V_{DD}=3.0V$, $I_{idle}=180mA$, $f=1.9GHz$, $T_a=25^\circ C$)



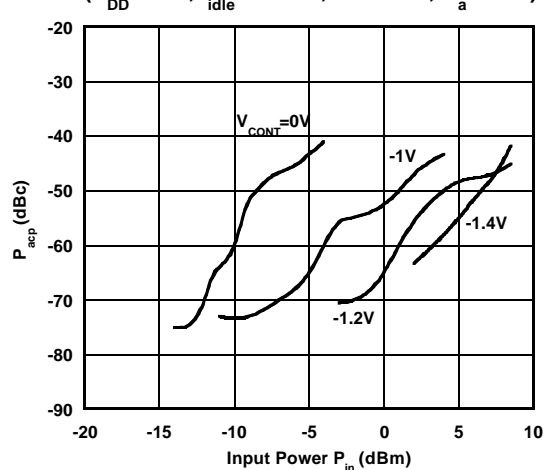
Output Power, Gate Current vs. Input Power

($V_{DD}=3.0V$, $V_{cont}=0V$, $I_{idle}=180mA$, $f=1.9GHz$, $T_a=25^\circ C$)



P_{acp} vs. Input Power vs. Control Voltage

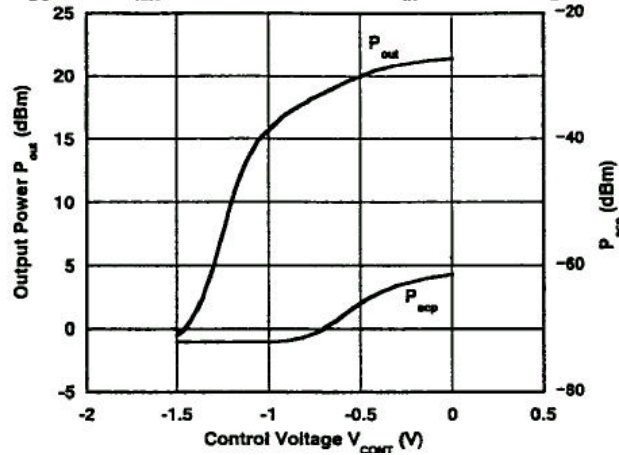
($V_{DD}=3.0V$, $I_{idle}=180mA$, $f=1.9GHz$, $T_a=25^\circ C$)



TYPICAL CHARACTERISTICS

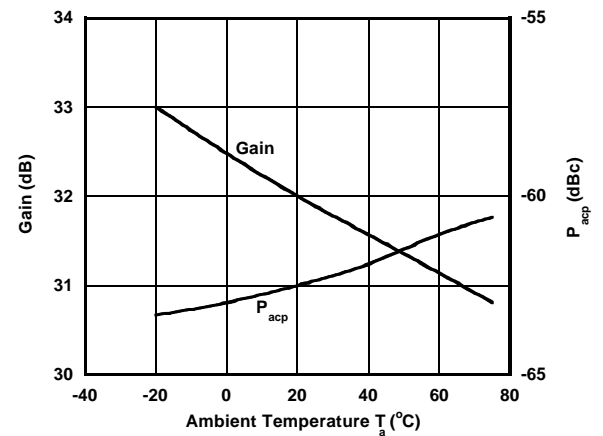
Output Power, P_{out} vs. Control Voltage

($V_{DD}=3.0V$, $I_{idle}=180mA$, $f=1.9GHz$, $P_{in}=-11dBm$, $T_a=25^\circ C$)



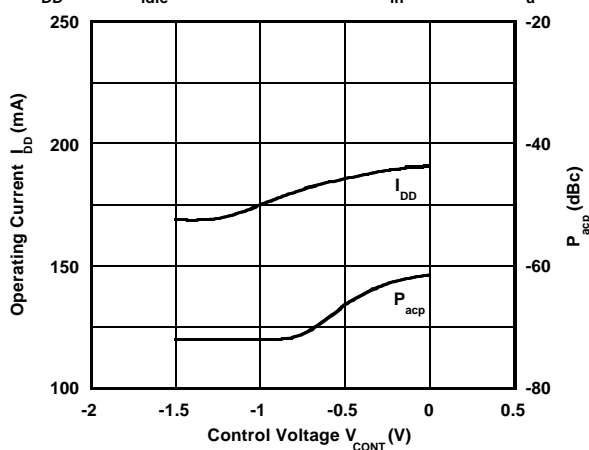
Gain, P_{acp} vs. Ambient Temperature

($V_{DD}=3.0V$, $V_{cont}=0V$, $I_{idle}=180mA$, $P_{out}=21dBm$, $f=1.9GHz$)



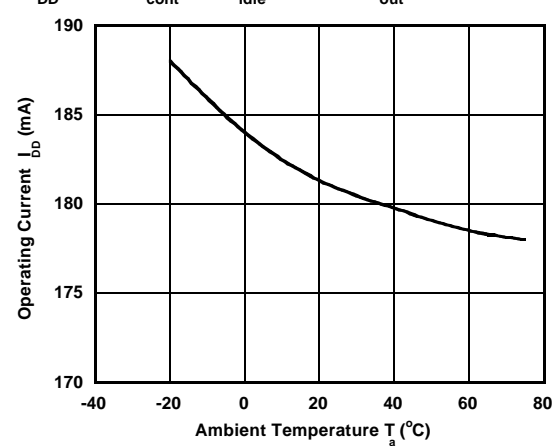
Operating Current, P_{acp} vs. Control Voltage

($V_{DD}=3.0V$, $I_{idle}=180mA$, $f=1.9GHz$, $P_{in}=-11dBm$, $T_a=25^\circ C$)



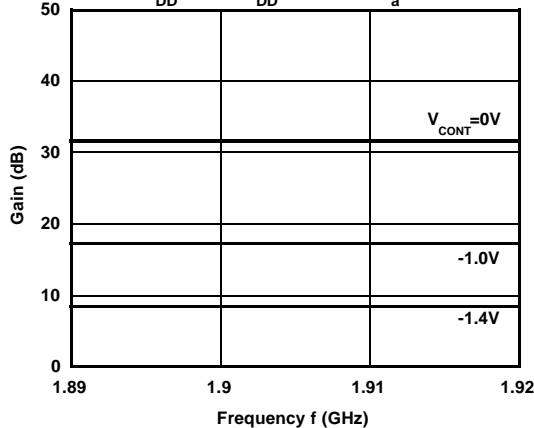
Operating Current vs. Ambient Temperature

($V_{DD}=3.0V$, $V_{cont}=0V$, $I_{idle}=180mA$, $P_{out}=21dBm$, $f=1.9GHz$)



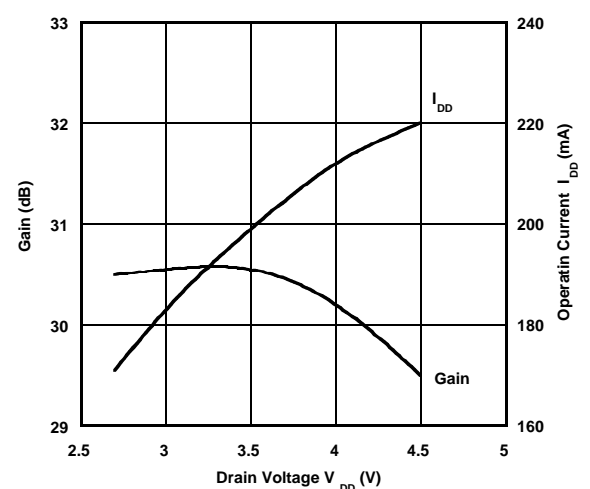
Gain vs. PHS Band Frequency vs. Control Voltage

($V_{DD}=3.0V$, $I_{DD}=180mA$, $T_a=25^\circ C$)



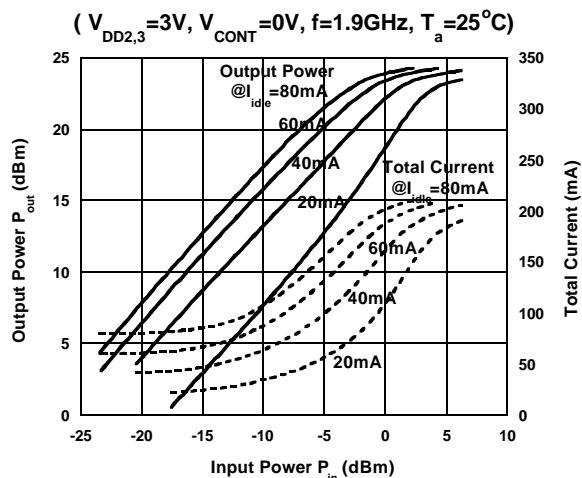
Gain, Operating Current vs. V_{DD}

($V_{cont}=0V$, $I_{idle}=180mA$ @ $V_{DD}=3.6V$, $P_{out}=21dBm$, $f=1.9GHz$, $T_a=25^\circ C$)

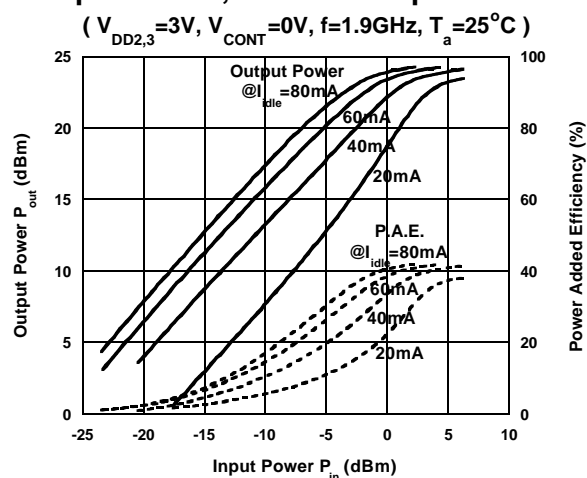


TYPICAL CHARACTERISTICS

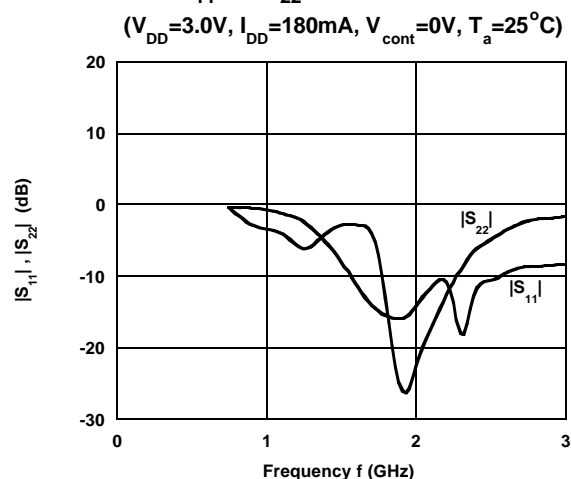
Output Power, Total Current vs. Input Power



Output Power, P.A.E. vs. Input Power

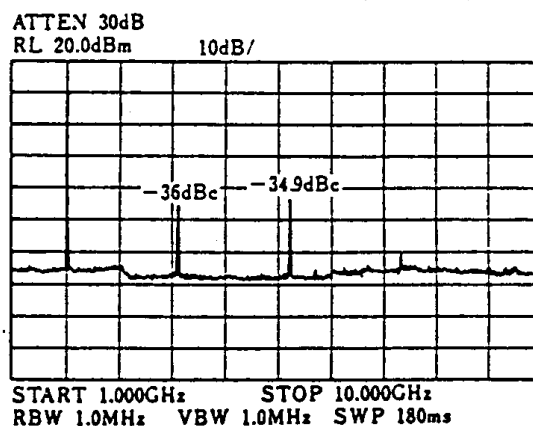


$|S_{11}|$, $|S_{22}|$ vs. Frequency



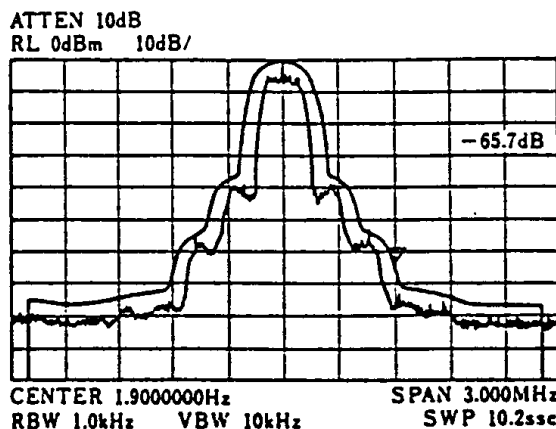
Harmonic Spectrum

(Suppressed Level for Fundamental Signal Level)
($P_{out}=21dBm$, $V_{DD}=3.0V$, $V_{cont}=0V$, $I_{dce}=180mA$, $T_a=25^\circ C$)



Output Spectrum

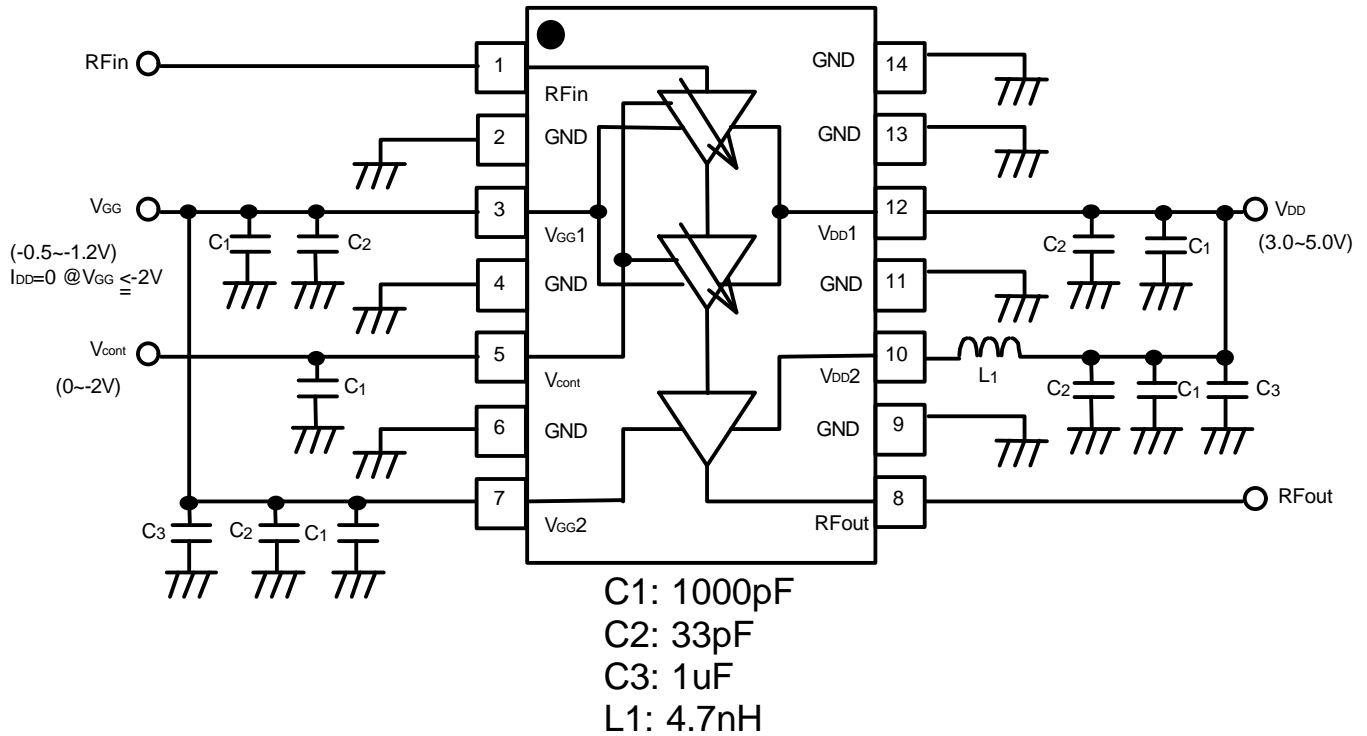
($V_{DD}=3.0V$, $I_{dce}=180mA$, $P_{out}=21dBm$, $V_{cont}=0V$, $T_a=25^\circ C$)



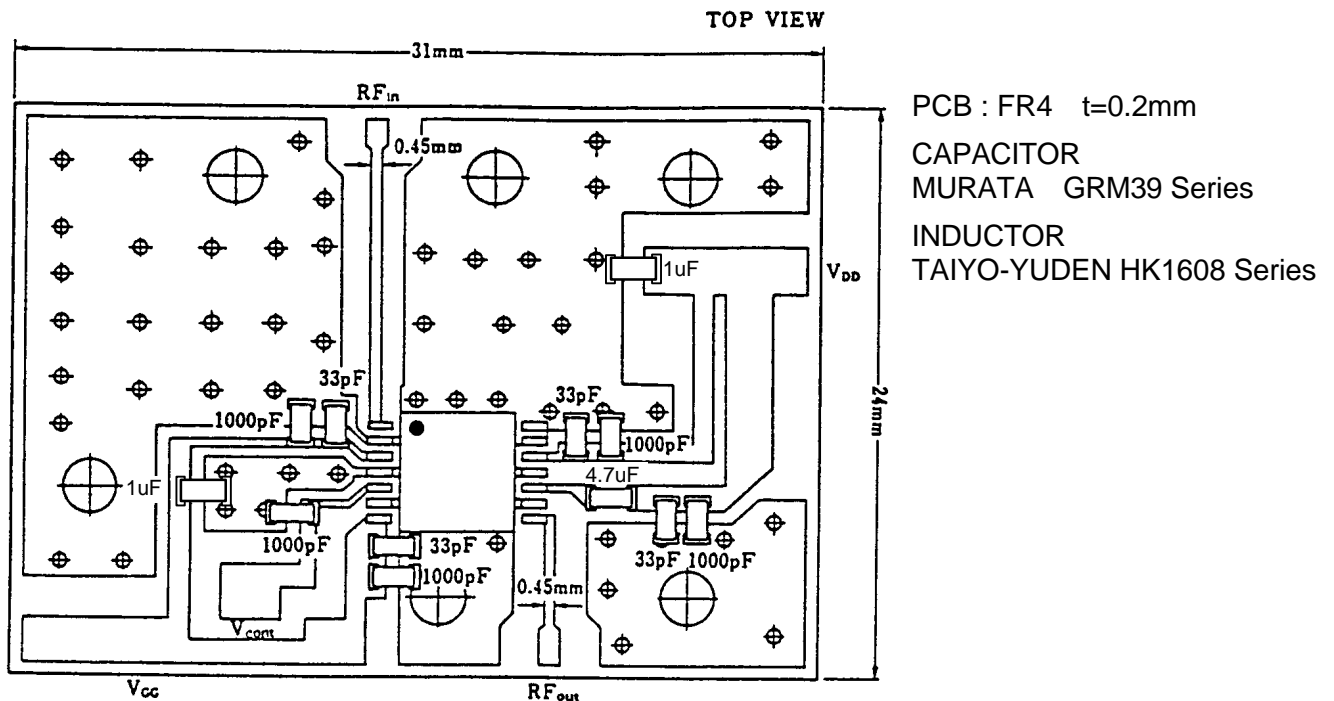
※All adjacent channel leakage power used in these evaluations are those of 600kHz offset from fundamental wave at PHS operating condition($\pi/4$ QPSK modulation)

NJG1302V

RECOMMENDED CIRCUIT



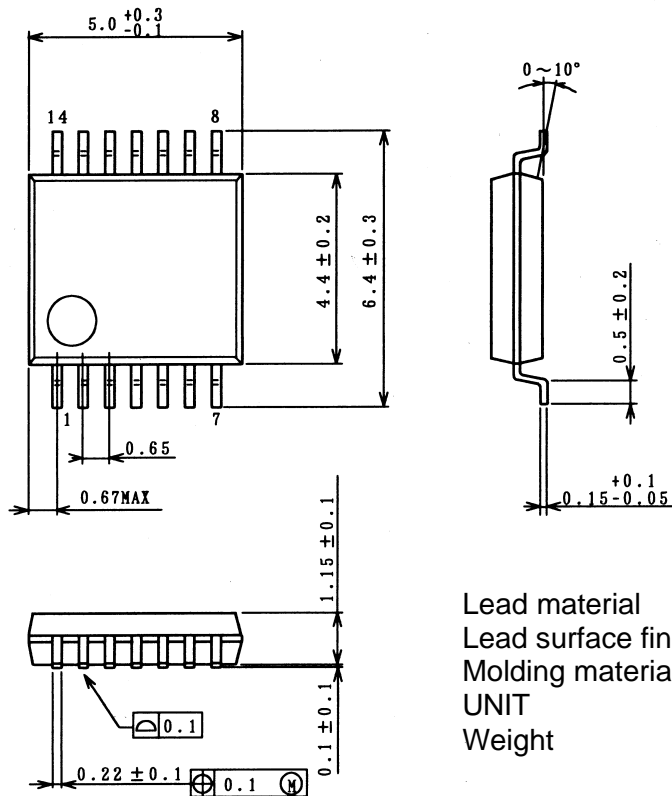
RECOMMENDED PCB DESIGN



The reflow method is recommended for this device to attach on PCB

NJG1302V

■PACKAGE OUTLINE (SSOP14)



Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.