

1Mb Ultra-Low Power Asynchronous CMOS SRAM

64Kx16 bit

Overview

The N01L163WN1A is an integrated memory device containing a 1 Mbit Static Random Access Memory organized as 65,536 words by 16 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology to provide both high-speed performance and ultra-low power. The base design is the same as NanoAmp's N01L1618N1A, which is processed to operate at lower voltages. The device operates with a single chip enable (\overline{CE}) control and output enable (\overline{OE}) to allow for easy memory expansion. Byte controls (\overline{UB} and \overline{LB}) allow the upper and lower bytes to be accessed independently. The N01L163WN1A is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to $+85^{\circ}\text{C}$ and is available in JEDEC standard packages compatible with other standard 64Kb x 16 SRAMs.

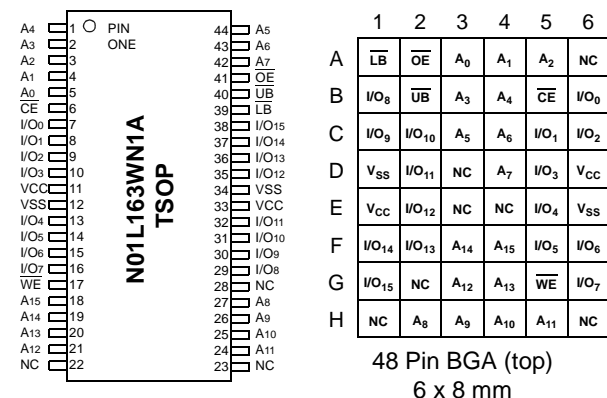
Features

- **Single Wide Power Supply Range**
2.3 to 3.6 Volts
- **Very low standby current**
2.0 μA at 3.0V (Typical)
- **Very low operating current**
2.0mA at 3.0V and 1 μs (Typical)
- **Very low Page Mode operating current**
0.8mA at 3.0V and 1 μs (Typical)
- **Simple memory control**
Single Chip Enable (\overline{CE})
Byte control for independent byte operation
Output Enable (\overline{OE}) for memory expansion
- **Low voltage data retention**
 $V_{CC} = 1.8\text{V}$
- **Very fast output enable access time**
30ns \overline{OE} access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **Compact space saving BGA package available**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply (V_{CC})	Speed	Standby Current (I_{SB}), Max	Operating Current (I_{CC}), Max
N01L163WN1AB	48 - BGA	-40°C to $+85^{\circ}\text{C}$	2.3V - 3.6V	55ns @ 2.7V 70ns @ 2.3V	20 μA	3 mA @ 1MHz
N01L163WN1AT	44 - TSOP II					

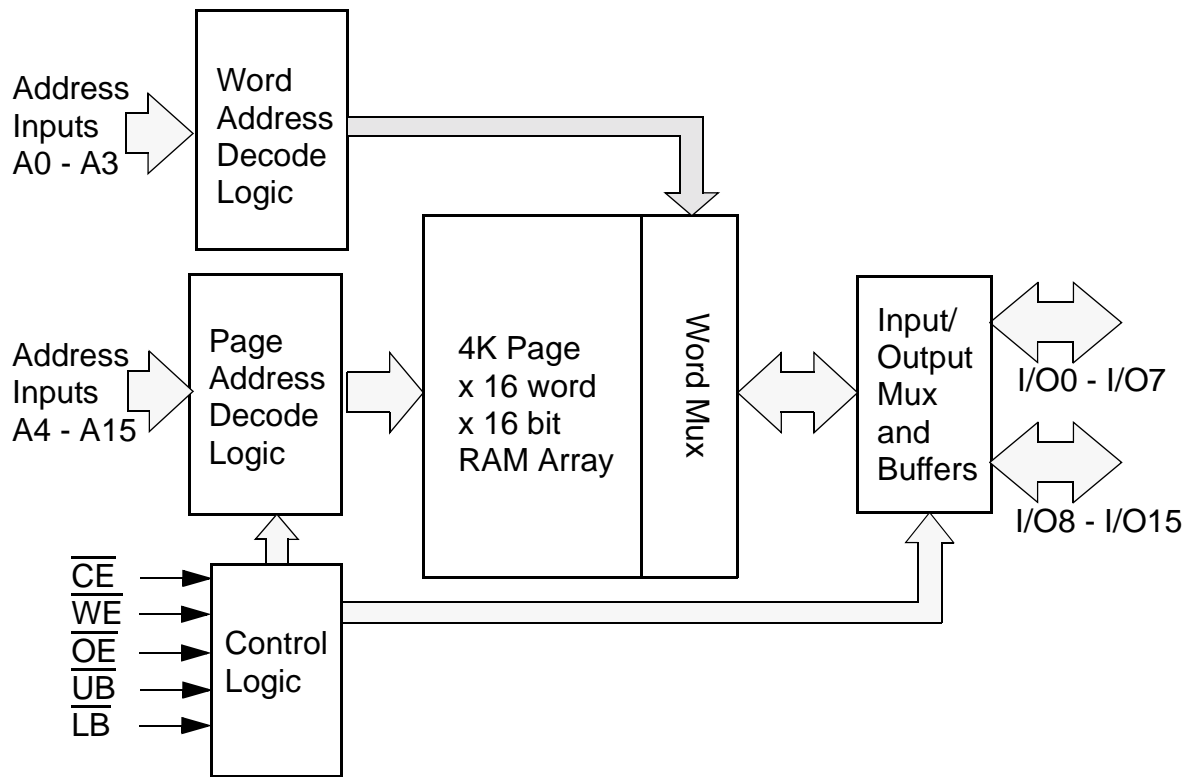
Pin Configurations



Pin Descriptions

Pin Name	Pin Function
A_0 - A_{15}	Address Inputs
\overline{WE}	Write Enable Input
\overline{CE}	Chip Enable Input
\overline{OE}	Output Enable Input
\overline{LB}	Lower Byte Enable Input
\overline{UB}	Upper Byte Enable Input
I/O_0 - I/O_{15}	Data Inputs/Outputs
NC	Not Connected
V_{CC}	Power
V_{SS}	Ground

Functional Block Diagram



Functional Description

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{UB}}$	$\overline{\text{LB}}$	$\text{I/O}_0 - \text{I/O}_{15}^1$	MODE	POWER
H	X	X	X	X	High Z	Standby ²	Standby
L	X	X	H	H	High Z	Active	Active
L	L	X ³	L ¹	L ¹	Data In	Write ³	Active
L	H	L	L ¹	L ¹	Data Out	Read	Active
L	H	H	L ¹	L ¹	High Z	Active	Active

- When $\overline{\text{UB}}$ and $\overline{\text{LB}}$ are in select mode (low), $\text{I/O}_0 - \text{I/O}_{15}$ are affected as shown. When $\overline{\text{LB}}$ only is in the select mode only $\text{I/O}_0 - \text{I/O}_7$ are affected as shown. When $\overline{\text{UB}}$ is in the select mode only $\text{I/O}_8 - \text{I/O}_{15}$ are affected as shown.
- When the device is in standby mode, control inputs ($\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{UB}}$, and $\overline{\text{LB}}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
- When $\overline{\text{WE}}$ is invoked, the $\overline{\text{OE}}$ input is internally disabled and has no effect on the circuit.

Capacitance¹

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{\text{IN}} = 0\text{V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$		8	pF
I/O Capacitance	$C_{\text{I/O}}$	$V_{\text{IN}} = 0\text{V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$		8	pF

- These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings¹

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	-0.3 to $V_{CC}+0.3$	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	-40 to 125	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	240°C, 10sec(Lead only)	°C

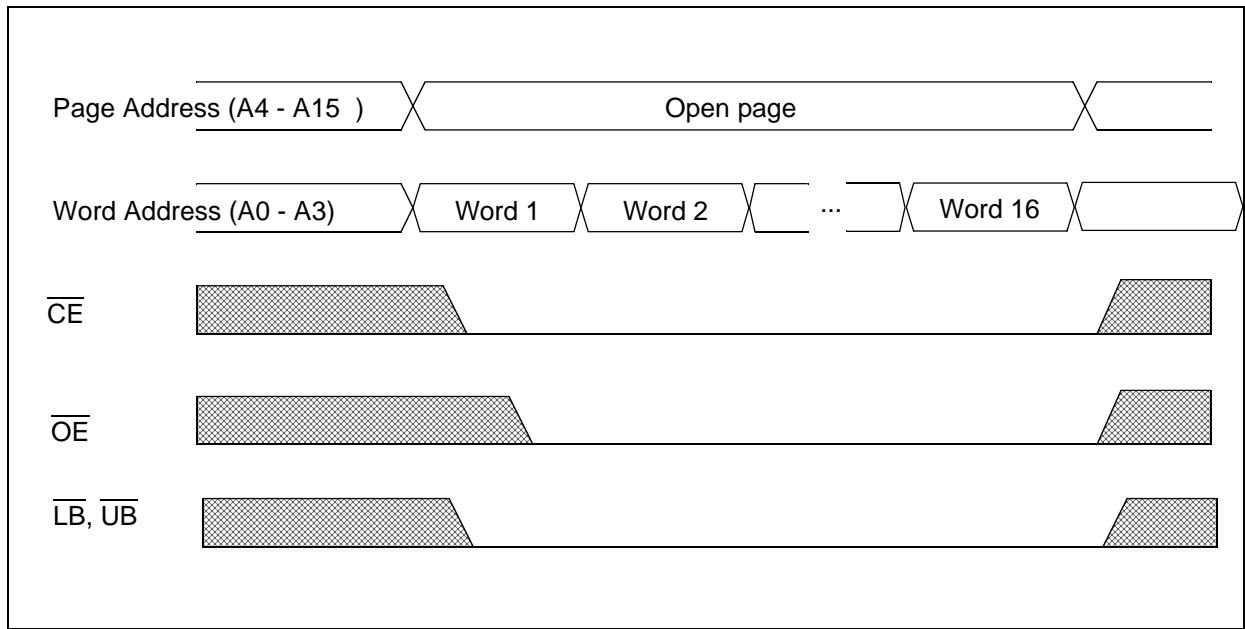
1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions	Min.	Typ ¹	Max	Unit
Supply Voltage	V_{CC}		2.3		3.6	V
Data Retention Voltage	V_{DR}	Chip Disabled ³	1.8			V
Input High Voltage	V_{IH}		1.8		$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}		-0.3		0.6	V
Output High Voltage	V_{OH}	$I_{OH} = 0.2mA$	$V_{CC}-0.2$			V
Output Low Voltage	V_{OL}	$I_{OL} = -0.2mA$			0.2	V
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}			0.5	μA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$ or Chip Disabled			0.5	μA
Read/Write Operating Supply Current @ 1 μs Cycle Time ²	I_{CC1}	$V_{CC}=3.6V$, $V_{IN}=V_{IH}$ or V_{IL} Chip Enabled, $I_{OUT} = 0$		2.0	3.0	mA
Read/Write Operating Supply Current @ 70 ns Cycle Time ²	I_{CC2}	$V_{CC}=3.6V$, $V_{IN}=V_{IH}$ or V_{IL} Chip Enabled, $I_{OUT} = 0$		9.5	14.0	mA
Page Mode Operating Supply Current @ 70ns Cycle Time ³ (Refer to Power Savings with Page Mode Operation diagram)	I_{CC3}	$V_{CC}=3.6V$, $V_{IN}=V_{IH}$ or V_{IL} Chip Enabled, $I_{OUT} = 0$		4.0		mA
Read/Write Quiescent Operating Supply Current ³	I_{CC4}	$V_{CC}=3.6V$, $V_{IN}=V_{IH}$ or V_{IL} Chip Enabled, $I_{OUT} = 0$, $f = 0$			3.0	mA
Maximum Standby Current ³	I_{SB1}	$V_{IN} = V_{CC}$ or 0V Chip Disabled $t_A = 85^\circ C$, $V_{CC} = 3.6V$		2.0	20	μA
Maximum Data Retention Current ³	I_{DR}	$V_{CC} = 1.8V$, $V_{IN} = V_{CC}$ or 0 Chip Disabled, $t_A = 85^\circ C$			10	μA

1. Typical values are measured at $V_{CC}=V_{CC}$ Typ., $T_A=25^\circ C$ and are not 100% tested.
2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
3. This device assumes a standby mode if the chip is disabled (\overline{CE} high). In order to achieve low standby current all inputs must be within 0.2 volts of either V_{CC} or V_{SS}

Power Savings with Page Mode Operation ($\overline{WE} = V_{IH}$)



Note: Page mode operation is a method of addressing the SRAM to save operating current. The internal organization of the SRAM is optimized to allow this unique operating mode to be used as a valuable power saving feature.

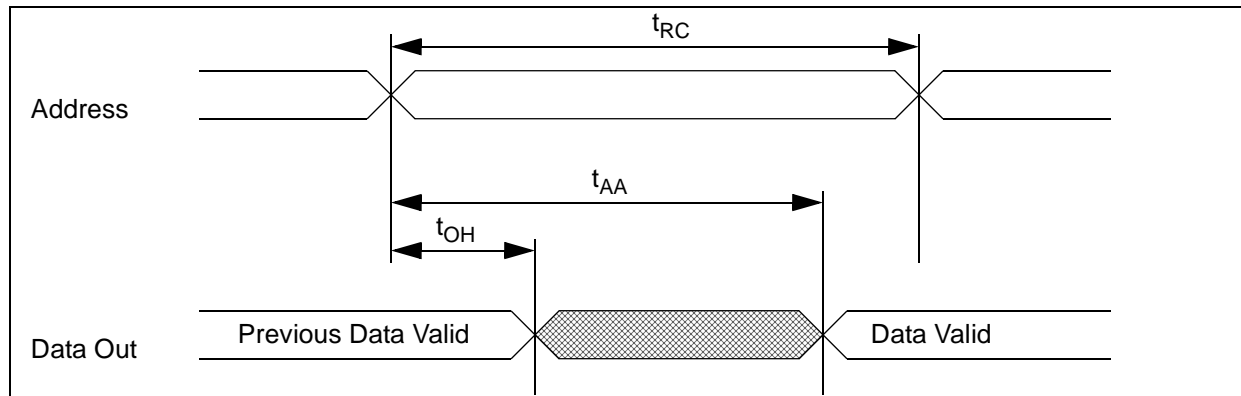
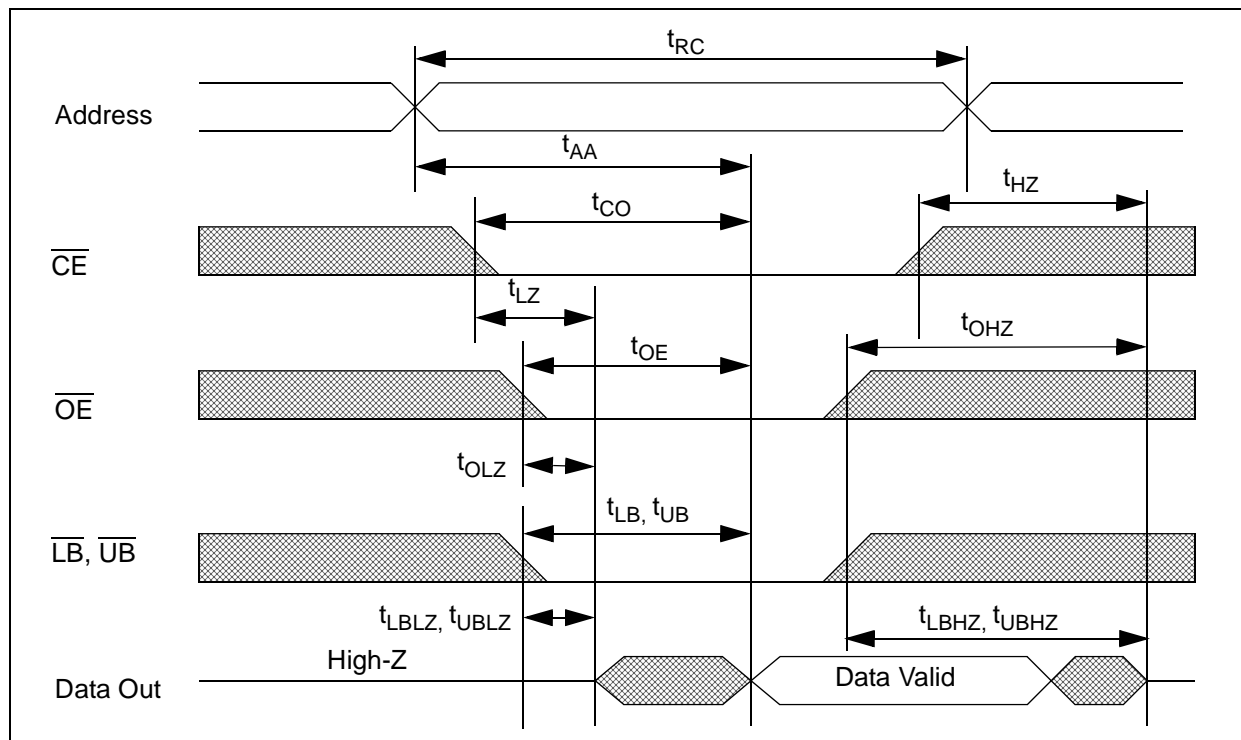
The only thing that needs to be done is to address the SRAM in a manner that the internal page is left open and 16-bit words of data are read from the open page. By treating addresses A0-A3 as the least significant bits and addressing the 16 words within the open page, power is reduced to the page mode value which is considerably lower than standard operating currents for low power SRAMs.

Timing Test Conditions

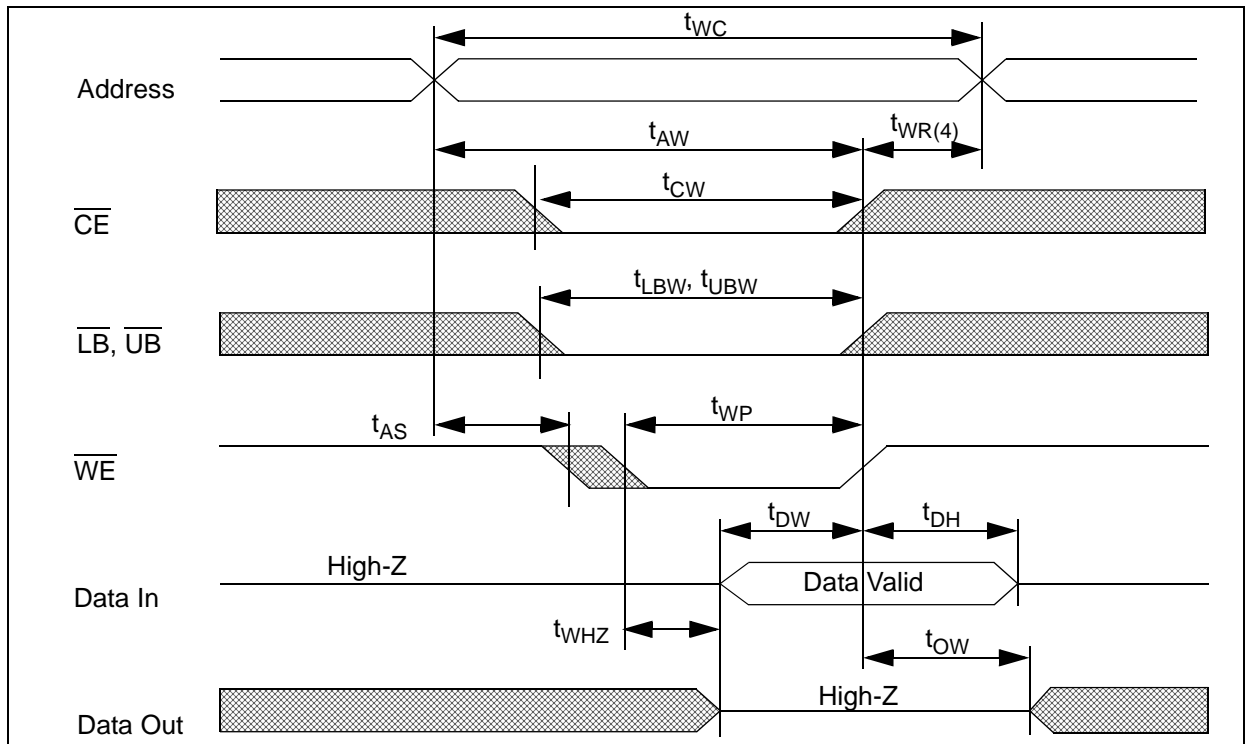
Item	
Input Pulse Level	$0.1V_{CC}$ to $0.9V_{CC}$
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5V_{CC}$
Output Load	CL = 30pF
Operating Temperature	-40 to +85 °C

Timing

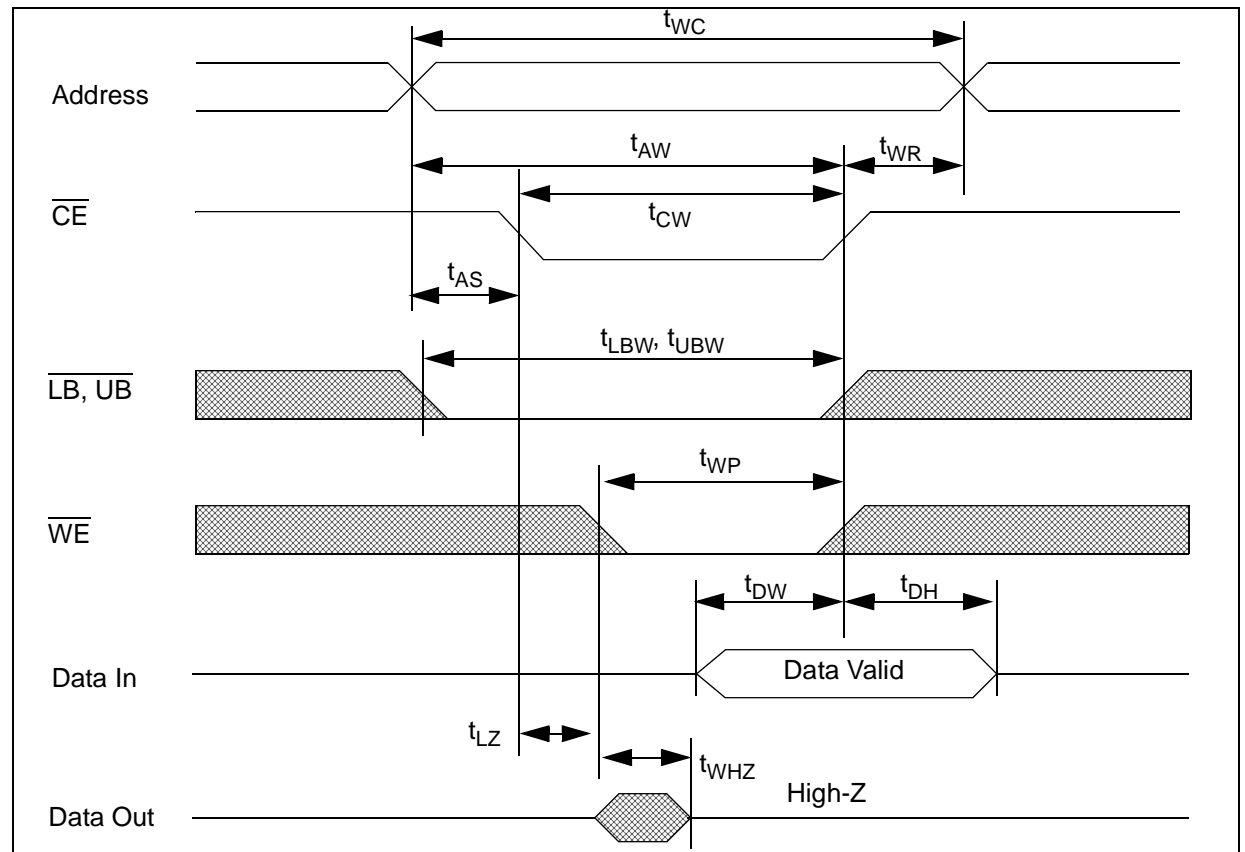
Item	Symbol	2.3 - 3.6 V		2.7 - 3.6 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	70		55		ns
Address Access Time	t_{AA}		70		55	ns
Chip Enable to Valid Output	t_{CO}		70		55	ns
Output Enable to Valid Output	t_{OE}		35		30	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		35		30	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	20	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	20	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	0	20	0	20	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Write Cycle Time	t_{WC}	70		55		ns
Chip Enable to End of Write	t_{CW}	50		40		ns
Address Valid to End of Write	t_{AW}	50		40		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	50		40		ns
Write Pulse Width	t_{WP}	40		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		20		20	ns
Data to Write Time Overlap	t_{DW}	40		35		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	5		10		ns

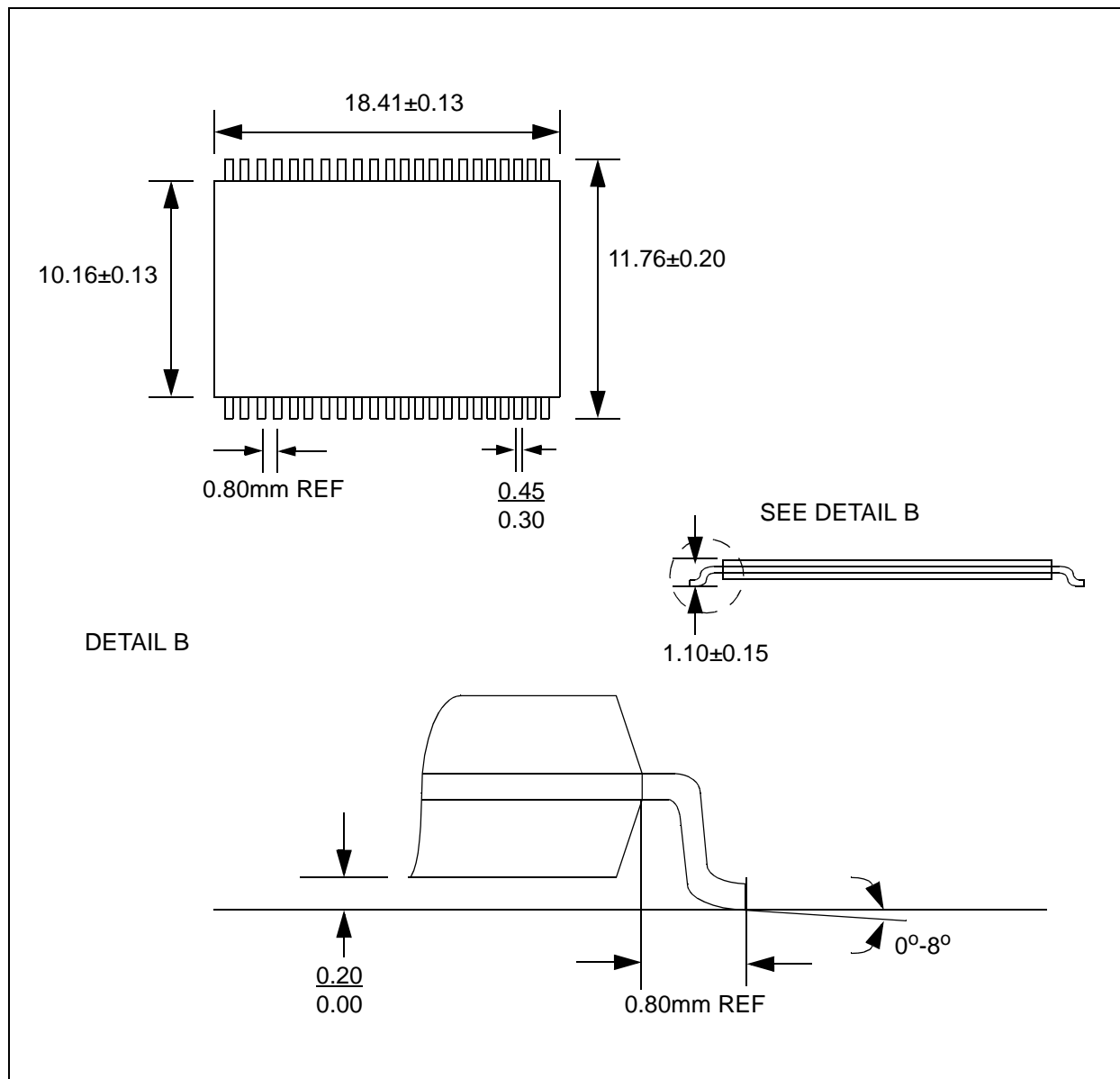
Timing of Read Cycle ($\overline{\text{CE}} = \overline{\text{OE}} = V_{\text{IL}}, \overline{\text{WE}} = V_{\text{IH}}$)**Timing Waveform of Read Cycle ($\overline{\text{WE}} = V_{\text{IH}}$)**

Timing Waveform of Write Cycle ($\overline{\text{WE}}$ control)



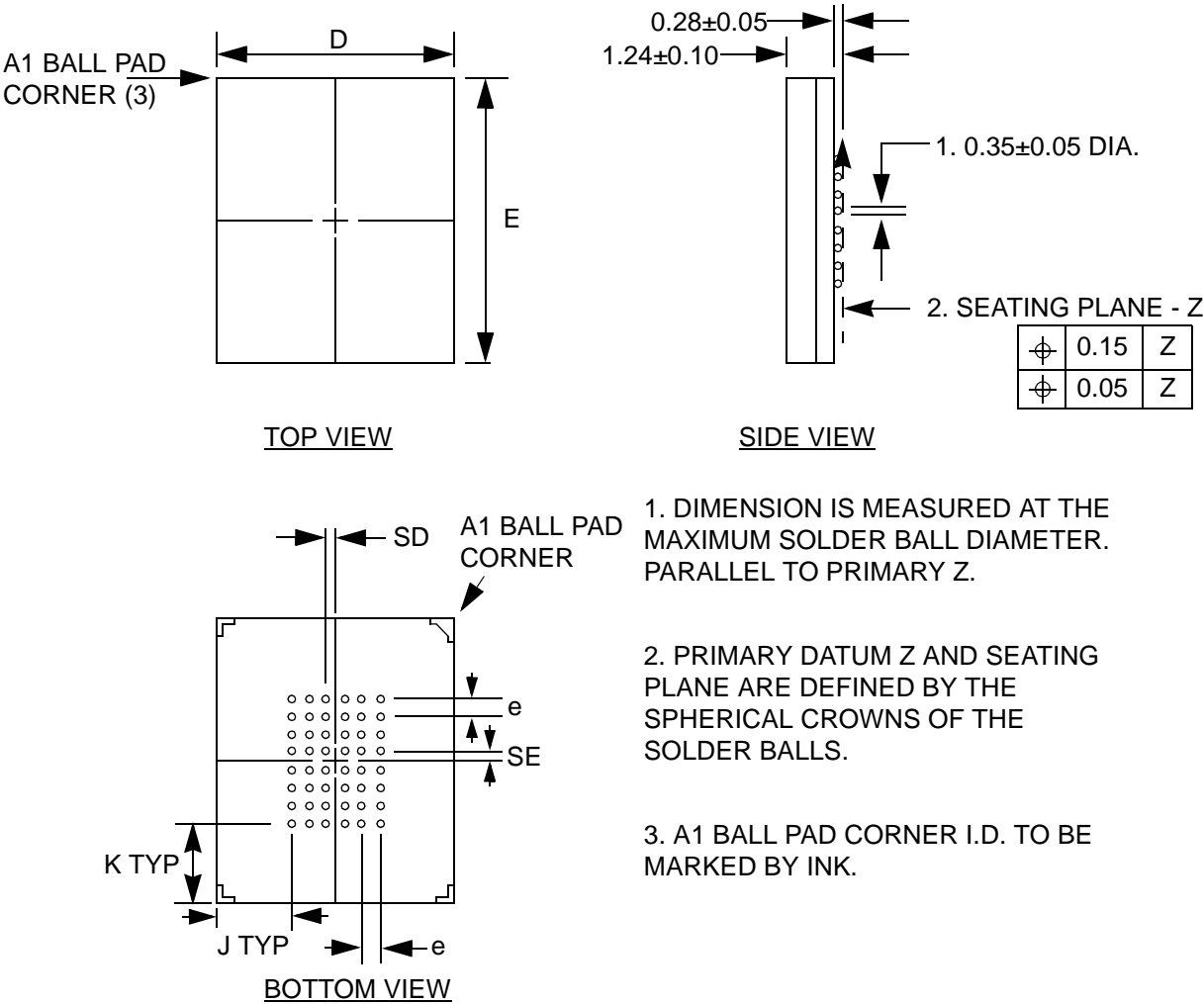
Timing Waveform of Write Cycle ($\overline{\text{CE}}$ Control)



44-Lead TSOP II Package (T44)**Note:**

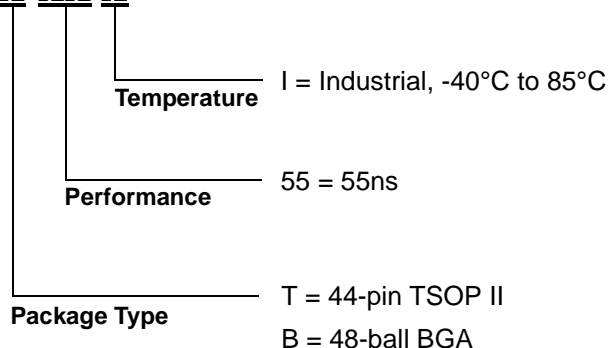
1. All dimensions in inches (Millimeters)
2. Package dimensions exclude molding flash

Ball Grid Array Package



Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

Ordering Information**N01L163WN1AX-XX X**

Note: Add -T&R following the part number for Tape and Reel. Orders will be considered in tray if not noted.

Revision History

Revision #	Date	Change Description
01	Jan. 2000	Initial advance release
02	Apr. 2001	Access time 55ns @ 3.0V, corrected voltage range, TSOP mechanical package drawing, misc. errata
03	Sept. 2001	Misc. modifications, preliminary release
04	Dec. 2001	Part number change from EM064L16, modified Overview and Features, added Page Mode Operation diagram, revised Operating Characteristics table, Functional Description table and Ordering Information diagram

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