Single-Chip SXGA LCD Controller

GENERAL DESCRIPTION

The MTL013 Single-Chip SXGA LCD Controller is a low-cost input format converter for TFT-LCD Monitor or LCD TV application which accepts 15-pin D-sub RGB graphic signals, YUV signals from digital video decoder or digital RGB graphic signals from PanelLink TMDS receiver. It includes a RGB/YUV input processor, video scaling up and down processor, OSD input interface and output display processor programmable timing controller in 208-pin PQFP package.

FEATURES

General

- Auto configuration of sampling clock frequency, phase, H/V center, as well as white balance.
- Auto detection of present or non-present or over range sync signals and their polarities.
- Composite sync separation and odd/even field detection of interlaced video.
- No external memory required.
- On-chip output PLL provide clock frequency fine-tune (inverse, duty cycle and delay).
- Serial 2-wire I^2C host interface.
- Parallel 6-wire or 10-wire data transfer host interface.
- Embedded OSD engine.
- Embedded 8-bit resolution ADC.
- Embedded programmable timing controller.
- Embedded power on reset circuit.
- 2.5V/3.3V supplier in 208-pin PQFP package.

Input Processor

- ADC sample rate and Digital Single RGB (24-bit) input rates up to 135MHz.
- Support both non-interlaced and interlaced RGB graphic input signals.
- Support sync on green input format.
- YUV 4:2:2 or YUV 4:1:1 (CCIR601/CCIR656) interlaced video input.
- Glue-less connection to Philips SAA711x digital video decoder
- Built-in YUV to RGB color space converter.
- Compliant with digital LVDS/PanelLink TMDS input interface.
- PC input resolution up to SXGA 1280X1024 @ 75Hz.

Video Processor

- Independent programmable Horizontal and Vertical scaling up ratios from 1 to 32
- Support scaling down ratios from 1 to 1/2.
- Flexible de-interlacing unit for digital YUV video input data.
- Zoom to full screen resolution of de-interlaced YUV video data stream.
- Built-in programmable gain control for white balance alignments.
- Built-in programmable 10-bit gamma correction table.
- Built-in programmable temporal color dithering
- Built-in programmable interpolation look-up table.
- Built-in programmable sharpening & smoothing filters for edge enhancement.
- Support smooth panning under viewing window change.

Output Processor

- Single pixel (18/24-bit) or Dual pixel (36/48-bit) per clock digital RGB output.
- Built-in output timing generator with programmable clock and H/V sync.
- Support VGA/SVGA/XGA/SXGA display resolution.
- Overlay input interface with external OSD controller.
- Double scan capability for interlaced input.

Preliminary

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BLOCK DIAGRAM

APPLICATIONS