System Reset (with built-in watchdog timer)
Monolithic IC MM1145

Outline

This IC has a built-in watchdog timer, with 2 channels for a clock monitoring function that monitors the microcomputer and outputs an intermittent reset signal if the microcomputer runs wild. Also, it has a power supply voltage monitoring function (system reset function) which generates a reset signal if power supply voltage is momentarily interrupted or drops, and performs power ON reset during normal power supply recovery and when power is turned on.

Features

1. Built-in edge trigger input watchdog timer
2. 2 clock pulse monitoring
3. Power ON reset time (T_{PR}) and watchdog timer monitoring time (T_{WD}) can be set individually with external elements (R, C)
4. Excellent watchdog timer monitoring time (T_{WD}) precision — A type : ±20%, B type : ±30%
5. Watchdog function stop pin allows use as system reset IC
6. Accurate power supply voltage drop detection — 4.2V±3.5%
7. Detection voltage has hysteresis — 100mV typ. ±0.14%/°C
8. Low reset minimum voltage
9. Low current consumption — 150µA typ.

Package

SOP-8C (MM1145AF, MM1145BF)

Applications

Voltage detection for CPUs, microcomputers, etc. and clock pulse monitoring

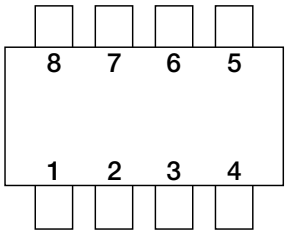
Series Table

Model	V_{SL}	T_{PR}	T_{WD}	T_{WR}
MM1145A	4.2	100ms	50ms	10ms
MM1145B		40ms	110ms	10ms

*C_T=0.02µF, RC_T=1MΩ

V_{SL} : Reset detection voltage
T_{PR} : Reset hold time during Vcc rise
T_{WD} : Watchdog timer monitoring time
T_{WR} : Reset time

Pin Assignment



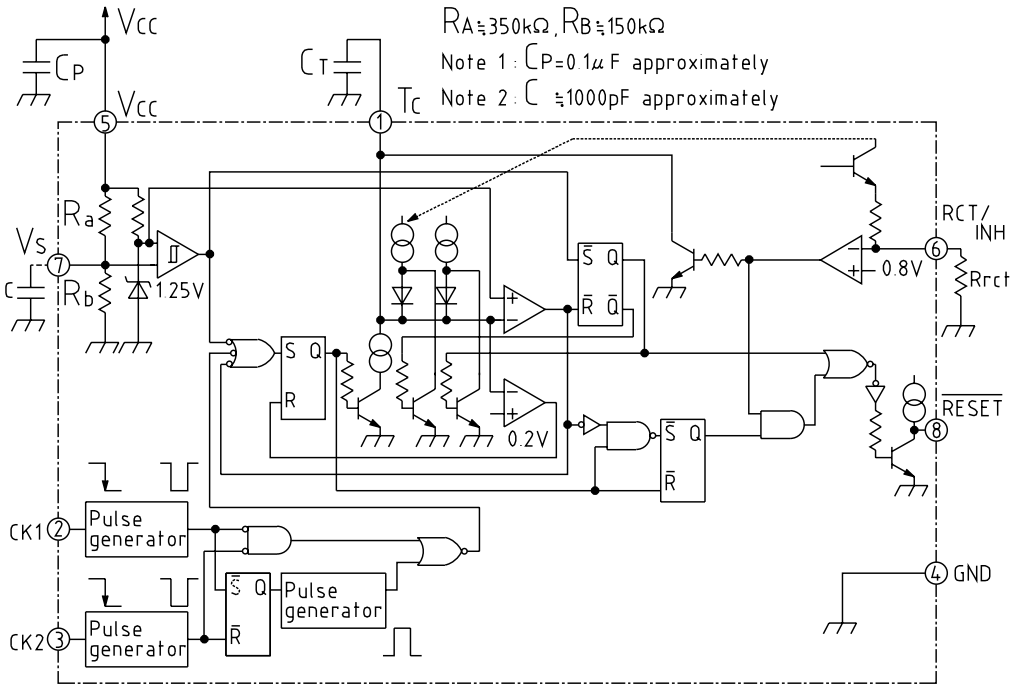
SOP-8C
(TOP VIEW)

1	TC
2	CK1
3	CK2
4	GND
5	Vcc
6	RCT
7	Vs
8	$\overline{\text{RESET}}$

Pin Description

Pin No.	Pin name	Function
1	TC	T_{WD}, T_{WR}, T_{PR} time setting pins. Time determined by external capacitor.
2	CK1	Clock input pin 1 Clock input from logic system
3	CK2	Clock input pin 2 Clock input from logic system
4	GND	GND pin
5	Vcc	Power supply pin Detection voltage 4.2V
6	RCT	Watchdog timer stop pin and T_{WD} adjustment pin Operation modes : Operation → Vcc, Stop → GND T_{WD} time determined by external resistor R_{RCT} and C_T
7	Vs	Detection voltage adjustment pin
8	$\overline{\text{RESET}}$	Reset output pin (low output)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	V_{CC} max.	−0.3~+7.5	V
CK pin input voltage	V_{CK}	−0.3~V_{CC}+0.3 (≦+7.5)	V
VS pin input voltage	V_{VS}	−0.3~V_{CC}+0.3 (≦+7.5)	V
Voltage applied to RCT pin	V_{RCT}	−0.3~V_{CC}+0.3 (≦+7.5)	V
Voltage applied to $\overline{\text{RESET}}$ pin	V_{OH}	−0.3~V_{CC}+0.3 (≦+7.5)	V
Allowable loss	Pd	300	mW
Storage temperature	T_{STG}	−40~+125	℃

Recommended Operating Conditions

Item	Symbol	Rating	Units
Power supply voltage	V_{CC}	+2.2~+7.0	V
$\overline{\text{RESET}}$ sync current	I_{OL}	0~4.0	mA
Clock monitoring time setting	T_{WD}	1.95~10000	ms
Power supply voltage rise and fall times	t_{FV}, t_{RV}	<300	µs
Clock rise and fall times	t_{FC}, t_{RC}	<100	µs
C_T pin capacitance	C_T	0.002~2	µF
RCT pin resistance	R_{RCT}	0.39~2	MΩ
Operating temperature	T_{OP}	−25~+75	℃

Electrical Characteristics (DC) (Except where noted otherwise, Ta=25℃, Vcc=5.0V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current		I_{CC}	During watchdog timer operation		150	180	µA
Detection voltage		V_{SL}	V_S=OPEN, V_{CC}	4.05	4.20	4.35	V
		V_{SH}	V_S=OPEN, V_{CC}	4.15	4.30	4.45	
Detection voltage temperature coefficient		$\frac{V_S}{\Delta T}$	V_{SH}−V_{SL}, V_{CC}		±0.01		%/℃
Hysteresis voltage		V_{HYS}		50	100	150	mV
CK input threshold		V_{TH}		0.8	1.2	2	V
CK input current		I_{IH}	V_{CK}=5.0V		0	1	µA
		I_{IL}	V_{CK}=0V	−14.5	−8.5	−4.5	
Output voltage (High)		V_{OH}	$I_{\overline{\text{RESET}}}$=−1µA, V_S=OPEN	4.0	4.5		V
Output voltage (Low)		$V_{OL}1$	$I_{\overline{\text{RESET}}}$=0.5mA, V_S=0V		0.10	0.20	V
		$V_{OL}2$	$I_{\overline{\text{RESET}}}$=2.0mA, V_S=0V		0.15	0.35	
						0.30	
Output sync current		I_{OL}	$V_{\overline{\text{RESET}}}$=1.0V, V_S=0V	2	4		mA
C_T charge current	MM1145A	$I_{CT}1$	During watchdog timer operation	−0.40	−0.48	−0.60	µA
	MM1145B			−0.17	−0.22	−0.30	
	MM1145A	$I_{CT}2$	During power ON reset operation	−0.21	−0.31	−0.62	µA
	MM1145B			−0.62	−0.93	−2.33	
Minimum operating power supply voltage to ensure $\overline{\text{RESET}}$		V_{CCL}	$V_{\overline{\text{RESET}}}$=0.4V $I_{\overline{\text{RESET}}}$=0.1mA		0.8	1.0	V

Electrical Characteristics (DC)

(Except where noted otherwise, Ta=25°C, V_{CC}=5.0V)
(Except where noted otherwise, resistance unit is Ω)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V_{CC} input pulse width		T_{PI}	V_{CC} 5.0V / 4.0V	8			µs
CK input pulse width		T_{CKW1} T_{CKW2}	CK or	3			µs
CK input cycle *7		T_{CK1} T_{CK2}	or	200			µs
Watchdog timer monitoring time *1	MM1145A	T_{WD}	C_T=0.02µF, R_{RCT}=1M	40	50	60	ms
	MM1145B			80	110	140	
Watchdog timer reset time *2	MM1145A	T_{WR}	C_T=0.02µF, R_{RCT}=1M	5	10	15	ms
	MM1145B			5	10	15	
Reset hold time for power supply rise *3	MM1145A	T_{PR}	C_T=0.02µF, R_{RCT}=1M, V_{CC}	50	100	150	ms
	MM1145B			20	40	60	
Output delay time from V_{CC} *4		T_{PD}	$\overline{RESET}$ pin, R_L=10k, C_L=20pF		2	10	µs
Output rise time *5		t_R	$\overline{RESET}$ pin, R_L=10k, C_L=20pF		2.0	4.0	µs
Output fall time *5		t_F	$\overline{RESET}$ pin, R_L=10k, C_L=20pF		0.2	1.0	µs

Notes:

*1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output.
In other words, reset output is output if a clock pulse is not input during this time.

*2 Reset time means reset pulse width. However, this does not apply to power ON reset.

*3 Reset hold time is the time from when V_{CC} exceeds detection voltage (V_{SHR}) during power ON reset until reset release ($\overline{RESET}$ output high).

*4 Output delay time is the time from when power supply voltage drops below detection voltage (V_{SL}) until reset state occurs ($\overline{RESET}$ output low).

*5 The voltage range when measuring output rise and fall time is 10~90%.

*7 1 Set CK1 and CK2 input cycles within the following range.

$T_{CK1} \leqq nT_{CK2} < T_{WD}$ (ms) ($n \leqq 1$)

$\overline{RESET}$ output may go low even if CK1 and CK2 are input without these conditions being met.
(Recommended use is for $T_{CK1} \leqq nT_{CK2}$)

2 T_{CK1}, $T_{CK2} \leqq$ 200 µs results in the following operation.
Discharge switches to charging with the CK2 pulse (negative edge) that inputs 200µs after C_T switches from charging to discharge by the CK2 pulse (negative edge). $\overline{RESET}$ output stays high while this operation is being repeated. (However, T_{CK1}, $T_{CK2} \geqq$ 20µs.)

Formula for C_T Pin External Constant

Watchdog timer monitoring time (T_{WD}), watchdog timer reset time (T_{WR}) and reset hold time (T_{PR}) during power supply rise can be changed by varying C_T capacitance. T_{WD} also can be changed with R_{RCT}.
The variable times are expressed by the following.

1. MM1145A

T_{PR} (ms) ≒ 5000 × C_T (μF)
T_{WD} (ms) ≒ 2500 × C_T (μF) × R_{RCT} (MΩ)
T_{WR} (ms) ≒ 500 × C_T (μF)

Example : when C_T=0.02μF, R_{RCT}=1MΩ
T_{PR} ≒ 100ms
T_{WD} ≒ 50ms
T_{WR} ≒ 10ms

2. MM1145B

T_{PR} (ms) ≒ 2000 × C_T (μF)
T_{WD} (ms) ≒ 5500 × C_T (μF) × R_{RCT} (MΩ)
T_{WR} (ms) ≒ 500 × C_T (μF)

Example : when C_T=0.02μF, R_{RCT}=1MΩ
T_{PR} ≒ 40ms
T_{WD} ≒ 110ms
T_{WR} ≒ 10ms

Formula for Watchdog Timer Monitoring Time (T_{WD}) Adjustment

The ratio between T_{PR} and T_{WD} can be changed within the range below by adjusting T_{WD} with R_{RCT}.

1. MM1145A

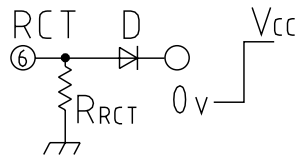
T_{WD}/T_{PR} ≒ 2.0 × R_{RCT} (0.39 (MΩ) ≦ R_{RCT} ≦ 2 (MΩ))

2. MM1145B

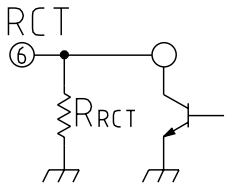
T_{WD}/T_{PR} ≒ 2.75 × R_{RCT} (0.39 (MΩ) ≦ R_{RCT} ≦ 2 (MΩ)

How to Use RCT Pin

Example 1



Example 2



1. Watchdog timer operates when RCT pin is open.
2. Watchdog timer stops operating when RCT pin is connected to ground.

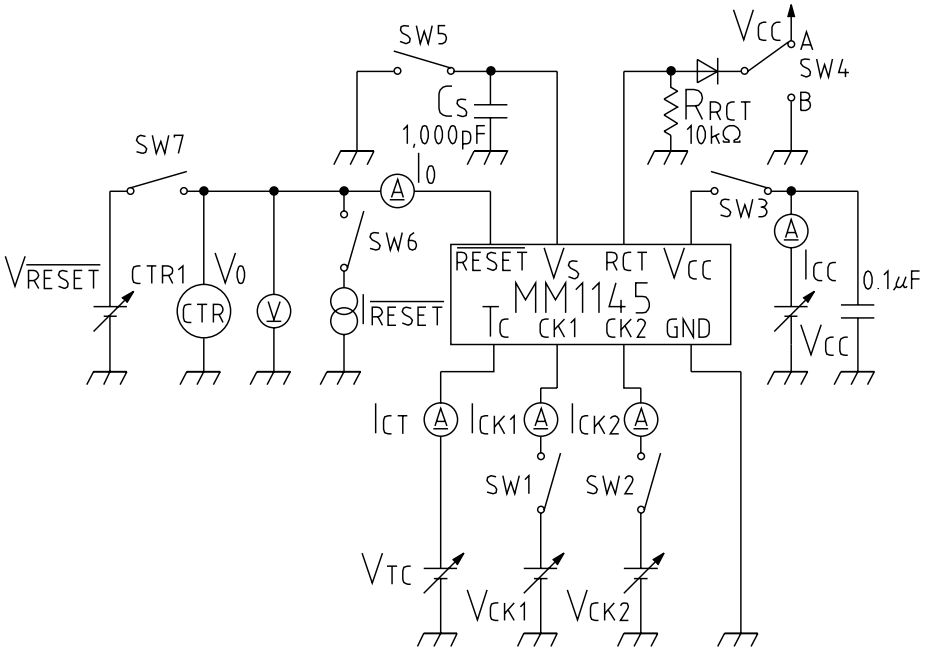
Description of Operation

1. $\overline{\text{RESET}}$ goes low when V_{CC} rises to approximately 0.8V.
   Approximately 1μA (V_{CC}=0.8V) of pull up current is output from RESET.
2. Capacitor C_T charging starts when V_{CC} rises to V_{SH} (≒ 4.3V). Output is in reset state at this time.
3. Output reset is released ($\overline{\text{RESET}}$ goes high) after a certain time (T_{PR}), from when C_T starts charging until discharge (the time from when C_T voltage reaches a certain threshold value VT1 (≒ 1.4V) until C_T voltage drops to a certain threshold value VT2 (≒ 0.2V).
   Reset hold time : T_{PR} is as follows.
   T_{PR} (ms) ≒ 5000 × C_T (μF)
   C_T charging starts again after reset release, and watchdog timer operation begins.
   Clock input during power ON reset time (T_{PR}) will cause mis-operation.
4. If CK1 and CK2 are input in that order (or simultaneously) during C_T charging, CK2 negative edge trigger causes the TC pin to switch from charging to discharge.
5. Discharge switches to charging when C_T voltage drops to threshold value VT2 (≒ 0.2V). Steps 4 and 5 are repeated while a normal clock is input from the logic system.

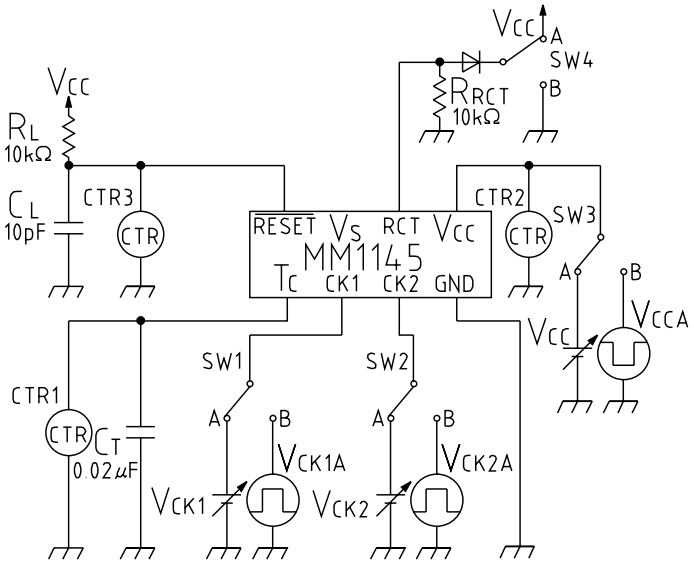
6. Operation is as follows if either clock CK1 or CK2 ceases (the figure shows CK1).
   Output goes to reset state ($\overline{\text{RESET}}$ goes low) when C_T voltage reaches reset ON threshold value VT1 (≒ 1.4V).
   The formula for C_T charging time (T_{WD} : watchdog timer monitoring time) until reset is output is as follows.
   T_{WD} (ms) ≒ 2500 × C_T (μF)
7. Watchdog timer reset time T_{WR} is the discharge time until C_T voltage drops to reset OFF threshold value VT2 from reset ON threshold value VT1. The formula is as follows.
   T_{WR} (ms) ≒ 500 × C_T (μF)
   After reset OFF threshold value is reached, output reset is released and C_T starts charging. Thereafter, steps 4 and 5 are repeated if a normal clock is input, and when one of the clocks ceases, 6 and 7 are repeated.
   In the same way, 6 and 7 are repeated if both clocks CK1 and CK2 cease.
8. Reset is output when V_{CC} drops to V_{SL} (≒ 4.2V). C_T is charged simultaneously.
9. C_T charging starts when V_{CC} rises to V_{SH}.
   When V_{CC} drops momentarily, C_T charging begins after the charge is first discharged, if the time from V_{CC} dropping below V_{SL} until it rises to V_{SH} is longer than the V_{CC} input pulse width standard value T_{PI}.
10. Output reset is released after V_{CC} goes above V_{SH} and after T_{PR}, and the watchdog timer starts.
11. Watchdog timer operation can be stopped by switching R_{CT} voltage from high to low. (Clocks CK1 and CK2 are invalid. Regardless of status, TC pin voltage discharges quickly and goes to 0V.) This operation can be applied from any timing. In this state the IC functions as a reset IC with power ON reset.
12. Watchdog timer operation re-starts when R_{CT} voltage switches to high.
13. When power is OFF, reset is output if V_{CC} goes below V_{SL}.
14. When Vcc drops to 0V, reset output is held until V_{CC} reaches 0.8V.

Measuring Circuit

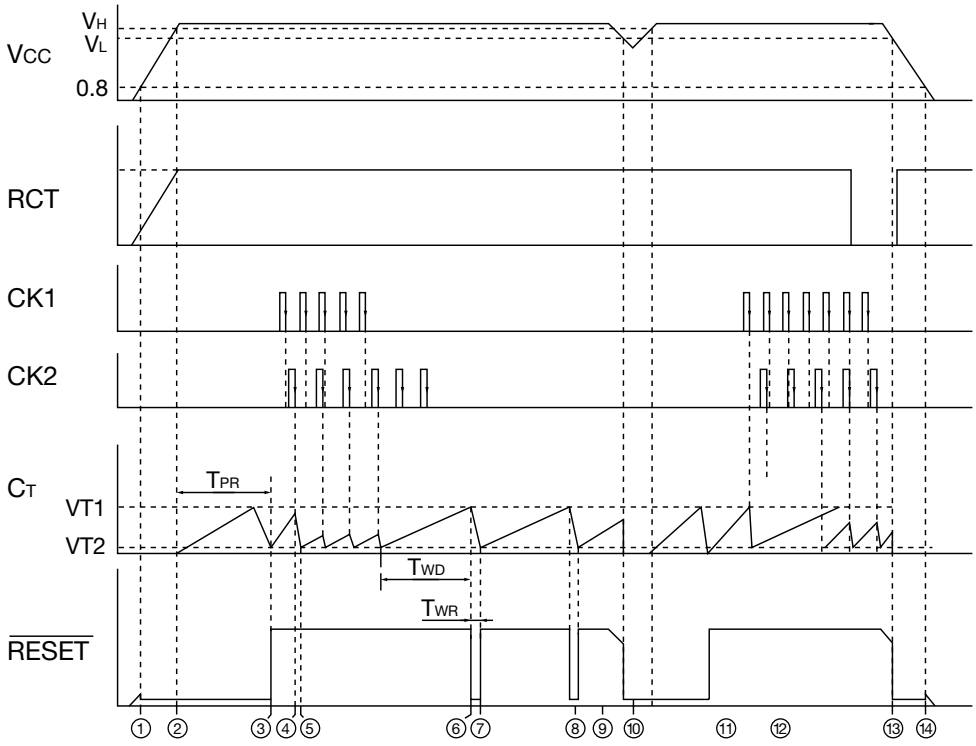
Measuring Circuit 1



Measuring Circuit 2



Timing Chart



Basic Circuit Diagram