AGP MEMORY MODULE

MT1LSDT132AGP

For the latest data sheet, please refer to the Micron Web site: www.micron.com/datasheets

FEATURES

- AGP Inline Memory Module (AIMM)
- 4MB (1 Meg x 32)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Fits in AGP port slot

OPTIONS — MARKING

- Timing (Cycle Time)
  6ns — -6

KEY SDRAM COMPONENT TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME CL = 3*	SETUP TIME	HOLD TIME
-6	166 MHz	5.5ns	1.5ns	1ns

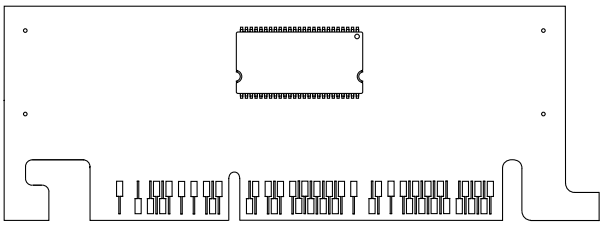
*CL = CAS (READ) latency

PART NUMBERS

PART NUMBER	CONFIGURATION	DEVICE PACKAGE
MT1LSDT132AGP-6_	1 Meg x 32	TSOP

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT1LSDT132AGP-6E1.

66-Pin AIMM (Front View)



PIN ASSIGNMENT

PIN	B	A	PIN	B	A
1	NC	NC	34	VDDQ	VDDQ
2	NC	TYPEDET	35	DQ16	A0
3	NC	NC	36	DQ15	A9
4	NC	NC	37	GND	GND
5	GND	GND	38	DQ14	A11
6	NC	NC	39	DQ13	A8
7	NC	NC	40	VDDQ	VDDQ
8	DQ27	NC	41	DQ12	A10
9	VCC	VCC	42	NC	NC
10	DQ28	DQM3	43	GND	GND
11	DQ29	NC	44	NC	NC
12	DQ30	DQ24	45	VCC	VCC
13	GND	GND	46	DQ11	A7
14	NC	NC	47	VDDQ	CS#
15	DQ31	DQ25	48	NC	NC
16	VCC	VCC	49	GND	GND
17	DQM2	DQ26	50	NC	A6
18	NC	NC	51	DQ10	A1
19	GND	GND	52	VDDQ	VDDQ
20	DQ23	WE#	53	DQ9	A5
21	DQ22	FSEL	54	DQ8	A2
22	KEYWAY	KEYWAY	55	GND	GND
23	KEYWAY	KEYWAY	56	DQM1	A4
24	KEYWAY	KEYWAY	57	DQ0	A3
25	KEYWAY	KEYWAY	58	VDDQ	VDDQ
26	DQ21	TCLK0	59	NC	NC
27	DQ20	TCLK1	60	DQ1	DQ5
28	VCC	VCC	61	GND	GND
29	DQ19	CAS#	62	DQ2	DQ6
30	DQ18	NC	63	DQ3	DQ7
31	GND	GND	64	VDDQ	VDDQ
32	NC	NC	65	DQ4	DQM0
33	DQ17	RAS#	66	NC	NC

NOTE: Pins 22A–25A and 22B–25B are keyway pins.

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INTRODUCTION

This module is designed to be used in the AGP port in PC motherboards and is intended to be a mid-level cost between no added graphics memory and more expensive AGP card solutions.

Accelerated Graphics Port (AGP) technology provides a dedicated, high-speed port for the movement of large blocks of 3D texture data between the PC's graphics controller and system memory. AGP is based on a set of performance extensions or enhancements to the PCI bus. AGP neither replaces nor diminishes the necessity of PCI in the system. This high speed port is physically, logically, and electrically independent of the PCI bus. This module is targeted for AGP systems supporting the AIMM socket.

GENERAL DESCRIPTION

The MT1LSDT132AGP is a high-speed CMOS, dynamic random-access, 4MB solid-state memory organized in a x32 configuration. This module is configured as a single bank with a synchronous interface (all signals are registered on the positive edge of the clock signal TCLK0). Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 selects the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

This module uses a single 64Mb 2 x 32 SDRAM component. Note: only 4MB of the component are addressed by the AIMM design.

This module provides for a programmable READ or WRITE burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. This module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

For more information regarding SDRAM operation, refer to the 64Mb: x32 SDRAM data sheet.

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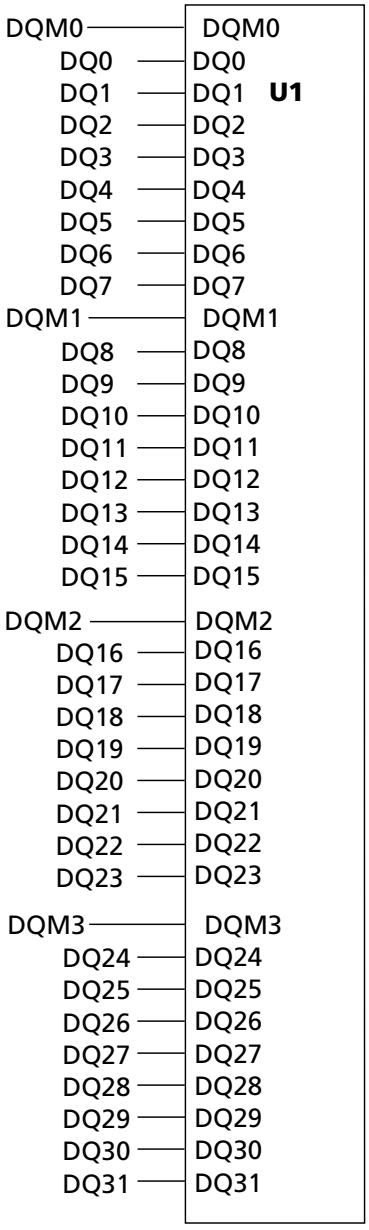
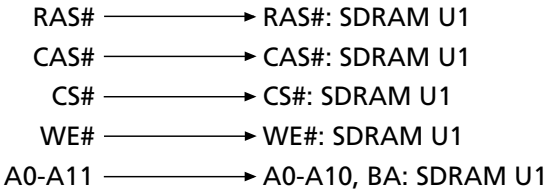
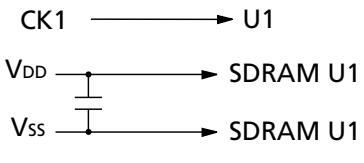
FUNCTIONAL BLOCK DIAGRAM
MT1LSDT132APG (4MB)







U1 = MT48LC2M32B2TG SDRAM

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PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
A33, A29, A20	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S0#-S3#) define the command being entered.
A26, A27	TCK0	Input	Clock: TCK0 is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
A47	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# is considered part of the command code.
A10, A17, A56, A65	DQM0-DQM3	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
A35, A36, A38, A39, A41, A46, A50, A51, A53, A54, A56, A57	A0-A11/BA	Input	Address Inputs: A0-A11/BA are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
B57, B60, B62, B63, B65, A60, A62, A63, B54, B53, B51, B46, B41, B39, B38, B36, B35, B33, B30, B29, B27, B26, B21, B20, A12, A15, A17, B8, B10, B11, B12, B15	DQ0-DQ31	Input/ Output	Data I/O: Data bus.
A64, B64, B58, A52, B52, B47, A40, B40, A34, B34	V_{SS}	Supply	Ground.
A45, B45, A28, B28, A25, B25, A16, B16, A9, B9	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
A5, B5, A13, B13, A19, B19, A23, B23, A31, B31, A61, B61, A55, B55, A49, B49, A43, B43, A37, B37	GND	Supply	Ground
A1, B1, B2, A3, B3, A4, B4, A6, B6, A7, B7, A8, A11, A14, B14, A18, B18, A30, A32, B32, A42, B42, A44, B44, A48, B48, B50, A59, B59, A66, B66	NC	–	No Connects: These pins are not connected.

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Commands

The Truth Table provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE – Commands and DQM Operation

Note: 1

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-A10 define the op-code written to the Mode Register.
3. A0-A10 provide row address, BA0 and BA1 determine which device bank is made active.
4. A0-A7 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0 and BA1 determine which device bank is being read from or written to.
5. A10 LOW: BA0 and BA1 determine the device bank being precharged. A10 HIGH: All device banks precharged and BA0 and BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay). DQM0 controls DQ0-DQ7; DQM1 controls DQ8-DQ15; DQM2 controls DQ16-DQ23; and DQM3 controls DQ24-DQ31.

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BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

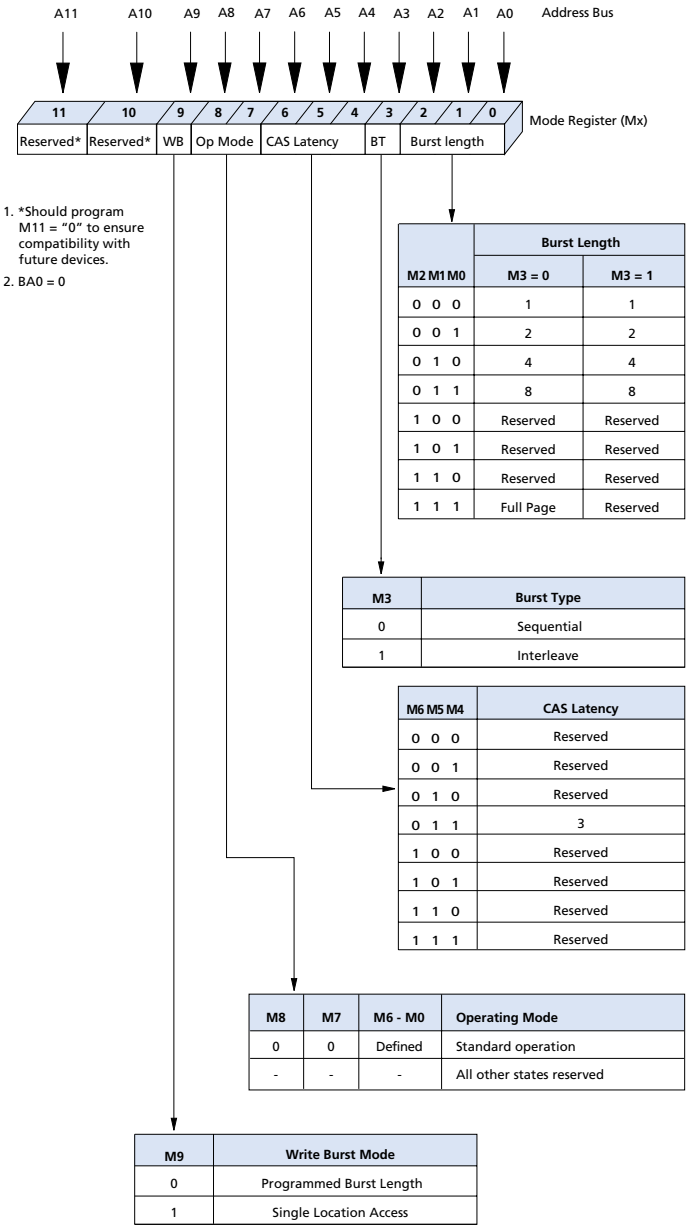

Figure 1
Mode Register Definition

Table 1
Burst Definition

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n = A0-A7 (Location 0-256)	Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... …Cn - 1, Cn…	Not Supported

NOTE:
1. For a burst length of two, A1-A7 select the block-of-two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2-A7 select the block-of-four burst; A0-A1 select the starting column within the block.
3. For a burst length of eight, A3-A7 select the block-of-eight burst; A0-A2 select the starting column within the block.
4. For a full-page burst, the full row is selected and A0-A7 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0-A7 select the unique column to be accessed, and mode register bit M3 is ignored.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) .. 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

Notes: 1, 6 (V_{DD} = +3.3V ±0.3V) (Notes following parameter tables.)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3.125	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	-5	5	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DD}	I_{OZ}	-5	5	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V	

I_{DD} SPECIFICATIONS AND CONDITIONS

Notes: 1, 6, 11, 13 (V_{DD} = +3.3V ±0.3V) (Notes following parameter tables.)

PARAMETER/CONDITION		SYMBOL	MAX -6	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^tRC = ^tRC (MIN); CAS latency = 3		I_{DD1}	150	mA	3, 18, 19, 26
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle		I_{DD2}	2	mA	
STANDBY CURRENT: Active Mode; CS# = HIGH; CKE = HIGH; All banks active after ^tRCD met; No accesses in progress		I_{DD3}	60	mA	3, 12, 19, 26
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3		I_{DD4}	180	mA	3, 18, 19, 26
AUTO REFRESH CURRENT: CAS latency = 3; CKE, CS# = HIGH	^tRFC = ^tRFC (MIN)	I_{DD5}	225	mA	3, 12, 18, 19, 26,29
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD6}	2	mA	4

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CAPACITANCE

(Notes following parameter tables.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CKL	C_{I1}	2.5	4	pF	2
Input Capacitance: All other input-only pins	C_{I2}	2.5	4	pF	2
Input/Output Capacitance: DQs	C_{IO}	4	6.5	pF	2

AC ELECTRICAL CHARACTERISTICS

Notes: 5, 6, 8, 9, 11 (Notes following parameter tables.)

AC CHARACTERISTICS			-6			
PARAMETER		SYMBOL	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	^tAC		5.5	ns	
Address hold time		^tAH	1		ns	
Address setup time		^tAS	1.5		ns	
CLK high-level width		^tCH	2.5		ns	
CLK low-level width		^tCL	2.5		ns	
Clock cycle time	CL = 3	^tCK	6		ns	23
CKE hold time		^tCKH	1		ns	
CKE setup time		^tCKS	1.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		ns	
Data-in hold time		^tDH	1		ns	
Data-in setup time		^tDS	1.5		ns	
Data-out high-impedance time	CL = 3	^tHZ		5.5	ns	10
Data-out low-impedance time		^tLZ	1		ns	
Data-out hold time		^tOH	2		ns	
ACTIVE to PRECHARGE command		^tRAS	42	120,000	ns	
ACTIVE to ACTIVE command period		^tRC	60		ns	
AUTO REFRESH period		^tRFC	60		ns	
ACTIVE to READ or WRITE delay		^tRCD	18		ns	
Refresh period (4,096 cycles)		^tREF		64	ms	
PRECHARGE command period		^tRP	18		ns	
ACTIVE bank A to ACTIVE bank B command		^tRRD	12		ns	25
Transition time		^tT	0.3	1.2	ns	7
WRITE recovery time		^tWR	1 + 6ns		^tCK	24
			12		ns	
Exit SELF REFRESH to ACTIVE command		^tXSR	70		ns	20

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AC FUNCTIONAL CHARACTERISTICS

Notes: 5, 6, 7, 8, 9, 11 (0°C ≤ T_A ≤ +70°C) (Notes following parameter tables.)

PARAMETER		SYMBOL	-6	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^tCCD	1	^tCK	17
CKE to clock disable or power-down entry mode		^tCKED	1	^tCK	14
CKE to clock enable or power-down exit setup mode		^tPED	1	^tCK	14
DQM to input data delay		^tDQD	0	^tCK	17
DQM to data mask during WRITEs		^tDQM	0	^tCK	17
DQM to data high-impedance during READs		^tDQZ	2	^tCK	17
WRITE command to input data delay		^tDWD	0	^tCK	17
Data-in to ACTIVE command	CL = 3	^tDAL	5	^tCK	15, 21
Data-in to PRECHARGE command		^tDPL	2	^tCK	16, 21
Last data-in to burst STOP command		^tBDL	1	^tCK	17
Last data-in to new READ/WRITE command		^tCDL	1	^tCK	17
Last data-in to PRECHARGE command		^tRDL	2	^tCK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^tMRD	2	^tCK	26
Data-out to high-impedance from PRECHARGE command	CL = 3	^tROH	3	^tCK	17

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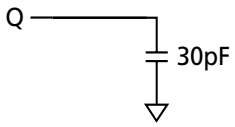
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ +70°C) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = .25 and V_{IH} = 2.75, with timing referenced to 1.5V crossover point.
12. Other input signals are allowed to transition no more than once in any two-clock period and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 166 MHz for -6.
22. V_{IH} overshoot: V_{IH}(MAX) = $V_{DD}Q$ + 1.2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL}(MIN) = -1.2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate.
23. The clock frequency must remain constant during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only.
25. JEDEC and PC100 specify three clocks.
26. ^{t}CK = 6ns for -6.

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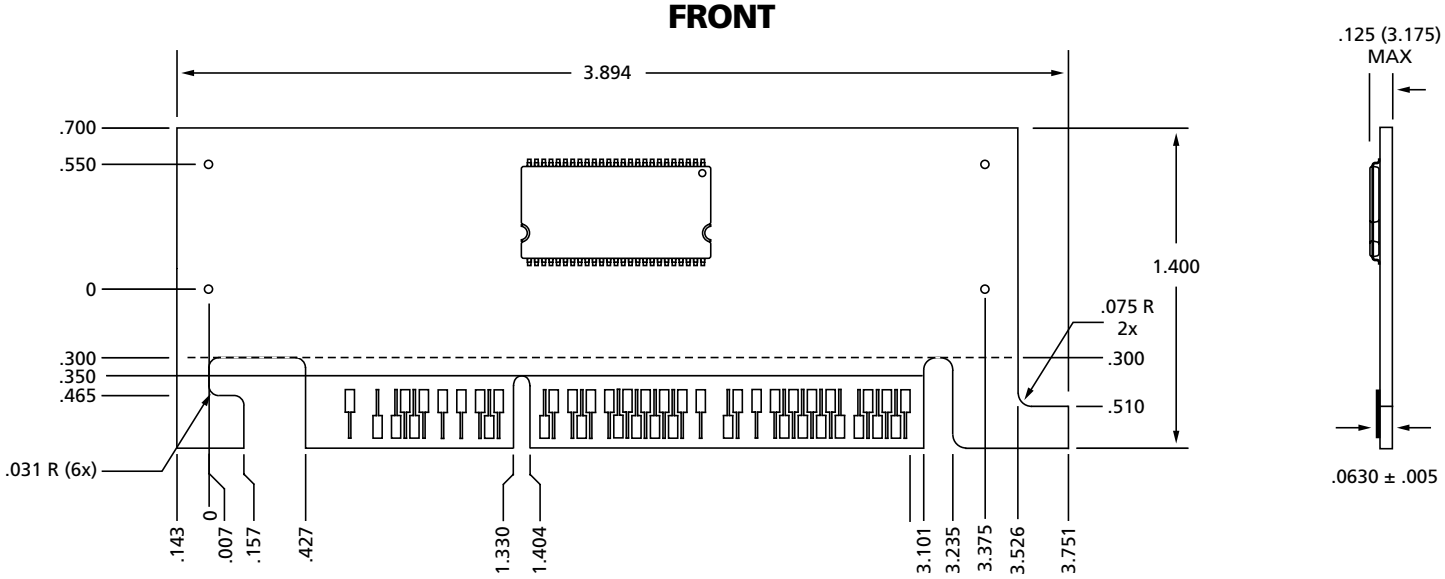
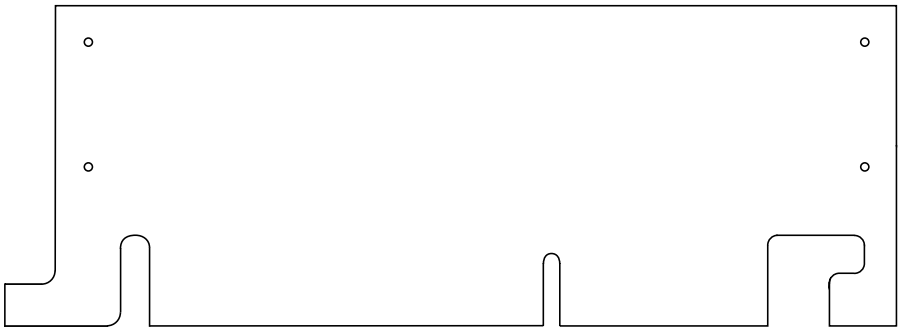
AIMM
(4MB Version)

FRONT



BACK



NOTE: 1. All dimensions in inches (millimeters).

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