

# Adjustable Output Low Voltage Boost Regulator with Detect

## GENERAL DESCRIPTION

The ML4961 is a boost regulator designed for DC to DC conversion in 1 to 3 cell battery powered systems. The combination of BiCMOS process technology, internal synchronous rectification, variable frequency operation, and low supply current make the ML4961 ideal for 1 cell applications. The ML4961 is capable of start-up with input voltages as low as 1V, and the output voltage can be set anywhere between 2.5V and 6V by an external resistor divider connected to the SENSE pin.

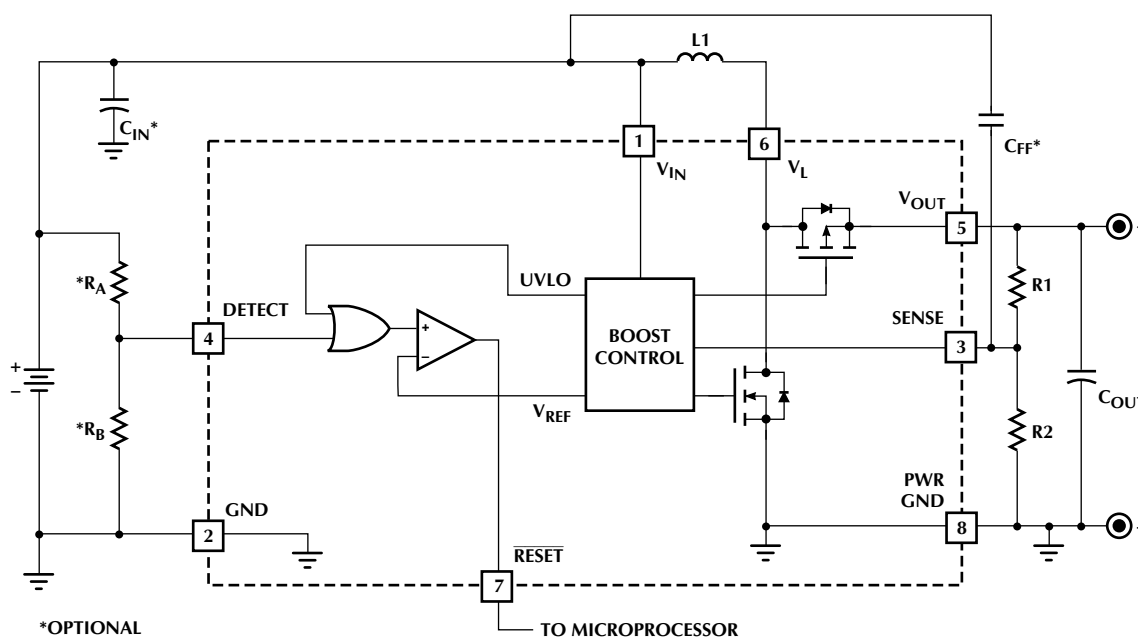
An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4961 requires a minimum number of external components to build a very small adjustable regulator circuit capable of achieving conversion efficiencies in excess of 90%.

The circuit also contains a  $\overline{\text{RESET}}$  output which goes low when the IC can no longer function due to low input voltage, or when the DETECT input drops below 200mV.

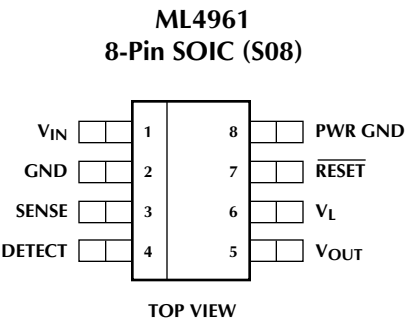
## FEATURES

- Guaranteed full load start-up and operation at 1V input
- Pulse Frequency Modulation and Internal Synchronous Rectification for high efficiency
- Minimum external components
- Low ON resistance internal switching FETs
- Micropower operation
- Adjustable output voltage (2.5V to 6V)

### BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

| PIN NO. | NAME            | FUNCTION   | PIN NO. | NAME             | FUNCTION  |
|---------|-----------------|--|---------|------------------|---|
| 1       | V <sub>IN</sub> | Battery input voltage  | 5       | V <sub>OUT</sub> | Boost regulator output  |
| 2       | GND             | Analog signal ground   | 6       | V <sub>L</sub>   | Boost inductor connection   |
| 3       | SENSE           | Programming pin for setting the output voltage                           | 7       | RESET            | Output goes low when regulation cannot be achieved, or when DETECT goes below 200mV |
| 4       | DETECT          | Pulling this pin below V <sub>REF</sub> , causes the RESET pin to go low | 8       | PWR GND          | Return for the NMOS output transistor   |

## ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

|  |                |
|--|----------------|
| Voltage on any pin .....                   | 7V             |
| Peak Switch Current, $I_{(PEAK)}$ .....    | 2A             |
| Average Switch Current, $I_{(AVG)}$ .....  | 500mA          |
| Junction Temperature .....                 | 150°C          |
| Storage Temperature Range .....            | -65°C to 150°C |
| Lead Temperature (Soldering 10 sec.) ..... | 260°C          |
| Thermal Resistance ( $\theta_{JA}$ ) ..... | 160°C/W        |

## OPERATING CONDITIONS

Temperature Range

|                |               |
|----------------|---------------|
| ML4961CS ..... | 0°C to 70°C   |
| ML4961ES ..... | -20°C to 70°C |
| ML4961IS ..... | -40°C to 85°C |

$V_{IN}$  Operating Range

|                          |                          |
|--------------------------|--------------------------|
| ML4961CS .....           | 1.0V to $V_{OUT} - 0.2V$ |
| ML4961ES, ML4961IS ..... | 1.1V to $V_{OUT} - 0.2V$ |

$V_{OUT}$  Operating Range .....

|              |
|--------------|
| 2.5V to 6.0V |
|--------------|

## ELECTRICAL CHARACTERISTICS

Unless otherwise specified,  $V_{IN}$  = Operating Voltage Range,  $T_A$  = Operating Temperature Range (Note 1)

| PARAMETER  | CONDITIONS  |            | MIN                    | TYP. | MAX  | UNITS |
|--|---|------------|------------------------|------|------|-------|
| Supply   |   |            |                        |      |      |       |
| V <sub>IN</sub> Current                                  | V <sub>IN</sub> = V <sub>OUT</sub> – 0.2V                       |            |                        | 45   | 55   | μA    |
| V <sub>OUT</sub> Quiescent Current                       |   |            |                        | 3    | 5    | μA    |
| V <sub>L</sub> Quiescent Current                         |   |            |                        |      | 1    | μA    |
| PFM Regulator  |   |            |                        |      |      |       |
| Pulse Width (T <sub>ON</sub> )                           | V <sub>IN</sub> = 2.4V  | C/E Suffix | 9                      | 10   | 11   | μs    |
|  |   | I Suffix   | 8.5                    | 10   | 11.5 | μs    |
| SENSE Comparator Threshold Voltage (V <sub>SENSE</sub> ) |   |            | 194                    | 200  | 206  | mV    |
| Load Regulation  | See Figure 1<br>V <sub>IN</sub> = 1.2V, I <sub>OUT</sub> ≤ 25mA |            | 4.85                   | 5.0  | 5.15 | V     |
|  | V <sub>IN</sub> = 2.4V, I <sub>OUT</sub> ≤ 135mA                |            | 4.85                   | 5.0  | 5.15 | V     |
| Undervoltage Lockout Threshold                           |   | C/E Suffix |                        | 0.85 | 0.95 | V     |
|  |   | I Suffix   |                        | 0.95 | 1.05 | V     |
| RESET Comparator   |   |            |                        |      |      |       |
| DETECT Threshold   |   |            | 190                    | 200  | 210  | mV    |
| DETECT Bias Current                                      |   |            | –100                   |      | 100  | nA    |
| RESET Output High Voltage (V <sub>OH</sub> )             | I <sub>OH</sub> = –100μA  |            | V <sub>OUT</sub> – 0.2 |      |      | V     |
| RESET Output Low Voltage (V <sub>OL</sub> )              | I <sub>OL</sub> = 100μA   |            |                        |      | 0.2  | V     |

**Note 1:** Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

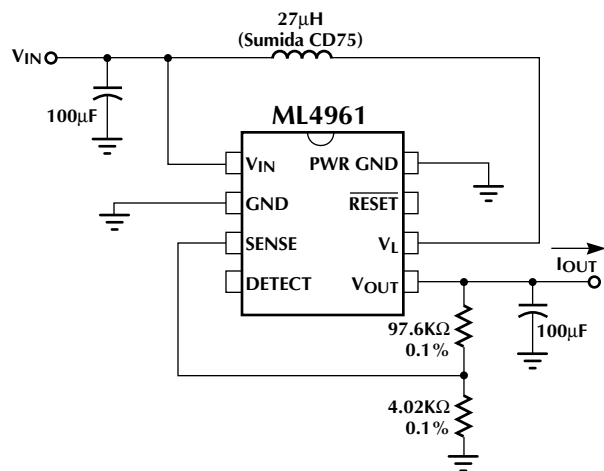


Figure 1. PFM Regulator Block Diagram.

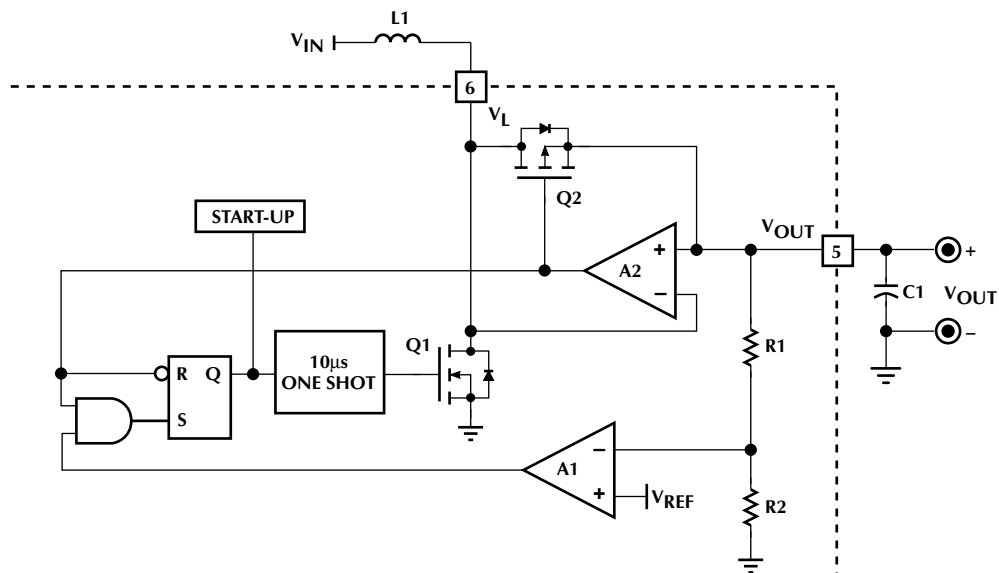


Figure 2. PFM Regulator Block Diagram.

## FUNCTIONAL DESCRIPTION

The ML4961 combines Pulse Frequency Modulation (PFM) and synchronous rectification to create a boost converter that is both highly efficient and simple to use. A PFM regulator charges a single inductor for a fixed period of time and then completely discharges before another cycle begins, simplifying the design by eliminating the need for conventional current limiting circuitry. Synchronous rectification is accomplished by replacing an external Schottky diode with an on-chip PMOS device, reducing switching losses and external component count.

### REGULATOR OPERATION

A block diagram of the boost converter is shown in Figure 2. The circuit remains idle when  $V_{OUT}$  is at or above the desired output voltage, drawing  $45\mu A$  from  $V_{IN}$ , and  $8\mu A$  from  $V_{OUT}$  through the feedback resistors R1 and R2. When  $V_{OUT}$  drops below the desired output level, the output of amplifier A1 goes high, signaling the regulator to deliver charge to the output. Since the output of amplifier A2 is normally high, the flip-flop captures the A1 set signal and creates a pulse at the gate of the NMOS transistor Q1. The NMOS transistor will charge the inductor L1 for  $10\mu s$ , resulting in a peak current given by:

$$I_{L(PEAK)} = \frac{T_{ON} \times V_{IN}}{L1} \approx \frac{10\mu s \times V_{IN}}{L1} \quad (1)$$

For reliable operation, L1 should be chosen so that  $I_{L(PEAK)}$  does not exceed 2A.

When the one-shot times out, the NMOS FET releases the  $V_L$  pin, allowing the inductor to fly-back and momentarily charge the output through the body diode of PMOS transistor Q2. But, as the voltage across the PMOS transistor changes polarity, its gate will be driven low by the current sense amplifier A2, causing Q2 to short out its body diode. The inductor then discharges into the load through Q2. The output of A2 also serves to reset the flip-flop and one-shot in preparation for the next charging cycle. A2 releases the gate of Q2 when its current falls to zero. If  $V_{OUT}$  is still low, the flip-flop will immediately initiate another pulse. The output capacitor (C1) filters the inductor current, limiting output voltage ripple. Inductor current and one-shot waveforms are shown in Figure 3.

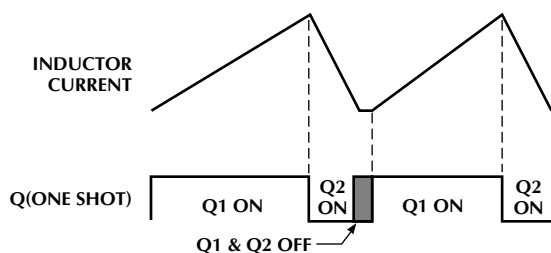


Figure 3. PFM Inductor Current Waveforms and Timing.

### RESET COMPARATOR

An additional comparator is provided to detect low  $V_{IN}$ , or any other error condition that is important to the user. The inverting input of the comparator is internally connected to  $V_{REF}$ , while the non-inverting input is provided externally at the DETECT pin. The output of the comparator is the RESET pin, which swings from  $V_{OUT}$  to GND when an error is detected.

## DESIGN CONSIDERATIONS

### INDUCTOR

Selecting the proper inductor for a specific application usually involves a trade-off between efficiency and maximum output current. Choosing too high a value will keep the regulator from delivering the required output current under worst case conditions. Choosing too low a value causes efficiency to suffer. It is necessary to know the maximum required output current and the input voltage range to select the proper inductor value. The maximum inductor value can be estimated using the following formula:

$$L_{MAX} = \frac{V_{IN(MIN)}^2 \times T_{ON(MIN)} \times \eta}{2 \times V_{OUT} \times I_{OUT(MAX)}} \quad (2)$$

where  $\eta$  is the efficiency, typically between 0.8 and 0.9. Note that this is the value of inductance that just barely delivers the required output current under worst case conditions. A lower value may be required to cover inductor tolerance, the effect of lower peak inductor currents caused by resistive losses, and minimum dead time between pulses.

Another method of determining the appropriate inductor value is to make an estimate based on the typical performance curves given in Figures 4 and 5. Figure 4 shows maximum output current as a function of input voltage for several inductor values. These are typical performance curves and leave no margin for inductance and ON-time variations. To accommodate worst case conditions, it is necessary to derate these curves by at least 10% in addition to inductor tolerance. Interpolation between the different curves will give a reasonable starting point for an inductor value.

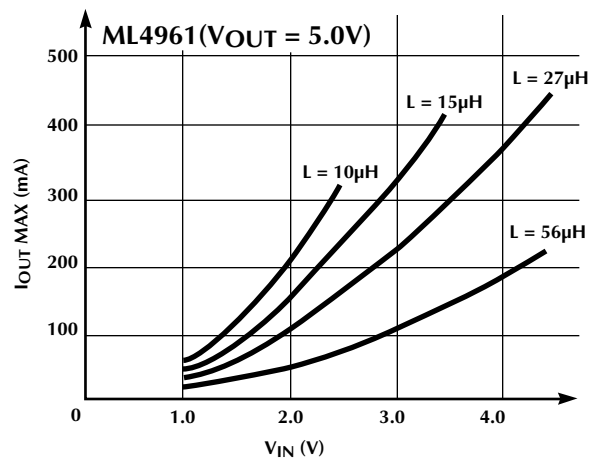
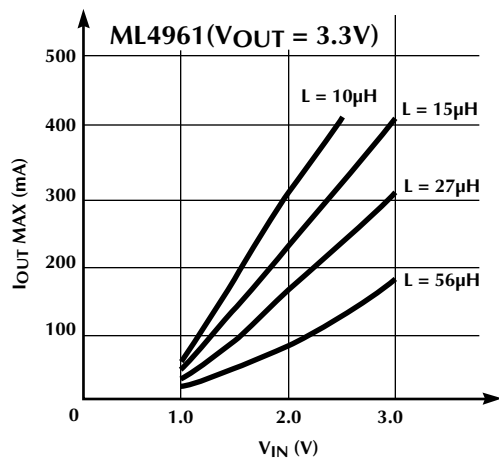


Figure 4. Output Current vs. Input Voltage.

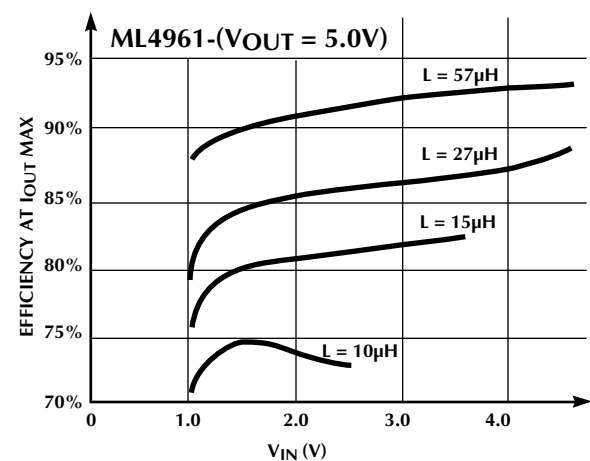
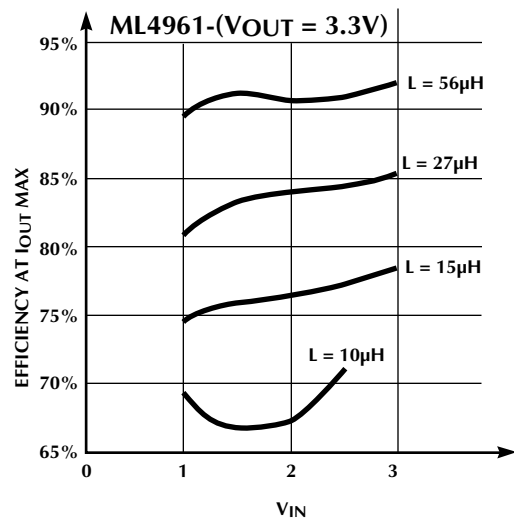


Figure 5. Typical Efficiency as a Function of  $V_{IN}$ .

Figure 5 shows efficiency under the conditions used to create Figure 4. It can be seen that efficiency is mostly independent of input voltage and is closely related to inductor value. This illustrates the need to keep the inductor value as high as possible to attain peak system efficiency. As the inductor value goes down to  $10\mu\text{H}$ , the efficiency drops to between 70% and 75%. With  $56\mu\text{H}$ , the efficiency exceeds 90% and there is little room for improvement. At values greater than  $100\mu\text{H}$ , the operation of the synchronous rectifier becomes unreliable because the inductor current is so small that it is difficult for the control circuitry to detect.

After the appropriate inductor value is chosen, it is necessary to find the minimum inductor current rating required. Peak inductor current is determined from the following formula:

$$I_{L(\text{PEAK})} = \frac{T_{\text{ON}(\text{MAX})} \times V_{\text{IN}(\text{MAX})}{L_{\text{MIN}}} \quad (3)$$

When comparing various inductors, it is important to keep in mind that suppliers use different criteria to determine their ratings. Many use a conservative current level, where inductance has dropped to 90% of its normal level. In any case, it is a good idea to try inductors of various current ratings with the ML4961 to determine which inductor is the best choice. Check efficiency and maximum output current, and if a current probe is available, look at the inductor current to see if it looks like the waveform shown in Figure 3. For additional information, see Application Note 29.

Suitable inductors can be purchased from the following suppliers:

|             |                |
|-------------|----------------|
| Coilcraft   | (708) 639-6400 |
| Coiltronics | (407) 241-7876 |
| Dale        | (605) 665-9301 |
| Sumida      | (708) 956-0666 |

## OUTPUT CAPACITOR

The choice of output capacitor is also important, as it controls the output ripple and optimizes the efficiency of the circuit. Output ripple is influenced by three capacitor parameters: capacitance, ESR, and ESL. The contribution due to capacitance can be determined by looking at the change in capacitor voltage required to store the energy delivered by the inductor in a single charge-discharge cycle, as determined by the following formula:

$$\Delta V_{OUT} = \frac{T_{ON}^2 \times V_{IN}^2}{2 \times L \times C \times (V_{OUT} - V_{IN})} \quad (4)$$

For a 2.4V input, and 5V output, a 27μH inductor, and a 47μF capacitor, the expected output ripple due to capacitor value is 87mV.

Capacitor Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), also contribute to the output ripple due to the inductor discharge current waveform. Just after the NMOS transistor turns off, the output current ramps quickly to match the peak inductor current. This fast change in current through the output capacitor's ESL causes a high frequency (5ns) spike that can be over 1V in magnitude. After the ESL spike settles, the output voltage still has a ripple component equal to the inductor discharge current times the ESR. This component will have a sawtooth shape and a peak value equal to the peak inductor current times the ESR. ESR also has a negative effect on efficiency by contributing I-squared R losses during the discharge cycle.

An output capacitor with a capacitance of 100μF, an ESR of less than 0.1Ω, and an ESL of less than 5nH is a good general purpose choice. Tantalum capacitors which meet these requirements can be obtained from the following suppliers:

AVX (207) 282-5111

Sprague (207) 324-4140

If ESL spikes are causing output noise problems, an EMI filter can be added in series with the output.

## INPUT CAPACITOR

Unless the input source is a very low impedance battery, it will be necessary to decouple the input with a capacitor with a value of between 47μF and 100μF. This provides the benefits of preventing input ripple from affecting the ML4961 control circuitry, and it also improves efficiency by reducing I-squared R losses during the charge and discharge cycles of the inductor. Again, a low ESR capacitor (such as tantalum) is recommended.

## SETTING THE OUTPUT VOLTAGE

The adjustable output can be set to any voltage between 2.5V and 6V by connecting a resistor divider to the SENSE pin as shown in the block diagram. The resistor values  $R_1$  and  $R_2$  can be calculated using the following equation:

$$V_{OUT} = 0.2 \times \frac{(R_1 + R_2)}{R_2} \quad (5)$$

The value of  $R_2$  should be 40kΩ or less to minimize bias current errors.  $R_1$  is then found by rearranging the equation:

$$R_1 = R_2 \times \left( \frac{V_{OUT}}{0.2} - 1 \right) \quad (6)$$

It is important to note that the accuracy of these resistors directly affects the accuracy of the output voltage. The SENSE pin threshold variation is ±3%, and the tolerances of  $R_1$  and  $R_2$  will add to this to determine the total output variation.

In some applications, input noise may cause output ripple to become excessive due to "pulse grouping", where the charge-discharge pulses are not evenly spaced in time. In such cases it may be necessary to add a small 20pF to 100pF ceramic feedforward capacitor ( $C_{FF}$ ) from the  $V_{IN}$  pin to the SENSE pin.

## SETTING THE RESET THRESHOLD

To use the  $\overline{RESET}$  comparator as an input voltage monitor, it is necessary to use an external resistor divider tied to the DETECT pin as shown in the block diagram. The resistor values  $R_A$  and  $R_B$  can be calculated using the following equation:

$$V_{IN(MIN)} = 0.2 \times \frac{(R_A + R_B)}{R_B} \quad (7)$$

The value of  $R_B$  should be 100kΩ or less to minimize bias current errors.  $R_A$  is then found by rearranging the equation:

$$R_A = R_B \times \left( \frac{V_{IN(MIN)}}{0.2} - 1 \right) \quad (8)$$

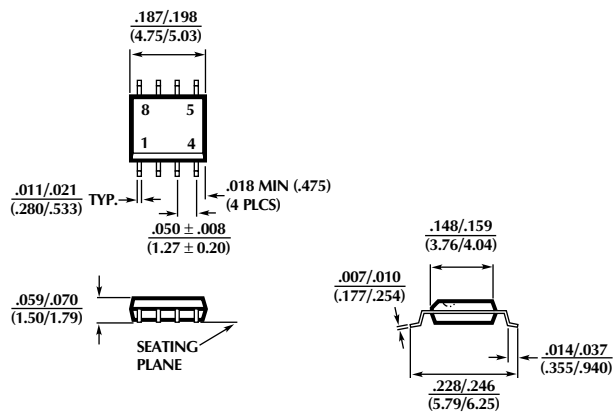
## LAYOUT

Good PC board layout practices will ensure the proper operation of the ML4961. Important layout considerations include:

- Use adequate ground and power traces or planes
- Keep components as close as possible to the ML4961
- Use short trace lengths from the inductor to the  $V_L$  pin and from the output capacitor to the  $V_{OUT}$  pin
- Use a single point ground for the ML4961 ground pins, and the input and output capacitors

## PHYSICAL DIMENSIONS inches (millimeters)

Package: S08  
8-Pin SOIC



## ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE          |
|-------------|-------------------|------------------|
| ML4961CS    | 0°C to 70°C       | 8-Pin SOIC (S08) |
| ML4961ES    | -20°C to 70°C     | 8-Pin SOIC (S08) |
| ML4961IS    | -40°C to 85°C     | 8-Pin SOIC (S08) |

© Micro Linear 1996  **Micro Linear** is a registered trademark of Micro Linear Corporation

Products described in this document may be covered by one or more of the following patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017, 5,559,470. Other patents are pending.

Micro Linear reserves the right to make changes to any product herein to improve reliability, function or design. Micro Linear does not assume any liability arising out of the application or use of any product described herein, neither does it convey any license under its patent right nor the rights of others. The circuits contained in this data sheet are offered as possible applications only. Micro Linear makes no warranties or representations as to whether the illustrated circuits infringe any intellectual property rights of others, and will accept no responsibility or liability for use of any application herein. The customer is urged to consult with appropriate legal counsel before deciding on a particular application.

2092 Concourse Drive  
San Jose, CA 95131  
Tel: 408/433-5200  
Fax: 408/432-0295