

ADVANCE DATASHEET

RapidChip™ *Xtreme* Platform ASIC Family

July 2004

This document is advance. As such, it describes a product under development. This information is intended to help you evaluate the product. LSI Logic reserves the right to change or discontinue this proposed product without notice.

This document contains proprietary information of LSI Logic Corporation. The information contained herein is not to be used by or disclosed to third parties without the express written permission of an officer of LSI Logic Corporation.

Document DB08-000245-00, July 2004

This document describes the LSI Logic Corporation RapidChip Xtreme platform ASIC family and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

LSI Logic Corporation reserves the right to make changes to any products herein at any time without notice. LSI Logic does not assume any responsibility or liability arising out of the application or use of any product described herein, except as expressly agreed to in writing by LSI Logic; nor does the purchase or use of a product from LSI Logic convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual property rights of LSI Logic or third parties.

Copyright © 2004 by LSI Logic Corporation. All rights reserved.

TRADEMARK ACKNOWLEDGMENT

LSI Logic, the LSI Logic logo design, CoreWare, G12, Gfix, GigaBlaze, HyperPHY, Pad on I/O, RapidChip, RapidReady, RapidWorx, System CoreWare, and ZSP are trademarks or registered trademarks of LSI Logic Corporation. ARM is a registered trademark of ARM Ltd., used under license. MIPS and MIPS32 are trademarks or registered trademarks of MIPS Technologies, Inc. All other brand and product names may be trademarks of their respective companies.

EH

To receive product literature, visit us at

<http://www.lsillogic.com>

For news and updates about RapidChip technology products, visit

www.rapidchip.com

For a current list of our distributors, sales offices, and design resource centers, visit

<http://www.lsillogic.com/contacts/index.html>

Preface

This document is an overview of the RapidChip™ technology and a detailed description of the RapidChip Xtreme platform ASIC family, which is based on the Gflx™ process technology. These descriptions include functional block descriptions, configurability, testing, packaging data, and specifications.

Audience

This document assumes you are familiar with custom logic design, either with ASICs or FPGAs, and related support tools. The people who benefit from this book are:

- Engineers and managers who are evaluating the RapidChip Xtreme platform ASICs for possible use in a system
 - Engineers who are designing the RapidChip Xtreme platform ASICs into a system
-

Organization

This document has the following sections:

- [Section 1, “RapidChip™ Technology Overview,”](#) provides a high-level description of the RapidChip technology.
- [Section 2, “RapidChip Xtreme Platform ASIC Overview,”](#) is a functional description of the RapidChip Xtreme platform ASIC family.
- [Section 3, “RapidChip Xtreme Platform ASIC Details,”](#) provides detailed information on each RapidChip Xtreme platform ASIC family member.
- [Section 4, “Specifications,”](#) provides the electrical specifications for the RapidChip Xtreme platform ASIC family.

- [Section 5, “Packaging,”](#) is an overview of the packaging of the RapidChip Xtreme platform ASIC family.
 - [Appendix A, “Packaging Details,”](#) provides detailed information about the packaging and the pinouts of the RapidChip Xtreme platform ASIC family.
-

Related Publications

RapidChip™ Memory Overview, document number DB06-000471-01

ARM966EJ-S Technical Reference Manual, ARM Ltd.

MIPS32 4KEc Processor Core Datasheet, MIPS Technologies, Inc.

Preliminary Gfx-r RapidChip Cell Technology Databook, document number DB04-000094-02

Using RapidBuilder to Generate a Clock Factory, Application Note, document number DB06-000470-01.

Conventions Used in This Manual

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

Contents

1	RapidChip™ Technology Overview	1
1.1	RapidChip Platform ASICs	2
1.2	RapidChip Platform ASIC Building Blocks	2
1.3	Packaging	5
1.4	Library Elements	5
1.5	RapidWorx Design Methodology	6
2	RapidChip Xtreme Platform ASIC Overview	12
2.1	Feature Summary	14
2.2	Naming Conventions	15
2.3	Family Members	15
2.4	Memory Implementation	16
2.5	Configurable I/Os	21
2.6	Clock Networks and PLLs	22
2.7	High-Speed SERDES Cores	27
2.8	Double-Data-Rate (DDR) PHY Support	38
2.9	Embedded Microprocessor Support	41
3	RapidChip Xtreme Platform ASIC Details	44
3.1	RC11XT404	44
3.2	RC11XT416	49
3.3	RC11XT432	53
3.4	RC11XT531	58
4	Specifications	64
4.1	VDD Terminology	65
4.2	Absolute Maximum Ratings	66
4.3	Recommended Operating Conditions	67
4.4	SSTL2 Buffer	67
4.5	HSTL Buffers	72
4.6	2.5 V LVDS Buffers	77
4.7	3.3 V LVDS Buffers	81
4.8	PECL Buffer	85

4.9	PCI/PCI-X Buffer	86
4.10	2.5 V Controlled Impedance Buffers	90
4.11	3.3 V Controlled Impedance Buffers	93
4.12	1.8 V LVTTL/LVCMOS Buffers	96
4.13	2.5 V LVTTL/LVCMOS Buffers	98
4.14	3.3 V LVTTL/LVCMOS Buffers	101
5	Packaging	105
5.1	Optimized Package Design	105
5.2	Efficient I/O Escape Routing	107
5.3	Thermal Design Considerations	108
5.4	Packages and Pinouts	110

Appendix A

Packaging Details

A.1	BG672 Package and Pinouts	A-1
A.2	FC672 Package and Pinouts	A-4
A.2.1	RC11XT416 in the FC672 Package	A-4
A.2.2	RC11XT432 in the FC672 Package	A-6
A.3	FC896 Package and Pinouts	A-30
A.3.1	RC11XT416 in the FC896 Package	A-31
A.3.2	RC11XT432 in the FC896 Package	A-33
A.3.3	RC11XT531 in the FC896 Package	A-66
A.4	Package Mechanical Drawings	A-97

Figures

1	Typical RapidChip Platform ASIC	3
2	Design Flow	7
3	Product Numbering	15
4	Logic Symbol for 1rw Memory	17
5	Logic Symbol for 1r1w Memory	17
6	Logic Symbol for 2rw Memory	17
7	Tiling Diffused Memory	20
8	Tiling R-Cell Memory	20
9	Combining R-Cell and Diffused Memory	21
10	Simple Clock Network	23
11	Clock Factory	24
12	Clock Factory Element	24
13	PLL Block Diagram	25
14	GigaBlaze Transceiver Core	29
15	GigaBlaze x1 Core	31
16	GigaBlaze x4 Core	31
17	Simplified HyperPHY Transmitter Block Diagram	34
18	Simplified HyperPHY Receiver Block Diagram	35
19	SFI-4 Transmit Block Diagram	37
20	SFI-4 Receive Block Diagram	38
21	DDR PHY Simplified Block Diagram	40
22	ARM966EJ-S Processor and System CoreWare IP with 4-Port DDR Controller	42
23	Logic Diagram for the RC11XT404	46
24	Logic Diagram for the RC11XT416	50
25	Logic Diagram for the RC11XT432	55
26	Logic Diagram for the RC11XT531	60
27	SSTL2 Buffer Block Diagram	68
28	SSTL Driver Timing Waveforms	71
29	SSTL2 Receiver Timing Waveforms	72
30	HSTL Buffer Block Diagram	73
31	Ring Back Switching Diagram	75
32	HSTL Receiver Timing Waveforms	76
33	HSTL Driver Timing Waveforms	77
34	2.5 V LVDS Driver Block Diagram	78
35	2.5 V LVDS Receiver Block Diagram	78

36	3.3 V LVDS Driver Block Diagram	82
37	3.3 V LVDS Receiver Block Diagram	82
38	PECL Buffer Block Diagram	85
39	PCI/PCI-X Buffer Block Diagram	87
40	2.5 V Controlled Impedance Block Diagram	91
41	2.5 V Controlled Impedance Buffer Timing $a > i_o$	93
42	2.5 V Controlled Impedance Buffer Timing $i_o > z_i$	93
43	3.3 V Controlled Impedance Buffer Block Diagram	94
44	3.3 V Controlled Impedance Buffer Timing $a > i_o$	96
45	3.3 V Controlled Impedance Buffer Timing $i_o > z_i$	96
46	1.8 V LVTTL/LVCMOS Buffer Block Diagram	97
47	2.5 V LVTTL/LVCMOS Buffer Block Diagram	100
48	3.3 V LVTTL/LVCMOS Buffer Block Diagram	103
49	Cross Section of EPBGA-T Package	108
50	Cross Section of FCBGA Package	109
51	RC11XT404 in the BG672 Package Diagram	112
52	RC11XT416 in the FC672 Package Diagram	114
53	RC11XT432 in the FC672 Package Diagram	116
54	RC11XT416 in the FC896 Package Diagram	119
55	RC11XT432 in the FC896 Package Diagram	121
56	RC11XT531 in the FC896 Package Diagram	124
A.1	RC11XT404 in the BG672 Package Diagram	A-2
A.2	RC11XT416 in the FC672 Package Diagram	A-5
A.3	RC11XT432 in the FC672 Package Diagram	A-7
A.4	RC11XT416 in the FC896 Package Diagram	A-32
A.5	RC11XT432 in the FC896 Package Diagram	A-34
A.6	RC11XT531 in the FC896 Package Diagram	A-67
A.7	672-Ball Count EPBGA-T (5E) Mechanical Drawing	A-98
A.8	672-Ball Count FCBGA Mechanical Drawing	A-99
A.9	896-Ball Count FCBGA (9P) Mechanical Drawing	A-100

Tables

1	CoreWare IP Characteristics	4
2	Design Milestone Acronyms	7
3	RapidWorx Design Kit	8
4	RapidChip Xtreme Platform ASIC Family Summary	16
5	Diffused Memory Configurations	18
6	R-Cell Memory	19
7	R-Cell Memory Dimensions	19
8	I/O Driver Types	22
9	GigaBlaze Supported Communications Standards	28
10	HyperPHY Supported Communications Standards	33
11	Framer Supported Communications Standards	36
12	Supported DDR Memories	41
13	RC11XT404 Diffused Memory Banks	45
14	RC11XT416 Diffused Memory Banks	49
15	RC11XT432 Diffused Memory Banks	54
16	RC11XT531 Diffused Memory Banks	59
17	Cross Reference of VDD Terms for RapidChip Xtreme Family	65
18	Absolute Maximum Ratings	66
19	Recommended Operating Conditions	67
20	SSTL2 Buffer DC Characteristics	69
21	SSTL2 Buffer AC Characteristics	69
22	SSTL2 Driver Timing Characteristics	70
23	SSTL2 Receiver Timing Characteristics	71
24	HSTL Buffer AC/DC Electrical Characteristics	74
25	HSTL Driver Timing Characteristics	75
26	HSTL Receiver Timing Characteristics	76
27	2.5 V LVDS Drivers and Receivers	77
28	2.5 V LVDS Driver DC Characteristics	79
29	2.5 V LVDS Receiver DC Characteristics	79
30	2.5 V LVDS Driver AC Characteristics	79
31	2.5 V LVDS Receiver AC Characteristics	80
32	2.5 V LVDS Driver Timing Characteristics	80
33	2.5 V LVDS Receiver Timing Characteristics	81
34	3.3 V LVDS Drivers and Receivers	81
35	3.3 V LVDS Driver DC Characteristics	83

36	3.3 V LVDS Receiver DC Characteristics	83
37	3.3 V LVDS Driver AC Characteristics	83
38	3.3 V LVDS Receiver AC Characteristics	84
39	3.3 V LVDS Driver Timing Characteristics	84
40	3.3 V LVDS Receiver Timing Characteristics	84
41	PECL Buffer DC Electrical Characteristics	86
42	PECL Buffer Propagation Delay	86
43	PCI/PCI-X Buffer DC Characteristics	88
44	PCI-X 66/100/133 MHz AC Characteristics	88
45	PCI 33/66 MHz AC Characteristics	89
46	PCI-X 66/100/133 MHz Slew Rate	89
47	PCI 33/66 MHz Slew Rate	90
48	PCI-X 66/100/133 MHz Delay Characteristics	90
49	2.5 V Controlled Impedance Buffer DC Characteristics	92
50	2.5 V Controlled Impedance Buffer AC Characteristics	92
51	3.3 V Controlled Impedance Buffer DC Characteristics	95
52	3.3 V Controlled Impedance Buffer AC Characteristics	95
53	1.8 V LVTTL/LVCMOS Buffer DC Characteristics	98
54	1.8 V LVTTL/LVCMOS Buffer AC Characteristics	98
55	2.5 V LVTTL/LVCMOS Buffer DC Characteristics	101
56	2.5 V LVTTL/LVCMOS Buffer AC Characteristics	101
57	3.3 V LVTTL/LVCMOS Buffer DC Characteristics	104
58	3.3 V LVTTL/LVCMOS Buffer AC Characteristics	104
59	Xtreme Platform ASIC Package Thermal Characteristics	109
60	BG672 Package I/O Summary (RC11XT404)	113
61	FC672 Package I/O Summary (RC11XT416)	115
62	FC672 Package I/O Summary (RC11XT432)	117
63	FC896 Package I/O Summary (RC11XT416)	120
64	FC896 Package I/O Summary (RC11XT432)	122
65	FC896 Package I/O Summary (RC11XT531)	125
A.1	BG672 Package Power Connections (RC11XT404)	A-3
A.2	BG672 Package I/O Assignments (RC11XT404)	A-3
A.3	FC672 Package Power Connections (RC11XT416)	A-6
A.4	FC672 Package I/O Assignments (RC11XT416)	A-6
A.5	FC672 Package Power Connections (RC11XT432)	A-8
A.6	FC672 Package I/O Assignments (RC11XT432)	A-10
A.7	FC896 Package Power Connections (RC11XT416)	A-33
A.8	FC896 Package I/O Assignments (RC11XT416)	A-33

A.9	FC896 Package Power Connections (RC11XT432)	A-35
A.10	FC896 Package I/O Signals (RC11XT432)	A-37
A.11	FC896 Package Power Connections (RC11XT531)	A-68
A.12	FC896 Package I/O Assignments (RC11XT531)	A-70

RapidChip™ Xtreme Platform ASIC Family Advance Datasheet

1 RapidChip™ Technology Overview

The RapidChip Xtreme platform ASIC family belongs to the second generation of RapidChip platform ASICs from LSI Logic. All RapidChip platform ASICs are based on RapidChip technology, which is a fundamentally new way to design custom ICs. This robust platform approach to IC design combines the best attributes of FPGA and cell-based ASIC products.

By combining RapidChip platform ASICs with the RapidWorx™ Design Kit, which consists of design tools, design methodology, and a design library, you can develop packaged, tested, working silicon with complex embedded Intellectual Property (IP) in half the time needed by current methods and at one-quarter your development costs.

The primary objectives of RapidChip technology are:

- Dramatically reduce time-to-market for complex, highly integrated, high-performance custom ICs
- Dramatically reduce engineering costs, EDA tool costs, and tooling costs associated with the development of deep submicron devices
- Deliver a very cost-effective product for use in medium-volume applications

The fundamental approach of RapidChip technology is to customize the metal layers of a partially manufactured semiconductor wafer, containing multiple copies of a predefined RapidChip platform ASIC. The silicon layers of a RapidChip platform ASIC have diffused IP resources that are connected later with user-specific metallization patterns.

Because RapidChip platform ASICs are available as partially manufactured devices, known as slices, lead times for prototypes and

production units are reduced dramatically, and you benefit from lower inventory costs. The broad range of resources available in RapidChip platform ASICs meets the needs of many different systems and applications.

Each slice incorporates diffused memory blocks, PLLs, and IP blocks from the extensive CoreWare® library. In addition each slice has a transistor fabric region and an I/O ring. The transistor fabric region and I/O ring are both user-configurable.

All RapidChip platform ASICs use proven LSI Logic cell-based ASIC technologies. The diffused memories and diffused IP cores included within RapidChip platform ASICs are the same as those used in LSI Logic cell-based ASIC product offerings, giving RapidChip platform ASICs near cell-based ASIC performance, density, and power consumption.

1.1 RapidChip Platform ASICs

There are now three families of RapidChip platform ASICs:

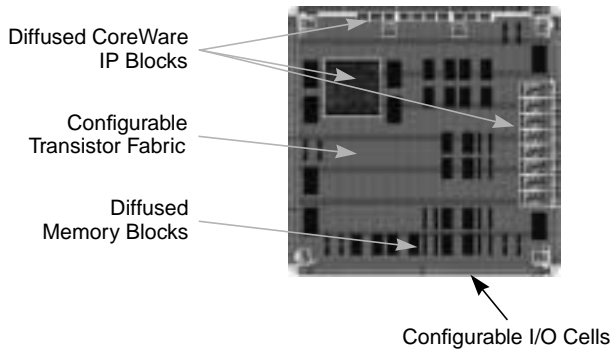
- RapidChip Foundation platform ASICs
- RapidChip Xtreme platform ASICs
- RapidChip Integrator platform ASICs

The Foundation platform ASICs are general-purpose platforms that are manufactured in a 0.18 um process technology, the G12® process. The RapidChip Integrator platform ASIC and the RapidChip Xtreme platform ASIC use second-generation RapidChip technology and are manufactured in a 0.11 um process technology, the Gflx™ process. RapidChip Integrator platform ASICs are suitable for a broad range of custom logic applications in multiple markets. RapidChip Xtreme platform ASICs, which are the subject of this datasheet, are optimized for complex, high-performance applications.

1.2 RapidChip Platform ASIC Building Blocks

This section describes the diffused CoreWare IP blocks, diffused memory blocks, configurable transistor fabric, and configurable I/O cells that make up a typical RapidChip platform ASIC. [Figure 1](#) shows a typical RapidChip platform ASIC with these major elements highlighted.

Figure 1 Typical RapidChip Platform ASIC



1.2.1 Configurable Transistor Fabric

User logic is implemented in the configurable transistor fabric region. An R-Cell is the basic unit within the transistor fabric; it is made up of specially sized “N” and “P” type transistors for maximum flexibility and performance. R-Cells are diffused in a regular pattern throughout the transistor fabric and are architected to implement logic structures and small memory arrays efficiently. Using the metal layers, the R-Cells can be configured to implement the full range of logic functions available in the logic cell library. The library contains over 400 cells that have a range of drive strengths. Transistors within the fabric are activated only when they are part of the implementation of a function used in the design, ensuring the most power-efficient solution.

1.2.2 Diffused Memory Blocks

High-density, high-performance RAM blocks (single-port, two-port, and dual-port) are diffused into each slice, creating a memory space that can be customized to suit a particular application. The RapidWorx Design Kit is used to customize the memory spaces. Using these tools, diffused memory blocks can be combined to create larger memories. Diffused memory blocks also can be combined with small memory blocks (R-Cell Memory) that are constructed in the transistor fabric region, allowing you to construct memory arrays that vary in width and depth. This architecture allows the most efficient use of resources without sacrificing diffused RAM capacity.

1.2.3 CoreWare IP Blocks

CoreWare Intellectual Property (IP) blocks are delivered in four distinct forms: Diffused IP, Hard IP, Firm IP, and Soft IP.

- Diffused IP, which can be standard cell, mixed signal, or full custom logic, is placed, routed, and verified in the diffused region of a RapidChip platform ASIC. Diffused IP, which is not relocatable, has the same high-performance specifications as a cell-based ASIC. SERDES transceivers, PLLs, and ARM® CPUs are examples of diffused IP that are designed into RapidChip platform ASICs at slice creation.
- Hard IP is placed and routed in the transistor fabric region (R-Cells) of a slice and can be relocated as a single block. Predefined layouts enable maximum performance.
- Firm IP is placed but not routed in the transistor fabric region (R-Cells) of a slice, which provides greater flexibility where maximum performance is not a requirement. Firm IP is delivered as a netlist with timing constraints. Routing of Firm IP is completed during chip-level routing.
- Soft IP is implemented in the transistor fabric region (R-Cells) of the slice. Soft IP is delivered as RTL. Therefore, Soft IP is not placed or routed. Soft IP provides maximum flexibility because it is synthesized during the physical synthesis step using the RapidWorx Design Kit.

[Table 1](#) summarizes the characteristics of the CoreWare IP blocks.

Table 1 CoreWare IP Characteristics

IP Type	Region	Relocatable	Placed	Routed	Deliverables
Diffused	Diffused Region	No	Yes	Yes	Netlist
Hard	Transistor Fabric	Yes (Limited)	Yes	Yes	Netlist
Firm	Transistor Fabric	Yes	Yes	No	Netlist with timing constraints
Soft	Transistor Fabric	Yes	No	No	RTL with timing constraints

1.2.4 I/Os

High-performance I/O is a key feature of RapidChip platform ASICs. Because you require I/O flexibility, all slices have configurable I/Os that

can be configured to meet the most commonly used signalling standards, such as LVTTTL, LVDS, HSTL, and SSTL.

Using RapidBuilder, a tool in the RapidWorx Design Kit, you can select the I/O type, I/O direction, voltage level, drive strength, and pin locations. Then, RapidBuilder creates customized metal patterns that connect uncommitted transistor networks in a slice's I/O region to implement all required buffer types.

In combination with packages optimized for the I/O capabilities of the RapidChip platform ASICs, LSI Logic configurable buffer technology provides extremely flexible I/O assignments that are simultaneous switching output (SSO) hazard-free.

Where required to meet interface standards, dedicated I/Os are diffused into the slice. For example, slices that include a GigaBlaze® SERDES transceiver have the dedicated I/Os required to support high-speed communications protocols, such as Fibre Channel, InfiniBand, 1G Ethernet, and 10G Ethernet, which can operate at up to 4.25 Gbits/s per SERDES channel.

1.3 Packaging

RapidChip platform ASICs have individually optimized packages to ensure all electrical and mechanical design requirements are met under worst-case conditions. Co-design methodology between package engineers, circuit designers, and process development engineers ensures all aspects of silicon and package are designed together. The result of this co-development environment is robust, predictable performance. RapidChip Xtreme platform ASIC packaging solutions have been specially designed to support the high-speed SERDES interfaces available on these slices.

1.4 Library Elements

The principal goal of RapidChip technology is to ensure a repeatable and predictable design flow that accelerates the design process and avoids the common pitfalls of deep submicron design. In common with cell-based ASIC design practices, design source files for a RapidChip platform ASIC are captured in RTL form. The RTL is synthesized to a library of cells using EDA tools to create a netlist that conforms to timing and certain other constraints. The RapidChip platform ASIC library of

logic cells extends to over 400 members, covering simple and complex gates, multiplexers, and flip-flops.

The design rules of each RapidChip platform ASIC family set limits on the maximum clock speed for customer logic. Below this frequency limit, synthesis tools typically can implement up to 25 levels of logic between successive clock edges. Faster operation is possible, for example, with Hard IP block layouts. However, for your logic, this approach comes at the expense of less predictable design time (because the block requires optimization and a dedicated layout) and increased NRE.

The goal of custom IC design is to create specific circuitry that meets unique system requirements. However, many functions within a custom IC, such as memory interfaces, link layers, controllers, and embedded microprocessors, can be standardized to ensure hardware/software interoperability within a system. Such functions are available in the CoreWare library, which consists of proven, complex IP functions that meet specific LSI Logic standards for design integrity, ease of use, reusability, supportability, quality, and deliverables, including supporting infrastructure.

LSI Logic also offers System CoreWare IP building blocks, which comprise two or more CoreWare IP blocks that have been pre-integrated and pre-verified to create an IP function at a higher level of abstraction, to meet the needs of many target applications. System CoreWare IP building blocks give you a substantial head start in designing a custom IC by eliminating the burden of designing and integrating multiple cores that might not differentiate a system, but are essential to its operation.

CoreWare IP blocks and System CoreWare IP have RapidReady™ certification, which means that they are compatible with RapidWorx design methodology and design tools and are ready to be integrated into RapidChip platform ASICs.

1.5 RapidWorx Design Methodology

All LSI Logic RapidChip platform ASIC designs follow the 6-step process shown in [Figure 2](#). This process requires regular controls and checks of the design by the joint design teams. Each step in the flow has a checklist associated with it to guide design teams through to successful silicon prototypes.

Figure 2 Design Flow

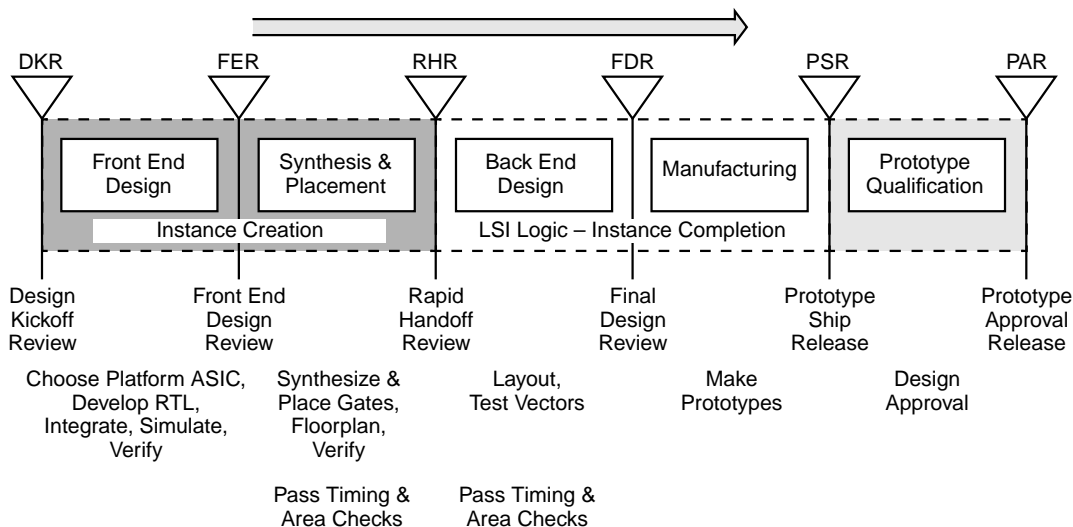


Table 2 explains the acronyms used in Figure 2.

Table 2 Design Milestone Acronyms

Acronym	Milestone	Responsibility	Description
DKR	Design Kickoff Review	Design Team / LSI Logic	Design specification and SOW review, training, RTL coding and synthesis guidelines provided.
FER	Front-End Design Review	Design Team / LSI Logic	RTL analysis and sign off
RHR	Rapid Handoff Review	Design Team / LSI Logic	
FDR	Final Design Review	Design Team / LSI Logic	Sign off of design by both parties
PSR	Prototype Ship Release	LSI Logic	Completion of manufacturing, ship prototypes.
PAR	Prototype Approval Release	Design Team	Prototype approval.

You are responsible for the initial steps in the design flow, shown in [Figure 2](#) as Instance Creation. In these steps, you use the RapidWorx Design Kit to choose the slice, and design, simulate, and verify RTL for your application. LSI Logic provides you with coding and synthesis guidelines to ensure that the remainder of the flow progresses smoothly.

The RapidWorx Design Kit is a streamlined set of highly integrated tools that you use in this process. It eliminates the barriers to designing high-performance, custom silicon through the combination of a streamlined design flow, rule-based methodology, and automated, correct-by-construction tools. The cost of the complete RapidWorx Design Kit tool suite is far below that of typical cell-based tool suites. [Section 1.5.1, “RapidWorx Design Kit,”](#) describes the design kit in more detail.

1.5.1 RapidWorx Design Kit

The RapidWorx Design Kit is a complete RTL to placed-gates, timing-closed design flow, consisting of five steps, summarized in [Table 3](#). Tools are launched from an intuitive, easy-to-use RapidWorx Design Kit “cockpit.”

Table 3 RapidWorx Design Kit

Step	Associated Tool	Tool Function
1	RapidBuilder	Configuration and RTL generation of memories, I/Os, and clocks.
2	RapidView	Map memories, I/Os, and diffused IP to physical locations on the slice.
3	RapidPRO	Analysis of RTL code for adherence to physical design feasibility of timing closure, congestion, and electrical rule checks to meet signoff criteria.
4	Physical Synthesis	RTL to placed-gates synthesis.
5	RapidCheck	Gate-level netlist and physical database handoff checks.

The RapidWorx Design Kit facilitates cross-probing between tools. Each RapidWorx Design Kit tool is described more fully in the following sections.

1.5.2 RapidBuilder

The RapidBuilder tool lets you configure the memory, I/O, diffused IP, and clock resources on the RapidChip slice. The tool generates RTL code containing configured memory, I/O, and clock circuits that conform to all physical design and test rules. The I/Os and PLLs are included in the top module RTL, while the memories and clocks are included in wrappers that are subsequently instantiated in your RTL code.

RTL generation for memory blocks configures the prediffused RAM available on the RapidChip slice. RTL memory wrappers organize and tile physical memory blocks according to the desired depth and width. Individual memories can be reconfigured to become deeper and narrower.

Memory tiling can aggregate two or more diffused memories to generate wider memories, deeper memories, or combinations of smaller R-Cell and diffused memories to match design requirements. The wrapper includes the memory Built-In Self Test (BIST) logic that is used to exhaustively test the memory.

The next step of the RapidBuilder tool is the package pin assignment and configuration of I/O types. You simply enter the signal name and desired I/O configuration associated with a particular package ball, and the RapidBuilder tool generates top-module RTL code instantiating I/O buffers, boundary scan cells, JTAG TAP controller, and clock structures. You then surround the custom logic with the RapidBuilder tool generated top-level module.

The RapidBuilder tool automates the generation of correct-by-construction “clock factories” by allowing you a selection of oscillator and reset sources, coefficients for frequency division/multiplication, and clock powerdown modes. Additional features of the clock factory are: insertion delay matching across different generated clocks from the same PLL, and clock branch gating for powerdown mode. A single PLL can feed several clock factory elements that generate output clocks with known phase and frequency relationships.

You enter the clock features into the RapidBuilder tool user interface, and the resultant RTL is instantiated into the final design.

The RapidChip technology clock generation strategy differs from a typical ASIC flow in that all clocks are required to originate from the clock factory

modules. Because all RapidChip technology designs use a familiar and structured approach to handle clocks, the test strategy, timing closure, and final timing tuning are simplified. Note that the number of clocks allowed on a RapidChip slice is not limited, as is the case with other programmable or structured ASICs. The R-Cell fabric does not predesignate flip-flop locations, allowing much greater flexibility for flip-flop placement on the die and more degrees of freedom in clock generation. You are only limited to a fixed number of clocks that require tuning to one another in order to minimize backend turnaround time within the limits defined by LSI Logic.

1.5.3 RapidView

The RapidView tool associates physical slice resources to logical instances in the RTL. It provides a graphical representation of the physical slice resources. Using its cross-probing capability with the RapidBuilder tool, the RapidView tool can highlight a memory, I/O, or IP block selected within the RapidBuilder tool, then bind a logical instance in the RTL to a physical resource on the die.

The RapidView tool is also used as a general-purpose physical design interface to view the initial floorplan, the placed-gates database, or the final placed-and-routed design. Another RapidView tool feature is the preplacement of R-Cells prior to RTL physical synthesis, which is used to automatically locate timing-critical cells next to their respective I/Os; for example, placing boundary scan cells next to their corresponding I/Os. After the binding and preplacement, you write out a physical definition file containing the RapidChip platform ASIC floorplan, mapped I/Os, memories, IP, and preplaced R-Cells. This file is used in the RTL physical synthesis step.

1.5.4 RapidPRO

The RapidPRO tool combines the RapidChip technology PRO rule set with the Tera Systems TeraForm software, and analyzes the RTL code for rule conformance. RapidWorx Design Kit rules limit the number of tuned clocks, prohibit gated clocks outside of the clock factories, and prohibit combinational feedback paths.

LSI Logic pioneered physical RTL analysis for ASICs; that technology is leveraged in the RapidChip technology. RTL physical analysis is used to check the RTL code of RapidChip technology designs against

implementation rules to find problematic RTL structures. Such structures include large, centralized muxes, and configuration blocks that create congestion and timing closure bottlenecks. RTL analysis is done early in the design cycle, preventing problems that can only be fixed with changes in RTL code or synthesis strategy from propagating further into the design flow.

1.5.5 Physical Synthesis

A key component of the RapidWorx Design Kit is physical synthesis. Physical synthesis combines RTL synthesis, placement, and optimization in a single integrated process. The output is a placed-gates netlist and associated placement def file based on a global route timing estimation. The RTL to placed-gates synthesis approach lets you bypass the iterative timing closure loop associated with gate-level netlist handoff by providing much more accurate timing estimation than is possible with wireload models based on fanout. Correlation between the placed-gates handoff and final routed design database is typically within 250 ps, which is a much higher correlation to final layout than commonly seen with a netlist handoff. The RapidWorx Design Kit includes upfront avoidance of signal integrity issues, such as SSO, IR drop, and core noise. Avoidance and/or mitigation of physical effects, such as congestion and crosstalk, are addressed up-front by the physical synthesis tools.

The RapidWorx Design Kit includes support for the Amplify tool for the RapidChip technology. This tool, jointly developed by Synplicity and LSI Logic, provides you with easy-to-use physical synthesis. The RapidChip Design Kit RTL to placed-gates synthesis flow is done at the chip level, letting you specify timing constraints at the I/O level. This flow is simpler than managing multiple modules using bottom-up compile strategies.

1.5.6 RapidCheck

The RapidWorx Design Kit enforces design rules to achieve the fastest possible design turnaround without iterations. The RapidCheck tool is a comprehensive handoff checker that examines the gate-level netlist for legal connectivity and legal cell placement. The RapidCheck tool also generates all outputs necessary for handoff to LSI Logic for layout completion, test vector generation, and manufacture. These final checks before handoff remove the need for design iterations and eliminate design closure problems.

The layout starting point at LSI Logic consists of a prebuilt RapidChip platform ASIC with I/Os, diffused IP, PLLs, memories, power mesh, decoupling capacitors, and timing-critical transceiver-to-I/O nets completed. Final layout after design handoff commences with importing the placed-gates database, and running the clock and signal routers. LVS/DRC is run prior to tapeout. However, the majority of LVS/DRC violations are repaired during slice creation, and therefore are not encountered in the Instance Creation phase of the design, which results in acceleration of this phase.

2 RapidChip Xtreme Platform ASIC Overview

The RapidChip Xtreme platform ASIC family has been architected to satisfy the needs of a broad cross section of custom logic applications that require high-speed SERDES interfaces. The initial family members feature two types of high-speed SERDES interfaces that can interface to a wide range of industry standard I/Os, including:

- GigaBlaze High-Speed SERDES (1 Gbits/s to 4.25 Gbits/s)
 - 1G Ethernet
 - 10G Ethernet
 - XAUI
 - Fibre Channel
 - PCI Express
 - Serial-RIO
 - SATA
 - SAS
 - InfiniBand
- HyperPHY™ High-Speed Buses (155 Mbits/s to 1.3 Gbits/s)
 - SPI4-2
 - OC3 / STS3 / STM1
 - OC12 / STS12 / STM4
 - Parallel-RIO
 - SGMII

LSI Logic has over seven years experience in developing standards-compliant high-speed SERDES cores and integrating these cores. LSI Logic has a complete engineering and support team for these high-speed cores including:

- Design Engineering
- Signal Integrity Experts
- Characterization and Test Engineering
- Core Integration Engineering

Both the GigaBlaze and HyperPHY cores are fully integrated SERDES cores offering full-duplex operation and include noise isolation techniques. They support multiple data rates and have integrated termination, which is selectable for 50 or 75 ohms, with pre-emphasis for improved signal integrity.

The cores also have built-in testability, including full scan in the digital sections of the core, BIST in both the digital and analog sections, plus LOOPBACK options for complete testing in or out of system. These cores are implemented as Diffused IP to ensure maximum performance and predictable design.

The RapidChip Xtreme platform ASIC family also offers relocatable IP. For example, DDR memory controllers can be implemented using Hard or Soft IP and Config I/Os. These options allow you to closely match bit widths to application needs or to have multiple, independent DDR interfaces of different widths at any position around the periphery of the RapidChip slice. The DDR interfaces can operate at up to 200 MHz (400Mbps/s) point to point, and 167 MHz (333 Mbps/s) multidrop.

The advantage of using a Soft IP strategy is that if IP is not required in a design, then the area they consume (all the gates and memories) is freed up for use as custom random logic. The high-performance R-Cell transistor architecture allows IP to be implemented in this way as it does not force artificial constraints on the logic fabric.

The RapidChip Xtreme platform ASICs support popular open-architecture processors, such as ARM966, MIPS4K, and ZSP[®] digital signal processors. Some slices include a specially designed *Landing Zone* region that can be used to implement soft processors or a Hard ARM966 with at least 32 Kbytes each of Instruction and Data of tightly

coupled RAM (refer to [Section 2.9, “Embedded Microprocessor Support,”](#) for more details). The advantage of using the Hard R-Cell ARM966 is that it has been specially optimized for use in the Landing Zone region at a speed of 212.5 MHz.

By allowing you the flexibility to chose how to implement your IP, including processors, the RapidChip Xtreme platform ASIC family combines the advantages of predefined/predesigned IP with the benefits of RapidChip technology: high performance, design scalability, pinout selection, and fine tuning of resources to optimize cost.

2.1 Feature Summary

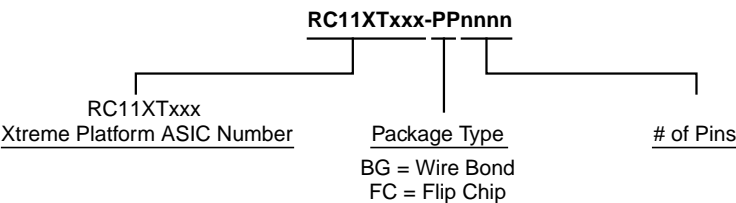
The key features of the RapidChip Xtreme platform ASIC family are:

- Multiple channels of high-speed SERDES operating up to 4.25 Gbits/s
- Flexible DDR on-demand implementation using Hard IP and Config I/Os, offering you complete flexibility in your memory interface designs. Multidrop operation is between 133 MHz (266 Mbits/s) up to 167 MHz (333 Mbits/s) and point-to-point is up to 200 MHz (400 Mbits/s).
- Support for leading-edge, open-architecture microprocessor cores using either:
 - Soft or Firm IP whose location is determined by you
 - Hard IP located in a dedicated Landing Zone region. If no processor is needed, the processor gates and memory of this Landing Zone region are 100% reusable as designer logic.
- Memory options
 - High-performance single (1rw), two (1r1w), and true dual-port (2rw) diffused RAMs are available in various configurations depending on the slice.
 - Diffused RAMs range from 9 Kbits up to 144 Kbits, and are configurable by width and depth.
 - Small RAMs (up to 5 Kbits) are implemented efficiently in R-Cells, which are relocatable in the transistor fabric region.

2.2 Naming Conventions

Figure 3 shows the RapidChip Xtreme platform ASIC product numbering conventions. For example, the RC11XT404-BG672 platform ASIC is packaged in a 672-pin wire-bond package, and the RC11XT432-FC896 platform ASIC is packaged in a 896-pin high-performance flip-chip package.

Figure 3 Product Numbering



2.3 Family Members

The RapidChip Xtreme platform ASIC family initially consists of four slices. Family members differ from each other in the number and types of high-speed SERDES interfaces they offer. All slices support leading-edge Hard, Firm, and Soft IPs. Because these IP cores are optional, they are implemented on the RapidChip platform ASIC only when needed. In designs that do not require IP cores, the gates, memory, and I/O are available for other purposes.

Table 4 summarizes the available resources for each member of the RapidChip Xtreme platform ASIC family. A range of usable gates is listed for each RapidChip platform ASIC. The actual number of usable gates is dependent on the design.

Table 4 RapidChip Xtreme Platform ASIC Family Summary

	RC11XT404	RC11XT416	RC11XT432	RC11XT531
Available Logic Gates (MGates)	3.7	5.7	4.8	5.2
Usable Gates (MGates)	1.4 - 2.1	2.1 - 3.3	1.7 - 2.7	1.8 - 2.8
Usable RAM (Mbits)	1.9	1.9	1.9	1.6
GigaBlaze SERDES Core up to 4.25 Gbits/s	4 x1 = 4	4 x4 = 16	8 x4 = 32	3 x4 =12
HyperPHY SERDES Core 155 Mbits/s - 1300 Mbits/s	-	-	-	18
PLL	3	4	4	4
Maximum Config I/Os	362	355/519	259/427	396
Package	672 EPBGA	672/896 FCBGA	672/896 FCBGA	896 FCBGA

2.4 Memory Implementation

To implement memory in RapidChip Xtreme platform ASICs, you use the RapidWorx Design Kit to configure the diffused memory blocks and to instantiate small memory arrays that are built from the R-Cells in the transistor fabric region.

By tiling and combining these diffused and R-Cell memory arrays, you can flexibly define memory spaces that meet your needs.

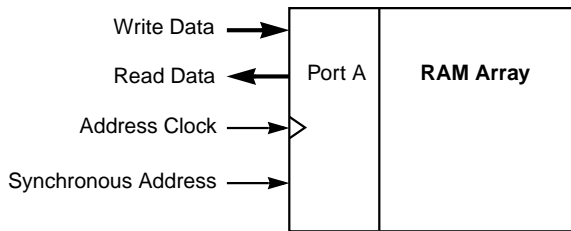
RapidChip platform ASICs typically implement three types of memory architecture, referred to as 1rw, 1r1w, and 2rw. Although the number, size, and mix of types of general-purpose RAMs is specific to a particular slice, they are selected from one or more of these three types.

The characteristics of the three memory types are described briefly:

- 1rw memory

The 1rw memory, often referred to as a “single port” RAM, has one address port available to conduct either a single read or a single write command synchronously with the port clock.

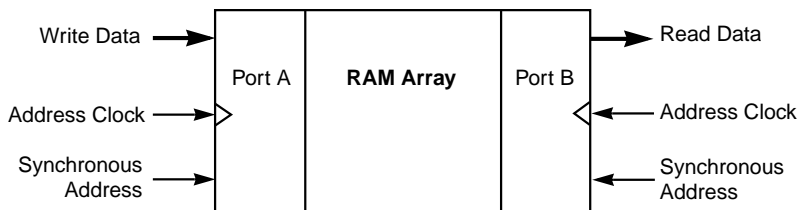
Figure 4 Logic Symbol for 1rw Memory



- 1r1w memory

The 1r1w memory, sometimes referred to as a “simple dual port” RAM, has two address ports. One is a dedicated read port; the other is a dedicated write port. Each port operates independently of the other, and has its own port clock to conduct synchronous transactions.

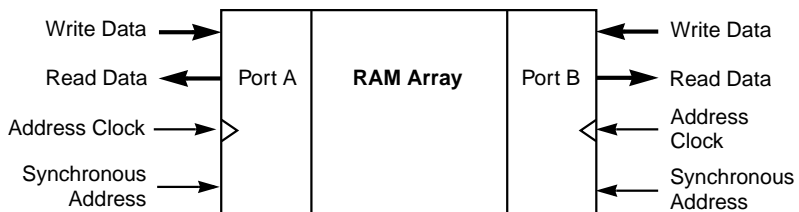
Figure 5 Logic Symbol for 1r1w Memory



- 2rw memory

The 2rw memory, sometimes referred to as a “true dual port” RAM, has two address ports. Each of its ports can perform either a read or a write command synchronously with the port clock. Each port operates independently of the other, so both ports can operate simultaneously and with different clock speeds.

Figure 6 Logic Symbol for 2rw Memory



2.4.1 Diffused Memory Blocks

Each slice has several fixed-size, diffused memory blocks. These memory blocks range in size from 9 Kbits to 144 Kbits. All blocks operate synchronously and have a bit-level write enable mask. [Table 5](#) outlines the different memory configurations available on each of the slices. Additional memories are possible on every slice by using the R-Cell memories, as described in [Section 2.4.2, “R-Cell Memory.”](#)

Table 5 Diffused Memory Configurations

RAM Type	Block Size	RC11XT404	RC11XT416	RC11XT432	RC11XT531
2rw	256 x 38 (9 Kb)	16	16	16	-
2rw	512 x 38 (18 Kb)	-	12	12	-
2rw	512 x 76 (36 Kb)	-	16	16	-
2rw	1K x 38 (38 Kb)	8	-	-	-
2rw	256 x 36 (9 Kb)	-	-	-	36
1r1w	1K x 36 (36 Kb)	-	-	-	36
1rw	4K X 36 (144 Kb)	8	4	4	-
1rw	2K x 72 (144 Kb)	2	2	2	-
Total Memory Bits (Mb)		1.9	1.9	1.9	1.6

Note: Further memories can be implemented using R-Cells. See [Section 2.4.2, “R-Cell Memory.”](#)

2.4.2 R-Cell Memory

You can use the RapidWorx Design Kit to instantiate fully synchronous R-Cell memory in the transistor fabric region. [Table 6](#) summarizes the features and the allowable configurations of R-Cell memory arrays when the arrays are implemented at the maximum size. Both R-Cell memory types feature write ports with independent word-level enable masks.

Table 6 R-Cell Memory

Architecture	Maximum Array Size	Maximum Configurations	
		Address Range	Word Width
1r1w	5,120 bits	32 Words	160 bits
		64 Words	80 bits
		128 Words	40 bits
		256 Words	20 bits
2rw	2,560 bits	16 Words	160 bits
		32 Words	80 bits
		64 Words	40 bits
		128 Words	20 bits

You can also implement smaller memory arrays than those shown in [Table 6](#). [Table 7](#) lists the minimum and maximum memory sizes, address ranges, and word widths for 1r1w and 2rw memories.

Table 7 R-Cell Memory Dimensions

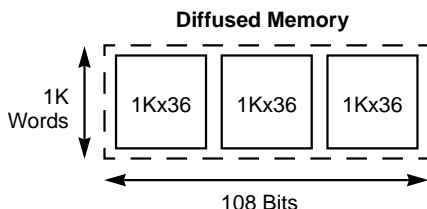
Memory Size		Address Range		Word Width	
Minimum	4 bits	Minimum	2 Words	Minimum	2 bits
Maximum	5,120 bits ¹	Maximum	256 Words	Maximum	160 bits

1. 2rw memory is limited to 2,560 bits.

2.4.3 Flexible Memory Configurations

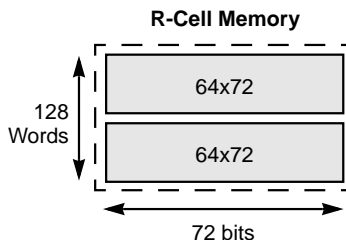
You can tile and combine memory to create larger logical arrays. For example, [Figure 7](#) shows three 1K x 36 diffused memories tiled horizontally to create a single logical 1K x 108 array. Although not shown, these memories also can be tiled vertically to create a single logical 3K x 36 array.

Figure 7 Tiling Diffused Memory



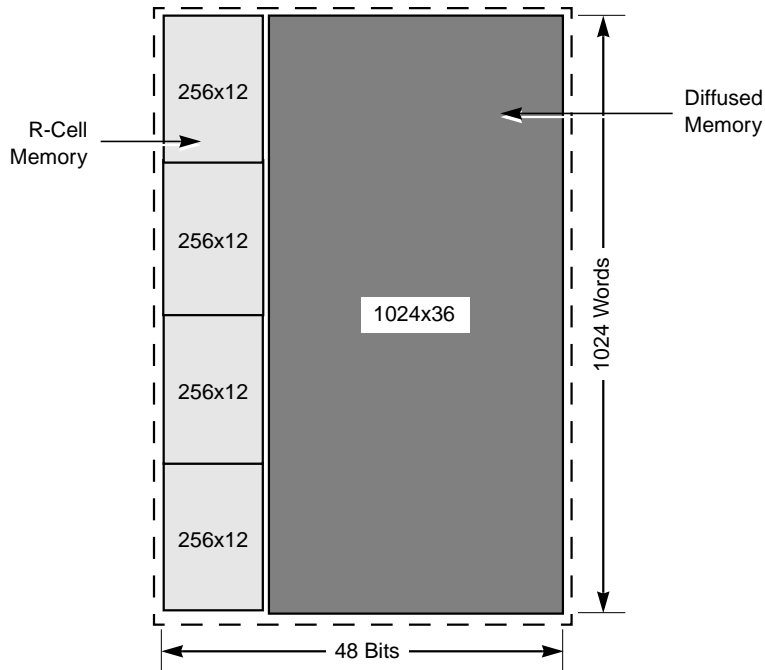
[Figure 8](#) shows two 64 x 72 R-Cell memories tiled to create a single logical 128 x 72 array. Although not shown, these memories can also be tiled in the other dimension to create a single logical 64 x 144 array.

Figure 8 Tiling R-Cell Memory



Diffused memory can also be combined with R-Cell memory to create a larger logical array. [Figure 9](#) shows four tiled 256 x 12 R-Cell memories combined with a single 1024 x 36 diffused memory to create a single logical 1024 x 48 array.

Figure 9 Combining R-Cell and Diffused Memory



2.5 Configurable I/Os

The RapidChip Xtreme platform ASIC family provides a broad range of user-configurable I/O types that are configured by patterning of the metal interconnects. I/O buffers are compact, but address the majority of industry-standard applications without the overheads associated with reprogrammability.

[Table 8](#) lists all the available I/O driver types.

Table 8 I/O Driver Types

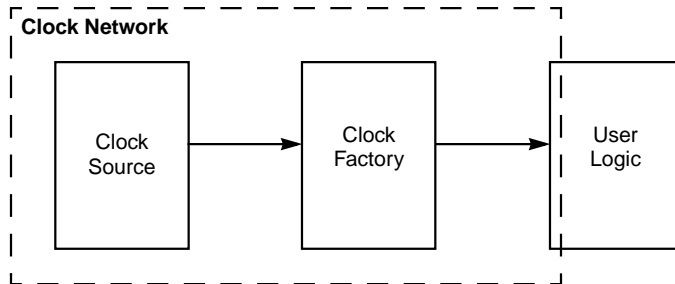
Type	I/O	V _{DD}	Drive Strength
Controlled Impedance ¹	Bidirectional 3-State	2.5 V	25, 50 Ω
		3.3 V	25, 50 Ω
HSTL	Single-Ended Bidirectional	1.5 V	Class I (8 mA)
	Single-Ended Bidirectional	1.5 V	Class II (16 mA)
LVDS2.5	Differential Output	2.5 V	1.7 mA/3.2 mA
	Differential Input	2.5 V	-
LVDS3.3	Differential Output	3.3 V	1.7 mA/3.2 mA
	Differential Input	3.3 V	-
LVTTTL (LVCMOS) ¹	Bidirectional	1.8 V	25, 50 Ω
		2.5 V	25, 50 Ω
		3.3 V	25, 50 Ω
PCI-X 100/133 PCI-33/-66	Bidirectional	3.3 V	Controlled Impedance Slew Limited
PECL	Differential Input	3.3 V	-
SSTL2	Bidirectional	2.5 V	Class I (9 mA)
			Class II (16 mA)

1. Available with pull-ups or pull-downs.

2.6 Clock Networks and PLLs

Slices provide you with a number of options for creating and managing clock networks ([Figure 10](#)). Clock networks consist of one or more clock sources, a Clock Factory, and the clock signals required by your user logic.

Figure 10 Simple Clock Network



The clock source can be one of the general-purpose PLLs ([Figure 13](#)) on the slice, an external clock source, or another on-chip clock source that you instantiate in the transistor fabric region. The Clock Factory uses the clock sources to derive the clock, reset, and test signals that your user logic requires. Using the RapidWorx Design Kit, you configure the PLLs and specify a Clock Factory that meets the clocking requirements of your user logic. The application note, *Using RapidBuilder to Generate a Clock Factory*, provides more information about these subjects.

2.6.1 Clock Factory

A Clock Factory is a module that you create with the RapidWorx Design Kit. You specify the clock source, feedback dividers, output frequencies, resets, reset synchronizers, and test bypass modes. Clock factories ensure a consistent coding and implementation style for every clock in the design. All clock sources, including those from user logic, must be intercepted and passed through the known good structures of the Clock Factory. Therefore, after netlist hand-off, physical design and test flow key off regular, known structures.

[Figure 11](#) is a block diagram of a sample clock factory module. The clock source can be an external oscillator, a PLL output, or a recovered clock from a communications data stream. The Clock Factory provides one synchronous reset signal for each clock in the module, which sets or resets all the flip-flops in the clock's domain. The asynchronous reset signal can originate from an external pin or from internal logic.

Figure 11 Clock Factory

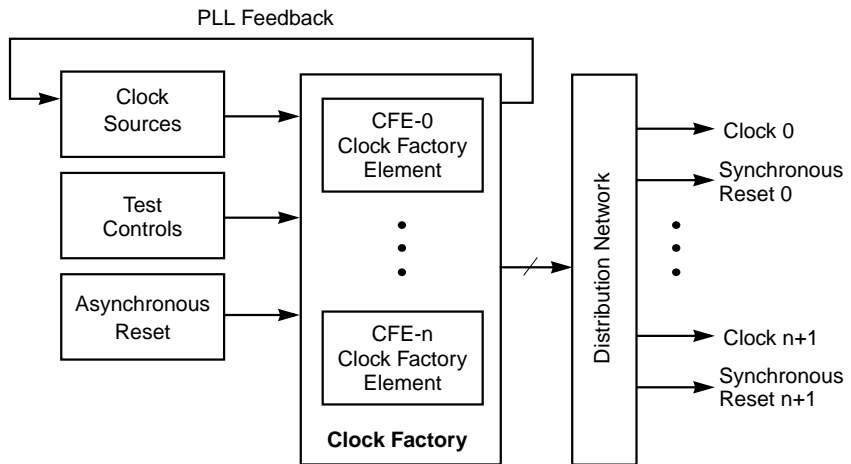
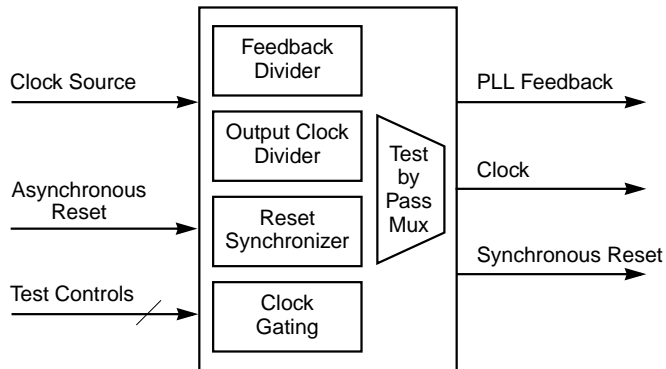


Figure 12 shows a clock factory element in greater detail.

Figure 12 Clock Factory Element



The Clock Factory's output signal (Clock) has a 50/50 duty cycle. Using the RapidBuilder tool, you set the output frequency (Clock) to a multiple of the clock source frequency by specifying values of 1 to 64 for the Feedback Divider and the Output Clock Divider. The Reset Synchronizer accepts an asynchronous reset and generates a synchronous reset aligned to the clock output. The clock factory module is included in the RapidChip platform ASIC RTL description. The module, which is

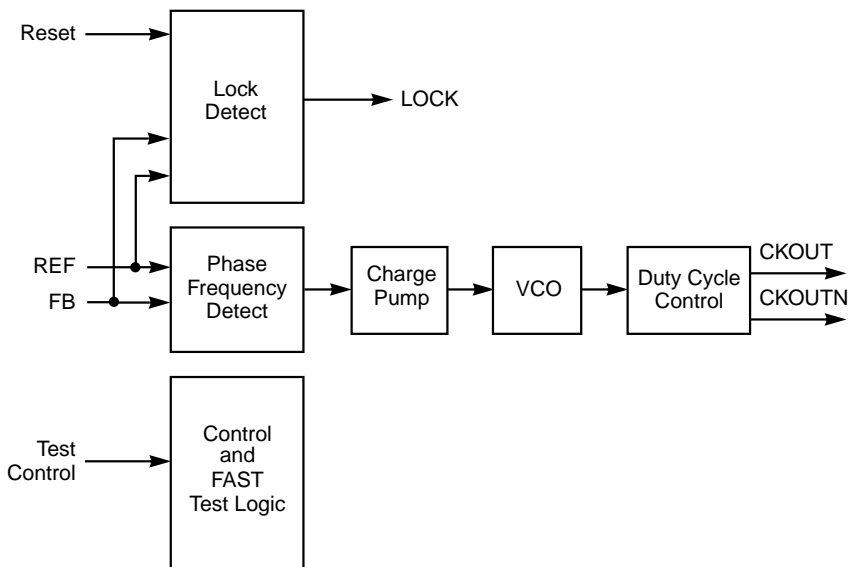
instantiated in the R-Cell region, is placed close to its clock source to ensure predictable behavior in the back-end place and route flow.

You can specify an unlimited number of clock factory elements in one Clock Factory. However, the number of tuned clock networks (where edge alignment must fall within a given tolerance) in one Clock Factory is limited to four that must be derived from the same clock source.

2.6.2 General-Purpose PLLs

Each RapidChip Xtreme platform ASIC includes three or more fully integrated, internal loop filter PLLs. [Figure 13](#) shows a simplified PLL block diagram for reference. The RapidWorx Design Kit is used to configure the PLL options and then build a PLL wrapper that instantiates a diffused PLL with the features that you specify.

Figure 13 PLL Block Diagram



The PLL outputs, CKOUT and CKOUTN, can be used as the clock source for a Clock Factory. The reference clock input (REF) can be either a single-ended signal or a differential signal. The PLL feedback signal (FB) comes from the Clock Factory. A programmable charge pump supports frequency multiplication up to $M = 64$. The VCO is powered by an integrated, self-referenced, voltage regulator for reduced susceptibility

to power supply noise. The Duty Cycle Control logic ensures a 50/50 duty cycle. During chip-level testing, the Lock Detect macrocell is used to verify that the PLL locks properly and that jitter is within specifications.

Each PLL has its own dedicated power supply balls to ensure maximum noise immunity. All PLL I/Os have dedicated and optimized traces assigned within the RapidChip platform ASIC package.

The RapidWorx Design Kit specifies the Clock Factory and configures the PLLs. The RapidWorx Design Kit allows you to manage clock networks with a consistent approach to clock domain reset and scan chain control, which simplifies test.

Using the RapidWorx Design Kit, you enter the various parameters for the Clock Factory, such as the clock source, feedback dividers, reset synchronizers, clock reset and test bypass modes, and the output frequencies. Key features of the clock factory module include:

- Fixed 50/50 duty cycle output
- Fixed active edge (positive)
- No user-varied insertion delay/skew relationships
- Fixed reset scheme
 - Asynchronous assert/synchronous removal
 - Logic or external pin triggered

The RapidChip Xtreme platform ASICs contain several different PLL types. For the exact combination, refer to the individual RapidChip platform ASIC information in [Section 3, “RapidChip Xtreme Platform ASIC Details.”](#)

For further information on the PLLs, contact your local LSI Logic representative.

2.6.2.1 Wide-Range PLL

The wide-range PLL has an output frequency range from 60 MHz to 1250 MHz. There are four output frequency ranges, which are metal selectable:

- 60 MHz to 300 MHz
- 300 MHz to 500 MHz

- 500 MHz to 800 MHz
- 800 MHz to 1250 MHz

The external reference clock for each PLL can be either single-ended or differential, as selected by you using the RapidWorx Design Kit. The clock has dedicated impedance-controlled traces assigned within the RapidChip platform ASIC's package to ensure minimum crosstalk or interference from any other signals within the slice.

Programmable charge pump settings allow stable operation and acceptable bandwidths to be achieved for frequency multiplication as high as $M = 64$ (wide-range PLL). The PLL employs a differential VCO powered by an integrated self-referenced voltage regulator for reduced susceptibility to supply noise. The PLL is powered through a 1.2 V supply voltage.

2.6.2.2 Fixed-Range PLL

Some RapidChip Xtreme platform ASICs also use a fixed-range PLL, offering output frequencies between 100 MHz and 500 MHz.

2.7 High-Speed SERDES Cores

The RapidChip Xtreme platform ASICs are designed to meet the needs of today's high-performance Storage, Networking, and Communications systems. In addition to gates and memory, the RapidChip Xtreme platform ASICs contain the diffused high-speed SERDES cores that you require. Two types of SERDES cores are offered in the RapidChip Xtreme platform ASICs:

- GigaBlaze SERDES cores with PCML I/Os, which operate from 1 Gbits/s to 4.25 Gbits/s.
- HyperPHY SERDES cores with LVDS I/Os, which operate in full-rate mode, -ate mode, or -ate mode, making their data rate range from 155 Mbits/s to 1300 Mbits/s.

Soft CoreWare IP can be combined with these diffused high-speed SERDES channels to implement a number of industry standards including, but not limited to, 1G Ethernet, 10G Ethernet, Fibre Channel, InfiniBand, PCI Express, Serial-RIO, Parallel-RIO, SATA, SAS, SFI-4, and SPI4-2. Using these high-speed SERDES cores and Soft CoreWare IP,

you can concentrate your efforts on meeting unique system needs rather than spending time developing standard interfaces.

LSI Logic's high-speed SERDES interfaces are compliant with a wide range of industry-standard high-speed specifications.

The following subsections give a more detailed introduction of the two different types of high-speed SERDES cores. Complete datasheets on these cores are available from your LSI Logic representative or can be found on the web at <http://www.lsilogic.com/products/serdes/index.html>.

2.7.1 GigaBlaze SERDES Transceivers

The GigaBlaze SERDES transceivers provide the physical layer for standard high-speed communications protocols such as Fibre Channel, 1G Ethernet, 10G Ethernet, PCI Express, SATA, SAS, Serial-RIO, and InfiniBand. The transceivers provide point-to-point serial communications links that operate between 1 Gbits/s and 4.25 Gbits/s.

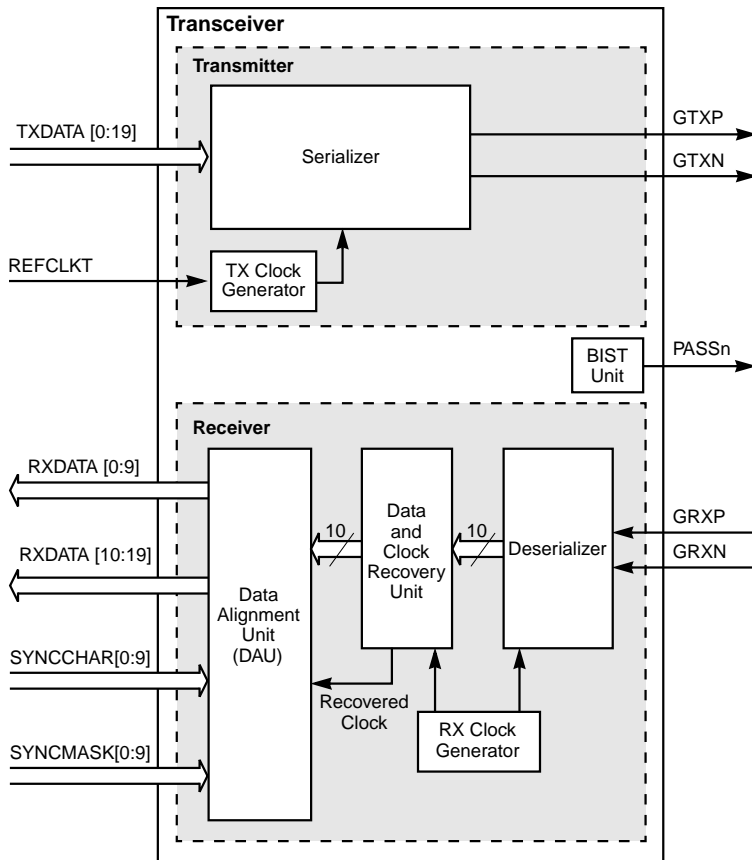
[Table 9](#) lists the supported communications standards with their respective data rates.

Table 9 GigaBlaze Supported Communications Standards

Standard	Serial Data Rate (Gbits/s)
Fibre Channel	1.0625 2.125 4.25
1G Ethernet	1.25
SATA, SAS	1.5
InfiniBand	2.5
SAS	3.0
10G Ethernet XAUI	3.125
Fibre Channel XAUI	3.1875
Serial-RIO	2.5 3.125
PCI Express	2.5

The GigaBlaze transceiver core shown in [Figure 14](#) transfers data between an internal 20-bit bus and a differential serial I/O pair. The clock rate is 1/20th the serial data rate; thus for 3.125 Gbits/s, the clock frequency is 156.25 MHz. The GigaBlaze design includes receiver clock recovery and clock synchronization. Built-In Self Test (BIST) and various loopbacks provide testability and debugging capabilities.

Figure 14 GigaBlaze Transceiver Core



The serial I/O is composed of a transmit PCML differential pair and a receive PCML differential pair. The transmit signal ranges from 1 V peak-to-peak to 2.4 V peak-to-peak. Each transceiver can be programmed to add up to 38% pre-emphasis to the signal. In typical applications, the receive I/O pair is AC coupled. Both the transmit and receive I/Os have programmable internal terminations to match the signal traces. Because

the transmitter and receiver operate independently, the GigaBlaze SERDES transceiver can send and receive data simultaneously. Also the transmitter and receiver can operate at different data transfer rates.

The transmitter transmits data at a rate controlled by the Reference Clock (REFCLKT). It accepts 20-bit parallel data (TXDATA[19:0]) clocked in on REFCLKT. The transmitter serializes and transmits the data at 20 times the REFCLKT frequency. The serial bitstream is transmitted in nonreturn-to-zero (NRZ) format on the differential pair (GTXP, GTXN).

The receive buffer accepts a serial bitstream operating between 1 Gbits/s to 4.25 Gbits/s from the differential pair (GRXP, GRXN). It deserializes the bitstream and recovers the embedded clock (RBC) and parallel data. The recovered parallel data is output on the 20-bit RXDATA bus at the RBC frequency, which is 1/20th the serial data rate. The receiver optionally can align RXDATA to a selectable synchronization pattern. Control inputs to the receiver select the synchronization pattern. Other logic can use the complementary recovered clock outputs (RBC[0:1]) to clock the output on the RXDATA bus.

To facilitate testing and system bring-up, the GigaBlaze SERDES transceiver includes:

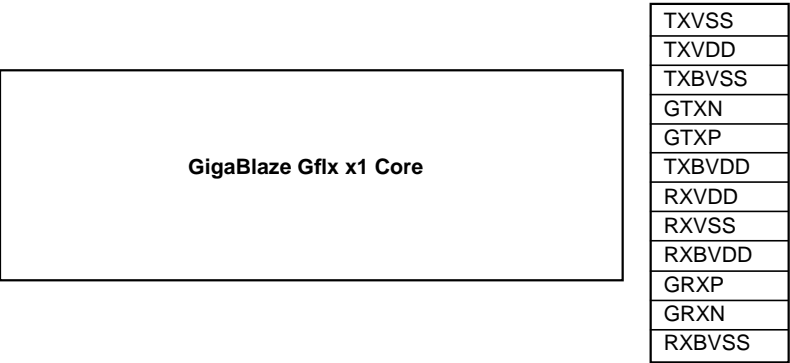
- Two internal serial loopback paths from GTXP/GTXN to GRXP/GRXN
- An internal serial reverse loopback path from GRXP/GRXN to GTXP/GTXN
- An internal parallel wrapback from the transmitter's input parallel data to the receiver's data alignment unit (DAU)
- Full scan to achieve high fault coverage in the transceiver's digital section
- A BIST unit that tests digital and analog sections

Through the internal loopback/wrapback or an external link, the BIST unit can transmit test patterns, compare them with received patterns, and alert external logic when there is a mismatch. With standards-compliant GigaBlaze SERDES transceivers, you also benefit from the LSI Logic CoreWare library of link layer functions. The combination provides a low-risk route to enabling fully compliant 10G Ethernet, Fibre Channel, and other applications.

The GigaBlaze transceivers are available in two subsystem formats, either single channel or quad channel; both are based on the same core IP.

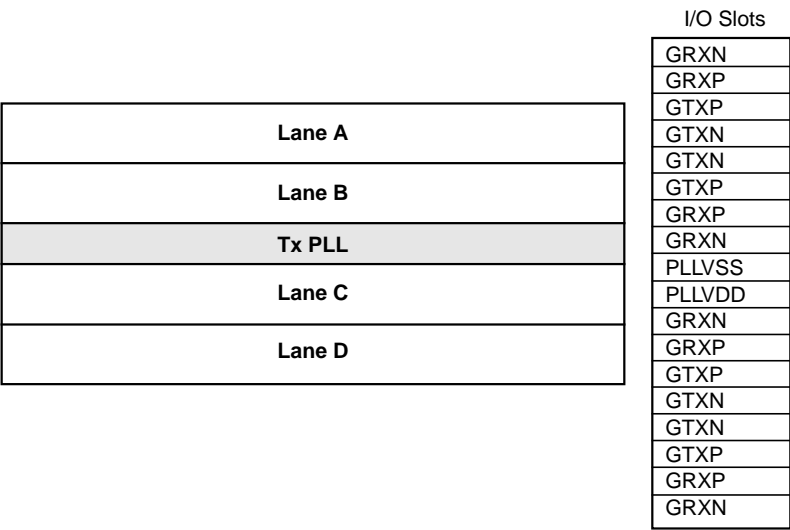
The single channel subsystem works with either wirebond or flip-chip packages; it uses 12 I/O slots as shown in [Figure 15](#).

Figure 15 GigaBlaze x1 Core



The quad channel devices have been optimized for use on flip-chip packages where a large number of GigaBlaze channels are required (see [Figure 16](#)).

Figure 16 GigaBlaze x4 Core



Within the x4 GigaBlaze subsystem, the number of I/O slots required for four x4 GigaBlaze cores is reduced to 18 compared to the 48 that are required for four x1 GigaBlaze cores. This difference represents an enormous saving for designs using a large number of high-speed SERDES transceivers, for example 10 Gbits/s switches, bridges and routers, SAS/SATA/Fibre Channel/iSCSI I/O controllers, bridges, expanders, and switches. For example, for 16 channels of high-speed SERDES transceivers, the number of I/O slots is reduced from 192 to 72, a savings of greater than 60%.

This reduction is achieved by sharing the transmit PLL across the four lanes, while still maintaining separate PLLs for the receive side of each SERDES transceiver. This ensures that high-speed signals from varied sources with different clock sources can be received by the subsystem with no problems.

The RapidChip Xtreme platform ASICs contain different combinations of GigaBlaze subsystem cores as indicated in [Section 2.3, "Family Members."](#)

Both the x4 and x1 GigaBlaze subsystems are based on the same basic GigaBlaze core shown in [Figure 14](#).

The key features of the GigaBlaze SERDES transceiver are:

- serial transfer rates up to 4.25 Gbits/s with a bit error rate less than 10^{-12}
- standards support for Fibre Channel, 1G Ethernet, XAUI, SATA, SAS, InfiniBand, PCI Express, Serial-RIO
- full-duplex operation, where the transmitter and receiver can work at different data rates
- internal serial loopback, digital parallel wrapback, BIST, and full scan to facilitate testing
- adjustable differential output swing for driving coaxial and twinaxial cables, or a fiber-optic transmitter
- low-swing differential input sensitivity
- support for standard serial line impedances of 50 Ω and 75 Ω (100 Ω and 150 Ω differential) with internal termination

Contact your local LSI Logic representative for further information on the GigaBlaze SERDES transceiver.

2.7.2 HyperPHY SERDES Core

The HyperPHY core provides point-to-point communication links that operate between 155 Mbits/s and 1300 Mbits/s. They can be used to implement many I/O standards, some of which are outlined in [Table 10](#), with or without clock recovery as required.

Table 10 HyperPHY Supported Communications Standards

Standard	Serial Data Rate (Mbits/s)
SPI4-2 (dynamic)	622 - 1300
SPI4-2 (static)	622 - 1300
OC12 / STS12 / STM4	622
OC3 / STS3 / STM1	155
Parallel-RIO	1000

The RapidChip Xtreme platform ASICs contain different combinations of HyperPHY channels as indicated in [Section 2.3, "Family Members."](#)

Each HyperPHY channel transfers data between an 8-bit internal bus and a differential serial I/O pair. The HyperPHY design includes clock recovery and clock synchronization circuitry. The HyperPHY channels connect to the I/O through LVDS buffers. The HyperPHY core accepts clocks from a high-speed PLL and creates buffered and aligned clocks.

[Figure 17](#) shows an internal block diagram of the HyperPHY transmitter, and [Figure 18](#) shows an internal block diagram of the HyperPHY receiver.

Figure 17 Simplified HyperPHY Transmitter Block Diagram

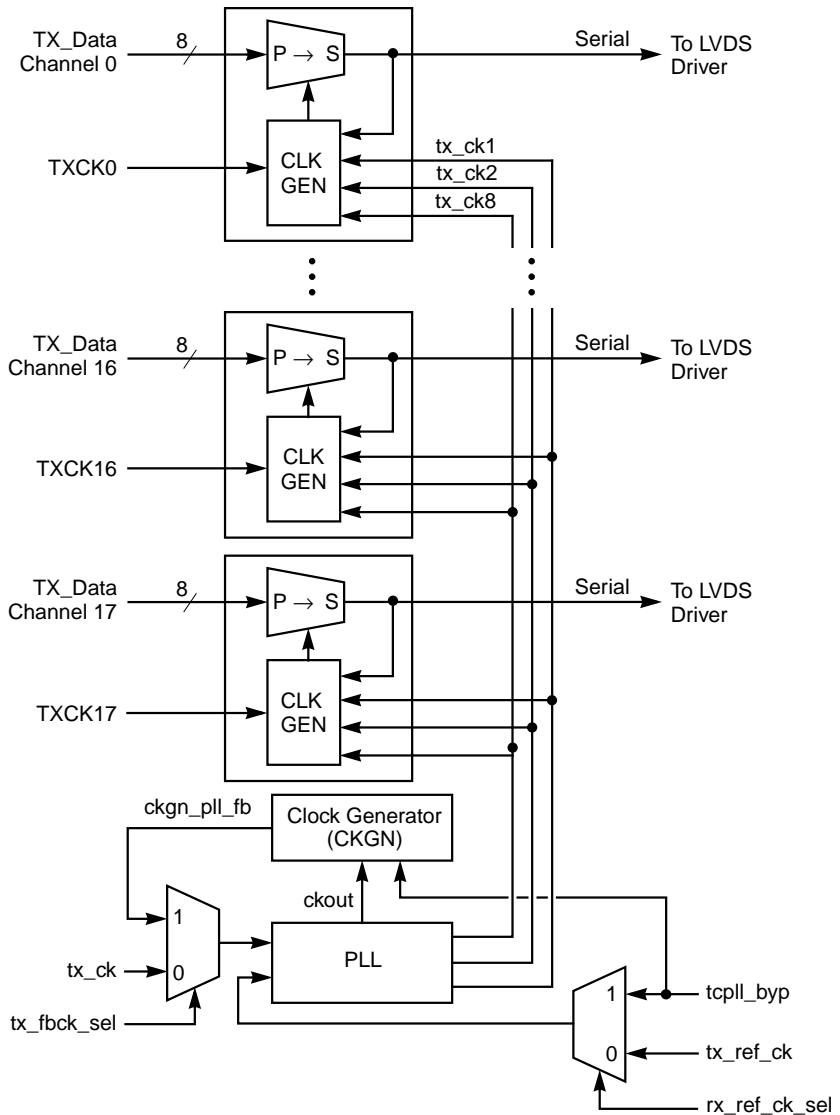
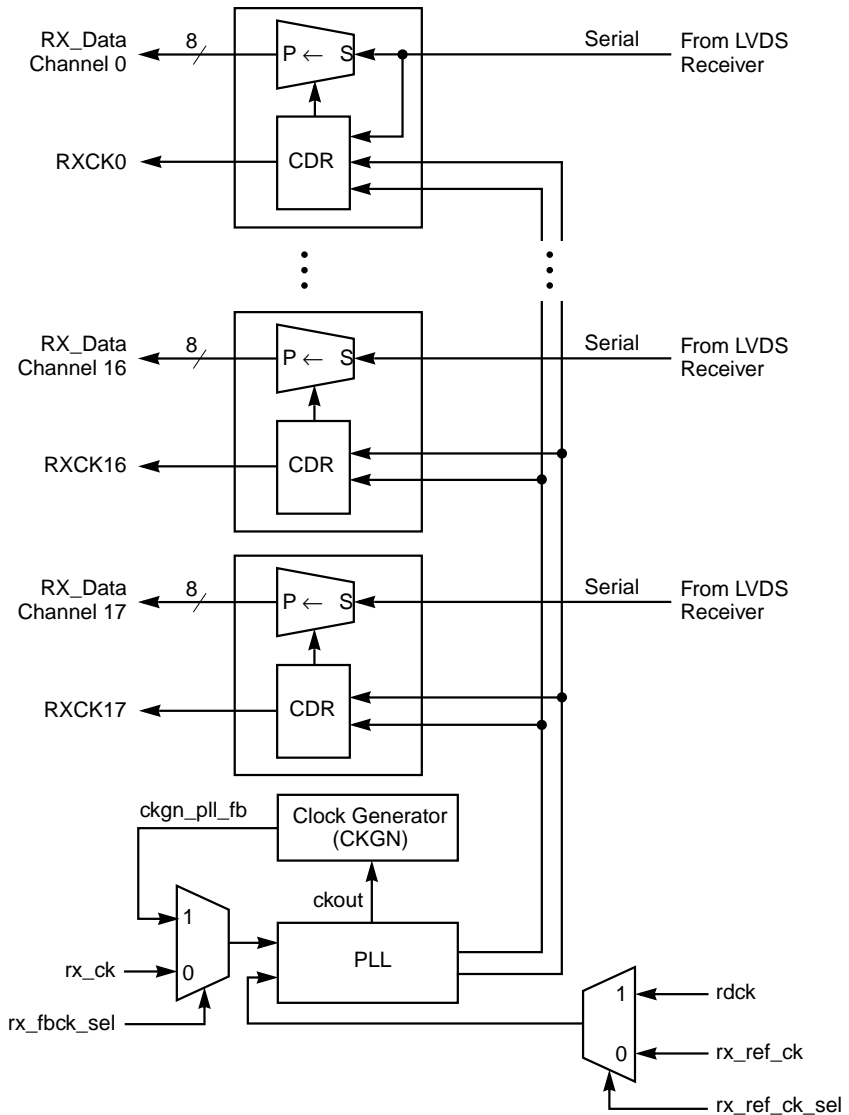


Figure 18 Simplified HyperPHY Receiver Block Diagram



Each core has its own clock and data recovery circuit. Using the buffered clock as a reference, a digital locked loop (DLL) locks on to the received data and generates the clock for the serial-to-parallel converter.

In addition to full-rate operation (the data rate equals the clock rate), the HyperPHY channels can operate at one-half or one-quarter rate. In each

channel, the DLL can be set to generate clocks at the input clock frequency, one-half the input clock frequency, or one-quarter the input clock frequency. The operation is set by a two-wire rate input control.

The key features of the HyperPHY cores are:

- OC12/STM4 data rate support
- OC3/STM1 data rate in 1/4-rate mode
- SPI4-2 standard
- SFI-4 standard
- Parallel-RIO standard
- Serial data received at rates from 155 Mbits/s to 1300 Mbits/s is demultiplexed to an 8-bit word with associated clock
- An 8-bit word and associated clock are multiplexed and transmitted serially at rates from 155 Mbits/s to 1300 Mbits/s
- Typical power consumption of 85 mW per full-duplex channel at 622 Mbits/s including LVDS buffers
- At-speed BIST of full transmit and receive/clock recovery functions
- Reliable data reception even with long sequences of data without transitions
- 1.8 V LVDS buffers

Contact your local LSI Logic representative for further information on the HyperPHY SERDES transceiver.

2.7.3 SERDES Framer Interface (SFI-4)

The SFI-4 interface can be used to implement many I/O standards, some of which are outlined in [Table 11](#).

Table 11 Framer Supported Communications Standards

Standard	Serial Data Rate (Mbits/s)
SFI-4	622 - 800
XSBI	644

This extended interface has separate transmit and receive channels. There is one clock for every four channels. Alternatively, a single clock can be configured to run all 16 channels. [Figure 19](#) shows the transmit block diagram, and [Figure 20](#) shows the receive block diagram. When the SFI-4 interface is used, the corresponding ConfigIO buffers are configured as LVDS inputs and LVDS outputs. When the SFI-4 interface is not used, these buffers are available as ConfigIO buffers.

Figure 19 SFI-4 Transmit Block Diagram

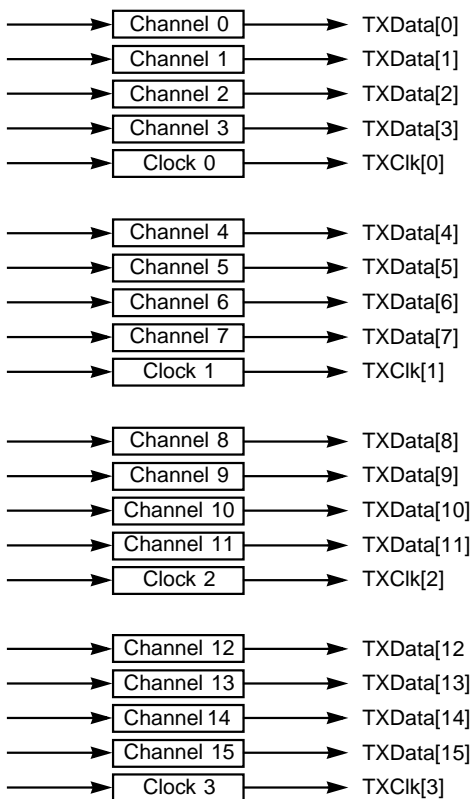
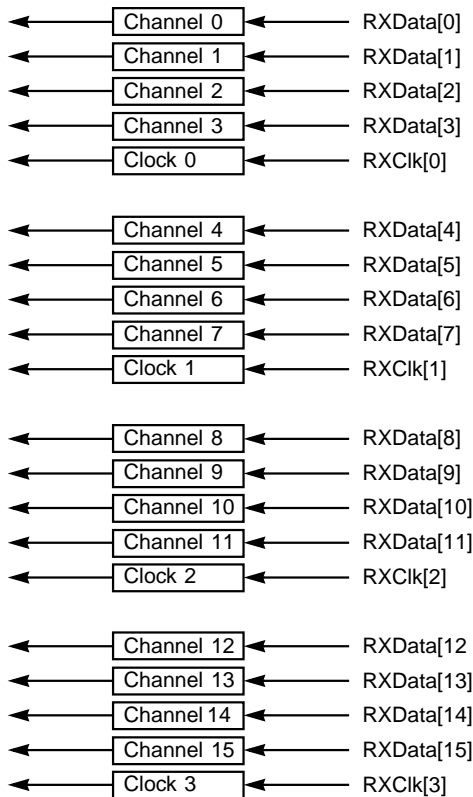


Figure 20 SFI-4 Receive Block Diagram



2.8 Double-Data-Rate (DDR) PHY Support

The RapidChip Xtreme platform ASIC family offers a flexible approach to DDR implementation using Hard or Soft R-Cell IP combined with Config I/Os to achieve speeds of up to 200 MHz (400 Mbits/s) per pin point to point.

The key features of the DDR PHY resources for the RapidChip Xtreme platform ASIC family are:

- For Hard R-Cell DDR PHY, operation up to 200 MHz (400 Mbits/s) point to point and 167 MHz (333 Mbits/s) multidrop.
- Memory controller interfaces for x4, x8, x16, and x32 DDR configurations

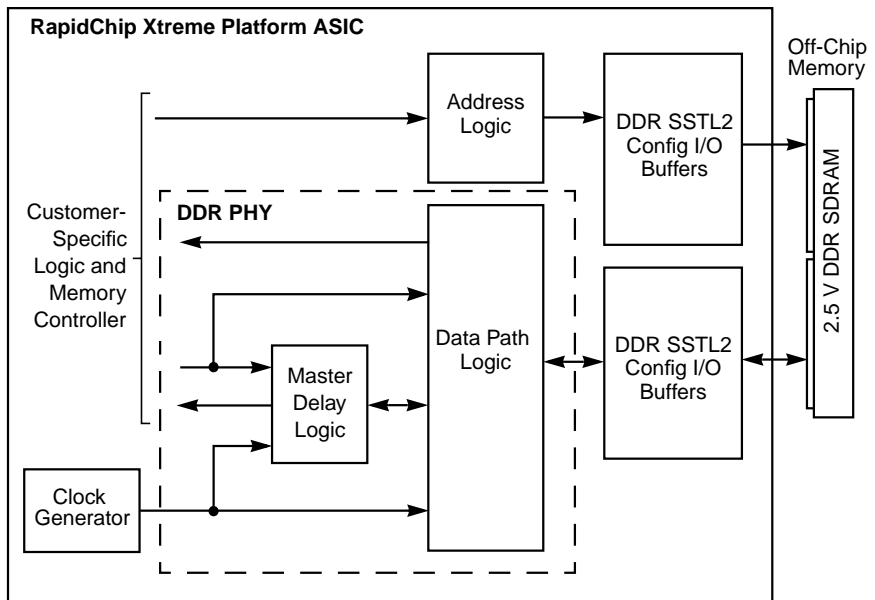
- Burst lengths of 2, 4, and 8
- Programmable delay of data strobe for read operations
- Digital Delay Locked Loop (DLL) to maintain constant programmable delay over variations in process, voltage, and temperature (PVT)
- 2X clock architecture to ensure 90-degree phase shift for DQS during a write cycle
- Internal scan and self test

The number of DDR bits that can be configured as Hard R-Cell is determined by the characteristics of the slice and will be further outlined in an application note from LSI Logic (please contact your LSI Logic sales representative for the status of this application note).

If no DDR is required in the application, then all of the Config I/Os can be used for other purposes. In this way RapidChip Xtreme platform ASICs offer you the maximum flexibility and re-useability.

LSI Logic DDR PHY CoreWare IP building blocks perform 2:1 compression and decompression, and alignment and strobe forwarding of DQ/DQS signals. [Figure 21](#) shows a simplified block diagram of the DDR PHY and its system interconnections.

Figure 21 DDR PHY Simplified Block Diagram



The memory address signals, memory control signals, and differential clock signals are generated outside the DDR PHY as part of random logic implemented by you.

Datapath cells are implemented with a granularity of eight bits per block, permitting controller width to be tailored to system requirements, as well as permitting multiple independent DDR memory controllers per slice.

The Config I/Os are suitable for both single-point and multipoint applications. The Hard version of the datapath macro (DP), providing data, clock, and control signals, and the master delay hardmacro (MDELAY) are optimized to meet the critical timing requirements of the early and late clocks and thus to detect early and late data.

In designs using the DDR interface, the corresponding ConfigIO buffers operate in the SSTL2 I/O standard.

2.8.1 Memory I/O Types

[Table 12](#) lists the memories that can be configured for use with the DDR-specific resources available in slices. FCRAM memories typically are

used for networking applications. Such memories support bit widths up to 32 bits and speeds in excess of 200 MHz.

Table 12 Supported DDR Memories

Memory Type	DC Levels	Density	Organization (bits)
DDR1 SDRAM	SSTL2 @ 2.5V Config I/O	64 Mbits	x32
		128 Mbits	x4, x8, x16
		256 Mbits	x4, x8, x16
		512 Mbits	x4, x8, x16
		1024 Mbits	x4, x8, x16
FCRAM	SSTL2 @ 2.5V, 2.5V V_{DD}	256 Mbits	x8, x16

2.9 Embedded Microprocessor Support

LSI Logic has pioneered the Landing Zone region to support different CPU cores as Hard, Firm, or Soft IP. This feature is available on all the RapidChip Integrator platform ASICs and most RapidChip Xtreme platform ASICs. The RC11XT4xx series of RapidChip platform ASICs offer a Landing Zone region specifically designed for the ARM966 processor with at least 32 Kbytes each of tightly coupled memory for instruction and data.

The Landing Zone region comprises a pre-assigned region of the transistor fabric onto which a dedicated Hard R-Cell ARM966 can be placed. The Landing Zone region always is located next to a PLL and prediffused memories. The memories in turn are used to implement a microprocessor's caches or tightly coupled memories. The Landing Zone region is floorplanned onto these RapidChip platform ASICs such that there is a free region of greater than 150,000 usable gates for implementing system peripherals and preverified System CoreWare IP around the processor.

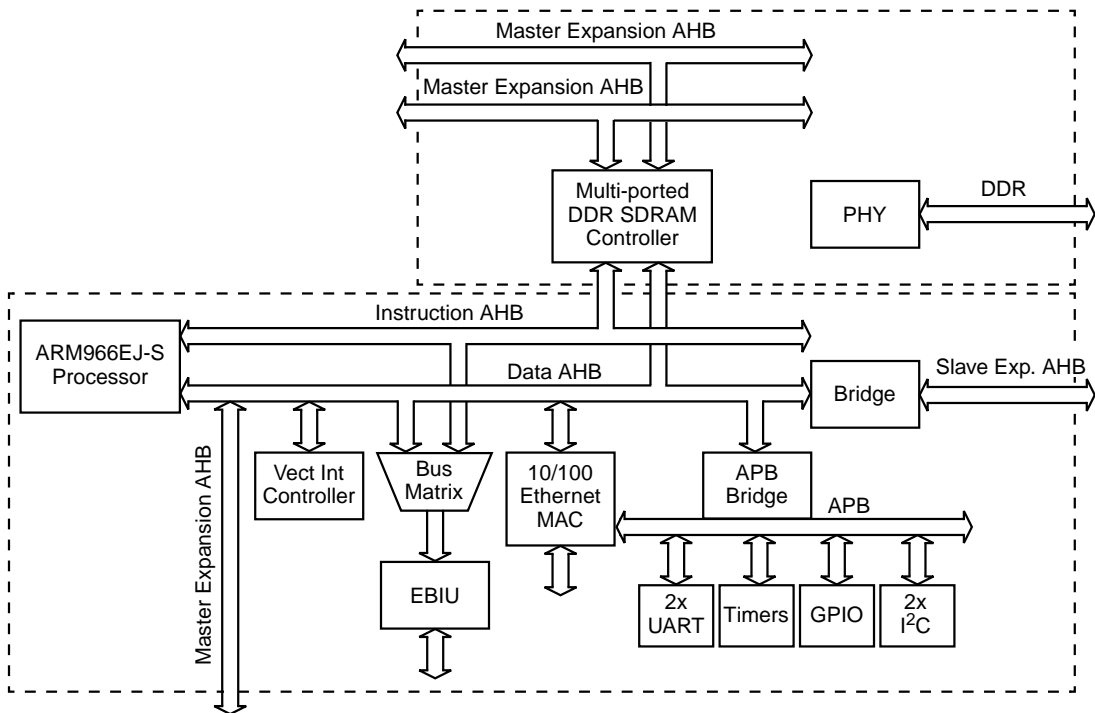
One main benefit of the Landing Zone implementations of processors is when a processor is not needed, you can recover all gates and memory from the Landing Zone region and re-use them for other purposes as required.

2.9.1 AMBA On-Chip Bus Architecture

LSI Logic's open processor architectures (ARM, MIPS, and ZSP) include native support for the AMBA bus protocol to simplify reuse of peripherals and to broaden access to leading third-party IP providers. To accelerate development and reduce design risk, LSI Logic provides you with completed, preverified System CoreWare IP containing the most popular peripherals used in embedded processor systems.

Figure 22 shows a reference configuration implementing the ARM966EJ-S processor within System CoreWare IP.

Figure 22 ARM966EJ-S Processor and System CoreWare IP with 4-Port DDR Controller



2.9.2 ARM966 Landing Zone Processor

The ARM966 microprocessor available on RapidChip Xtreme platform ASICs includes at least 32 Kbytes of tightly coupled instruction and data memories. It operates at up to 212.5 MHz and implements ARM

architecture version 5TEJ. This processor core supports the 32-bit ARM and 16-bit THUMB instruction sets and can execute 8-bit JAVA byte codes.

The ARM966 processor also includes support for external coprocessors.

In summary, the key features of the ARM966 implemented in the Landing Zone region are:

- Up to 212.5 MHz operation
- 32 Kbytes each Instruction and Data TCMs
- ARM Advanced High-performance Bus (AHB) interface unit with write buffer. Choice of 2:1 or 1:1 CPU-to-bus clock ratios for AHB operation

For further details on the ARM966 processor or any other processor, please either contact your LSI Logic representative or look on LSI Logic Web pages at <http://www.lsilogic.com/products/arm/index.html>

3 RapidChip Xtreme Platform ASIC Details

The RapidChip Xtreme platform ASIC family initially contains four slices, which have been designed to fit your needs in the Storage, Networking, Computing, and Communications markets.

The diffused high-speed SERDES cores in these devices can be used in conjunction with System CoreWare IP available from LSI Logic and also third-party IP providers, for example:

- XGXS 10G serial interface macros
- 10M/100M/1G/10G Ethernet MACs
- SGMII
- SFI-4/SPI4-2 interfaces
- PCI Express controllers
- Serial-RIO and Parallel-RIO interface controllers
- SATA / SAS controllers

Using these building blocks, you can quickly create bridges, switches, or routers for a wide variety of applications. You can benefit from the flexibility of the customizable slice while still achieving fast time to market and low unit cost.

The following sections outline the main features of the four initial RapidChip Xtreme platform ASICs.

3.1 RC11XT404

The RC11XT404 RapidChip Xtreme platform ASIC provides a basis for a wide range of differentiated designs, for example:

- I/O Controllers
SAS, SATA, Fibre Channel, iSCSI (TOE external)
- Bridges
 - Host side
Serial-RIO, InfiniBand, PCI-33, PCI-66, PCI-X 1.0, DMA
 - Fabric/Target
SATA, SAS, Fibre Channel, PCI Express, Serial-RIO

- Switches and Expanders
Serial-RIO, PCI Express, InfiniBand, SATA, SAS

3.1.1 Basic Features

This section summarizes the basic features of the RC11XT404:

- The RC11XT404 contains 3.7 million available gates, resulting in between 1.4 million and 2.1 million user-configurable logic gates depending on the architecture of the system.
- The maximum frequency for the user logic is 212.5 MHz.
- [Table 13](#) lists the types of diffused SRAM banks available on the RC11XT404 that can run at the specified maximum core frequency.

Table 13 RC11XT404 Diffused Memory Banks

RAM Type	Size	# Banks
2rw	256 x 38	16
2rw	1K X 38	8
1rw ¹	4k x 36	8
1rw	2k x 72	2

1. Available for use as Tightly Coupled Memory (TCM) for the ARM966 processor.

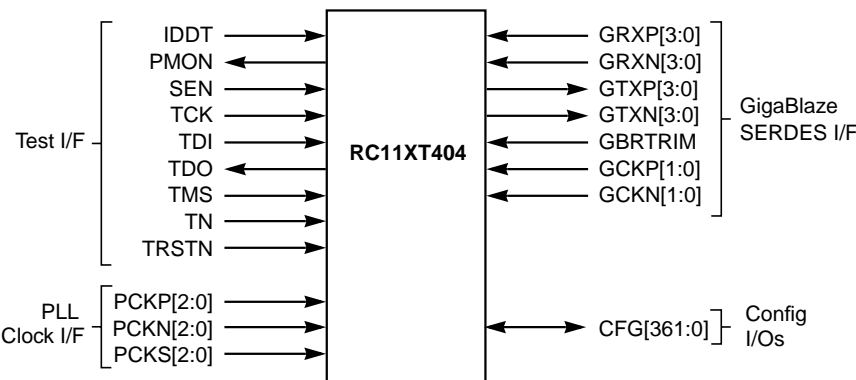
- The RC11XT404 contains a Landing Zone region for an ARM966 processor.
- The RC11XT404 can interface to PCI-X 100/133 using the configurable I/O on-chip.
- The RC11XT404 contains 362 Config I/O buffers.
- The RC11XT404 contains four x1 GigaBlaze SERDES cores.
- The RC11XT404 contains:
 - One wide-range 601250 PLL (see [page 26](#))
 - Two fixed-range 100500 PLLs (see [page 27](#))
- The RC11XT404 provides an IEEE 1149.1 JTAG interface, allowing manufacturing test, boundary scan, and access to BIST routines.

3.1.2 Signal Descriptions

This section describes the signals that comprise the RC11XT404 external interface. The descriptions are categorized according to the interface. The signal descriptions are listed alphabetically within the interface.

Figure 23 shows the logic diagram of the RC11XT404.

Figure 23 Logic Diagram for the RC11XT404



3.1.2.1 Config I/Os

This subsection describes the Configuration I/O interface.

CFG[361:0] User-Configurable I/Os Programmable
The RC11XT404 has 362 Config I/O signals.

3.1.2.2 GigaBlaze SERDES Interface

This subsection describes the GigaBlaze SERDES signals.

GBRTRIM GigaBlaze Termination Trimming Reference Input
Connecting this input V_{DD} through an external resistor (3 k Ω , 1%) provides a reference voltage for the internal Automatic Trimming circuit. When enabled, the Automatic Trimming circuit uses this reference voltage to adjust the termination impedance of the GigaBlaze receiver and transmitter.

GCKN[1:0] / GCKP[1:0]**GigaBlaze Transmit Clock Differential Pair** **Input**

These signals are the transmit clock differential-pair inputs.

GRXN[3:0] / GRXP[3:0]**GigaBlaze Receiver Differential Pair** **Input**

These signals are the high-speed differential-pair serial inputs for Channels 3 through 0.

GTXN[3:0] / GTXP[3:0]**GigaBlaze Transmit Differential Pair** **Output**

These signals are the high-speed differential-pair serial outputs for Channels 3 through 0.

3.1.2.3 PLL Clock Interface

This subsection describes the PLL clocks.

PCKN[2:0] / PCKP[2:0]**Differential-Pair PLL Clocks** **Input**

These inputs provide the differential-pair reference clocks for the three PLLs.

PCKS[2:0]**Single-Ended PLL Clocks** **Input**

These inputs are the single-ended reference clock inputs.

3.1.2.4 Test Interface

This subsection describes the signals that comprise the test interface.

IDDT**Power Down Enable** **Input**

This pin is for manufacturer's use only. Tie it to V_{SS} for normal operation.

PMON**Process Monitor** **Output**

This pin is for manufacturer's use only. It is a no connect on the board for normal operation.

SEN**Scan Chain Enable** **Input**

This pin is for manufacturer's use only. Tie it to V_{SS} for normal operation.

TCK**JTAG Test Clock** **Input**

Tie this pin to V_{SS} or the board's JTAG TCK, if one exists, for normal operation.

TDI	JTAG Test Data Tie this pin to V_{SS} or the board's JTAG TDI, if one exists, for normal operation.	Input
TDO	JTAG Test Data This pin is for manufacturer's use only. It either is a no connect on the board or is tied to the board's JTAG TDO, if one exists, for normal operation.	Output
TMS	JTAG Test Mode Enable Tie this pin to V_{SS} or the board's JTAG TMS, if one exists, for normal operation.	Input
TN	High-Impedance Stage Enable This pin is for manufacturer's use only. Tie it to V_{DD} for normal operation.	Input
TRSTN	JTAG Test Reset Tie this pin to V_{SS} or the board's JTAG TRSTN, if one exists, for normal operation.	Input

3.1.3 Packaging

The RC11XT404 is available in a BG672 enhanced ball grid array package (EPBGA-T). The package design is optimized to support the electrical performance requirements of single-ended, high-speed I/Os with a controlled impedance of 55 ohms. Multiple low-inductance V_{DD} I/O domains for the configurable I/O region is provided to enhance signal integrity.

GigaBlaze I/O routing is designed within its own V_{DD} domain ensuring optimal performance. All differential signals are routed together to minimize crosstalk and ensure a controlled impedance of 100 ohms.

Pad on I/O™ wire-bond interconnect is used to provide high I/O density and power/ground distribution similar to that of flip-chip designs. The package utilizes an embedded heat spreader, which provides enhanced thermal performance of the device and provides you with extended thermal management solutions at system level.

This package uses 1 mm pitch solder ball full array to maximize I/O count while reducing package body size. See [Section 5.3, "Thermal Design Considerations,"](#) for the thermal details and [Section A.4, "Package Mechanical Drawings,"](#) for the mechanical details of this package.

3.2 RC11XT416

The RC11XT416 RapidChip Xtreme platform ASIC provides a basis for a wide range of differentiated designs, for example:

- Host adapters, bridges, switches, power PC companion:
 - Host Side: PCI-X 1.0, PCI Express
 - Fabric Side: InfiniBand, PCI Express, Serial-RIO, Fibre Channel, 10G Ethernet
 - Target Side: Fibre Channel (up to 4G), SATA/SAS

3.2.1 Basic Features

This section summarizes the basic features of the RC11XT416:

- The RC11XT416 contains 5.7 million available gates, resulting in between 2.1 million and 3.3 million user-configurable logic gates depending on the architecture of the system.
- The maximum frequency for the user logic is 250 MHz.
- [Table 14](#) lists the types of diffused SRAM banks that can run at the specified maximum core frequency.

Table 14 RC11XT416 Diffused Memory Banks

RAM Type	Size	# Banks
2rw	256 x 38	16
2rw	512 x 38	12
2rw	512 x 76	16
1rw	4k x 36	4
1rw	2k x 72	2

- The RC11XT416 offers a Landing Zone region for an ARM966 processor with at least 32 Kbytes of tightly coupled instruction and data memory (TCM).
- The RC11XT416 can interface to PCI-X 100/133 using the configurable I/O on-chip.

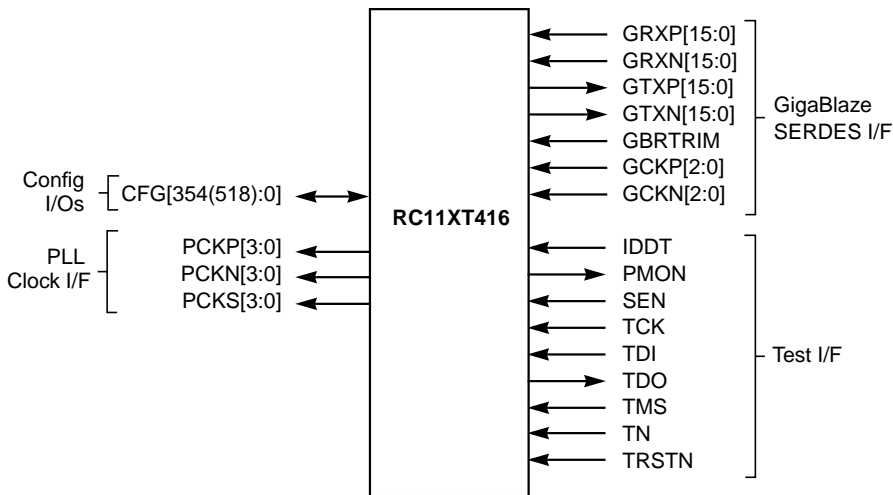
- The RC11XT416 is available in two different package options, and the total number of available configurable I/Os is dependent on that package:
 - 672-pin FCBGA - 355 Config I/Os
 - 896-pin FCBGA - 519 Config I/Os
- The RC11XT416 contains four x4 GigaBlaze cores, or a total of 16 GigaBlaze SERDES transceivers.
- The RC11XT416 contains:
 - One wide-range 601250 PLL (see [page 26](#))
 - Three fixed-range 100500 PLLs (see [page 27](#))
- The RC11XT416 provides an IEEE 1149.1 JTAG interface, allowing manufacturing test, boundary scan, and access to BIST routines.

3.2.2 Signal Descriptions

This section describes the signals that comprise the RC11XT416 external interface. The descriptions are categorized according to the interface. The signal descriptions are listed alphabetically within the interface.

[Figure 24](#) shows the RC11XT416 logic diagram.

Figure 24 Logic Diagram for the RC11XT416



3.2.2.1 Config I/Os

This subsection describes the Configuration I/O interface.

CFG[354(518):0]

User-Configurable I/Os

Programmable

The RC11XT416 has 519 Config I/O signals for the 896-pin FCBGA package and has 355 Config I/O signals for the 672-pin FCBGA package.

3.2.2.2 GigaBlaze SERDES Interface

This subsection describes the GigaBlaze SERDES signals.

GBRTRIM

GigaBlaze Termination Trimming Reference

Input

Connecting this input V_{DD} through an external resistor (3 k Ω , 1%) provides a reference voltage for the internal Automatic Trimming circuit. When enabled, the Automatic Trimming circuit uses this reference voltage to adjust the termination impedance of the GigaBlaze receiver and transmitter.

GCKN[2:0] / GCKP[2:0]

GigaBlaze Transmit Clock Differential Pair

Input

These signals are the transmit clock differential-pair inputs.

GRXN[15:0] / GRXP[15:0]

GigaBlaze Receiver Differential Pair

Input

These signals are the high-speed differential-pair serial inputs for Channels 15 through 0.

GTXN[15:0] / GTXP[15:0]

GigaBlaze Transmit Differential Pair

Output

These signals are the high-speed differential-pair serial outputs for Channels 15 through 0.

3.2.2.3 PLL Clock Interface

This subsection describes the PLL clocks.

PCKN[3:0] / PCKP[3:0]

Differential-Pair PLL Clocks

Input

These inputs provide the differential-pair reference clocks for the four PLLs.

PCKS[3:0]	Single-Ended PLL Clocks	Input
These inputs are the single-ended reference clock inputs.		

3.2.2.4 Test Interface

This subsection describes the signals that comprise the test interface.

IDDT	Power Down Enable	Input
This pin is for manufacturer's use only. Tie it to V_{SS} for normal operation.		

PMON	Process Monitor	Output
This pin is for manufacturer's use only. It is a no connect on the board for normal operation.		

SEN	Scan Chain Enable	Input
This pin is for manufacturer's use only. Tie it to V_{SS} for normal operation.		

TCK	JTAG Test Clock	Input
Tie this pin to V_{SS} or the board's JTAG TCK, if one exists, for normal operation.		

TDI	JTAG Test Data	Input
Tie this pin to V_{SS} or the board's JTAG TDI, if one exists, for normal operation.		

TDO	JTAG Test Data	Output
This pin is for manufacturer's use only. It either is a no connect on the board or is tied to the board's JTAG TDO, if one exists, for normal operation.		

TMS	JTAG Test Mode Enable	Input
Tie this pin to V_{SS} or the board's JTAG TMS, if one exists, for normal operation.		

TN	High-Impedance Stage Enable	Input
This pin is for manufacturer's use only. Tie it to V_{DD} for normal operation.		

TRSTN	JTAG Test Reset	Input
Tie this pin to V_{SS} or the board's JTAG TRSTN, if one exists, for normal operation.		

3.2.3 Packaging

The RC11XT416 is available in two different package options; the total number of available configurable I/Os is dependent on that package:

- 672-pin FCBGA - 355 Config I/Os
- 896-pin FCBGA - 519 Config I/Os

The FCBGA package utilizes an organic multi-layer strip line substrate that supports high-density interconnect and optimal electrical performance.

The package design is optimized to support the electrical performance requirements of single-ended, high-speed I/Os with a controlled impedance of 55 ohms. Multiple low-inductance V_{DD} I/O domains for the configurable I/O region are provided to enhance signal integrity.

GigaBlaze I/O routing is designed within its own V_{DD} domain, ensuring optimal performance. All differential signals are routed together to minimize crosstalk and ensure a controlled impedance of 100 ohms.

The package construction utilizes a copper heat spreader that directly connects to the die, resulting in an extremely low theta Jc of $\sim 0.5^{\circ}\text{C/W}$.

The package uses a 1 mm pitch solder ball full array to maximize I/O count while reducing package body size. See [Section 5.3, "Thermal Design Considerations,"](#) for the thermal details and [Section A.4, "Package Mechanical Drawings,"](#) for the mechanical details of this package.

3.3 RC11XT432

The RC11XT432 RapidChip Xtreme platform ASIC provides a basis for a wide range of differentiated designs, for example:

- Switching/Bridging Serial Architectures:
 - Serial-RIO
 - PCI Express
 - InfiniBand
 - 1G Ethernet
- Storage Expanders:

- SATA
- SAS
- Fibre Channel

3.3.1 Basic Features

This section summarizes the basic features of the RC11XT432:

- The RC11XT432 contains 4.8 million available gates, resulting in between 1.7 million and 2.7 million user-configurable logic gates depending on the architecture of the system.
- The maximum frequency for the user logic is 250 MHz.
- [Table 15](#) lists the types of diffused SRAM banks that can run at the specified maximum core frequency.

Table 15 RC11XT432 Diffused Memory Banks

Type	Size	# Banks
2rw	256 x 38	16
2rw	512 x 38	12
2rw	512 x 76	16
1rw	4k x 36	4
1rw	2k x 72	2

- The RC11XT432 offers a Landing Zone region for an ARM966 processor with at least 32 Kbytes each of tightly coupled instruction and data memory (TCM).
- The RC11XT432 can interface to PCI-X 100/133 using the configurable I/O on-chip.
- The RC11XT432 is available in two different package options, and the total number of configurable I/Os available is dependent on that package:
 - 672-pin FCBGA - 259 Config I/Os
 - 896-pin FCBGA - 427 Config I/Os
- The RC11XT432 contains eight x4 GigaBlaze SERDES cores, that is, 32 GigaBlaze channels.
- The RC11XT432 contains:

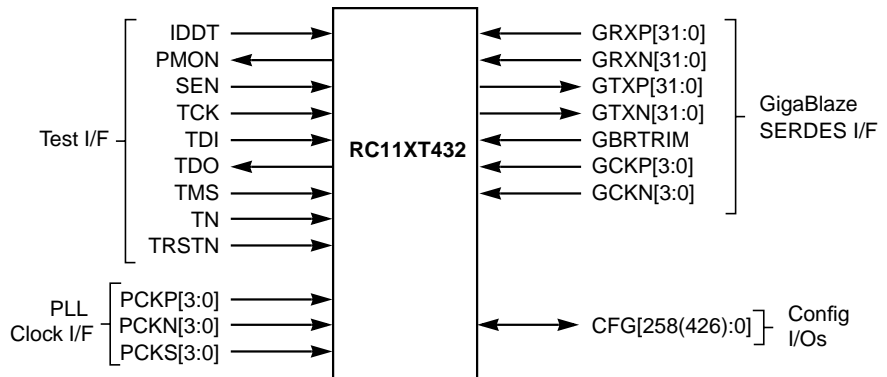
- One wide-range 601250 PLL (see [page 26](#))
- Three fixed range 100500 PLLs (see [page 27](#))
- The RC11XT432 provides an IEEE 1149.1 JTAG interface, allowing manufacturing test, boundary scan, and access to BIST routines.

3.3.2 Signal Descriptions

This section describes the signals that comprise the RC11XT432 external interface. The descriptions are categorized according to the interface. The signal descriptions are listed alphabetically within the interface.

[Figure 25](#) shows the RC11XT432 logic diagram.

Figure 25 Logic Diagram for the RC11XT432



3.3.2.1 Config I/Os

This subsection describes the Configuration I/O interface.

CFG[258(426):0]

User-Configurable I/Os

Programmable

The RC11XT432 has 259 Config I/O signals for the 672-pin package; it has 427 Config I/O signals for the 896-pin package.

3.3.2.2 GigaBlaze SERDES Interface

This subsection describes the GigaBlaze SERDES signals.

GBRTRIM	GigaBlaze Termination Trimming Reference	Input
	Connecting this input V_{DD} through an external resistor (3 k Ω , 1%) provides a reference voltage for the internal Automatic Trimming circuit. When enabled, the Automatic Trimming circuit uses this reference voltage to adjust the termination impedance of the GigaBlaze receiver and transmitter.	
GCKN[3:0] / GCKP[3:0]	GigaBlaze Transmit Clock Differential Pair	Input
	These signals are the transmit clock differential-pair inputs.	
GRXN[31:0] / GRXP[31:0]	GigaBlaze Receiver Differential Pair	Input
	These signals are the high-speed differential-pair serial inputs for Channels 31 through 0.	
GTXN[31:0] / GTXP[31:0]	GigaBlaze Transmit Differential Pair	Output
	These signals are the high-speed differential-pair serial outputs for Channels 31 through 0.	
RSVD[3:0]	Reserved	Input
	These signals are LSI Logic reserved pins. Drive these inputs LOW for normal operation.	

3.3.2.3 PLL Clock Interface

This subsection describes the PLL clocks.

PCKN[3:0] / PCKP[3:0]	Differential-Pair PLL Clocks	Input
	These inputs provide the differential-pair reference clocks for the four PLLs.	
PCKS[3:0]	Single-Ended PLL Clocks	Input
	These inputs are the single-ended reference clock inputs.	

3.3.2.4 Test Interface

This subsection describes the signals that comprise the test interface.

IDDT	Power Down Enable	Input
	This pin is for manufacturer's use only. Tie it to V_{SS} for normal operation.	

PMON	Process Monitor This pin is for manufacturer's use only. It is a no connect on the board for normal operation.	Output
SEN	Scan Chain Enable This pin is for manufacturer's use only. Tie it to V_{SS} for normal operation.	Input
TCK	JTAG Test Clock Tie this pin to V_{SS} or the board's JTAG TCK, if one exists, for normal operation.	Input
TDI	JTAG Test Data Tie this pin to V_{SS} or the board's JTAG TDI, if one exists, for normal operation.	Input
TDO	JTAG Test Data This pin is for manufacturer's use only. It either is a no connect on the board or is tied to the board's JTAG TDO, if one exists, for normal operation.	Output
TMS	JTAG Test Mode Enable Tie this pin to V_{SS} or the board's JTAG TMS, if one exists, for normal operation.	Input
TN	High-Impedance Stage Enable This pin is for manufacturer's use only. Tie it to V_{DD} for normal operation.	Input
TRSTN	JTAG Test Reset Tie this pin to V_{SS} or the board's JTAG TRSTN, if one exists, for normal operation.	Input

3.3.3 Packaging

The RC11XT432 is available in two different package options; the total number of available configurable I/Os is dependent on that package:

- 672-pin FCBGA - 259 Config I/Os
- 896-pin FCBGA - 427 Config I/Os

The FCBGA package utilizes an organic multi-layer strip line substrate that supports high-density interconnect and optimal electrical performance.

The package design is optimized to support the electrical performance requirements of single-ended, high-speed I/Os with controlled impedance of 55 ohms. Multiple low-inductance V_{DD} I/O domains for the configurable I/O region are provided to enhance signal integrity.

GigaBlaze I/O routing is designed within its own V_{DD} domain, ensuring optimal performance. All differential signals are routed together to minimize crosstalk and ensure a controlled impedance of 100 ohms.

The package construction utilizes a copper heat spreader that directly connects to the die, resulting in an extremely low theta Jc of $\sim 0.5^{\circ}\text{C/W}$.

The package uses a 1 mm pitch solder ball full array to maximize I/O count while reducing package body size. See [Section 5.3, “Thermal Design Considerations,”](#) for the thermal details and [Section A.4, “Package Mechanical Drawings,”](#) for the mechanical details of this package.

3.4 RC11XT531

The RC11XT531 RapidChip Xtreme platform ASIC provides a basis for a wide range of differentiated designs, for example:

- 1G/10G Ethernet switch
- Core or edge router
- Backplane interface
- 10G Ethernet controller
- Fibre Channel switch controller
- SPI4-2 to SATA or SAS switch controller

3.4.1 Basic Features

This section summarizes the basic features of the RC11XT531:

- The RC11XT531 contains 5.2 million available gates, which results in between 1.8 million and 2.8 million user-configurable logic gates depending on the architecture of the system.
- The maximum frequency for the user logic is 250 MHz.

- [Table 16](#) lists the two types of diffused SRAM banks that can run at the specified maximum core frequency.

Table 16 RC11XT531 Diffused Memory Banks

RAM Type	Size	# Banks
2rw	256 x 36	36
1r1w	1K X 36	36

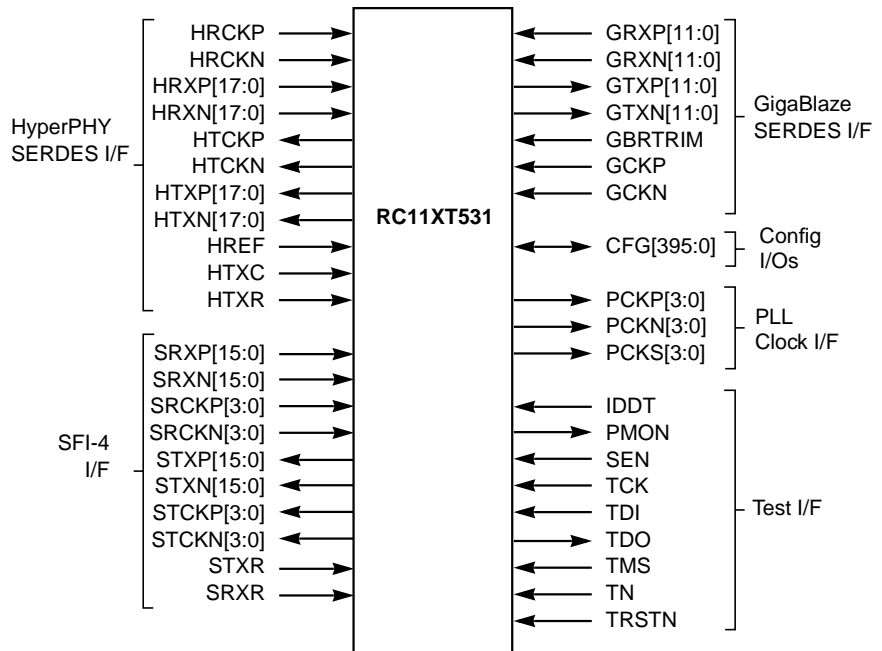
- The RC11XT531 has a maximum of 396 Config I/O signals. When the SFI-4 interface is implemented, it uses 82 of these Config I/O signals.
- The RC11XT531 contains three x4 GigaBlaze SERDES cores (12 channels), 18 HyperPHY channels, and 16 SFI-4 PHY channels.
- The RC11XT531 contains four wide-range 601250 PLLs (see [page 26](#))
- The RC11XT531 provides an IEEE 1149.1 JTAG interface, allowing manufacturing test, boundary scan, and access to BIST routines.

3.4.2 Signal Descriptions

This section describes the signals that comprise the RC11XT531 external interface. The descriptions are categorized according to the interface. The signal descriptions are listed alphabetically within the interface.

[Figure 26](#) shows the RC11XT531 logic diagram.

Figure 26 Logic Diagram for the RC11XT531



3.4.2.1 Config I/Os

This subsection describes the Configuration I/O interface.

CFG[395:0] User-Configurable I/Os Programmable
The RC11XT531 has 396 Config I/O signals.

3.4.2.2 GigaBlaze SERDES Interface

This subsection describes the GigaBlaze SERDES signals.

GBRTRIM GigaBlaze Termination Trimming Reference Input
Connecting this input V_{DD} through an external resistor (3 k Ω , 1%) provides a reference voltage for the internal Automatic Trimming circuit. When enabled, the Automatic Trimming circuit uses this reference voltage to adjust the termination impedance of the GigaBlaze receiver and transmitter.

GCKN / GCKP

GigaBlaze Transmit Clock Differential Pair **Input**
This signal pair is the transmit clock differential-pair input.

GRXN[11:0] / GRXP[11:0]

GigaBlaze Receiver Differential Pair **Input**
These signals are the high-speed differential-pair serial inputs for Channels 11 through 0.

GTXN[11:0] / GTXP[11:0]

GigaBlaze Transmit Differential Pair **Output**
These signals are the high-speed differential-pair serial outputs for Channels 11 through 0.

3.4.2.3 HyperPHY SERDES Interface

This subsection describes the HyperPHY SERDES signals.

HRCKN / HRCKP

HyperPHY Differential Pair Receive Clock **Input**
This signal pair is the receive data clock.

HREF

HyperPHY LVDS Bias Cell Reference **Input**
This input is the 1.025 V reference required for diffused HyperPHY LVDS buffers.

HRXN[17:0] / HRXP[17:0]

HyperPHY Receiver Differential Pairs **Input**
These signals are the high-speed, differential-pair serial inputs for the receiver.

HTCKN / HTCKP

HyperPHY Differential-Pair Transmit Clock **Output**
This signal pair is the transmit data clock.

HTXC

HyperPHY LVDS Buffer CTAP **Input**
This input is the center tap for setting the DC common mode level. For AC coupling, set this input to 1.025 V. For DC coupling, leave this input floating.

HTXN[17:0] / HTXP[17:0]

HyperPHY Transmitter Differential Pairs **Output**
These signals are the high-speed, differential-pair serial outputs for the transmitter.

HTXR	HyperPHY PLL Voltage Regulator 1.2V Reference	Input
	This input is the 1.025 V reference required for diffused HyperPHY LVDS buffers.	

3.4.2.4 PLL Clock Interface

This subsection describes the PLL clocks.

PCKN[3:0] / PCKP[3:0]	Differential-Pair PLL Clocks	Input
	These inputs provide the differential-pair reference clocks for the four PLLs.	

PCKS[3:0]	Single-Ended PLL Clocks	Input
	These inputs are the single-ended reference clock inputs.	

3.4.2.5 SFI-4 Interface

This subsection describes the SFI-4 signals.

SRCKN[3:0] / SRCKP[3:0]	SFI-4 Differential-Pair Receive Clocks	Input
	These signal pairs are the receive data clocks.	

SRXN[15:0] / SRXP[15:0]	SFI-4 Differential-Pair Receive Data	Input
	These signals are the high-speed, differential-pair serial inputs for the receiver.	

SRXR	SFI-4 RX LVDS Reference	Input
	This signal is the 1.025 V voltage reference input required for LVDS I/Os used on the RX SFI-4 interface.	

STCKN[3:0] / STCKP[3:0]	SFI-4 Differential-Pair Transmit Clocks	Output
	These signal pairs are the transmit data clocks.	

STXN[15:0] / STXP[15:0]	SFI-4 Differential-Pair Transmit Data Bus	Output
	These signals are the differential-pair serial outputs for the transmitter.	

STXR	SFI-4 TX LVDS Reference	Input
	This signal is the 1.025 V \pm 5% voltage reference input required for LVDS I/Os used on the TX SFI-4 interface.	

3.4.2.6 Test Interface

This subsection describes the signals that comprise the test interface.

IDDT	Power Down Enable This pin is for manufacturer's use only. Tie it to V_{SS} for normal operation.	Input
PMON	Process Monitor This pin is for manufacturer's use only. It is a no connect on the board for normal operation.	Output
SEN	Scan Chain Enable This pin is for manufacturer's use only. Tie it to V_{SS} for normal operation.	Input
TCK	JTAG Test Clock Tie this pin to V_{SS} or the board's JTAG TCK, if one exists, for normal operation.	Input
TDI	JTAG Test Data Tie this pin to V_{SS} or the board's JTAG TDI, if one exists, for normal operation.	Input
TDO	JTAG Test Data This pin is for manufacturer's use only. It either is a no connect on the board or is tied to the board's JTAG TDO, if one exists, for normal operation.	Output
TMS	JTAG Test Mode Enable Tie this pin to V_{SS} or the board's JTAG TMS, if one exists, for normal operation.	Input
TN	High-Impedance Stage Enable This pin is for manufacturer's use only. Tie it to V_{DD} for normal operation.	Input
TRSTN	JTAG Test Reset Tie this pin to V_{SS} or the board's JTAG TRSTN, if one exists, for normal operation.	Input

3.4.3 Packaging

The RC11XT531 is available in an FC896 flip-chip ball grid array package (FCBGA). The FCBGA package utilizes an organic multi-layer

strip line substrate that supports high-density interconnect and optimal electrical performance.

The package design is optimized to support the electrical performance requirements of single-ended, high-speed I/Os with a controlled impedance of 55 ohms. Multiple low-inductance V_{DD} I/O domains for the configurable I/O region is provided to enhance signal integrity.

GigaBlaze I/O routing is designed within its own V_{DD} domain, ensuring optimal performance. All differential signals are routed together to minimize crosstalk and ensure a controlled impedance of 100 ohms.

The package construction utilizes a copper heat spreader that directly connects to the die, resulting in an extremely low theta Jc of $\sim 0.5^{\circ}\text{C/W}$.

The package uses a 1 mm pitch solder ball full array to maximize I/O count while reducing package body size. See [Section 5.3, “Thermal Design Considerations,”](#) for the thermal details and [Section A.4, “Package Mechanical Drawings,”](#) for the mechanical details of this package.

4 Specifications

This section specifies the electrical characteristics and AC timing for the RapidChip Xtreme platform ASIC family. This section includes the following subsections:

- [Section 4.1, “VDD Terminology”](#)
- [Section 4.2, “Absolute Maximum Ratings”](#)
- [Section 4.3, “Recommended Operating Conditions”](#)
- [Section 4.4, “SSTL2 Buffer”](#)
- [Section 4.5, “HSTL Buffers”](#)
- [Section 4.6, “2.5 V LVDS Buffers”](#)
- [Section 4.7, “3.3 V LVDS Buffers”](#)
- [Section 4.8, “PECL Buffer”](#)
- [Section 4.9, “PCI/PCI-X Buffer”](#)
- [Section 4.10, “2.5 V Controlled Impedance Buffers”](#)

- [Section 4.11, “3.3 V Controlled Impedance Buffers”](#)
- [Section 4.12, “1.8 V LVTTTL/LVCMOS Buffers”](#)
- [Section 4.13, “2.5 V LVTTTL/LVCMOS Buffers”](#)
- [Section 4.14, “3.3 V LVTTTL/LVCMOS Buffers”](#)

The *Preliminary Gflx-r RapidChip Cell Technology Databook* (DB04-000094-03) has additional information about the RapidChip platform ASIC I/O buffers that are described in this section.

4.1 VDD Terminology

[Table 17](#) compares the VDD terms used by the RapidChip Xtreme platform ASIC family with their corresponding generic VDD terms. The generic terms are used in [Table 18, Absolute Maximum Ratings](#), and [Table 19, Recommended Operating Conditions](#).

Table 17 Cross Reference of VDD Terms for RapidChip Xtreme Family

RapidChip Xtreme VDD Name	Equivalent Generic VDD Name	Description
VDDG	VDD12	GigaBlaze Analog VDD Plane
VDDGCK	VDD33	GigaBlaze 3.3V PECL Reference Clock VDD Plane
VDDR	VDDIO	Config I/O Specific VDD Plane
VDDP	VDD12	PLL VDD Plane
VDDS	VDD18	HyperPHY I/O VDD Plane
VDDH	VDD12	HyperPHY Hardmac VDD Plane
VDDHRX	VDD12	HyperPHY RX PLL VDD Plane
VDDHTX	VDD12	HyperPHY TX PLL VDD Plane

4.2 Absolute Maximum Ratings

Table 18 lists the absolute maximum ratings for the RapidChip Xtreme platform ASIC family. Permanent damage is likely to occur for operation beyond the ratings listed in this table.

Table 18 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V _{DD}	Core Supply Voltage	-0.3	2.0	V
V _{DD12}	1.2 V I/O Supply Voltage	-0.3	2.0	V
V _{DD15}	1.5 V I/O Supply Voltage	-0.3	2.0	V
V _{DD18}	1.8 V I/O Supply Voltage	-0.3	2.0	V
V _{DD25}	2.5 V I/O Supply Voltage	-0.3	3.96	V
V _{DD33}	3.3 V I/O Supply Voltage	-0.3	3.96	V
V _{IO}	I/O Voltage	-0.6	V _{DDIO} + 0.5 ¹	V
T _{STG}	Storage Temperature	-55	+150	°C

1. V_{DDIO} refers to the nominal I/O supply voltage for that type I/O. For example, the maximum I/O voltage for an I/O buffer operating at 3.3 V must be equal to or less than 3.3 V + 0.5 V.

4.3 Recommended Operating Conditions

Table 19 lists the recommended operating conditions for the RapidChip Xtreme platform ASIC family. Operation beyond these limits can impair the useful life of the device.

Table 19 Recommended Operating Conditions¹

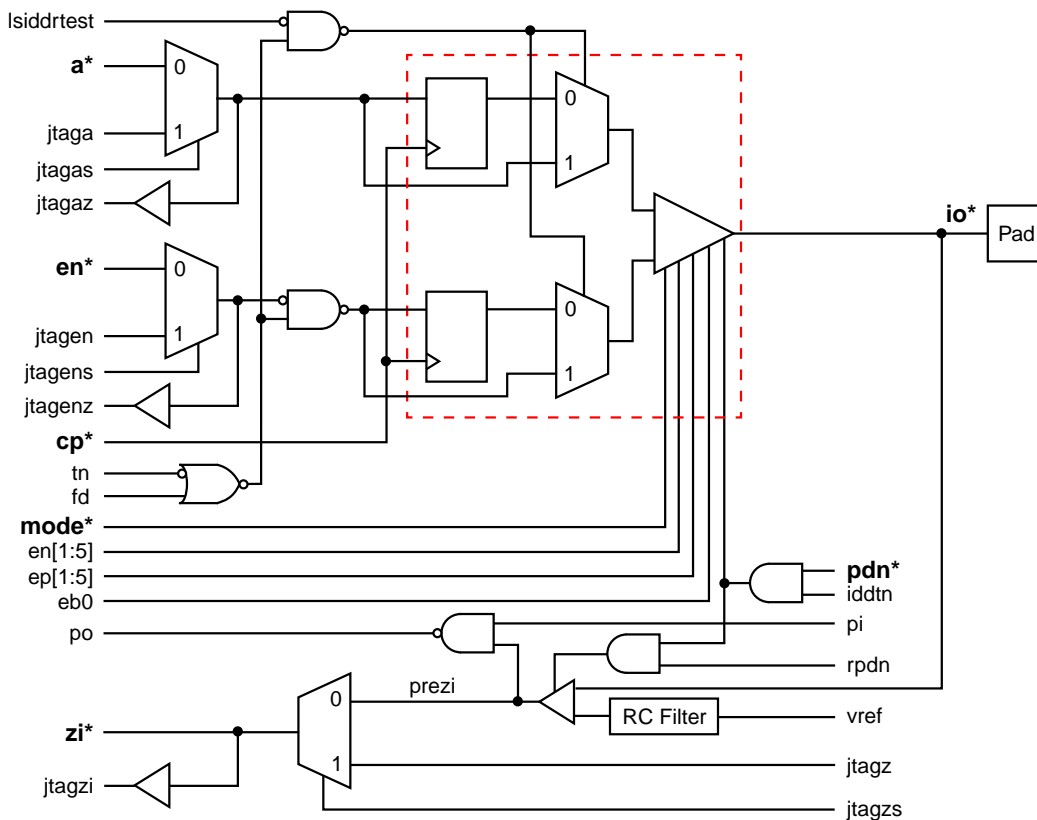
Symbol	Parameter	Min	Typ	Max	Units
V _{DD}	Core Supply Voltage	1.14	1.20	1.26	V
V _{DD12}	1.2 V I/O Supply Voltage	1.14	1.20	1.26	V
V _{DD15}	1.5 V I/O Supply Voltage	1.43	1.50	1.58	V
V _{DD18}	1.8 V I/O Supply Voltage	1.71	1.80	1.89	V
V _{DD25}	2.5 V I/O Supply Voltage	2.38	2.50	2.63	V
V _{DD33}	3.3 V I/O Supply Voltage	3.14	3.30	3.47	V
T _A	Ambient Temperature	0	25	70	°C
T _J	Junction Temperature	0	-	115	°C

1. For normal device operation, adhere to the limits in this table. Device functionality to stated DC and AC operation is not guaranteed if conditions exceed recommended operating conditions.

4.4 SSTL2 Buffer

The SSTL2 buffer (bdzsstli9i16ddrjls25rc) is a 2.5 V, impedance controlled, bidirectional buffer that complies with the JEDEC SSTL2 standard (EIA/JESD8-9). The SSTL2 buffer is created from a single configurable I/O slot, and its output drive strength is electrically programmable. The SSTL2 buffer is intended to be used in Double Data Rate (DDR) applications. It supports a data frequency of up to 200 MHz (400 Mbits/s) for multi-drop topologies and up to 266 MHz (533 Mbits/s) for point-to-point topologies. Figure 27 is a block diagram of the SSTL2 buffer.

Figure 27 SSTL2 Buffer Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type. Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 20 lists the SSTL2 buffer DC characteristics.

Table 20 SSTL2 Buffer DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DDIO}^1	I/O Supply Voltage: DDR200/266/333 Multi-Drop, 533 Mb/s point-to-point	2.3	2.5	2.7	V	$\pm 8\%$
V_{DDIO}^1	I/O Supply Voltage: DDR400 Multi-Drop	2.5	2.6	2.7	V	$\pm 3.8\%$
V_{REF}^2	Reference Voltage	$0.49 \cdot V_{DDIO}$	$0.50 \cdot V_{DDIO}$	$0.51 \cdot V_{DDIO}$	V	-
V_{TT}^2	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	-
I_{OZL}^3	3-state Output LOW Current	–	–	+10	μA	$V_{IO} = V_{SS}$
I_{OZH}^4	3-state Output HIGH Current	–	–	-10	μA	$V_{IO} = V_{DDIO}$
$V_{IL(DC)}$	Receiver Input LOW Voltage	$V_{SS} - 0.3$	–	$V_{REF} - 0.15$	V	-
$V_{IH(DC)}$	Receiver Input HIGH Voltage	$V_{REF} + 0.15$	–	$V_{DDIO} + 0.3$	V	-
R_{IMPM1}^5	Driver Output Impedance, Mode=1	18	21	24	Ω	$\pm 3 \Omega$
R_{IMPM0}^4	Driver Output Impedance, Mode=0	30	33	36	Ω	$\pm 3 \Omega$

1. Equivalent to JEDEC V_{DDQ} .
2. V_{TT} and V_{REF} must track V_{DDIO} . Use same V_{DDIO} for RX and TX to guarantee tracking.
3. Equivalent to I_{IL} for bidirectional I/O.
4. Equivalent to I_{IH} for bidirectional I/O.
5. Measured at $V_{OUT} = V_{DDIO}/2$ point from the driver output I/V characteristics.

Table 21 lists the SSTL2 buffer AC characteristics.

Table 21 SSTL2 Buffer AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$V_{IL(AC)}$	Receiver Input LOW Voltage	–	–	$V_{REF} - 0.31$	V
$V_{IH(AC)}$	Receiver Input HIGH Voltage	$V_{REF} + 0.31$	–	–	V
t_{SRR}^1	Driver Output Rise Slew Rate	1.0	–	4.5	V/ns
t_{SRF}	Driver Output Fall Slew Rate	1.0	–	4.5	V/ns

1. Measured at the package pin when the output crosses $V_{REF} \pm 0.310$ V.

Table 22 lists the SSTL2 buffer driver timing characteristics.

Table 22 SSTL2 Driver Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DR_{PP}^1	Data Rate: Point-to-Point	200	-	533	Mbits/s	-
DR_{MD400}^1	Data Rate: Multi-Drop 400	200	-	400	Mbits/s	-
DR_{MD333}^1	Data Rate: Multi-Drop 333	200	-	333	Mbits/s	-
$t_{PD LH_cp_io}$	Propagation Delay LOW to HIGH	-	-	3.0	ns	-
$t_{PD HL_cp_io}$	Propagation Delay HIGH to LOW	-	-	3.0	ns	-
$t_{S_a_cp1}^2$	Setup Time	-	-	0.8	ns	-
$t_{S_en_cp1}^2$	Setup Time	-	-	0.8	ns	-
$t_{H_a_cp1}^2$	Hold Time	-	-	0.0	ns	-
$t_{H_en_cp1}^2$	Hold Time	-	-	0.0	ns	-
$t_{PD LH_a_io}$	Propagation Delay LOW to HIGH	-	-	10.0	ns	LSIDDR TEST=1
$t_{PD HL_a_io}$	Propagation Delay HIGH to LOW	-	-	10.0	ns	LSIDDR TEST=1
$t_{PD_en_io}$	Propagation Delay	-	-	10.0	ns	LSIDDR TEST=1

1. The SSTL2 buffer is targeted at DDR memory applications. Therefore, data frequency, not clock frequency, is the key specification. For example, a 533 Mbits/s data rate is equivalent to a 267 MHz clock frequency in a DDR application because there are two data bits in each 3.76 ns period. The maximum data frequency depends on the application and system environment (loading).
2. Setup and hold times are measured using a clock with a 50% duty cycle and the worst case ramp time (200 ps). The ramp time is measured at the 0% and the 100% points on the waveform.

Figure 28 shows the SSTL2 buffer driver timing waveforms.

Figure 28 SSTL Driver Timing Waveforms

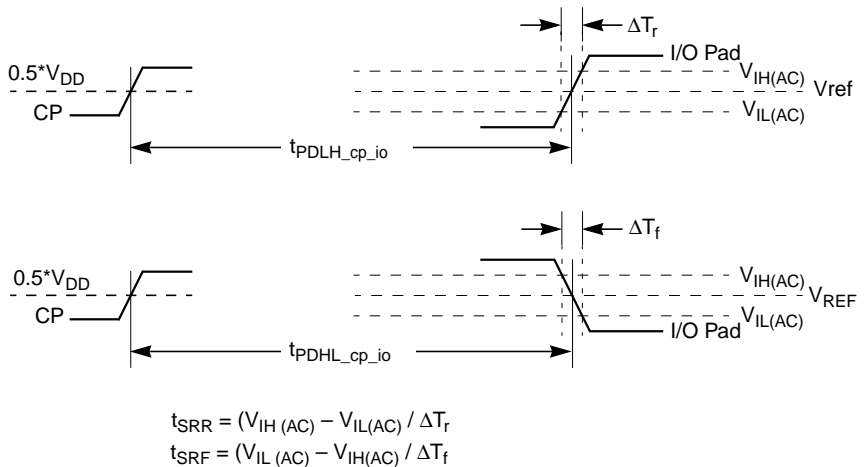


Table 23 lists the SSTL2 buffer receiver timing characteristics.

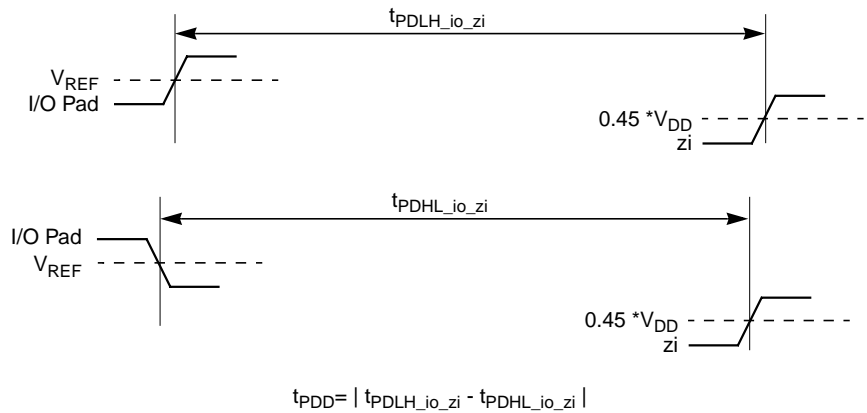
Table 23 SSTL2 Receiver Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
DR ^{1,2}	Data Rate	200	—	533	Mbits/s	V _{REF} tracking V _{DDIO}
t _{PDLH_io_zi} ²	Propagation Delay LOW to HIGH	—	—	1.0	ns	V _{REF} tracking V _{DDIO}
				1.5	ns	V _{REF} not tracking V _{DDIO}
t _{PDHL_io_zi} ²	Propagation Delay HIGH to LOW	—	—	1.0	ns	V _{REF} tracking V _{DDIO}
				1.5	ns	V _{REF} not tracking V _{DDIO}
t _{PDD} ² (P2P)	Receiver Delta Propagation Delay	—	—	100	ps	V _{REF} tracking V _{DDIO}
				300	ps	V _{REF} not tracking V _{DDIO}
t _{PU_zi}	Receiver Wake Up Timing	—	—	7.5	ns	zi starts toggle after RPDN deasserted
t _{PD_zi}	Receiver Power Down Timing	—	—	6.0	ns	zi goes to power down state (logic 0) after RPDN asserted

1. The SSTL2 buffer is targeted at DDR memory applications. Therefore, data frequency, not clock frequency, is the key specification. For example, a 533 Mbits/s data rate is equivalent to a 267 MHz clock frequency in a DDR application because there are two data bits in each 3.76 ns period. The maximum data frequency depends on the application and system environment (loading).
2. A timing penalty is incurred when V_{REF} does not track V_{DDIO}.

Figure 29 shows the SSTL2 buffer receiver timing waveforms.

Figure 29 SSTL2 Receiver Timing Waveforms



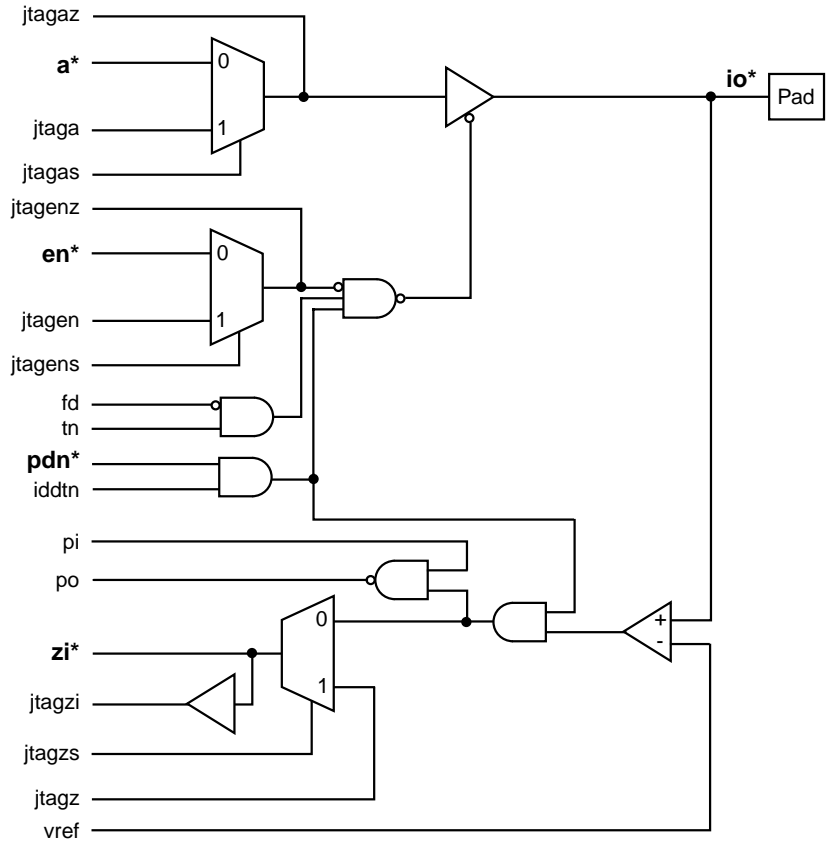
Note: $0.45 * V_{DD}$ switching threshold is used for all receiver timing measurements related to zi.

4.5 HSTL Buffers

The HSTL bidirectional buffers (bdhstl1jls15rc, bdhstl2jls15rc) are used for high-speed processor-to-memory and chip-to-chip interfaces. Both buffers consist of an input receiver cell and an output driver cell that are created from a single configurable I/O slot. Both buffers have a low-voltage (~ 0.3 V) swing above and below a reference voltage (~ 0.75 V).

The bdhstl1jls15rc is a Class-I buffer intended for unterminated interconnect structures, lumped-capacitance interconnect systems, and symmetrically terminated interconnect systems. The bdhstl2jls15rc is a Class-II buffer intended for externally source series terminated or symmetrically double parallel terminated interconnect structures. The two HSTL buffers differ only in drive strength. Figure 30 is a block diagram of the Class-I HSTL buffer.

Figure 30 HSTL Buffer Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type.
 Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 24 lists the HSTL buffers AC and DC electrical characteristics.

Table 24 HSTL Buffer AC/DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DDIO}	I/O Supply Voltage	1.35	1.5	1.65	V	-
$V_{REF} = 1/2 V_{DDIO}^{1,2}$	Reference Voltage	0.675	0.75	0.825	V	-
$V_{IH(DC)}^3$	Receiver Static Input HIGH Voltage	$V_{REF} + 0.10$	—	$V_{DDIO} + 0.3$	V	-
$V_{IL(DC)}^3$	Receiver Static Input LOW Voltage	-0.30	—	$V_{REF} - 0.10$	V	-
$V_{IH(AC)}^3$	Receiver Dynamic Input HIGH Voltage	$V_{REF} + 0.20$	—	—	V	-
$V_{IL(AC)}^3$	Receiver Dynamic Input LOW Voltage	—	—	$V_{REF} - 0.20$	V	-
$I_{OL(DC)}$	Output LOW Current	-8 (Class I)	—	—	mA	$V_{OL} \text{ (max)} = 0.4$
$I_{OH(DC)}$	Static Output HIGH Current	8 (Class I)	—	—	mA	$V_{OH} \text{ (min)} = V_{DDIO} - 0.4$
$I_{OL(DC)}$	Output LOW Current	-16 (Class II)	—	—	mA	$V_{OL} \text{ (max)} = 0.4$
$I_{OH(DC)}$	Output HIGH Current	16 (Class II)	—	—	mA	$V_{OH} \text{ (min)} = V_{DDIO} - 0.4$

1. For best noise margins, V_{REF} of RX should track TX V_{DDIO} . Select the value of V_{REF} that provides the optimum noise margin for your conditions.
2. Peak-to-peak noise on V_{REF} must not exceed 2% V_{REF} .
3. The AC values are chosen to indicate the levels at which the receiver must meet its timing specifications. The DC values are chosen such that the final logic state is unambiguously defined. The reason for this approach is that many input waveforms include a certain amount of ringing. You can be sure that the device will switch state a certain amount of time after the input has crossed AC threshold and not switch back as long as the input stays beyond the DC threshold.

Figure 31 shows the relationship between the parameters listed in Table 24.

Figure 31 Ring Back Switching Diagram

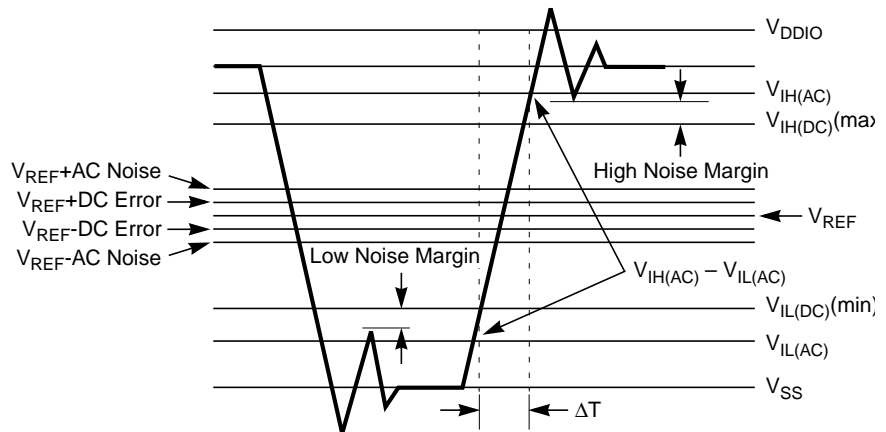


Table 25 lists the HSTL driver timing characteristics.

Table 25 HSTL Driver Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{DATA}	Data Frequency	—	—	266	MHz	—
DC ^{1,2,3}	Driver Duty Cycle	46	50	54	%	$t_{\text{DPD}} = 150 \text{ ps}$
$t_{\text{PDD}}^{2,3,4}$	Driver Delta Propagation Delay	—	—	150	ps	@ 266 MHz
t_{PD1}^2	Class-I Driver Propagation Delay	—	—	2.5	ns	@ 266 MHz
$t_{\text{PD2}}^{2,3}$	Class-II Driver Propagation Delay	—	—	2.3	ns	@ 266 MHz

1. Output driver timing characteristics are measured at the I/O pin.

2. Duty Cycle [%] = $[(\text{PWH} / T_{\text{PERIOD}}) * 100]$.

3. Input Ramp time = 150 ps.

4. Delta Propagation Delay (t_{PDD}) = $|t_{\text{PDLH_a_io}} - t_{\text{PDHL_a_io}}|$ = absolute value of maximum delay mismatch.

Timing characteristics apply to any of these load conditions:

- 10 pF load only
- Or, series terminated (25 Ω resistor, through a 50 Ω T-line) with a 10 pF load at far end
- Or, double parallel terminated (50 Ω T-line with both near and far end 50 Ω termination to VTT), with a 10 pF load at far end

Table 26 lists the HSTL receiver timing characteristics.

Table 26 HSTL Receiver Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{DATA}	Data Frequency	–	–	266	MHz	–
DC ^{1,2,3}	Input Receiver Duty Cycle	46	50	54	%	$t_{\text{PDD}} = 150 \text{ ps}$ @ 266 MHz
$t_{\text{PDD}}^{2,4,5}$	Input Receiver Delta Propagation Delay	–	–	150	ps	@ 266 MHz
$t_{\text{PD}}^{2,4,5}$	Input Receiver Propagation Delay	–	–	1.2	ns	@ 266 MHz

1. Duty Cycle [%] = $[(\text{PWH} / T_{\text{PERIOD}}) * 100]$.
2. Receiver timing characteristics are measured from the I/O pad (not the package pin) to the zi pin.
3. Input ramp time is 1 V/ns, and input swing for timing is $\pm 500 \text{ mV}$ around V_{REF} .
4. Loading characteristics on the zi pin for this measurements is 80 pF (approximately 16 standard loads).
5. Delta Propagation Delay (t_{PDD}) = $|t_{\text{PDLH_io_zi}} - t_{\text{PDHL_io_zi}}|$ absolute value of maximum delay mismatch.

Figure 32 shows the HSTL receiver timing waveforms.

Figure 32 HSTL Receiver Timing Waveforms

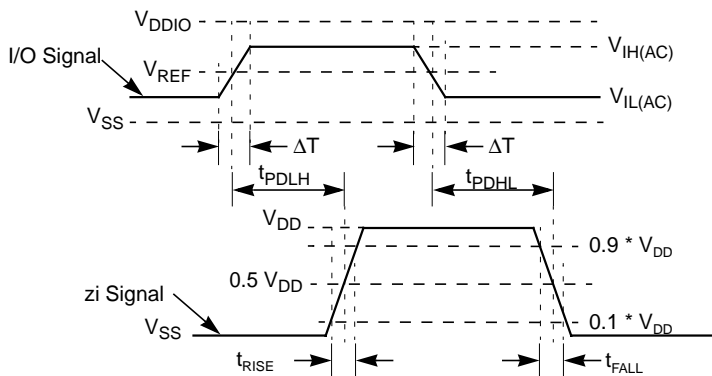
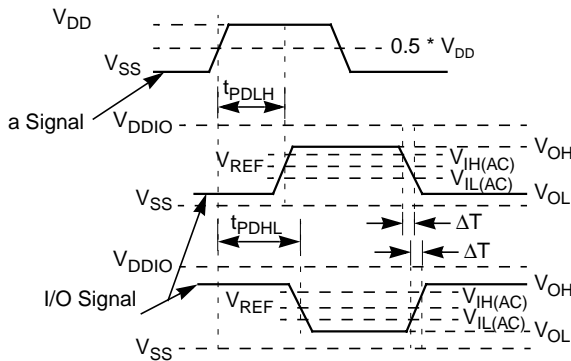


Figure 33 shows the HSTL driver timing waveforms.

Figure 33 HSTL Driver Timing Waveforms



4.6 2.5 V LVDS Buffers

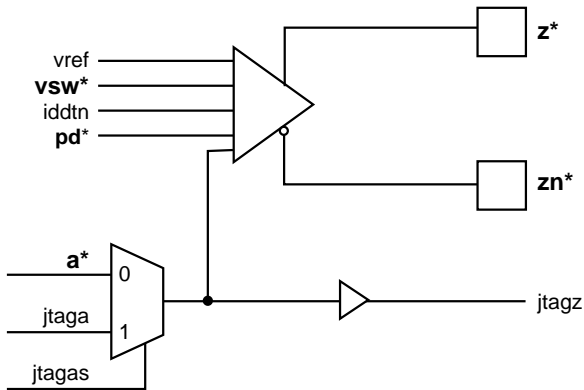
The 2.5 V LVDS buffers (lvdsinsjls25rc, lvdsinrsjls25rc, lvdsoutjls25rc, lvdsoutrjls25rc) are separate differential drivers and receivers, which require a 1.2 V reference (off-chip). Each driver and each receiver require one configurable slot. The driver output current can be programed to meet the IEEE LVDS standard or to meet the needs of very low power applications. The receivers have input oscillation suppression to protect against floating inputs. As shown in Table 27, the driver and the receiver are available with internal terminations.

Table 27 2.5 V LVDS Drivers and Receivers

Buffer	Function	Termination
lvdsinsjls25rc	Receiver	No
lvdsinrsjls25rc	Receiver	Yes
lvdsoutjls25rc	Driver	No
lvdsoutrjls25rc	Driver	Yes

Figure 34 is a block diagram of the 2.5 V LVDS driver.

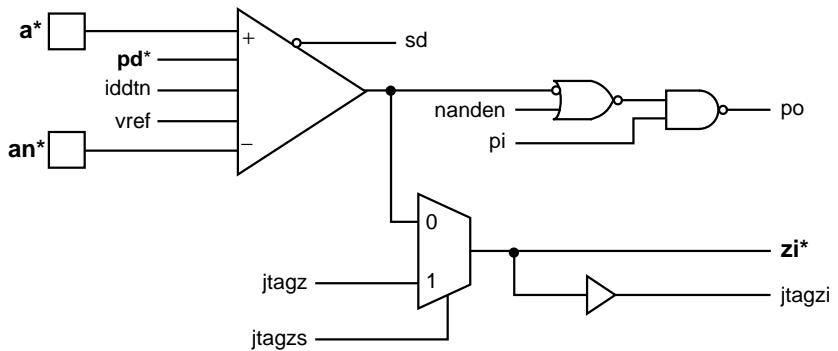
Figure 34 2.5 V LVDS Driver Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type.
Signals presented in plain type are configured by the RapidWorx Design Kit.

Figure 35 is a block diagram of the 2.5 V LVDS receiver.

Figure 35 2.5 V LVDS Receiver Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type.
Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 28 lists the 2.5 V LVDS driver DC characteristics.

Table 28 2.5 V LVDS Driver DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V _{DDIO}	I/O Supply Voltage	2.25	2.75	V	V _{DDIO} = 2.5 V Nominal
V _{OH}	Output HIGH Voltage, z or zi	–	1475	mV	Load = 100 Ω \pm 1%
V _{OL}	Output LOW Voltage, z or zi	925	–	mV	Load = 100 Ω \pm 1%
V _{OD}	Output Differential Voltage	250	400	mV	Load = 100 Ω \pm 1%
V _{OS}	Output Offset Voltage	1125	1275	mV	Load = 100 Ω \pm 1%
\Delta V _{OD}	Change in V _{OD} LOW to HIGH	–	25	mV	Load = 100 Ω \pm 1%
\Delta V _{OS}	Change in V _{OS} LOW to HIGH	–	25	mV	Load = 100 Ω \pm 1%
I _{SG}	Output Current	–	24	mA	Output shorted to ground
I _{SZZI}	Output Current	–	12	mA	Outputs shorted together
I _X	Power-Off Output Leakage Current	–	20	uA	Power Down = V _{DD}

Table 29 lists the 2.5 V LVDS receiver DC characteristics.

Table 29 2.5 V LVDS Receiver DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V _I	Input Voltage Range, a or an	0	V _{DDIO} – 0.5	V	V _{gpd} < 925 mV
V _{IDTH}	Input Differential Threshold	-100	+100	mV	V _{gpd} < 925 mV
R _{IN}	Differential Input Impedance.	75	125	Ω	–

Table 30 lists the 2.5 V LVDS driver AC characteristics.

Table 30 2.5 V LVDS Driver AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
t _{DC} ¹	Clock Duty Cycle	45	55	%	622 MHz
		40	60	%	800 MHz
t _{FALL}	V _{OD} Fall Time, 20-80%	80	300	ps	Load = 100 Ω \pm 1%, 2 pF
t _{RISE}	V _{OD} Rise Time, 20-80%	80	300	ps	Load = 100 Ω \pm 1%, 2 pF
t _{SKEW1}	tpHLA-tpLHB or tpHLB-tpLHA , differential skew	–	50	ps	Any differential pair on package
t _{SKEW2}	tpdiff[m]-tpdiff[n] channel to channel skew	–	200	ps	Any two signals on package

1. Input signal A ramp time 0.2 ns, duty cycle 50%

Table 31 lists the 2.5 V LVDS receiver AC characteristics.

Table 31 2.5 V LVDS Receiver AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
t_{DC}^1	Clock Duty Cycle	45	55	%	622 MHz
		40	60	%	800 MHz
t_{FALL}	zi Fall Time, 90-10%	—	80	ps	16 std. loads
t_{RISE}	zi Rise Time, 10-90%	—	80	ps	16 std. loads

1. Without package and transmission line attached.

Table 32 lists the 2.5 V LVDS driver timing characteristics.

Table 32 2.5 V LVDS Driver Timing Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Conditions
t_{PDLH}	Output Propagation Delay- LOW to HIGH	—	1.0		ns	Load = 50 Ω termination, 2 pF capacitor, w/o package
t_{PDHL}	Input Propagation Delay- HIGH to LOW	—	1.0		ns	Load = 50 Ω termination, 2 pF capacitor, w/o package
t_{FALL}	V_{OD} Fall Time, 20–80%	80	—	300	ps	Load = 50 Ω termination, 2 pF capacitor, w/o package
t_{RISE}	V_{OD} Rise Time, 20–80%	80	—	300	ps	Load = 50 Ω termination, 2 pF capacitor, w/o package
t_{PU}	Power-Up Time	—	—	800	ns	-
t_{DC}	Clock Duty Cycle	45	50	55	%	622 MHz
		40	50	60	%	800 MHz

[Table 33](#) lists the 2.5 V LVDS receiver timing characteristics.

Table 33 2.5 V LVDS Receiver Timing Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Conditions
t_{PDLH}	Input Propagation Delay LOW to HIGH	–	0.8 1.0	–	ns	1 std. load (0.0027 pF) 16 std. loads
t_{PDHL}	Input Propagation Delay HIGH to LOW	–	0.8 1.0	–	ns	1 std. load (0.0027 pF) 16 std. load
t_{FALL}	zi Fall Time, 90–10%	–	–	80	ps	16 std. loads
t_{RISE}	zi Rise Time, 10–90%	–	–	80	ps	16 std. loads
t_{DC}	Clock Duty Cycle	45	50	55	%	622 MHz
		40	50	60	%	800 MHz
$t_{RECOVER}$	Power Down to Receiver Active Time	–	–	800	ns	-
$t_{INACTIVE}$	Power Down to Receiver Inactive Time	–	–	2.5	ns	-

4.7 3.3 V LVDS Buffers

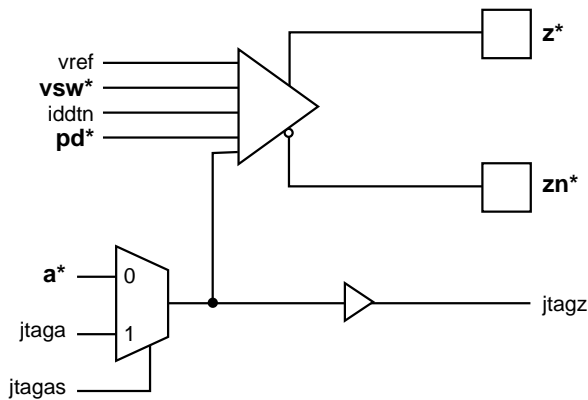
The 3.3 V LVDS buffers (lvdsinsjls33rc, lvdsinrsjls33rc, lvdsoutjls33rc, lvdsoutrjls33rc) are separate differential drivers and receivers, which require a 1.2 V reference (off-chip). Each driver and each receiver require one configurable slot. The driver output current can be programmed to meet the IEEE LVDS standard or to meet the needs of very low power applications. The receivers have input oscillation suppression to protect against floating inputs. As shown in [Table 34](#), the driver and the receiver are available with internal terminations.

Table 34 3.3 V LVDS Drivers and Receivers

Buffer	Function	Termination
lvdsinsjls33rc	Receiver	No
lvdsinrsjls33rc	Receiver	Yes
lvdsoutjls33rc	Driver	No
lvdsoutrjls33rc	Driver	Yes

Figure 36 is a 3.3 V LVDS driver block diagram.

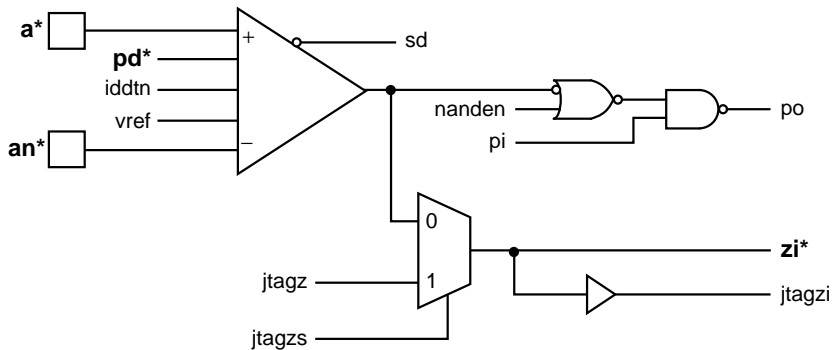
Figure 36 3.3 V LVDS Driver Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type.
Signals presented in plain type are configured by the RapidWorx Design Kit.

Figure 37 is a 3.3 V LVDS receiver block diagram.

Figure 37 3.3 V LVDS Receiver Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type.
Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 35 lists the 3.3 V LVDS driver DC characteristics.

Table 35 3.3 V LVDS Driver DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V _{DDIO}	I/O Supply Voltage	2.97	3.63	V	V _{DDIO} = 3.3 V Nominal
V _{OH}	Output Voltage High, z or zi	–	1475	mV	Load = 100 Ω +/- 1%
V _{OL}	Output Voltage Low, z or zi	925	–	mV	Load = 100 Ω +/- 1%
V _{OD}	Output Differential Voltage	250	400	mV	Load = 100 Ω +/- 1%
V _{OS}	Output Offset Voltage	1125	1275	mV	Load = 100 Ω +/- 1%
\Delta V _{OD}	Change in V _{od} LOW to HIGH	–	25	mV	Load = 100 Ω +/- 1%
\Delta V _{OS}	Change in V _{OS} LOW to HIGH	–	25	mV	Load = 100 Ω +/- 1%
I _{SG}	Output Current	–	24	mA	Output shorted to ground
I _{SZZI}	Output Current	–	12	mA	Outputs shorted together
I _x	Power-Off Output Leakage Current	–	20	uA	PD = V _{DD}

Table 36 lists the 3.3 V LVDS receiver DC characteristics.

Table 36 3.3 V LVDS Receiver DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V _I	Input Voltage Range, a or an	0	2400	mV	V _{gpd} < 925 mV
V _{IDTH}	Input Differential Threshold Voltage	-100	+100	mV	V _{gpd} < 925 mV
R _{IN}	Differential Input Impedance	75	125	Ω	-

Table 37 lists the 3.3 V LVDS driver AC characteristics.

Table 37 3.3 V LVDS Driver AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
t _{DC} ¹	Clock Duty Cycle	45	55	%	622 MHz
		40	60	%	800 MHz
t _{FALL}	V _{OD} Fall Time, 20-80%	80	300	ps	Load = 100 Ω +/-1%, 2 pF
t _{RISE}	V _{OD} Rise Time, 20-80%	80	300	ps	Load = 100 Ω +/-1%, 2 pF
t _{SKEW1}	tpHLA-tpLHB or tpHLB-tpLHA , differential skew	–	50	ps	Any differential pair on package
t _{SKEW2}	tpdiff[m]-tpdiff[n] channel to channel skew	–	200	ps	Any two signals on package

1. Input signal A ramp time 0.2 ns, duty cycle 50%

Table 38 lists the 3.3 V LVDS receiver AC characteristics.

Table 38 3.3 V LVDS Receiver AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
t_{DC}^1	Clock Duty Cycle	45	55	%	622 MHz
		40	60	%	800 MHz
t_{FALL}	zi Fall Time, 90-10%	–	80	ps	16 std. loads
t_{RISE}	zi Rise Time, 10-90%	–	80	ps	16 std. loads

1. Without package and transmission line attached

Table 39 lists the 3.3 V LVDS driver timing characteristics.

Table 39 3.3 V LVDS Driver Timing Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Conditions
t_{PDLH}	Output Propagation Delay LOW to HIGH	–	1.0	–	ns	Load = 50 Ω termination, 2 pF cap, w/o package
t_{PDHL}	Input Propagation Delay HIGH to LOW	–	1.0	–	ns	Load = 50 Ω termination, 2 pF cap, w/o package
t_{FALL}	V_{OD} Fall Time, 20-80%	80	–	300	ps	Load = 50 Ω termination, 2 pF cap, w/o package
t_{RISE}	V_{OD} Fall Time, 20-80%	80	–	300	ps	Load = 50 Ω termination, 2 pF cap, w/o package
t_{PU}	Power-Up Time	–	–	200	ns	–
t_{DC}	Clock Duty Cycle	45	50	55	%	622 MHz
		40	50	60	%	800 MHz

Table 40 lists the 3.3 V LVDS receiver timing characteristics.

Table 40 3.3 V LVDS Receiver Timing Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Conditions
t_{PDLH}	Input Propagation Delay LOW to HIGH	–	0.8 1.0	–	ns	1 std. load (0.0027 pF) 16 std load
t_{PDHL}	Input Propagation Delay HIGH to LOW	–	0.8 1.0	–	ns	1 std. load (0.0027 pF) 16 std load
t_{FALL}	zi Fall Time, 90-10%	–	–	80	ps	16 std. load
t_{RISE}	zi Rise Time, 10-90%	–	–	80	ps	16 std. load

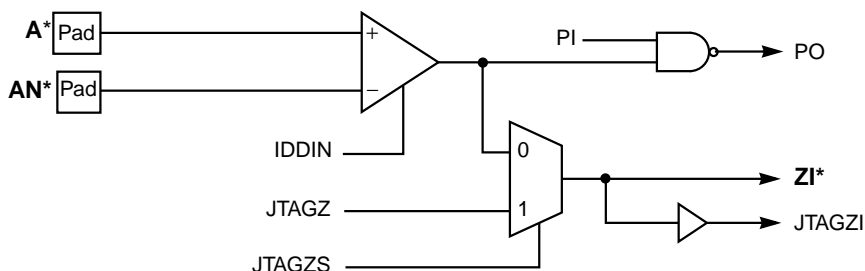
Table 40 3.3 V LVDS Receiver Timing Characteristics (Cont.)

Symbol	Parameter	Min	Nom	Max	Units	Conditions
t_{DC}	Clock Duty Cycle	45	50	55	%	622 MHz
		40	50	60	%	800 MHz
$t_{RECOVER}$	Power Down to Receiver Active Time	–	–	200	ns	–
$t_{INACTIVE}$	Power Down to Receiver Inactive Time	–	–	2.5	ns	–

4.8 PECL Buffer

The PECL input buffer (peclindiffjls33rc) is a high-speed differential receiver that is created from two configurable I/O slots. The receiver accepts an input signal with an 800 mV swing (usually 1.6 V to 2.4 V). The receiver is intended for heavily loaded backplanes and medium to high-speed point-to-point interfaces where standard CMOS or LVTTTL buffers do not provide adequate speed or do not have the necessary DC drive characteristics, generate too much switching noise, or consume too much power. [Figure 38](#) is a block diagram of the PECL buffer.

Figure 38 PECL Buffer Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type.
 Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 41 lists the PECL buffer DC electrical characteristics.

Table 41 PECL Buffer DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DDIO}	I/O Power Supply Voltage	2.97	3.30	3.63	V	—
V_{IL}	Input LOW Voltage	—	1.60	2.10	V	—
V_{IH}	Input HIGH Voltage	1.90	2.40	—	V	—
I_{IL}	Input LOW Leakage Current	-10.0		—	uA	$A = V_{SS}$
I_{IH}	Input HIGH Leakage Current	—	—	+10.00	uA	$A = V_{DDIO}$

Table 42 lists the PECL buffer propagation delays.

Table 42 PECL Buffer Propagation Delay

Symbol	Parameter	NOM	WC	BC	Unit
$t_{PDLH_A_ZI}$	Output Propagation Delay LOW to HIGH	0.75	1.15	0.55	ns
$t_{PDHL_A_ZI}$	Output Propagation Delay HIGH to LOW	0.75	1.15	0.55	ns

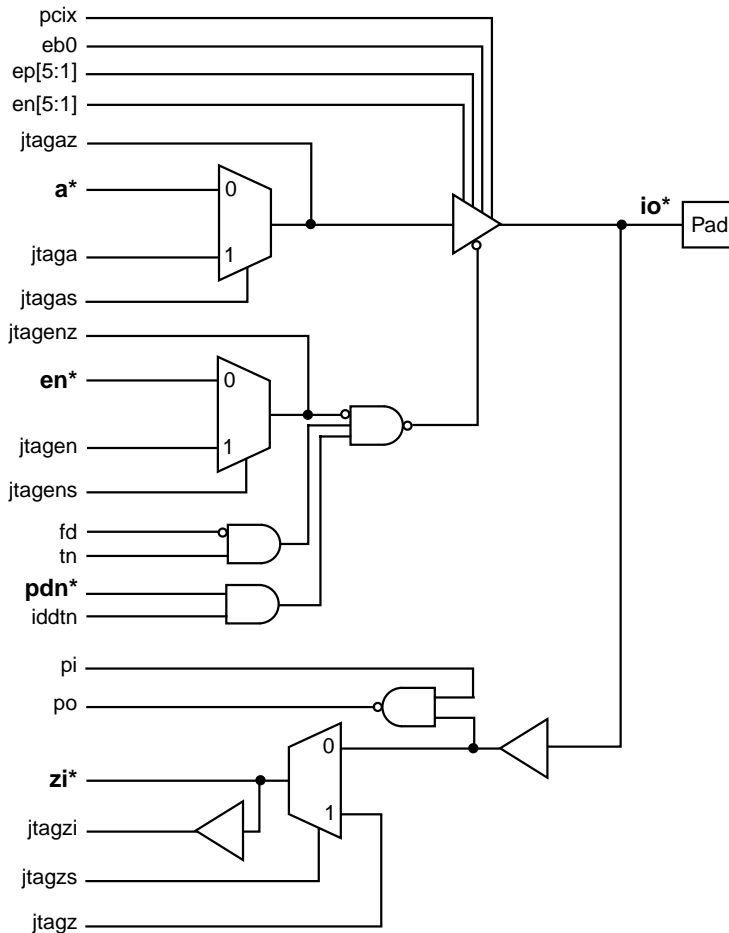
4.9 PCI/PCI-X Buffer

The PCI/PCI-X buffer (bdzpcixjls33rc) is a controlled impedance buffer that is created from a single configurable I/O slot. The buffer complies with the following specifications:

- *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0, for 66/100/133 MHz in 3.3 V Signaling Environment*
- *PCI Specification Revision 2.3 for 66 MHz in 3.3 V Signaling Environment*

Figure 39 is a block diagram of the PCI/PCI-X buffer.

Figure 39 PCI/PCI-X Buffer Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type.
 Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 43 lists the DC characteristics of the PCI/PCI-X buffer for PCI-X 66/100/133 MHz and conventional PCI 33/66 MHz applications.

Table 43 PCI/PCI-X Buffer DC Characteristics

Symbol	Parameter	Min	Typ	Max	Conditions
V_{DDIO}	I/O Supply Voltage	2.97 V	3.30 V	3.63 V	—
V_{IH}	Input HIGH Voltage	$0.5 \cdot V_{DDIO}$	—	$V_{DDIO} + 0.5 \text{ V}$	—
V_{IL_PCIX}	Input LOW Voltage	-0.5 V	—	$0.35 \cdot V_{DDIO}$	—
V_{IL_PCI}	Input LOW Voltage	-0.5 V	—	$0.3 \cdot V_{DDIO}$	—
V_{IPU}	Input Pull-Up Voltage ¹	$0.7 \cdot V_{DDIO}$	—	—	—
I_{IH}	Input HIGH Leakage Current ²	—	—	+10 μ A	$V_{IO} = V_{DDIO}$
I_{IL}	Input LOW Leakage Current ²	—	—	-10 μ A	$V_{IO} = V_{SS}$
V_{OH}	Output HIGH Voltage	$0.9 \cdot V_{DDIO}$	—	—	$I_{OUT} = -500 \text{ } \mu$ A
V_{OL}	Output LOW Voltage	—	—	$0.1 \cdot V_{DDIO}$	$I_{OUT} = 1500 \text{ } \mu$ A

1. This is the minimum voltage to which pull-up resistors are calculated to pull-up a floated network. Applications sensitive to static power utilization must assure the input buffer is conducting minimum current at this input voltage.
2. Input leakage currents include High-Z output leakage for all bidirectional buffers with 3-state outputs.

Table 44 lists the AC characteristics of the PCI/PCI-X buffer for PCI-X 66/100/133 MHz applications.

Table 44 PCI-X 66/100/133 MHz AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
$I_{OH (AC)}$	Switching Current HIGH	—	$74 (V_{DDIO} - V_{OUT})$	mA	$0 < V_{DDIO} - V_{out} \leq 3.6 \text{ V}$
		$-32(V_{DDIO} - V_{OUT})$	—	mA	$0 < V_{DDIO} - V_{OUT} \leq 1.2 \text{ V}$
		$-11(V_{DDIO} - V_{OUT}) - 25.2$	—	mA	$1.2 \text{ V} < V_{DDIO} - V_{OUT} \leq 1.9 \text{ V}$
		$-1.8(V_{DDIO} - V_{OUT}) - 42.7$	—	mA	$1.9 \text{ V} < V_{DDIO} - V_{OUT} \leq 3.6 \text{ V}$
$I_{OL (AC)}^1$	Switching Current LOW	—	$100V_{OUT}$	mA	$0 \leq V_{DDIO} - V_{OUT} \leq 3.6 \text{ V}$
		$48 \cdot V_{OUT}$	—	mA	$0 < V_{OUT} \leq 1.3 \text{ V}$
		$5.7 \cdot V_{OUT} + 55$	—	mA	$1.3 \text{ V} < V_{OUT} \leq 3.6 \text{ V}$
I_{CL}	Clamp Current LOW	$-40 + (V_{IN} + 1)/0.005$	—	mA	$-3 < V_{IN} \leq -0.8875 \text{ V}$
		$-25 + (V_{IN} + 1)/0.015$	—	mA	$-0.8875 \text{ V} < V_{IN} \leq -0.625 \text{ V}$
I_{CH}	Clamp Current HIGH	$40 + (V_{IN} - V_{DDIO} - 1)/0.005$	—	mA	$0.8875 \text{ V} \leq V_{IN} - V_{DDIO} < 4 \text{ V}$
		$25 + (V_{IN} - V_{DDIO} - 1)/0.015$	—	mA	$0.625 \text{ V} \leq V_{IN} - V_{DDIO} < 0.8875 \text{ V}$

Table 45 lists the AC characteristics of the PCI/PCI-X buffer for conventional PCI 33/66 MHz applications.

Table 45 PCI 33/66 MHz AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{OH} (AC)	Switching Current HIGH	$-12 \cdot V_{DDIO}$	—	mA	$0 < V_{out} \leq 0.3 V_{DDIO}$
		$-17.1 \cdot (V_{DDIO} - V_{OUT})$	—	mA	$0.3 V_{DDIO} < V_{OUT} < 0.9 V_{DDIO}$
		—	$(98/V_{DDIO}) \cdot (V_{out} - V_{DDIO}) \cdot (V_{out} + 0.4 V_{DDIO})$	mA	$0.7 V_{DDIO} < V_{OUT} < V_{DDIO}$
		—	$-32 V_{DDIO}$	mA	Test Point ($V_{out} = 0.7 V_{DDIO}$)
I_{OL} (AC)	Switching Current LOW	$16 \cdot V_{DDIO}$	—	mA	$V_{DDIO} > V_{OUT} \geq 0.6 V_{DDIO}$
		$26.7 \cdot V_{OUT}$	—	mA	$0.6 V_{DDIO} > V_{OUT} > 0.1 V_{DDIO}$
		—	$(256/V_{DDIO} \cdot V_{OUT} \cdot (V_{DDIO} - V_{OUT}))$	mA	$0.18 V_{DDIO} > V_{OUT} > 0$
		—	$38 V_{DDIO}$	mA	Test Point ($V_{OUT} = 0.18 V_{DDIO}$)
I_{CL}	Clamp Current LOW	$-25 + (V_{IN} + 1)/0.015$	—	mA	$-3 < V_{IN} \leq -1$
I_{CH}	Clamp Current High	$25 + (V_{IN} - V_{DDIO} - 1)/0.015$	—	mA	$V_{DDIO} + 1 \leq V_{IN} < V_{DDIO} + 4$

Table 46 lists the slew rate characteristics of the PCI/PCI-X buffer for PCI-X 66/100/133 MHz applications.

Table 46 PCI-X 66/100/133 MHz Slew Rate

Symbol	Parameter	Min	Max	Conditions
t_{SRR}	Output Rise Slew Rate	1 V/ns	6 V/ns	$0.3 V_{DDIO}$ to $0.6 V_{DDIO}$
t_{SRF}	Output Fall Slew Rate	1 V/ns	6 V/ns	$0.6 V_{DDIO}$ to $0.3 V_{DDIO}$

Table 47 lists the slew rate characteristics of the PCI/PCI-X buffer for conventional PCI 33/66 MHz applications.

Table 47 PCI 33/66 MHz Slew Rate

Symbol	Parameter	Min	Max	Conditions
t_{SRR}	Output Rise Slew Rate	1 V/ns	4 V/ns	0.2 V_{DDIO} to 0.6 V_{DDIO} (33 MHz) 0.3 V_{DDIO} to 0.6 V_{DDIO} (66 MHz)
t_{SRF}	Output Fall Slew Rate	1 V/ns	4 V/ns	0.6 V_{DDIO} to 0.2 V_{DDIO} (33 MHz) 0.6 V_{DDIO} to 0.3 V_{DDIO} (66 MHz)

Table 48 lists the PCI/PCI-X buffer delay characteristics for PCI-X 66/100/133 MHz applications. In PCI-X operation, the enable signal and data are clocked out together; therefore the maximum delay specification for both a_to_io and en_to_io should be the same. The minimum delay specifications differ due to different measurement requirements.

Table 48 PCI-X 66/100/133 MHz Delay Characteristics

Symbol	Parameter	Min	Max	Units
$t_{PDLH_a_io}$	Propagation Delay LOW to HIGH	0.733 ¹	2.2 ¹	ns
$t_{PDHL_a_io}$	Fall Delay HIGH to LOW	0.733 ¹	2.2 ¹	ns
$t_{PDZH_en_io}$	Propagation Delay 3-State to HIGH	—	2.2 ¹	ns
$t_{PDZL_en_io}$	Propagation Delay 3-State to LOW	—	2.2 ns ¹	ns
$t_{ONZH_en_io}$	Propagation Delay 3-State to HIGH	0.2 ns	—	ns
$t_{ONZL_en_io}$	Propagation Delay 3-State to LOW	0.2 ns	—	ns
$t_{OFFHZ_en_io}$	Propagation Delay HIGH to 3-State	—	5.0	ns
$t_{OFFLZ_en_io}$	Propagation Delay LOW to 3-State	—	5.0	ns

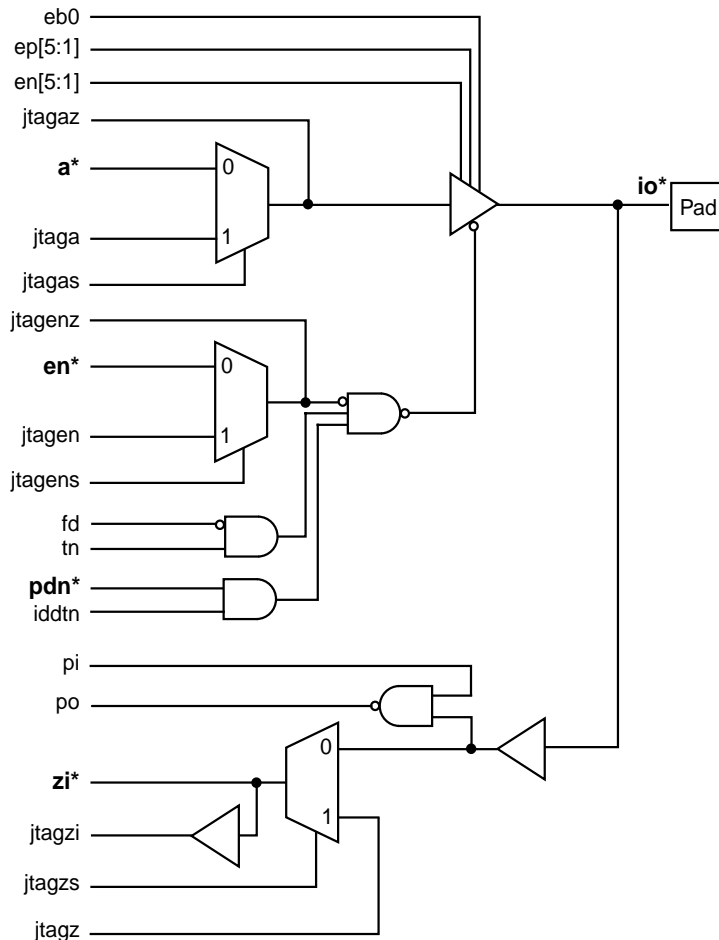
1. Refer to the 133 MHz PCI-X Tval budget.

4.10 2.5 V Controlled Impedance Buffers

The 2.5 V Controlled Impedance buffers (btz[25,50]jls25rc, bdz[25,50]j[c,cu,cd]ls25rc) are created from a single configurable I/O slot. These buffers adjust drive strength to match the impedance of their transmission lines, providing the highest effective data rate, consuming less power, and generating less crosstalk and simultaneous switching noise (SSO) than LVTTTL buffers. Drive strength is dynamically adjusted by a controller module in the RapidChip platform ASIC that senses impedance changes in external reference resistors and automatically

compensates for process, voltage, and temperature (PVT) variations. The controller module is constructed from the RapidChip platform ASIC's R-Cells, and the external resistors require three I/O cells. These buffers are available in bidirectional and 3-state versions with 25 Ω and 50 Ω drive impedances. [Figure 40](#) is a block diagram of a bidirectional 2.5 V Controlled Impedance buffer. The 3-state buffers do not have the receiver shown in [Figure 40](#).

Figure 40 2.5 V Controlled Impedance Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type. Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 49 lists the DC characteristics of the 2.5 V Controlled Impedance buffers.

Table 49 2.5 V Controlled Impedance Buffer DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V _{DDIO}	I/O Supply Voltage	2.25	2.5	2.75	V	-
V _{OH}	Output HIGH Voltage	2.0	—	—	V	@I _{OH} Rated DC minimum V _{DDIO} = V _{DDIO} , minimum
V _{OL}	Output LOW Voltage	—	—	0.4	V	@I _{OL} Rated DC minimum V _{DDIO} = V _{DDIO} , minimum
V _{IH}	Input HIGH Voltage	1.7	—	V _{DDIO} + 0.3	V	—
V _{IL}	Input LOW Voltage	-0.3	—	0.7	V	—
I _{PUO}	Pullup Option Current	—	—	-70	uA	IDDTN = PDN = 1 @ V _{IO} = 0 V
I _{PDO}	Pulldown Option Current	70	—	—	uA	IDDTN = PDN = 1 @ V _{IO} = V _{DDIO}

Table 50 lists the AC characteristics of the 2.5 V Controlled Impedance buffers.

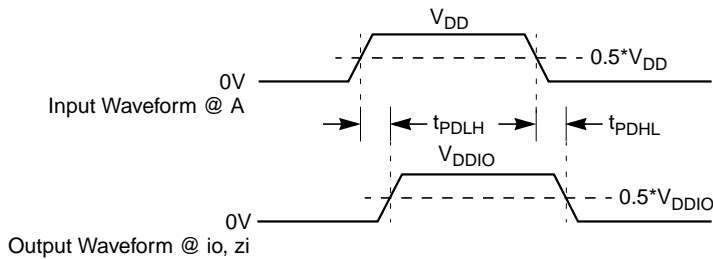
Table 50 2.5 V Controlled Impedance Buffer AC Characteristics

Symbol	Parameter	Max	Units	Conditions
t _{PDLH_en_io}	Output Propagation Delay LOW to HIGH	2.5	ns	Note ¹
t _{PDHL_en_io}	Output Propagation Delay HIGH to LOW	2.5	ns	Note ¹
t _{PDZH_en_io}	Output Propagation Delay 3-State to HIGH	2.5	ns	Note ¹
t _{PZL_en_io}	Output Propagation Delay, 3-State to LOW	2.5	ns	Note ¹
t _{PHZ_en_io}	Output Propagation Delay HIGH to 3-State Measured to (V _{DDIO} *0.9) of PMOS driver gate input	2.5	ns	Note ¹
t _{PLZ_en_io}	Output Propagation Delay LOW to 3-State Measured to (V _{DDIO} *0.1) of NMOS driver gate input	2.5	ns	Note ¹
t _{PLH_io_zi}	Input Propagation Delay LOW to HIGH	1	ns	Note ²
t _{PHL_io_zi}	Input Propagation Delay HIGH to LOW	1	ns	Note ²

1. All operating conditions, Input rise time < 0.2ns. io driving 15 pF, 7.5 pF for 25 Ω, 50 Ω respectively, no package or tline.
2. All PVT conditions, Input rise time < 1.0 ns. zi driving 16 std loads.

Figure 41 is a timing diagram for the 2.5 V Controlled Impedance buffers.

Figure 41 2.5 V Controlled Impedance Buffer Timing $a > io$



Note:

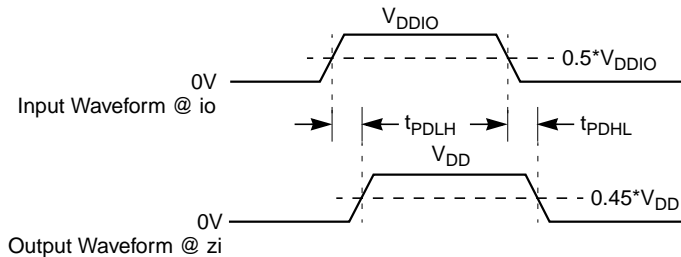
t_{PDLH} is measured from $0.45 \cdot V_{DD}$ of the input to $0.5 \cdot V_{DDIO}$ of the output.

t_{PDHL} is measured from $0.45 \cdot V_{DD}$ of the input to $0.5 \cdot V_{DDIO}$ of the output.

Input ramp time on a is set at 0.2 ns for the design.

Figure 42 is a timing diagram for the 2.5 V Controlled Impedance buffers.

Figure 42 2.5 V Controlled Impedance Buffer Timing $io > zi$



Note:

t_{PDLH} is measured from $0.5 \cdot V_{DDIO}$ of the input to $0.45 \cdot V_{DD}$ of the output.

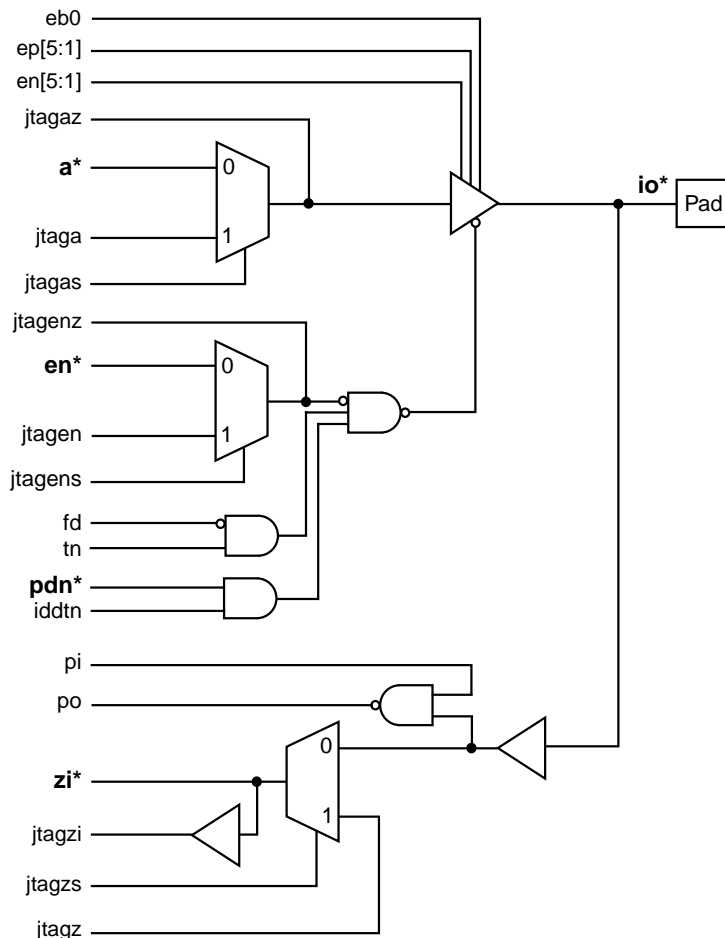
t_{PDHL} is measured from $0.5 \cdot V_{DDIO}$ of the input to $0.45 \cdot V_{DD}$ of the output.

4.11 3.3 V Controlled Impedance Buffers

The 3.3 V Controlled Impedance buffers (btz[25,50]jls33rc, bdz[25,50]j[c,cu,cd]ls33rc) are created from a single configurable I/O slot. These buffers adjust drive strength to match the impedance of their transmission lines, providing the highest effective data rate, consuming less power, and generating less crosstalk and simultaneous switching noise (SSO) than LVTTL buffers. Drive strength is dynamically adjusted by a controller module in the RapidChip platform ASIC that senses

impedance changes in external reference resistors and automatically compensates for process, voltage, and temperature (PVT) variations. The controller module is constructed from the RapidChip platform ASIC's R-Cells, and the external resistors require three I/O cells. These buffers are available in bidirectional and 3-state versions with 25 Ω and 50 Ω drive impedances. Figure 43 is a block diagram of a bidirectional 3.3 V Controlled Impedance buffer. The 3-state buffers do not have the receiver shown in Figure 43.

Figure 43 3.3 V Controlled Impedance Buffer Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type. Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 51 lists the DC characteristics of the 3.3 V Controlled Impedance buffers.

Table 51 3.3 V Controlled Impedance Buffer DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V _{DDIO}	I/O Supply Voltage	2.97	3.30	3.63	V	
V _{OH}	Output HIGH Voltage	2.4	–	–	V	@I _{OH} Rated DC minimum V _{DDIO} = V _{DDIO,minimum}
V _{OL}	Output LOW Voltage	–	–	0.4	V	@I _{OL} Rated DC minimum V _{DDIO} = V _{DDIO,minimum}
V _{IH}	Input HIGH Voltage	2.0	–	V _{DDIO} + 0.3	V	–
V _{IL}	Input LOW Voltage	-0.3	–	0.8	V	–
I _{PUO}	Pullup Option Current	–	–	-70	uA	IDDTN = PDN = 1 @ V _{IO} = 0V
I _{PDO}	Pulldown Option Current	70	–	–	uA	IDDTN = PDN = 1 @ V _{IO} = V _{DDIO}

Table 52 lists the AC characteristics of the 3.3 V Controlled Impedance buffers.

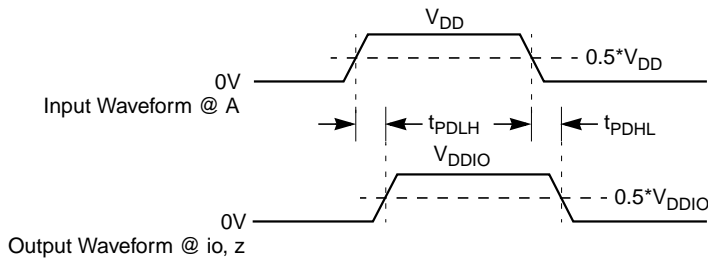
Table 52 3.3 V Controlled Impedance Buffer AC Characteristics

Symbol	Parameter	Max	Units	Conditions
t _{PDLH_en_io}	Output Propagation Delay LOW to HIGH	2.5	ns	Note ¹
t _{PDHL_en_io}	Output Propagation Delay HIGH to LOW	2.5	ns	Note ¹
t _{PDZH_en_io}	Output Propagation Delay 3-State to HIGH	2.5	ns	Note ¹
t _{PDZL_en_io}	Output Propagation Delay 3-State to LOW	2.5	ns	Note ¹
t _{PHZ_en_io}	Output Propagation Delay HIGH to 3-State (Measured to (V _{DDIO} *0.9) of PMOS driver gate input)	2.5	ns	Note ¹
t _{PDLZ_en_io}	Output Propagation Delay LOW to 3-State (Measured to (V _{DDIO} *0.1) of NMOS driver gate input)	2.5	ns	Note ¹
t _{PDLH_io_zi}	Input Propagation Delay LOW to HIGH	1	ns	Note ²
t _{PDHL_io_zi}	Input Propagation Delay HIGH to LOW	1	ns	Note ²

1. All PVT conditions, Input rise time < 0.2 ns. io driving 15 pF, 7.5 pF for 25 Ω, 50 Ω respectively, no package or tline.
2. All PVT conditions, Input rise time < 1.0 ns. zi driving 16 std loads.

Figure 44 is a timing diagram for the 3.3 V Controlled Impedance buffers.

Figure 44 3.3 V Controlled Impedance Buffer Timing $a > io$



Note:

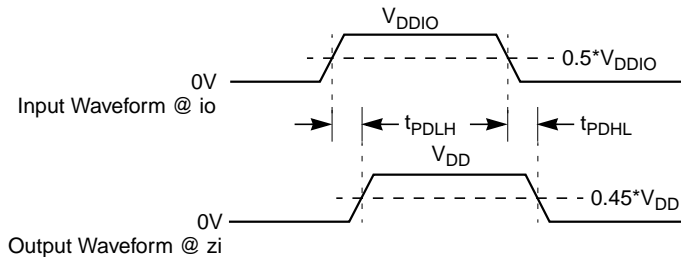
t_{PDLH} is measured from $0.45 \cdot V_{DD}$ of the input to $0.5 \cdot V_{DDIO}$ of the output.

t_{PDHL} is measured from $0.45 \cdot V_{DD}$ of the input to $0.5 \cdot V_{DDIO}$ of the output.

Input ramp time on a is set at 0.2 ns for the design.

Figure 45 is a timing diagram for the 3.3 V Controlled Impedance buffers.

Figure 45 3.3 V Controlled Impedance Buffer Timing $io > zi$



Note:

t_{PDLH} is measured from $0.5 \cdot V_{DDIO}$ of the input to $0.45 \cdot V_{DD}$ of the output.

t_{PDHL} is measured from $0.5 \cdot V_{DDIO}$ of the input to $0.45 \cdot V_{DD}$ of the output.

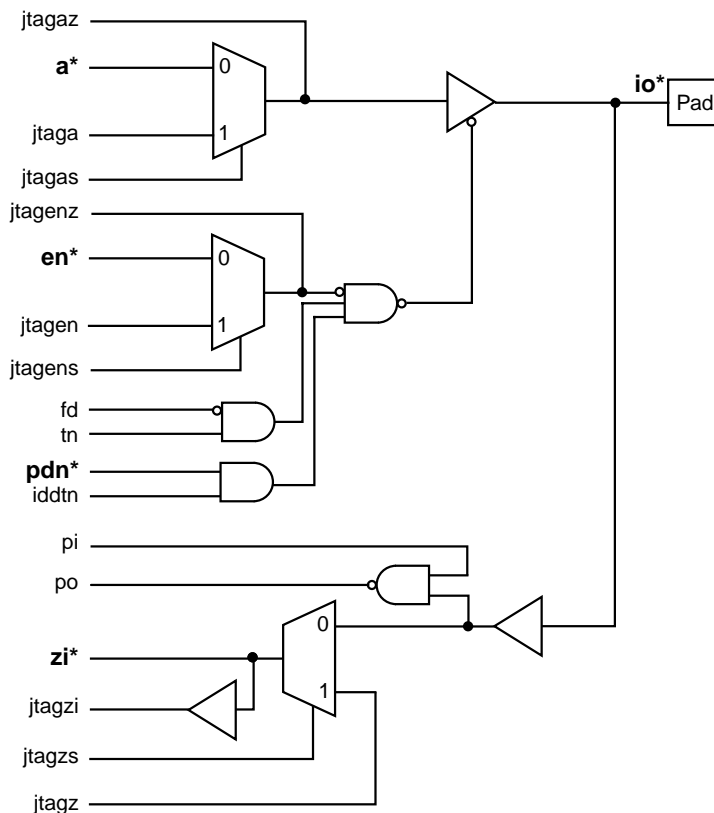
4.12 1.8 V LVTTTL/LVCMOS Buffers

The 1.8 V LVTTTL/LVCMOS buffers are general-purpose bidirectional I/O buffers that are meant for moderate speed (up to 150 MHz), direct digital CMOS interfaces. All of the buffers are designed for full-rail output switching. The buffers are identical except for three parameters: the nominal output impedance (measured at $V_{DDIO}/2$ on the I/O pin), the receiver type (straight CMOS or Schmitt-triggered), and the presence or absence of pullup or pulldown structures.

The LVTTL/LVCMOS buffers are impedance-matched buffers that are designed for a specific nominal impedance, but do not include circuitry to hold that impedance across PVT. Therefore, buffer impedance can vary significantly from corner to corner.

Each bidirectional buffer has an IDDTN pin and a PDN pin. Either pin can put the buffer into a low power state. The IDDTN pin turns off the pullup or pulldown resistor if it is present (for Iddq testing); the PDN pin does not. [Figure 46](#) is a block diagram of the 1.8 V LVTTL/LVCMOS buffer.

Figure 46 1.8 V LVTTL/LVCMOS Buffer Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type. Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 53 lists the DC characteristics of the 1.8 V LVTTTL/LVCMOS buffers.

Table 53 1.8 V LVTTTL/LVCMOS Buffer DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V_{DDIO}	I/O Supply Voltage	1.62	1.98	V	$V_{DDIO}=1.8$ V Nom.
V_{IH}	Input HIGH Voltage	TBD	TBD	V	—
V_{IL}	Input LOW Voltage	TBD	TBD	V	—
V_{OH}	Output HIGH Voltage	TBD	TBD	V	—
V_{OL}	Output LOW Voltage	TBD	TBD	V	—
I_{OZH}	3-State Output HIGH Current (equivalent to Input Leakage High Current I_{IH} for bidirectional I/O)	TBD	TBD	uA	—
I_{OZL}	3-State Output LOW Current (equivalent to Input Leakage Low Current I_{IL} for bidirectional I/O)	TBD	TBD	uA	—
$I_{PD/IPU}$	Pullup/Pulldown current	TBD	TBD	uA	—
V_{+}	Positive Threshold Voltage (Schmitt buffers only)	TBD	TBD	V	—
V_{-}	Negative Threshold Voltage (Schmitt buffers only)	TBD	TBD	V	—
V_H	Hysteresis Voltage (Schmitt buffers only)	TBD	TBD	mV	—

Table 54 shows the AC characteristics of the 1.8 V LVTTTL/LVCMOS buffers under nominal conditions with a 50 pF output load.

Table 54 1.8 V LVTTTL/LVCMOS Buffer AC Characteristics

Drive Strength	tpaz or tpd (a>io)
25 Ω	2.2 ns
50 Ω	3.0 ns

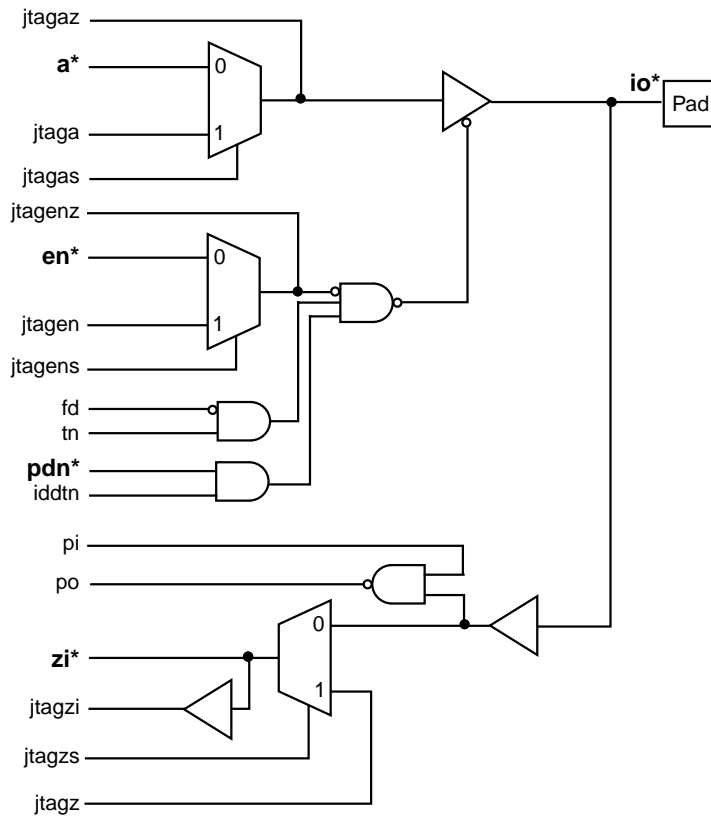
4.13 2.5 V LVTTTL/LVCMOS Buffers

The LVTTTL/LVCMOS buffers are general-purpose bidirectional I/O buffers that are meant for moderate speed (up to 150 MHz), direct digital CMOS

interfaces. All of the buffers are designed for full-rail output switching. The buffers are identical except for three parameters: the nominal output impedance (measured at $V_{DDIO}/2$ on the I/O pin), the receiver type (straight CMOS or Schmitt-triggered), and the presence or absence of pullup or pulldown structures. The LVTTTL/LVCMOS buffers are impedance matched buffers that are designed for a specific nominal impedance, but do not include circuitry to hold that impedance across PVT. Therefore, buffer impedance can vary significantly from corner to corner.

Each bidirectional buffer has an IDDTN pin and a PDN pin. Either pin can put the buffer into a low power state. The IDDTN pin turns off the pullup or pulldown resistor if it is present (for Iddq testing); the PDN pin does not. [Figure 47](#) is a block diagram of the 2.5 V LVTTTL/LVCMOS buffer.

Figure 47 2.5 V LVTTTL/LVCMOS Buffer Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type.
 Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 55 lists the DC characteristics of the 2.5 V LVTTL/LVCMOS buffers.

Table 55 2.5 V LVTTL/LVCMOS Buffer DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V_{DDIO}	I/O Supply Voltage	2.25	2.75	V	$V_{DDIO} = 2.5 \text{ V Nom.}$
V_{IH}	Input HIGH Voltage	1.7	–	V	–
V_{IL}	Input LOW Voltage	–	0.7	V	–
V_{OH}	Output HIGH Voltage	2.0	–	V	–
V_{OL}	Output LOW Voltage	–	0.4	V	–
I_{OZH}	3-State Output HIGH Current (equivalent to Input Leakage High Current I_{IH} for bidirectional I/O)	–	-10	uA	–
I_{OZL}	3-State Output LOW Current (equivalent to Input Leakage Low Current I_{IL} for bidirectional I/O)	–	10	uA	–
$I_{PD/IPU}$	Pullup/Pulldown current	70	300	uA	–
V_{+}	Positive Threshold Voltage (Schmitt buffers only)	–	1.8	V	–
V_{-}	Negative Threshold Voltage (Schmitt buffers only)	0.8	–	V	–
V_H	Hysteresis Voltage (Schmitt buffers only)	25	–	mV	–

Table 56 shows the AC characteristics of the 2.5 V LVTTL/LVCMOS buffers under nominal conditions with a 50 pF output load.

Table 56 2.5 V LVTTL/LVCMOS Buffer AC Characteristics

Drive Strength	tpaz or tpd (a>io)
25 Ω	1.9 ns
50 Ω	2.8 ns

4.14 3.3 V LVTTL/LVCMOS Buffers

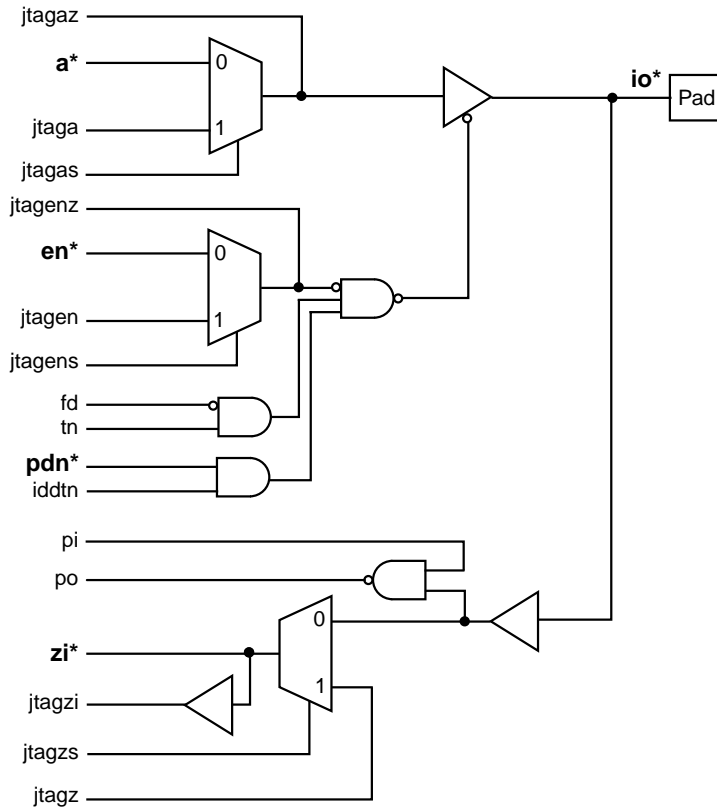
The LVTTL/LVCMOS buffers are general-purpose bidirectional I/O buffers that are meant for moderate speed (up to 150 MHz), direct digital CMOS

interfaces. All of the buffers are designed for full-rail output switching. The buffers are identical except for three parameters: the nominal output impedance (measured at $V_{DDIO}/2$ on the I/O pin), the receiver type (straight CMOS or Schmitt-triggered), and the presence or absence of pullup or pulldown structures. The LVTTL/LVCMOS buffers are impedance-matched buffers that are designed for a specific nominal impedance, but do not include circuitry to hold that impedance across PVT. Therefore, buffer impedance can vary significantly from corner to corner.

Each bidirectional buffer has an IDDTN pin and a PDN pin. Either pin can put the buffer into a low power state. The IDDTN pin turns off the pullup or pulldown resistor if it is present (for Iddq testing); the PDN pin does not.

[Figure 48](#) is a block diagram of the 3.3 V LVTTL/LVCMOS buffer.

Figure 48 3.3 V LVTTTL/LVCMOS Buffer Block Diagram



Note: * Signals connected to user-configurable pins are presented in bold type.
 Signals presented in plain type are configured by the RapidWorx Design Kit.

Table 57 lists the DC characteristics of the 3.3 V LVTTL/LVCMOS buffers.

Table 57 3.3 V LVTTL/LVCMOS Buffer DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
V_{DDIO}	I/O Supply Voltage	2.97	3.63	V	$V_{DDIO} = 3.3 \text{ V Nom.}$
V_{IH}	Input HIGH Voltage	2.0	–	V	–
V_{IL}	Input LOW Voltage	–	0.8	V	–
V_{OH}	Output HIGH Voltage	2.4	–	V	–
V_{OL}	Output LOW Voltage	–	0.4	V	–
I_{OZH}	3-State Output HIGH Current (equivalent to Input Leakage High Current I_{IH} for bidirectional I/O)	–	-10	μA	–
I_{OZL}	3-State Output LOW Current (equivalent to Input Leakage Low Current I_{IL} for bidirectional I/O)	–	10	μA	–
$I_{PD/IPU}$	Pullup/Pulldown current	70	300	μA	–
V_{+}	Positive Threshold Voltage (Schmitt buffers only)	–	2.0	V	–
V_{-}	Negative Threshold Voltage (Schmitt buffers only)	0.9	–	V	–
V_H	Hysteresis Voltage (Schmitt buffers only)	30	–	mV	–

Table 58 shows the AC characteristics of the 3.3 V LVTTL/LVCMOS buffers under nominal conditions with a 50 pF output load.

Table 58 3.3 V LVTTL/LVCMOS Buffer AC Characteristics

Drive Strength	t_{paz} or $t_{pd} (a > io)$
25 Ω	2.3 ns
50 Ω	3.0 ns

5 Packaging

All RapidChip platform ASIC package designs are optimized to provide the best electrical and thermal performance. Circuit design, IP design, and package design are done together, ensuring a robust, predictable product. The RapidChip Xtreme platform ASICs' ball layouts are optimized to support efficient I/O escape to the PCB while maintaining signal integrity. RapidChip Xtreme platform ASICs and packages are compliant to environmental legislation (European Union directives RoHS, Reduction of Hazardous Substances, and WEEE, Waste Electrical and Electronic Equipment), eliminating the use of defined hazardous substances, including lead (Pb). Please contact LSI Logic for more information.

[Appendix A, "Packaging Details"](#), provides comprehensive information about the packages of each RapidChip Xtreme platform ASIC.

5.1 Optimized Package Design

All RapidChip platform ASICs are the result of co-design methodology blending IP development together, resulting in an overall solution which is predictable and on time. Packaging technology is a key element of RapidChip technology in which each package is optimized to the performance requirements of the RapidChip platform ASIC. Package engineering teams work side by side with circuit designers and design center engineers, ensuring all IP functions are developed cohesively and have proven functionality across the RapidChip platform ASICs performance spectrum. The RapidChip Xtreme platform ASIC family is a true reflection of nanometer co-design. Design optimization has been performed on each RapidChip platform ASIC/package combination. Optimization provides the most robust electrical environment for improved signal integrity and the highest signal I/O density available.

The key features and benefits of the packaging for the RapidChip Xtreme platform ASIC family are:

- Dedicated V_{DD} splits for Core and I/O
- Multiple low-inductance V_{DD} I/O splits
 - Optimized signal routing within split planes to ensure proper referencing

- Differential routing for SERDES interfaces
 - Controlled impedance $Z_0 = 100$ ohms
- High-speed SERDES Rx and Tx are routed on separate signal layers
- Separate V_{DD} splits for high-speed SERDES
- Isolated PLL and GigaBlaze clock signals
- Optimized single-end routing for configurable I/O resulting in minimized crosstalk
 - Controlled impedance $Z_0 = 55$ ohms
- Design for system cost reduction
 - Effective and efficient escape routing
 - Design for signal integrity
 - Design for minimized PCB layers
- Environmentally conscious packaging available
 - RoHS compliant (wire bond and flip chip)
 - Pb Free (wire bond only)

5.1.1 Enhanced Plastic Ball Grid Array (EPBGA-T) Package

The Enhanced Plastic Ball Grid Array (EPBGA-T) package construction provides an optimized electrical environment and enhanced thermal performance while still providing a cost-effective solution. The EPBGA package uses 4-layer laminate microstrip substrate technology incorporating full V_{DD} and V_{SS} planes. EPBGA package technology uses 1 mm ball pitch and incorporates full-array ball layout to maximize I/O count and reduce package body size. The RapidChip Xtreme platform ASIC package design provides multiple independent low-inductance power domain segments with controlled impedance interconnects that are optimized to provide low crosstalk and overall superior signal integrity performance. An integrated copper heat spreader provides enhanced power dissipation properties.

5.1.2 High-Performance Flip-Chip Ball Grid Array (FCBGA)

Developed by LSI Logic in the mid 90s, the high-performance Flip-Chip Ball Grid Array (FCBGA) package is designed for maximum performance. Solder bumps on the active surface of the die are used to connect to the

substrate. The die is flipped face down, and the bumps are soldered to the corresponding pads on the substrate. The FCBGA utilizes multi-layer organic build-up substrate technology providing the industry's highest I/O densities and leading electrical performance.

The package design is optimized to support the electrical performance requirements of single-ended, high-speed I/Os with a controlled impedance of 55 ohms. Multiple low-inductance V_{DD} I/O domains for the configurable I/O region are provided to enhance signal integrity. HyperPHY and GigaBlaze I/O routings are optimized within their own V_{DD} domains, ensuring optimal performance. All differential signals are routed to minimize crosstalk and ensure a controlled impedance of 100 ohms. The package construction utilizes a copper heat spreader that directly connects to the die, resulting in an extremely low theta Jc of $\sim 0.5^{\circ}\text{C/W}$. The package uses a 1 mm pitch solder ball full array to maximize I/O count while reducing package body size. See [Section 5.3, "Thermal Design Considerations,"](#) for the thermal details and [Section A.4, "Package Mechanical Drawings,"](#) for the mechanical details of this package.

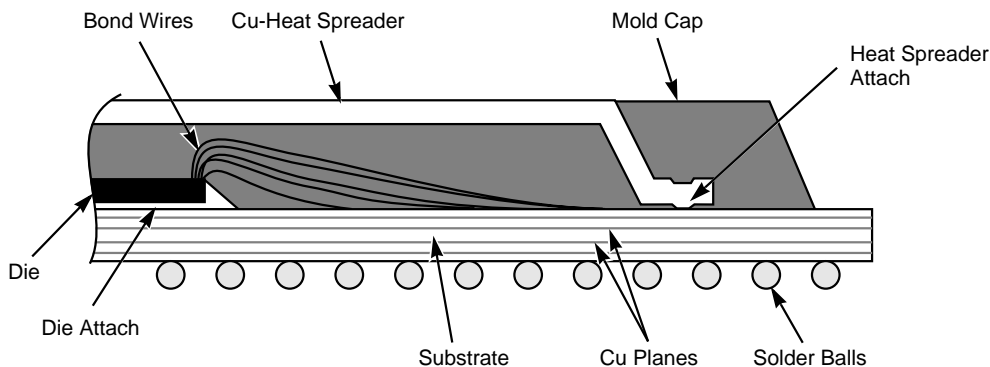
5.2 Efficient I/O Escape Routing

The RapidChip Xtreme platform ASIC family uses full-array BGA packages. These packages have been optimized for high-signal I/O density within a package body size using 1 mm ball pitch. The benefits of this approach include lower component cost (compared to peripheral approaches) and reduced area required for PCB design. Although the BGA packages are designed for high-signal I/O density, design for signal integrity is also a key attribute. PCB routing for full-array packages often is considered challenging because the through-hole vias in the PCB limit the number of signals that can be escaped between vias using reasonable design rules. The ball layouts for all RapidChip Xtreme platform ASIC family members are specifically designed and optimized to relieve these constraints. Ball layouts used by the RapidChip Xtreme platform ASIC family allow you to share one through-hole via between a pair of power (V_{DD}) or ground (V_{SS}) balls on the PCB in a particular orientation. This helps create a via pattern conducive for PCB routing on the signal layers, which increases routing density on each layer and helps to reduce the number of PCB layers required.

5.3 Thermal Design Considerations

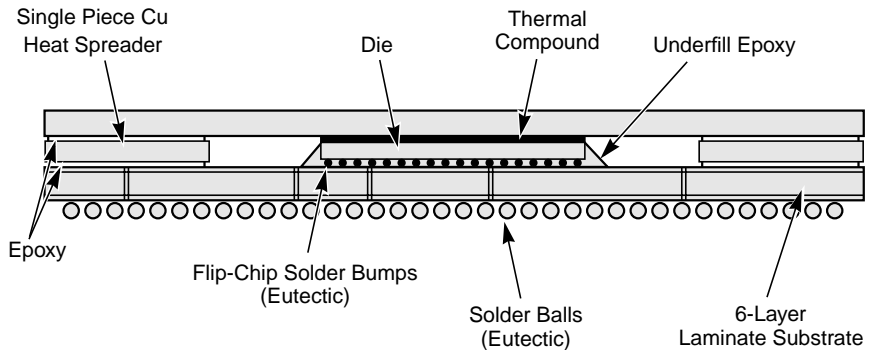
RapidChip Xtreme platform ASICs, with pin counts of 672 or greater, maximize thermal performance in the EPBGA-T packages by the inclusion of an integrated copper heat spreader in the mold of the package. [Figure 49](#) illustrates the copper heat spreader, which reduces thermal resistance by approximately 20% compared to standard PBGA packages. Additionally, such RapidChip Xtreme platform ASIC packages incorporate thermal vias under the die for V_{SS} and V_{DD} , giving you the option to connect these balls directly to V_{SS} and V_{DD} planes in the PCB to further reduce thermal impedance.

Figure 49 Cross Section of EPBGA-T Package



RapidChip Xtreme platform ASICs are also available in the high-performance Flip-Chip Ball Grid Array (FCBGA), which is designed to provide excellent thermal performance. [Figure 50](#) shows a cross section of the FCBGA package.

Figure 50 Cross Section of FCBGA Package



Thermal features of the FCBGA package include:

- Integrated single piece copper heat spreader for maximum thermal dissipation
- Direct thermal contact to flip-chip die
- Very low thermal resistance die attach compounds

[Table 59](#) outlines the thermal performance for all the RapidChip Xtreme platform ASICs.

Table 59 Xtreme Platform ASIC Package Thermal Characteristics

Platform ASIC Name	Package Code	Θ_{JC}	With Heat Sink	Θ_{JMA} with Airflow				
				0 m/s	0.5 m/s	1 m/s	2 m/s	3 m/s
RC11XT404	BG672	3.9	no	14.6	13.0	12.1	11.3	10.7
RC11XT404	BG672		yes	11.4	9.2	8.1	6.9	6.3
RC11XT416	FC672	0.7	no	10.8	9.3	8.5	7.4	6.8
RC11XT416	FC672		yes	8.0	6.5	5.4	3.4	2.5
RC11XT416	FC896	0.7	no	10.0	8.6	7.9	7.0	6.4
RC11XT416	FC896		yes	8.0	6.6	5.4	3.4	2.5

Table 59 Xtreme Platform ASIC Package Thermal Characteristics (Cont.)

Platform ASIC Name	Package Code	Θ_{JC}	With Heat Sink	Θ_{JMA} with Airflow				
				0 m/s	0.5 m/s	1 m/s	2 m/s	3 m/s
RC11XT432	FC672	0.7	no	10.8	9.3	8.5	7.4	6.8
RC11XT432	FC672		yes	8.0	6.5	5.4	3.4	2.5
RC11XT432	FC896	0.7	no	10.0	8.6	7.9	7.0	6.4
RC11XT432	FC896		yes	8.0	6.6	5.4	3.4	2.5
RC11XT531	FC896	0.7	no	10.0	8.6	7.9	7.0	6.4
RC11XT531	FC896		yes	8.0	6.6	5.4	3.4	2.5

Under standard conditions, the power that a package can dissipate (P) is calculated from:

- $P = (T_{\text{Junction}} - T_{\text{Ambient}}) / \Theta_{JA}$ At natural convection, $V_{\text{air}} = 0$ m/s
- $P = (T_{\text{Junction}} - T_{\text{Ambient}}) / \Theta_{JMA}$ At forced convection, $V_{\text{air}} > 0$ m/s

P_{max} increases as Θ_{JA} decreases and as the difference between T_{Junction} and T_{Ambient} increases. The maximum recommended T_{Junction} is 115 °C. Increasing the airflow across a package lowers its Θ_{JMA} value. Θ_{JMA} can be further reduced by attaching a heat sink to the surface of the package.

5.4 Packages and Pinouts

This section summarizes the packaging and the pinouts of the RapidChip Xtreme platform ASICs:

- [Section 5.4.1, “BG672 BGA Package”](#)
- [Section 5.4.2, “FC672 BGA Package”](#)
- [Section 5.4.3, “FC896 BGA Package”](#)

[Appendix A, “Packaging Details”](#), has more information on this subject.

5.4.1 BG672 BGA Package

The BG672 package is an enhanced ball grid array package (EPBGA) with a 27 mm body size. It has 672 balls arranged in a 26 x 26 matrix.

This arrangement offers high I/O density and competitive thermal characteristics.

[Figure 51](#) is a color-coded diagram of the RC11XT404 in the BG672 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure 51 RC11XT404 in the BG672 Package Diagram

TBD

Table 60 lists the number and type of I/O balls associated with each power domain.

Table 60 BG672 Package I/O Summary (RC11XT404)

Package Edge	Power Domain	Total I/Os	User I/Os	Dual Use I/Os	Reserved I/Os
TBD	TBD	TBD	TBD	TBD	TBD

5.4.2 FC672 BGA Package

The FC672 package is a high-performance 27 mm body size package. It has 672 pins arranged in a 26 x 26 matrix. This arrangement offers high I/O density with good electrical and thermal characteristics. The FC672 package is used for two RapidChip Xtreme platform ASICs:

- RC11XT416
- RC11XT432

5.4.2.1 RC11XT416 in the FC672 Package

Figure 54 is a color-coded diagram of the RC11XT416 in the FC672 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure 52 RC11XT416 in the FC672 Package Diagram

TBD

Table 63 summarizes the I/Os for the RC11XT416 platform ASICs that are packaged in the FC672 package. It lists the number and type of I/O balls associated with each power domain.

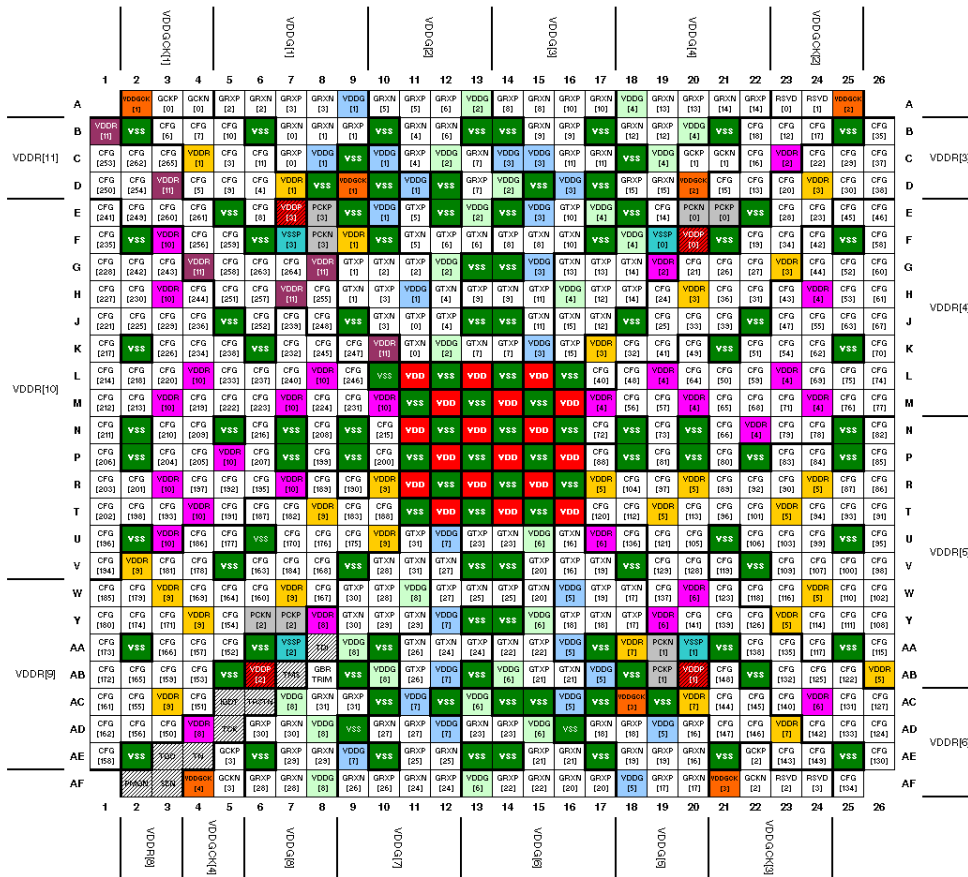
Table 61 FC672 Package I/O Summary (RC11XT416)

Package Edge	Power Domain	Total I/Os	User I/Os	Dual Use I/Os	Reserved I/Os
TBD	TBD	TBD	TBD	TBD	TBD

5.4.2.2 RC11XT432 in the FC672 Package

Figure 53 is a color-coded diagram of the RC11XT432 in the FC672 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure 53 RC11XT432 in the FC672 Package Diagram



- VSS Global VSS Ground Plane for Core Logic and Configurable I/O
- VDD VDD Power Supply for Core Logic
- VDDP [2] Independent VDD Power Supply for PLL
- VSSP [2] Independent VSS Power Supply for PLL
- VDDR [3] VDDR Power Supply Split Region for Configurable I/O
- VDDR [4] VDDR Power Supply Split Region for Configurable I/O
- VDDR [11] VDDR Power Supply Split Region for Configurable I/O
- VDDGK [1] 3.3V I/O Power Supply Region for GigaBlaze Clock Input Receiver
- VDDG [1] Power Supply Split Region for GigaBlaze Differential Pairs
- VDDG [2] Power Supply Split Region for GigaBlaze Differential Pairs

Note: To help distinguish between adjacent VDDR Splits, 2 alternating colors for VDD are used for Splits 1 through 10. A third color is used for Split 11 to distinguish it from splits 1 and 10. All splits are electrically independent of each other.

3.3V I/O Power Supply Region for GigaBlaze Clock Input Receiver

Power Supply Split Region for GigaBlaze Differential Pairs

Power Supply Split Region for GigaBlaze Differential Pairs

Note: To help distinguish between adjacent Power Supply Splits for the GigaBlaze differential pairs, 2 alternating colors are used for Splits VDDG[1] through VDDG[3]. All Splits are electrically independent of each other.

- Test balls
- Dual Use Pin: Either Differential Clock Input or User Configurable I/O

Table 62 summarizes the I/Os for the RC11XT432 in the FC672 package. It lists the number and type of I/O balls associated with each power domain.

Table 62 FC672 Package I/O Summary (RC11XT432)

Package Edge	Die Edge	Domain	Total I/Os	User I/Os	GigaBlaze I/Os	Dual Use I/Os	Reserved I/Os
Top	Left	VDDR[1]	13	11	0	2	0
Top	Left	VDDGCK[1]	2	0	2	0	0
Top	Left	VDDG[1]	16	0	16	0	0
Top	Left	VDDG[2]	16	0	16	0	0
Top	Left	VDDG[3]	16	0	16	0	0
Top	Left	VDDG[4]	16	0	16	0	0
Top	Left	VDDGCK[2]	2	0	2	0	0
Top	Left	VDDR[2]	7	7	0	0	0
Right	Bottom	VDDR[3]	25	23	0	2	0
Right	Bottom	VDDR[4]	40	40	0	0	0
Right	Bottom	VDDR[5]	40	40	0	0	0
Right	Bottom	VDDR[6]	21	21	0	0	0
Bottom	Right	VDDR[7]	9	7	0	2	0
Bottom	Right	VDDGCK[3]	2	0	2	0	0
Bottom	Right	VDDG[5]	16	0	16	0	0
Bottom	Right	VDDG[6]	16	0	16	0	0
Bottom	Right	VDDG[7]	16	0	16	0	0
Bottom	Right	VDDG[8]	17	0	17	0	0
(Sheet 1 of 2)							

Table 62 FC672 Package I/O Summary (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	Total I/Os	User I/Os	GigaBlaze I/Os	Dual Use I/Os	Reserved I/Os
Bottom	Right	VDDGCK[4]	2	0	2	0	0
Bottom	Right	VDDR[8]	9	0	0	0	9
Left	Top	VDDR[9]	42	40	0	2	0
Left	Top	VDDR[10]	57	57	0	0	0
Left	Top	VDDR[11]	19	19	0	0	0
Totals			419	265	137	8	9
(Sheet 2 of 2)							

5.4.3 FC896 BGA Package

The FC896 package is a high-performance 31 mm body size package. It has 896 pins arranged in a 30 x 30 matrix. This arrangement offers high I/O density with good electrical and thermal characteristics. The FC896 package is used for three RapidChip Xtreme platform ASICs:

- RC11XT416
- RC11XT432
- RC11XT531

The following sections outline the specifics for each of these RapidChip platform ASICs.

5.4.3.1 RC11XT416 in the FC896 Package

[Figure 54](#) is a color-coded diagram of the RC11XT416 in the FC896 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure 54 RC11XT416 in the FC896 Package Diagram

TBD

Table 63 summarizes the I/Os for the RC11XT416 in the FC896 package. It lists the number and type of I/O balls associated with each power domain.

Table 63 FC896 Package I/O Summary (RC11XT416)

Package Edge	Power Domain	Total I/Os	User I/Os	Dual Use I/Os	Reserved I/Os
TBD	TBD	TBD	TBD	TBD	TBD

5.4.3.2 RC11XT432 in the FC896 Package

Figure 55 is a color-coded diagram of the RC11XT432 in the FC896 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure 55 RC11XT432 in the FC896 Package Diagram

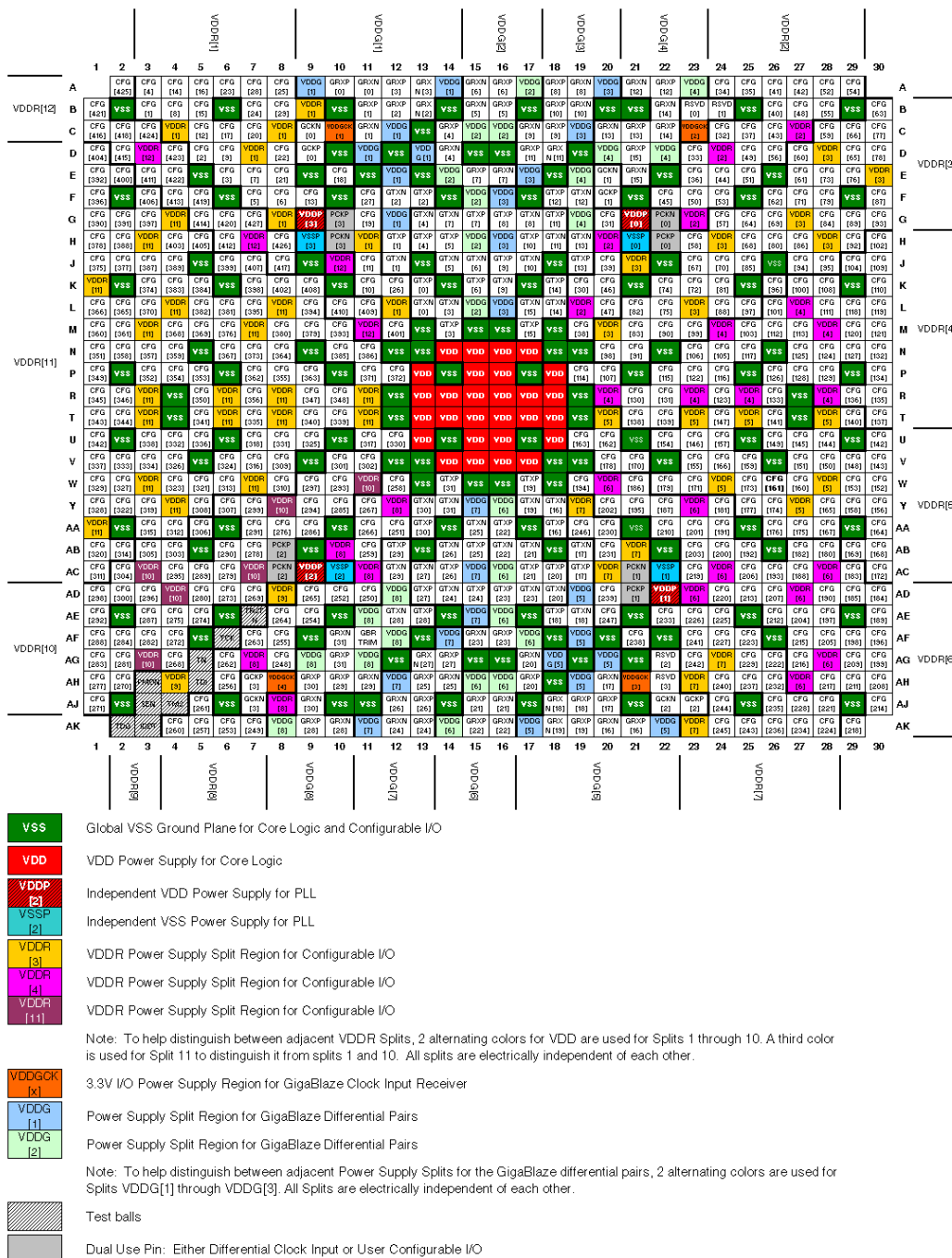


Table 64 summarizes the I/Os for the RC11XT432 in the FC896 package. It lists the number and type of I/O balls associated with each power domain.

Table 64 FC896 Package I/O Summary (RC11XT432)

Package Edge	Die Edge	Domain	Total I/Os	User I/Os	GigaBlaze I/Os	Dual Use I/Os	Reserved I/Os
Top	Left	VDDR[1]	31	29	0	2	0
Top	Left	VDDGCK[1]	2	0	2	0	0
Top	Left	VDDG[1]	16	0	16	0	0
Top	Left	VDDG[2]	16	0	16	0	0
Top	Left	VDDG[3]	16	0	16	0	0
Top	Left	VDDG[4]	16	0	16	0	0
Top	Left	VDDGCK[2]	2	0	2	0	0
Top	Left	VDDR[2]	27	27	0	0	0
Right	Bottom	VDDR[3]	45	43	0	2	0
Right	Bottom	VDDR[4]	40	40	0	0	0
Right	Bottom	VDDR[5]	40	40	0	0	0
Right	Bottom	VDDR[6]	41	41	0	0	0
Bottom	Right	VDDR[7]	29	27	0	2	0
Bottom	Right	VDDGCK[3]	2	0	2	0	0
Bottom	Right	VDDG[5]	16	0	16	0	0
Bottom	Right	VDDG[6]	16	0	16	0	0
Bottom	Right	VDDG[7]	16	0	16	0	0
Bottom	Right	VDDG[8]	17	0	17	0	0
Bottom	Right	VDDGCK[4]	2	0	2	0	0
(Sheet 1 of 2)							

Table 64 FC896 Package I/O Summary (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	Total I/Os	User I/Os	GigaBlaze I/Os	Dual Use I/Os	Reserved I/Os
Bottom	Right	VDDR[8]	20	20	0	0	0
Bottom	Right	VDDR[9]	9	0	0	0	9
Left	Top	VDDR[10]	42	40	0	2	0
Left	Top	VDDR[11]	101	101	0	0	0
Left	Top	VDDR[12]	19	19	0	0	0
Totals			581	427	137	8	9
(Sheet 2 of 2)							

5.4.3.3 RC11XT531 in the FC896 Package

[Figure 56](#) is a color-coded diagram of the RC11XT531 in the FC896 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Table 65 summarizes the I/Os for the RC11XT531 in the FC896 package. It lists the number and type of I/O balls associated with each power domain.

Table 65 FC896 Package I/O Summary (RC11XT531)

Package Edge	Die Edge	Domain	Total I/Os	User I/Os	GigaBlaze I/Os	HyperPHY I/Os	SFI-4 I/Os	Dual Use I/Os	Reserved I/Os
Top	Left	VDDR[1]	23	20	0	0	0	3	0
Top	Left	VDDS	84	0	0	84	0	0	0
Right	Bottom	VDDR[2]	44	0	0	0	41	3	0
Right	Bottom	VDDR[3]	41	0	0	0	41	0	0
Right	Bottom	VDDG[1]	16	0	16	0	0	0	0
Right	Bottom	VDDGCK[1]	4	0	4	0	0	0	0
Right	Bottom	VDDG[2]	16	0	16	0	0	0	0
Right	Bottom	VDDG[3]	17	0	17	0	0	0	0
Right	Bottom	VDDGCK[2]	2	0	2	0	0	0	0
Bottom	Right	VDDR[4]	22	19	0	0	0	3	0
Bottom	Right	VDDR[5]	20	20	0	0	0	0	0
Bottom	Right	VDDR[6]	20	20	0	0	0	0	0
Bottom	Right	VDDR[7]	20	20	0	0	0	0	0
Bottom	Right	VDDR[8]	20	20	0	0	0	0	0
Bottom	Right	VDDR[9]	20	20	0	0	0	0	0
Bottom	Right	VDDR[10]	17	17	0	0	0	0	0
Bottom	Right	VDDR[11]	9	0	0	0	0	0	9
(Sheet 1 of 2)									

Table 65 FC896 Package I/O Summary (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	Total I/Os	User I/Os	GigaBlaze I/Os	HyperPHY I/Os	SFI-4 I/Os	Dual Use I/Os	Reserved I/Os
Bottom	Right	VDDR[12]	18	15	0	0	0	3	0
Left	Top	VDDR[13]	34	34	0	0	0	0	0
Left	Top	VDDR[14]	34	34	0	0	0	0	0
Left	Top	VDDR[15]	34	34	0	0	0	0	0
Left	Top	VDDR[16]	41	41	0	0	0	0	0
Total			556	314	55	84	82	12	9
(Sheet 2 of 2)									

Appendix A

Packaging Details

This section provides detailed information about the package and the pinouts of each RapidChip Xtreme platform ASIC. It includes the following subsections:

- [Section A.1, “BG672 Package and Pinouts”](#)
- [Section A.2, “FC672 Package and Pinouts”](#)
- [Section A.3, “FC896 Package and Pinouts”](#)
- [Section A.4, “Package Mechanical Drawings”](#)

A.1 BG672 Package and Pinouts

The BG672 package is a high-performance 27 mm body size EPBGA with an integral copper heat spreader. It has 672 balls arranged in a 26 x 26 matrix. This arrangement offers high I/O density and competitive thermal characteristics. The BG672 package is used for one RapidChip Xtreme platform ASIC:

- RC11XT404

[Figure A.1](#) is a color-coded package diagram for the RC11XT404 platform ASIC in the BG672 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure A.1 RC11XT404 in the BG672 Package Diagram

TBD

Table A.1 lists the RC11XT404 BG672 package power connections. The core logic and I/Os share a common ground (V_{SS}). All the core logic is powered from a single power domain (V_{DD}). The I/Os are distributed across X separate power domains ($V_{DDR}[1:X]$). The PLLs are isolated; each PLL has its own dedicated power ($V_{DDP}[0:2]$) and ground ($V_{SSP}[0:2]$) connection.

Table A.1 BG672 Package Power Connections (RC11XT404)

Domain	VDD Plane Ball Location(s)	Description
TBD	TBD	TBD

Table A.2 lists the I/O assignments for the RC11XT404 BG672 package.

Table A.2 BG672 Package I/O Assignments (RC11XT404)

Package Side	VDDR Region Split	BG672 Package Ball	I/O Name	Description
TBD	TBD	TBD	TBD	TBD

A.2 FC672 Package and Pinouts

The FC672 package is a high-performance 27 mm body size package. It has 672 pins arranged in a 26 x 26 matrix. This arrangement offers high I/O density with good electrical and thermal characteristics. The FC672 package is used for two RapidChip Xtreme platform ASICs:

- RC11XT416
- RC11XT432

A.2.1 RC11XT416 in the FC672 Package

[Figure A.6](#) is a color-coded diagram of the RC11XT416 in the FC672 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure A.2 RC11XT416 in the FC672 Package Diagram

TBD

[Table A.7](#) lists the power connections for the RC11XT416 in the FC672 package. The core logic and I/Os share a common ground (V_{SS}).

Table A.3 FC672 Package Power Connections (RC11XT416)

VDD Plane	Package Ball Locations	Description
TBD	TBD	TBD

[Table A.8](#) lists the RC11XT416 in the FC672 package I/O assignments.

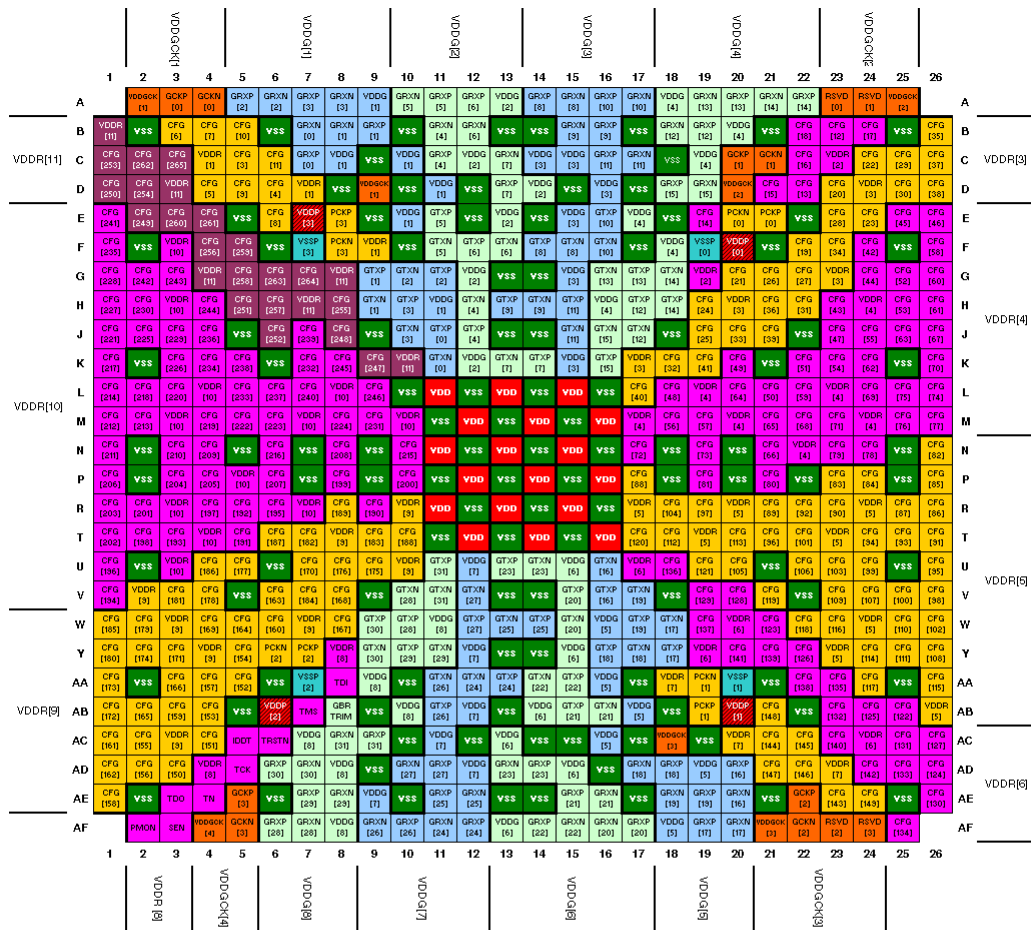
Table A.4 FC672 Package I/O Assignments (RC11XT416)

Package Side	VDDR Region Split	FC896 Package Ball	I/O Name	Description
TBD	TBD	TBD	TBD	TBD

A.2.2 RC11XT432 in the FC672 Package

[Figure A.3](#) is a color-coded package diagram for the RC11XT432 in the FC672 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure A.3 RC11XT432 in the FC672 Package Diagram



VSS Global VSS Ground Plane for Core Logic and Configurable I/O

VDD VDD Power Supply for Core Logic

VDDP Independent VDD Power Supply for PLL

VSSP Independent VSS Power Supply for PLL

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

Note: To help distinguish between adjacent VDDR Splits, 2 alternating colors for VDD are used for Splits 1 through 10. A third color is used for Split 11 to distinguish it from splits 1 and 10. All splits are electrically independent of each other.

VDDGK 3.3V I/O Power Supply Region for GigaBlaze Clock Input Receiver

VDDG Power Supply Split Region for GigaBlaze Differential Pairs

VDDG Power Supply Split Region for GigaBlaze Differential Pairs

Note: To help distinguish between adjacent Power Supply Splits for the GigaBlaze differential pairs, 2 alternating colors are used for Splits VDDG[1] through VDDG[3]. All Splits are electrically independent of each other.

Table A.5 lists the RC11XT432 FC672 package power connections. The core logic and I/Os share a common ground (V_{SS}). All the core logic is powered from a single power domain (V_{DD}). The I/Os are distributed across 10 separate power domains ($V_{DDR}[1:10]$). The four PLLs are isolated; each PLL has its own dedicated power ($V_{DDP}[0:3]$) and ground ($V_{SSP}[0:3]$) connection.

Table A.5 FC672 Package Power Connections (RC11XT432)

VDD Plane	Package Ball Location(s)	Description
VDD	L11, L13, L15, M12, M14, M16, N11, N13, N15, P12, P14, P16, R11, R13, R15, T12, T14, T16	Core Logic VDD
VSS	B02, B06, B10, B13, B14, B17, B21, B25, C09, C18, D08, D10, D12, D15, D17, E05, E09, E12, E14, E18, E22, F02, F06, F10, F17, F21, F25, G13, G14, J05, J09, J13, J14, J18, J22, K02, K06, K21, K25, L10, L12, L14, L16, M11, M13, M15, N02, N05, N07, N09, N12, N14, N16, N18, N20, N25, P02, P07, P09, P11, P13, P15, P18, P20, P22, P25, R12, R14, R16, T11, T13, T15, U02, U06, U21, U25, V05, V09, V13, V14, V18, V22, Y13, Y14, AA02, AA06, AA10, AA17, AA21, AA25, AB05, AB09, AB13, AB18, AB22, AC10, AC12, AC14, AC15, AC17, AC19, AD09, AD16, AE02, AE06, AE10, AE13, AE14, AE17, AE21, AE25	Core Logic & Configurable I/O Ground
VDDG[1]	A09, C08, C10, D11, E10, H11	GigaBlaze VDD
VDDG[2]	A13, C12, D14, E13, G12, K12	GigaBlaze VDD
VDDG[3]	C14, C15, D16, E15, G15, K15	GigaBlaze VDD
VDDG[4]	A18, B20, C19, E17, F18, H16	GigaBlaze VDD
VDDG[5]	W16, AA16, AB17, AC16, AD19, AF18	GigaBlaze VDD
VDDG[6]	U15, Y15, AB14, AC13, AD15, AF13	GigaBlaze VDD
VDDG[7]	U12, Y12, AB12, AC11, AD12, AE09	GigaBlaze VDD
VDDG[8]	W11, AA09, AB10, AC07, AD08, AF08	GigaBlaze VDD
(Sheet 1 of 3)		

Table A.5 FC672 Package Power Connections (RC11XT432) (Cont.)

VDD Plane	Package Ball Location(s)	Description
VDDGCK[1]	A02, D09	Dedicated 3.3V VDD for GigaBlaze TX clock input
VDDGCK[2]	A25, D20	Dedicated 3.3V VDD for GigaBlaze TX clock input
VDDGCK[3]	AC18, AF21	Dedicated 3.3V VDD for GigaBlaze TX clock input
VDDGCK[4]	AF04	Dedicated 3.3V VDD for GigaBlaze TX clock input
VDDR[1]	C04, D07, F09	Configurable I/O VDD
VDDR[2]	C23, G19	Configurable I/O VDD
VDDR[3]	D24, G23, H20, K17	Configurable I/O VDD
VDDR[4]	H24, L19, L23, M17, M20, M24, N22	Configurable I/O VDD
VDDR[5]	R17, R20, R24, T19, T23, W24, Y23, AB26	Configurable I/O VDD
VDDR[6]	AC24, U17, W20, Y19	Configurable I/O VDD
VDDR[7]	AA18, AC20, AD23	Configurable I/O VDD
VDDR[8]	Y08, AD04	Configurable I/O VDD
VDDR[9]	R10, T08, U10, V02, W03, W07, Y04, AC03	Configurable I/O VDD
VDDR[10]	F03, H03, L04, L08, M03, M07, M10, P05, R03, R07, T04, U03	Configurable I/O VDD
VDDR[11]	B01, D03, G04, G08, H07, K10	Configurable I/O VDD
VDDP[0]	F20	PLL VDD
VDDP[1]	AB20	PLL VDD
(Sheet 2 of 3)		

Table A.5 FC672 Package Power Connections (RC11XT432) (Cont.)

VDD Plane	Package Ball Location(s)	Description
VDDP[2]	AB06	PLL VDD
VDDP[3]	E07	PLL VDD
VSSP[0]	F19	PLL Ground
VSSP[1]	AA20	PLL Ground
VSSP[2]	AA07	PLL Ground
VSSP[3]	F07	PLL Ground
(Sheet 3 of 3)		

Table A.6 lists the I/O assignments for the RC11XT432 FC672 package.

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Top	Left	VDDR[1]	E08	PCKP[3]	PLL100500 Differential clock input / Configurable I/O
Top	Left	VDDR[1]	F08	PCKN[3]	PLL100500 Differential clock input / Configurable I/O
Top	Left	VDDR[1]	C05	CFG[3]	Configurable I/O
Top	Left	VDDR[1]	D06	CFG[4]	Configurable I/O
Top	Left	VDDR[1]	D04	CFG[5]	Configurable I/O
Top	Left	VDDR[1]	B03	CFG[6]	Configurable I/O
Top	Left	VDDR[1]	B04	CFG[7]	Configurable I/O
Top	Left	VDDR[1]	E06	CFG[8]	Configurable I/O
Top	Left	VDDR[1]	D05	CFG[9]	Configurable I/O
Top	Left	VDDR[1]	B05	CFG[10]	Configurable I/O
(Sheet 1 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Top	Left	VDDR[1]	C06	CFG[11]	Configurable I/O
Top	Left	VDDGCK[1]	A03	GCKP[0]	GigaBlaze differential TX reference clock
Top	Left	VDDGCK[1]	A04	GCKN[0]	GigaBlaze differential TX reference clock
Top	Left	VDDG[1]	B07	GRXN[0]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	C07	GRXP[0]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	J11	GTXP[0]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	K11	GTXN[0]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	H09	GTXN[1]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	G09	GTXP[1]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	B09	GRXP[1]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	B08	GRXN[1]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	A06	GRXN[2]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	A05	GRXP[2]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	G11	GTXP[2]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	G10	GTXN[2]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	J10	GTXN[3]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	H10	GTXP[3]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	A07	GRXP[3]	GigaBlaze RX differential pair
(Sheet 2 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Top	Left	VDDG[1]	A08	GRXN[3]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	B11	GRXN[4]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	C11	GRXP[4]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	J12	GTXP[4]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	H12	GTXN[4]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	F11	GTXN[5]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	E11	GTXP[5]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	A11	GRXP[5]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	A10	GRXN[5]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	B12	GRXN[6]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	A12	GRXP[6]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	F12	GTXP[6]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	F13	GTXN[6]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	K13	GTXN[7]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	K14	GTXP[7]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	D13	GRXP[7]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	C13	GRXN[7]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	A15	GRXN[8]	GigaBlaze RX differential pair
(Sheet 3 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Top	Left	VDDG[3]	A14	GRXP[8]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	F14	GTXP[8]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	F15	GTXN[8]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	H14	GTXN[9]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	H13	GTXP[9]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	B16	GRXP[9]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	B15	GRXN[9]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	A17	GRXN[10]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	A16	GRXP[10]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	E16	GTXP[10]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	F16	GTXN[10]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	J15	GTXN[11]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	H15	GTXP[11]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	C16	GRXP[11]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	C17	GRXN[11]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	B18	GRXN[12]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	B19	GRXP[12]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	H17	GTXP[12]	GigaBlaze TX differential pair
(Sheet 4 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Top	Left	VDDG[4]	J17	GTXN[12]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	G16	GTXN[13]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	G17	GTXP[13]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	A20	GRXP[13]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	A19	GRXN[13]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	A21	GRXN[14]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	A22	GRXP[14]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	H18	GTXP[14]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	G18	GTXN[14]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	J16	GTXN[15]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	K16	GTXP[15]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	D18	GRXP[15]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	D19	GRXN[15]	GigaBlaze RX differential pair
Top	Left	VDDGCK[2]	C20	GCKP[1]	GigaBlaze differential TX reference clock
Top	Left	VDDGCK[2]	C21	GCKN[1]	GigaBlaze differential TX reference clock
Top	Left	VDDGCK[2]	A23	RSVD[0]	Reserved
Top	Left	VDDGCK[2]	A24	RSVD[1]	Reserved
Top	Left	VDDR[2]	B23	CFG[12]	Configurable I/O
Top	Left	VDDR[2]	D22	CFG[13]	Configurable I/O
(Sheet 5 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Top	Left	VDDR[2]	E19	CFG[14]	Configurable I/O
Top	Left	VDDR[2]	D21	CFG[15]	Configurable I/O
Top	Left	VDDR[2]	C22	CFG[16]	Configurable I/O
Top	Left	VDDR[2]	B24	CFG[17]	Configurable I/O
Top	Left	VDDR[2]	B22	CFG[18]	Configurable I/O
Right	Bottom	VDDR[3]	E21	PCKP[0]	PLL100500 Differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	E20	PCKN[0]	PLL100500 Differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	F22	CFG[19]	Configurable I/O
Right	Bottom	VDDR[3]	D23	CFG[20]	Configurable I/O
Right	Bottom	VDDR[3]	G20	CFG[21]	Configurable I/O
Right	Bottom	VDDR[3]	C24	CFG[22]	Configurable I/O
Right	Bottom	VDDR[3]	E24	CFG[23]	Configurable I/O
Right	Bottom	VDDR[3]	H19	CFG[24]	Configurable I/O
Right	Bottom	VDDR[3]	J19	CFG[25]	Configurable I/O
Right	Bottom	VDDR[3]	G21	CFG[26]	Configurable I/O
Right	Bottom	VDDR[3]	G22	CFG[27]	Configurable I/O
Right	Bottom	VDDR[3]	E23	CFG[28]	Configurable I/O
Right	Bottom	VDDR[3]	C25	CFG[29]	Configurable I/O
Right	Bottom	VDDR[3]	D25	CFG[30]	Configurable I/O
Right	Bottom	VDDR[3]	H22	CFG[31]	Configurable I/O
Right	Bottom	VDDR[3]	K18	CFG[32]	Configurable I/O
Right	Bottom	VDDR[3]	J20	CFG[33]	Configurable I/O
(Sheet 6 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Right	Bottom	VDDR[3]	F23	CFG[34]	Configurable I/O
Right	Bottom	VDDR[3]	B26	CFG[35]	Configurable I/O
Right	Bottom	VDDR[3]	H21	CFG[36]	Configurable I/O
Right	Bottom	VDDR[3]	C26	CFG[37]	Configurable I/O
Right	Bottom	VDDR[3]	D26	CFG[38]	Configurable I/O
Right	Bottom	VDDR[3]	J21	CFG[39]	Configurable I/O
Right	Bottom	VDDR[3]	L17	CFG[40]	Configurable I/O
Right	Bottom	VDDR[3]	K19	CFG[41]	Configurable I/O
Right	Bottom	VDDR[4]	F24	CFG[42]	Configurable I/O
Right	Bottom	VDDR[4]	H23	CFG[43]	Configurable I/O
Right	Bottom	VDDR[4]	G24	CFG[44]	Configurable I/O
Right	Bottom	VDDR[4]	E25	CFG[45]	Configurable I/O
Right	Bottom	VDDR[4]	E26	CFG[46]	Configurable I/O
Right	Bottom	VDDR[4]	J23	CFG[47]	Configurable I/O
Right	Bottom	VDDR[4]	L18	CFG[48]	Configurable I/O
Right	Bottom	VDDR[4]	K20	CFG[49]	Configurable I/O
Right	Bottom	VDDR[4]	L21	CFG[50]	Configurable I/O
Right	Bottom	VDDR[4]	K22	CFG[51]	Configurable I/O
Right	Bottom	VDDR[4]	G25	CFG[52]	Configurable I/O
Right	Bottom	VDDR[4]	H25	CFG[53]	Configurable I/O
Right	Bottom	VDDR[4]	K23	CFG[54]	Configurable I/O
Right	Bottom	VDDR[4]	J24	CFG[55]	Configurable I/O
Right	Bottom	VDDR[4]	M18	CFG[56]	Configurable I/O
(Sheet 7 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Right	Bottom	VDDR[4]	M19	CFG[57]	Configurable I/O
Right	Bottom	VDDR[4]	F26	CFG[58]	Configurable I/O
Right	Bottom	VDDR[4]	L22	CFG[59]	Configurable I/O
Right	Bottom	VDDR[4]	G26	CFG[60]	Configurable I/O
Right	Bottom	VDDR[4]	H26	CFG[61]	Configurable I/O
Right	Bottom	VDDR[4]	K24	CFG[62]	Configurable I/O
Right	Bottom	VDDR[4]	J25	CFG[63]	Configurable I/O
Right	Bottom	VDDR[4]	L20	CFG[64]	Configurable I/O
Right	Bottom	VDDR[4]	M21	CFG[65]	Configurable I/O
Right	Bottom	VDDR[4]	N21	CFG[66]	Configurable I/O
Right	Bottom	VDDR[4]	J26	CFG[67]	Configurable I/O
Right	Bottom	VDDR[4]	M22	CFG[68]	Configurable I/O
Right	Bottom	VDDR[4]	L24	CFG[69]	Configurable I/O
Right	Bottom	VDDR[4]	K26	CFG[70]	Configurable I/O
Right	Bottom	VDDR[4]	M23	CFG[71]	Configurable I/O
Right	Bottom	VDDR[4]	N17	CFG[72]	Configurable I/O
Right	Bottom	VDDR[4]	N19	CFG[73]	Configurable I/O
Right	Bottom	VDDR[4]	L26	CFG[74]	Configurable I/O
Right	Bottom	VDDR[4]	L25	CFG[75]	Configurable I/O
Right	Bottom	VDDR[4]	M25	CFG[76]	Configurable I/O
Right	Bottom	VDDR[4]	M26	CFG[77]	Configurable I/O
Right	Bottom	VDDR[4]	N24	CFG[78]	Configurable I/O
Right	Bottom	VDDR[4]	N23	CFG[79]	Configurable I/O
(Sheet 8 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Right	Bottom	VDDR[4]	P21	CFG[80]	Configurable I/O
Right	Bottom	VDDR[4]	P19	CFG[81]	Configurable I/O
Right	Bottom	VDDR[5]	N26	CFG[82]	Configurable I/O
Right	Bottom	VDDR[5]	P23	CFG[83]	Configurable I/O
Right	Bottom	VDDR[5]	P24	CFG[84]	Configurable I/O
Right	Bottom	VDDR[5]	P26	CFG[85]	Configurable I/O
Right	Bottom	VDDR[5]	R26	CFG[86]	Configurable I/O
Right	Bottom	VDDR[5]	R25	CFG[87]	Configurable I/O
Right	Bottom	VDDR[5]	P17	CFG[88]	Configurable I/O
Right	Bottom	VDDR[5]	R21	CFG[89]	Configurable I/O
Right	Bottom	VDDR[5]	R23	CFG[90]	Configurable I/O
Right	Bottom	VDDR[5]	T26	CFG[91]	Configurable I/O
Right	Bottom	VDDR[5]	R22	CFG[92]	Configurable I/O
Right	Bottom	VDDR[5]	T25	CFG[93]	Configurable I/O
Right	Bottom	VDDR[5]	T24	CFG[94]	Configurable I/O
Right	Bottom	VDDR[5]	U26	CFG[95]	Configurable I/O
Right	Bottom	VDDR[5]	T21	CFG[96]	Configurable I/O
Right	Bottom	VDDR[5]	R19	CFG[97]	Configurable I/O
Right	Bottom	VDDR[5]	V26	CFG[98]	Configurable I/O
Right	Bottom	VDDR[5]	U24	CFG[99]	Configurable I/O
Right	Bottom	VDDR[5]	V25	CFG[100]	Configurable I/O
Right	Bottom	VDDR[5]	T22	CFG[101]	Configurable I/O
Right	Bottom	VDDR[5]	W26	CFG[102]	Configurable I/O
(Sheet 9 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Right	Bottom	VDDR[5]	U23	CFG[103]	Configurable I/O
Right	Bottom	VDDR[5]	R18	CFG[104]	Configurable I/O
Right	Bottom	VDDR[5]	U20	CFG[105]	Configurable I/O
Right	Bottom	VDDR[5]	U22	CFG[106]	Configurable I/O
Right	Bottom	VDDR[5]	V24	CFG[107]	Configurable I/O
Right	Bottom	VDDR[5]	Y26	CFG[108]	Configurable I/O
Right	Bottom	VDDR[5]	V23	CFG[109]	Configurable I/O
Right	Bottom	VDDR[5]	W25	CFG[110]	Configurable I/O
Right	Bottom	VDDR[5]	Y25	CFG[111]	Configurable I/O
Right	Bottom	VDDR[5]	T18	CFG[112]	Configurable I/O
Right	Bottom	VDDR[5]	T20	CFG[113]	Configurable I/O
Right	Bottom	VDDR[5]	Y24	CFG[114]	Configurable I/O
Right	Bottom	VDDR[5]	AA26	CFG[115]	Configurable I/O
Right	Bottom	VDDR[5]	W23	CFG[116]	Configurable I/O
Right	Bottom	VDDR[5]	AA24	CFG[117]	Configurable I/O
Right	Bottom	VDDR[5]	W22	CFG[118]	Configurable I/O
Right	Bottom	VDDR[5]	V21	CFG[119]	Configurable I/O
Right	Bottom	VDDR[5]	T17	CFG[120]	Configurable I/O
Right	Bottom	VDDR[5]	U19	CFG[121]	Configurable I/O
Right	Bottom	VDDR[6]	AB25	CFG[122]	Configurable I/O
Right	Bottom	VDDR[6]	W21	CFG[123]	Configurable I/O
Right	Bottom	VDDR[6]	AD26	CFG[124]	Configurable I/O
Right	Bottom	VDDR[6]	AB24	CFG[125]	Configurable I/O
(Sheet 10 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Right	Bottom	VDDR[6]	Y22	CFG[126]	Configurable I/O
Right	Bottom	VDDR[6]	AC26	CFG[127]	Configurable I/O
Right	Bottom	VDDR[6]	V20	CFG[128]	Configurable I/O
Right	Bottom	VDDR[6]	V19	CFG[129]	Configurable I/O
Right	Bottom	VDDR[6]	AE26	CFG[130]	Configurable I/O
Right	Bottom	VDDR[6]	AC25	CFG[131]	Configurable I/O
Right	Bottom	VDDR[6]	AB23	CFG[132]	Configurable I/O
Right	Bottom	VDDR[6]	AD25	CFG[133]	Configurable I/O
Right	Bottom	VDDR[6]	AF25	CFG[134]	Configurable I/O
Right	Bottom	VDDR[6]	AA23	CFG[135]	Configurable I/O
Right	Bottom	VDDR[6]	U18	CFG[136]	Configurable I/O
Right	Bottom	VDDR[6]	W19	CFG[137]	Configurable I/O
Right	Bottom	VDDR[6]	AA22	CFG[138]	Configurable I/O
Right	Bottom	VDDR[6]	Y21	CFG[139]	Configurable I/O
Right	Bottom	VDDR[6]	AC23	CFG[140]	Configurable I/O
Right	Bottom	VDDR[6]	Y20	CFG[141]	Configurable I/O
Right	Bottom	VDDR[6]	AD24	CFG[142]	Configurable I/O
Bottom	Right	VDDR[7]	AB19	PCKP[1]	PLL601250 Differential clock input / Configurable I/O
Bottom	Right	VDDR[7]	AA19	PCKN[1]	PLL601250 Differential clock input / Configurable I/O
Bottom	Right	VDDR[7]	AE23	CFG[143]	Configurable I/O
Bottom	Right	VDDR[7]	AC21	CFG[144]	Configurable I/O
Bottom	Right	VDDR[7]	AC22	CFG[145]	Configurable I/O
(Sheet 11 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Bottom	Right	VDDR[7]	AD22	CFG[146]	Configurable I/O
Bottom	Right	VDDR[7]	AD21	CFG[147]	Configurable I/O
Bottom	Right	VDDR[7]	AB21	CFG[148]	Configurable I/O
Bottom	Right	VDDR[7]	AE24	CFG[149]	Configurable I/O
Bottom	Right	VDDGCK[3]	AF23	RSVD[2]	Reserved
Bottom	Right	VDDGCK[3]	AF24	RSVD[3]	Reserved
Bottom	Right	VDDGCK[3]	AE22	GCKP[2]	GigaBlaze differential TX reference clock
Bottom	Right	VDDGCK[3]	AF22	GCKN[2]	GigaBlaze differential TX reference clock
Bottom	Right	VDDG[5]	AE20	GRXN[16]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AD20	GRXP[16]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	V16	GTXP[16]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	U16	GTXN[16]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	W18	GTXN[17]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	Y18	GTXP[17]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	AF19	GRXP[17]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AF20	GRXN[17]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AD17	GRXN[18]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AD18	GRXP[18]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	Y16	GTXP[18]	GigaBlaze TX differential pair
(Sheet 12 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Bottom	Right	VDDG[5]	Y17	GTXN[18]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	V17	GTXN[19]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	W17	GTXP[19]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	AE19	GRXP[19]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AE18	GRXN[19]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AF16	GRXN[20]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AF17	GRXP[20]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	V15	GTXP[20]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	W15	GTXN[20]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AB16	GTXN[21]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AB15	GTXP[21]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AE15	GRXP[21]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AE16	GRXN[21]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AF15	GRXN[22]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AF14	GRXP[22]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AA15	GTXP[22]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AA14	GTXN[22]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	U14	GTXN[23]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	U13	GTXP[23]	GigaBlaze TX differential pair
(Sheet 13 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Bottom	Right	VDDG[6]	AD14	GRXP[23]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AD13	GRXN[23]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AF11	GRXN[24]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AF12	GRXP[24]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AA13	GTXP[24]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AA12	GTXN[24]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	W13	GTXN[25]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	W14	GTXP[25]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AE11	GRXP[25]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AE12	GRXN[25]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AF09	GRXN[26]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AF10	GRXP[26]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AB11	GTXP[26]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AA11	GTXN[26]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	V12	GTXN[27]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	W12	GTXP[27]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AD11	GRXP[27]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AD10	GRXN[27]	GigaBlaze RX differential pair
(Sheet 14 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Bottom	Right	VDDG[8]	AF07	GRXN[28]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AF06	GRXP[28]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	W10	GTXP[28]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	V10	GTXN[28]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	Y11	GTXN[29]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	Y10	GTXP[29]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	AE07	GRXP[29]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AE08	GRXN[29]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AD07	GRXN[30]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AD06	GRXP[30]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	W09	GTXP[30]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	Y09	GTXN[30]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	V11	GTXN[31]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	U11	GTXP[31]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	AC09	GRXP[31]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AC08	GRXN[31]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AB08	GBRTRIM	GigaBlaze RTRIM
Bottom	Right	VDDGCK[4]	AE05	GCKP[3]	GigaBlaze differential TX reference clock
(Sheet 15 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Bottom	Right	VDDGCK[4]	AF05	GCKN[3]	GigaBlaze differential TX reference clock
Bottom	Right	VDDR[8]	AB07	TMS	Reserved Test
Bottom	Right	VDDR[8]	AA08	TDI	Reserved Test
Bottom	Right	VDDR[8]	AD05	TCK	Reserved Test
Bottom	Right	VDDR[8]	AC06	TRSTN	Reserved Test
Bottom	Right	VDDR[8]	AE04	TN	Reserved Test
Bottom	Right	VDDR[8]	AC05	IDDT	Reserved Test
Bottom	Right	VDDR[8]	AE03	TDO	Reserved Test
Bottom	Right	VDDR[8]	AF03	SEN	Reserved Test
Bottom	Right	VDDR[8]	AF02	PMON	Reserved Test
Left	Top	VDDR[9]	Y07	PCKP[2]	PLL100500 Differential clock input / Configurable I/O
Left	Top	VDDR[9]	Y06	PCKN[2]	PLL100500 Differential clock input / Configurable I/O
Left	Top	VDDR[9]	AD03	CFG[150]	Configurable I/O
Left	Top	VDDR[9]	AC04	CFG[151]	Configurable I/O
Left	Top	VDDR[9]	AA05	CFG[152]	Configurable I/O
Left	Top	VDDR[9]	AB04	CFG[153]	Configurable I/O
Left	Top	VDDR[9]	Y05	CFG[154]	Configurable I/O
Left	Top	VDDR[9]	AC02	CFG[155]	Configurable I/O
Left	Top	VDDR[9]	AD02	CFG[156]	Configurable I/O
Left	Top	VDDR[9]	AA04	CFG[157]	Configurable I/O
Left	Top	VDDR[9]	AE01	CFG[158]	Configurable I/O
(Sheet 16 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Left	Top	VDDR[9]	AB03	CFG[159]	Configurable I/O
Left	Top	VDDR[9]	W06	CFG[160]	Configurable I/O
Left	Top	VDDR[9]	AC01	CFG[161]	Configurable I/O
Left	Top	VDDR[9]	AD01	CFG[162]	Configurable I/O
Left	Top	VDDR[9]	V06	CFG[163]	Configurable I/O
Left	Top	VDDR[9]	W05	CFG[164]	Configurable I/O
Left	Top	VDDR[9]	AB02	CFG[165]	Configurable I/O
Left	Top	VDDR[9]	AA03	CFG[166]	Configurable I/O
Left	Top	VDDR[9]	W08	CFG[167]	Configurable I/O
Left	Top	VDDR[9]	V08	CFG[168]	Configurable I/O
Left	Top	VDDR[9]	W04	CFG[169]	Configurable I/O
Left	Top	VDDR[9]	U07	CFG[170]	Configurable I/O
Left	Top	VDDR[9]	Y03	CFG[171]	Configurable I/O
Left	Top	VDDR[9]	AB01	CFG[172]	Configurable I/O
Left	Top	VDDR[9]	AA01	CFG[173]	Configurable I/O
Left	Top	VDDR[9]	Y02	CFG[174]	Configurable I/O
Left	Top	VDDR[9]	U09	CFG[175]	Configurable I/O
Left	Top	VDDR[9]	U08	CFG[176]	Configurable I/O
Left	Top	VDDR[9]	U05	CFG[177]	Configurable I/O
Left	Top	VDDR[9]	V04	CFG[178]	Configurable I/O
Left	Top	VDDR[9]	W02	CFG[179]	Configurable I/O
Left	Top	VDDR[9]	Y01	CFG[180]	Configurable I/O
Left	Top	VDDR[9]	V03	CFG[181]	Configurable I/O
(Sheet 17 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Left	Top	VDDR[9]	T07	CFG[182]	Configurable I/O
Left	Top	VDDR[9]	T09	CFG[183]	Configurable I/O
Left	Top	VDDR[9]	V07	CFG[184]	Configurable I/O
Left	Top	VDDR[9]	W01	CFG[185]	Configurable I/O
Left	Top	VDDR[9]	U04	CFG[186]	Configurable I/O
Left	Top	VDDR[9]	T06	CFG[187]	Configurable I/O
Left	Top	VDDR[9]	T10	CFG[188]	Configurable I/O
Left	Top	VDDR[9]	R08	CFG[189]	Configurable I/O
Left	Top	VDDR[10]	R09	CFG[190]	Configurable I/O
Left	Top	VDDR[10]	T05	CFG[191]	Configurable I/O
Left	Top	VDDR[10]	R05	CFG[192]	Configurable I/O
Left	Top	VDDR[10]	T03	CFG[193]	Configurable I/O
Left	Top	VDDR[10]	V01	CFG[194]	Configurable I/O
Left	Top	VDDR[10]	R06	CFG[195]	Configurable I/O
Left	Top	VDDR[10]	U01	CFG[196]	Configurable I/O
Left	Top	VDDR[10]	R04	CFG[197]	Configurable I/O
Left	Top	VDDR[10]	T02	CFG[198]	Configurable I/O
Left	Top	VDDR[10]	P08	CFG[199]	Configurable I/O
Left	Top	VDDR[10]	P10	CFG[200]	Configurable I/O
Left	Top	VDDR[10]	R02	CFG[201]	Configurable I/O
Left	Top	VDDR[10]	T01	CFG[202]	Configurable I/O
Left	Top	VDDR[10]	R01	CFG[203]	Configurable I/O
Left	Top	VDDR[10]	P03	CFG[204]	Configurable I/O
(Sheet 18 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Left	Top	VDDR[10]	P04	CFG[205]	Configurable I/O
Left	Top	VDDR[10]	P01	CFG[206]	Configurable I/O
Left	Top	VDDR[10]	P06	CFG[207]	Configurable I/O
Left	Top	VDDR[10]	N08	CFG[208]	Configurable I/O
Left	Top	VDDR[10]	N04	CFG[209]	Configurable I/O
Left	Top	VDDR[10]	N03	CFG[210]	Configurable I/O
Left	Top	VDDR[10]	N01	CFG[211]	Configurable I/O
Left	Top	VDDR[10]	M01	CFG[212]	Configurable I/O
Left	Top	VDDR[10]	M02	CFG[213]	Configurable I/O
Left	Top	VDDR[10]	L01	CFG[214]	Configurable I/O
Left	Top	VDDR[10]	N10	CFG[215]	Configurable I/O
Left	Top	VDDR[10]	N06	CFG[216]	Configurable I/O
Left	Top	VDDR[10]	K01	CFG[217]	Configurable I/O
Left	Top	VDDR[10]	L02	CFG[218]	Configurable I/O
Left	Top	VDDR[10]	M04	CFG[219]	Configurable I/O
Left	Top	VDDR[10]	L03	CFG[220]	Configurable I/O
Left	Top	VDDR[10]	J01	CFG[221]	Configurable I/O
Left	Top	VDDR[10]	M05	CFG[222]	Configurable I/O
Left	Top	VDDR[10]	M06	CFG[223]	Configurable I/O
Left	Top	VDDR[10]	M08	CFG[224]	Configurable I/O
Left	Top	VDDR[10]	J02	CFG[225]	Configurable I/O
Left	Top	VDDR[10]	K03	CFG[226]	Configurable I/O
Left	Top	VDDR[10]	H01	CFG[227]	Configurable I/O
(Sheet 19 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Left	Top	VDDR[10]	G01	CFG[228]	Configurable I/O
Left	Top	VDDR[10]	J03	CFG[229]	Configurable I/O
Left	Top	VDDR[10]	H02	CFG[230]	Configurable I/O
Left	Top	VDDR[10]	M09	CFG[231]	Configurable I/O
Left	Top	VDDR[10]	K07	CFG[232]	Configurable I/O
Left	Top	VDDR[10]	L05	CFG[233]	Configurable I/O
Left	Top	VDDR[10]	K04	CFG[234]	Configurable I/O
Left	Top	VDDR[10]	F01	CFG[235]	Configurable I/O
Left	Top	VDDR[10]	J04	CFG[236]	Configurable I/O
Left	Top	VDDR[10]	L06	CFG[237]	Configurable I/O
Left	Top	VDDR[10]	K05	CFG[238]	Configurable I/O
Left	Top	VDDR[10]	J07	CFG[239]	Configurable I/O
Left	Top	VDDR[10]	L07	CFG[240]	Configurable I/O
Left	Top	VDDR[10]	E01	CFG[241]	Configurable I/O
Left	Top	VDDR[10]	G02	CFG[242]	Configurable I/O
Left	Top	VDDR[10]	G03	CFG[243]	Configurable I/O
Left	Top	VDDR[10]	H04	CFG[244]	Configurable I/O
Left	Top	VDDR[10]	K08	CFG[245]	Configurable I/O
Left	Top	VDDR[10]	L09	CFG[246]	Configurable I/O
Left	Top	VDDR[11]	K09	CFG[247]	Configurable I/O
Left	Top	VDDR[11]	J08	CFG[248]	Configurable I/O
Left	Top	VDDR[11]	E02	CFG[249]	Configurable I/O
Left	Top	VDDR[11]	D01	CFG[250]	Configurable I/O
(Sheet 20 of 21)					

Table A.6 FC672 Package I/O Assignments (RC11XT432)

Package Edge	Die Edge	Domain	FC672 Package Ball	Signal	Description
Left	Top	VDDR[11]	H05	CFG[251]	Configurable I/O
Left	Top	VDDR[11]	J06	CFG[252]	Configurable I/O
Left	Top	VDDR[11]	C01	CFG[253]	Configurable I/O
Left	Top	VDDR[11]	D02	CFG[254]	Configurable I/O
Left	Top	VDDR[11]	H08	CFG[255]	Configurable I/O
Left	Top	VDDR[11]	F04	CFG[256]	Configurable I/O
Left	Top	VDDR[11]	H06	CFG[257]	Configurable I/O
Left	Top	VDDR[11]	G05	CFG[258]	Configurable I/O
Left	Top	VDDR[11]	F05	CFG[259]	Configurable I/O
Left	Top	VDDR[11]	E03	CFG[260]	Configurable I/O
Left	Top	VDDR[11]	E04	CFG[261]	Configurable I/O
Left	Top	VDDR[11]	C02	CFG[262]	Configurable I/O
Left	Top	VDDR[11]	G06	CFG[263]	Configurable I/O
Left	Top	VDDR[11]	G07	CFG[264]	Configurable I/O
Left	Top	VDDR[11]	C03	CFG[265]	Configurable I/O
(Sheet 21 of 21)					

A.3 FC896 Package and Pinouts

The FC896 package is a high-performance 31 mm body size EPBGA with an integral copper heat spreader. It has 896 pins arranged in a 30 x 30 matrix. This arrangement offers high I/O density with good electrical and thermal characteristics. The FC896 package is used for three RapidChip Xtreme platform ASICs:

- RC11XT416
- RC11XT432

- RC11XT531

A.3.1 RC11XT416 in the FC896 Package

Figure A.6 is a color-coded diagram of the RC11XT416 in the FC896 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure A.4 RC11XT416 in the FC896 Package Diagram

TBD

[Table A.7](#) lists the power connections for the RC11XT416 in the FC896 package. The core logic and I/Os share a common ground (V_{SS}).

Table A.7 FC896 Package Power Connections (RC11XT416)

VDD Plane	Package Ball Locations	Description
TBD	TBD	TBD

[Table A.8](#) lists the RC11XT416 in the FC896 package I/O assignments.

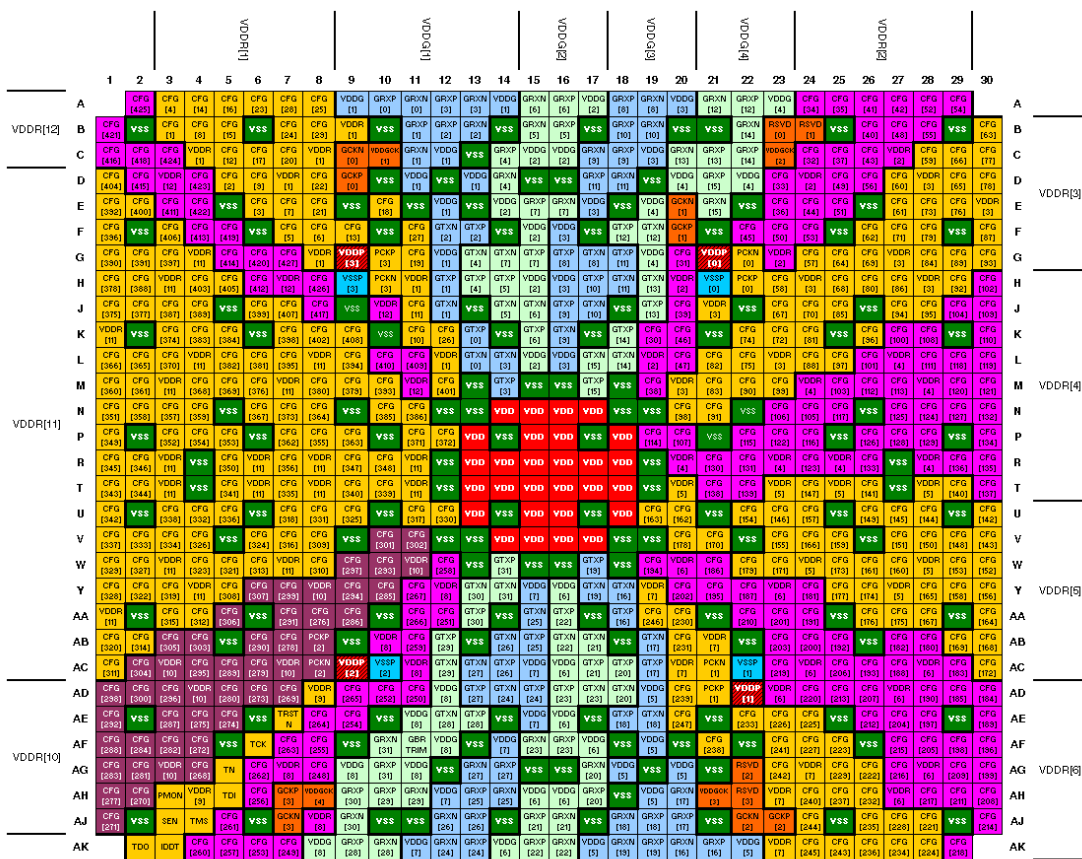
Table A.8 FC896 Package I/O Assignments (RC11XT416)

Package Side	VDDR Region Split	FC896 Package Ball	I/O Name	Description
TBD	TBD	TBD	TBD	TBD

A.3.2 RC11XT432 in the FC896 Package

[Figure A.5](#) is a color-coded diagram of the RC11XT432 in the FC896 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure A.5 RC11XT432 in the FC896 Package Diagram



VSS Global VSS Ground Plane for Core Logic and Configurable I/O

VDD VDD Power Supply for Core Logic

VDDP Independent VDD Power Supply for PLL

VSSP Independent VSS Power Supply for PLL

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDG VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

VDDR VDDR Power Supply Split Region for Configurable I/O

Note: To help distinguish between adjacent VDDR Splits, 2 alternating colors for VDD are used for Splits 1 through 10. A third color is used for Split 11 to distinguish it from splits 1 and 10. All splits are electrically independent of each other.

VDDGCK 3.3V I/O Power Supply Region for GigaBlaze Clock Input Receiver

VDDG Power Supply Split Region for GigaBlaze Differential Pairs

VDDG Power Supply Split Region for GigaBlaze Differential Pairs

Note: To help distinguish between adjacent Power Supply Splits for the GigaBlaze differential pairs, 2 alternating colors are used for Splits VDDG[1] through VDDG[3]. All Splits are electrically independent of each other.

Table A.9 lists the FC896 package power connections. The core logic and I/Os share a common ground (V_{SS}). All the core logic is powered from a single power domain (V_{DD}). The I/Os are distributed across 12 separate power domains ($V_{DDR}[1:12]$). The four PLLs are isolated; each PLL has its own dedicated power ($V_{DDP}[0:3]$) and ground ($V_{SSP}[0:3]$) connection.

Table A.9 FC896 Package Power Connections (RC11XT432)

VDD Plane	Package Ball Location(s)	Description
VDD	N14, N15, N16, N17, P13, P15, P16, P18, R13, R14, R15, R16, R17, R18, T13, T14, T15, T16, T17, T18, U13, U15, U16, U18, V14, V15, V16, V17	Core Logic VDD
VSS	B02, B06, B10, B14, B17, B20, B21, B25, B29, C13, D10, D12, D15, D16, D19, E05, E09, E11, E13, E18, E22, E26, F02, F06, F10, F14, F17, F21, F25, F29, J05, J09, J13, J18, J22, J26, K02, K06, K10, K14, K17, K21, K25, K29, M13, M15, M16, M18, N05, N09, N12, N13, N18, N19, N22, N26, P02, P06, P10, P14, P17, P21, P25, P29, R04, R12, R19, R27, T04, T12, T19, T27, U02, U06, U10, U14, U17, U21, U25, U29, V05, V09, V12, V13, V18, V19, V22, V26, W13, W15, W16, W18, AA02, AA06, AA10, AA14, AA17, AA21, AA25, AA29, AB05, AB09, AB13, AB18, AB22, AB26, AE02, AE06, AE10, AE14, AE17, AE21, AE25, AE29, AF05, AF09, AF13, AF18, AF20, AF22, AF26, AG12, AG15, AG16, AG19, AG21, AH18, AJ02, AJ06, AJ10, AJ11, AJ14, AJ17, AJ21, AJ25, AJ29	Core Logic & Configurable I/O Ground
VDDG[1]	A09, A14, C12, D11, D13, E12, G12	GigaBlaze VDD
VDDG[2]	A17, C15, C16, E14, F15, H15, L15	GigaBlaze VDD
VDDG[3]	A20, C19, E17, F16, H16, L16	GigaBlaze VDD
VDDG[4]	A23, D20, D22, E19, G19	GigaBlaze VDD
VDDG[5]	AD19, AF19, AG18, AG20, AH19, AK17, AK22	GigaBlaze VDD
VDDG[6]	Y16, AC16, AE16, AF17, AH15, AH16, AK14	GigaBlaze VDD
VDDG[7]	Y15, AC15, AE15, AF14, AH12, AK11	GigaBlaze VDD
VDDG[8]	AD12, AE11, AF12, AG09, AG11, AK08	GigaBlaze VDD
VDDGCK[1]	C10	Dedicated 3.3V VDD for GigaBlaze TX clock input
(Sheet 1 of 2)		

Table A.9 FC896 Package Power Connections (RC11XT432) (Cont.)

VDD Plane	Package Ball Location(s)	Description
VDDGCK[2]	C23	Dedicated 3.3V VDD for GigaBlaze TX clock input
VDDGCK[3]	AH21	Dedicated 3.3V VDD for GigaBlaze TX clock input
VDDGCK[4]	AH08	Dedicated 3.3V VDD for GigaBlaze TX clock input
VDDR[1]	B09, C04, C08, D07, G08, H11, L12	Configurable I/O VDD
VDDR[2]	C27, D24, G23, H20, L19	Configurable I/O VDD
VDDR[3]	D28, E30, G27, H24, H28, J21, L23, M20	Configurable I/O VDD
VDDR[4]	L27, M24, M28, R20, R23, R25, R28	Configurable I/O VDD
VDDR[5]	T20, T23, T25, T28, W24, W28, Y27	Configurable I/O VDD
VDDR[6]	W20, Y23, AC24, AC28, AD23, AD27, AG28, AH27	Configurable I/O VDD
VDDR[7]	Y19, AB21, AC20, AG24, AH23, AK23	Configurable I/O VDD
VDDR[8]	Y12, AB10, AC11, AG07, AJ08	Configurable I/O VDD
VDDR[9]	AD08, AH04	Configurable I/O VDD
VDDR[10]	W11, Y08, AC03, AC07, AD04, AG03	Configurable I/O VDD
VDDR[11]	G04, H03, K01, L04, L08, M03, M07, R03, R06, R08, R11, T03, T06, T08, T11, W03, W07, Y04, AA01	Configurable I/O VDD
VDDR[12]	D03, H07, J10, M11	Configurable I/O VDD
VDDP[0]	G21	PLL VDD
VDDP[1]	AD22	PLL VDD
VDDP[2]	AC09	PLL VDD
VDDP[3]	G09	PLL VDD
VSSP[0]	H21	PLL Ground
VSSP[1]	AC22	PLL Ground
VSSP[2]	AC10	PLL Ground
VSSP[3]	H09	PLL Ground
(Sheet 2 of 2)		

Table A.10 lists the I/O assignments for the RC11XT432 FC896 package.

Table A.10 FC896 Package I/O Signals (RC11XT432)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDR[1]	G10	PCKP[3]	PLL100500 Differential clock input / Configurable I/O
Top	Left	VDDR[1]	H10	PCKN[3]	PLL100500 Differential clock input / Configurable I/O
Top	Left	VDDR[1]	B03	CFG[1]	Configurable I/O
Top	Left	VDDR[1]	D05	CFG[2]	Configurable I/O
Top	Left	VDDR[1]	E06	CFG[3]	Configurable I/O
Top	Left	VDDR[1]	A03	CFG[4]	Configurable I/O
Top	Left	VDDR[1]	F07	CFG[5]	Configurable I/O
Top	Left	VDDR[1]	F08	CFG[6]	Configurable I/O
Top	Left	VDDR[1]	E07	CFG[7]	Configurable I/O
Top	Left	VDDR[1]	B04	CFG[8]	Configurable I/O
Top	Left	VDDR[1]	D06	CFG[9]	Configurable I/O
Top	Left	VDDR[1]	K11	CFG[10]	Configurable I/O
Top	Left	VDDR[1]	J11	CFG[11]	Configurable I/O
Top	Left	VDDR[1]	C05	CFG[12]	Configurable I/O
Top	Left	VDDR[1]	F09	CFG[13]	Configurable I/O
Top	Left	VDDR[1]	A04	CFG[14]	Configurable I/O
Top	Left	VDDR[1]	B05	CFG[15]	Configurable I/O
Top	Left	VDDR[1]	A05	CFG[16]	Configurable I/O
Top	Left	VDDR[1]	C06	CFG[17]	Configurable I/O
Top	Left	VDDR[1]	E10	CFG[18]	Configurable I/O
(Sheet 1 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDR[1]	G11	CFG[19]	Configurable I/O
Top	Left	VDDR[1]	C07	CFG[20]	Configurable I/O
Top	Left	VDDR[1]	E08	CFG[21]	Configurable I/O
Top	Left	VDDR[1]	D08	CFG[22]	Configurable I/O
Top	Left	VDDR[1]	A06	CFG[23]	Configurable I/O
Top	Left	VDDR[1]	B07	CFG[24]	Configurable I/O
Top	Left	VDDR[1]	A08	CFG[25]	Configurable I/O
Top	Left	VDDR[1]	K12	CFG[26]	Configurable I/O
Top	Left	VDDR[1]	F11	CFG[27]	Configurable I/O
Top	Left	VDDR[1]	A07	CFG[28]	Configurable I/O
Top	Left	VDDR[1]	B08	CFG[29]	Configurable I/O
Top	Left	VDDGCK[1]	D09	GCKP[0]	GigaBlaze differential TX reference clock
Top	Left	VDDGCK[1]	C09	GCKN[0]	GigaBlaze differential TX reference clock
Top	Left	VDDG[1]	A11	GRXN[0]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	A10	GRXP[0]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	K13	GTXP[0]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	L13	GTXN[0]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	J12	GTXN[1]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	H12	GTXP[1]	GigaBlaze TX differential pair
(Sheet 2 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDG[1]	B11	GRXP[1]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	C11	GRXN[1]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	B13	GRXN[2]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	B12	GRXP[2]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	F13	GTXP[2]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	F12	GTXN[2]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	L14	GTXN[3]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	M14	GTXP[3]	GigaBlaze TX differential pair
Top	Left	VDDG[1]	A12	GRXP[3]	GigaBlaze RX differential pair
Top	Left	VDDG[1]	A13	GRXN[3]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	D14	GRXN[4]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	C14	GRXP[4]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	H13	GTXP[4]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	G13	GTXN[4]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	J14	GTXN[5]	GigaBlaze TX differential pair
(Sheet 3 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDG[2]	H14	GTXP[5]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	B16	GRXP[5]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	B15	GRXN[5]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	A15	GRXN[6]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	A16	GRXP[6]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	K15	GTXP[6]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	J15	GTXN[6]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	G14	GTXN[7]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	G15	GTXP[7]	GigaBlaze TX differential pair
Top	Left	VDDG[2]	E15	GRXP[7]	GigaBlaze RX differential pair
Top	Left	VDDG[2]	E16	GRXN[7]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	A19	GRXN[8]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	A18	GRXP[8]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	G16	GTXP[8]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	G17	GTXN[8]	GigaBlaze TX differential pair
(Sheet 4 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDG[3]	K16	GTXN[9]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	J16	GTXP[9]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	C18	GRXP[9]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	C17	GRXN[9]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	B19	GRXN[10]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	B18	GRXP[10]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	H17	GTXP[10]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	J17	GTXN[10]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	H18	GTXN[11]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	G18	GTXP[11]	GigaBlaze TX differential pair
Top	Left	VDDG[3]	D17	GRXP[11]	GigaBlaze RX differential pair
Top	Left	VDDG[3]	D18	GRXN[11]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	A21	GRXN[12]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	A22	GRXP[12]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	F18	GTXP[12]	GigaBlaze TX differential pair
(Sheet 5 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDG[4]	F19	GTXN[12]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	H19	GTXN[13]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	J19	GTXP[13]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	C21	GRXP[13]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	C20	GRXN[13]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	B22	GRXN[14]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	C22	GRXP[14]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	K18	GTXP[14]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	L18	GTXN[14]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	L17	GTXN[15]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	M17	GTXP[15]	GigaBlaze TX differential pair
Top	Left	VDDG[4]	D21	GRXP[15]	GigaBlaze RX differential pair
Top	Left	VDDG[4]	E21	GRXN[15]	GigaBlaze RX differential pair
Top	Left	VDDGCK[2]	F20	GCKP[1]	GigaBlaze differential TX reference clock
Top	Left	VDDGCK[2]	E20	GCKN[1]	GigaBlaze differential TX reference clock
(Sheet 6 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDGCK[2]	B23	RSVD[0]	Reserved
Top	Left	VDDGCK[2]	B24	RSVD[1]	Reserved
Top	Left	VDDR[2]	K19	CFG[30]	Configurable I/O
Top	Left	VDDR[2]	G20	CFG[31]	Configurable I/O
Top	Left	VDDR[2]	C24	CFG[32]	Configurable I/O
Top	Left	VDDR[2]	D23	CFG[33]	Configurable I/O
Top	Left	VDDR[2]	A24	CFG[34]	Configurable I/O
Top	Left	VDDR[2]	A25	CFG[35]	Configurable I/O
Top	Left	VDDR[2]	E23	CFG[36]	Configurable I/O
Top	Left	VDDR[2]	C25	CFG[37]	Configurable I/O
Top	Left	VDDR[2]	M19	CFG[38]	Configurable I/O
Top	Left	VDDR[2]	J20	CFG[39]	Configurable I/O
Top	Left	VDDR[2]	B26	CFG[40]	Configurable I/O
Top	Left	VDDR[2]	A26	CFG[41]	Configurable I/O
Top	Left	VDDR[2]	A27	CFG[42]	Configurable I/O
Top	Left	VDDR[2]	C26	CFG[43]	Configurable I/O
Top	Left	VDDR[2]	E24	CFG[44]	Configurable I/O
Top	Left	VDDR[2]	F22	CFG[45]	Configurable I/O
Top	Left	VDDR[2]	K20	CFG[46]	Configurable I/O
Top	Left	VDDR[2]	L20	CFG[47]	Configurable I/O
Top	Left	VDDR[2]	B27	CFG[48]	Configurable I/O
Top	Left	VDDR[2]	D25	CFG[49]	Configurable I/O
Top	Left	VDDR[2]	F23	CFG[50]	Configurable I/O
(Sheet 7 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDR[2]	E25	CFG[51]	Configurable I/O
Top	Left	VDDR[2]	A28	CFG[52]	Configurable I/O
Top	Left	VDDR[2]	F24	CFG[53]	Configurable I/O
Top	Left	VDDR[2]	A29	CFG[54]	Configurable I/O
Top	Left	VDDR[2]	B28	CFG[55]	Configurable I/O
Top	Left	VDDR[2]	D26	CFG[56]	Configurable I/O
Right	Bottom	VDDR[3]	H22	PCKP[0]	PLL100500 Differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	G22	PCKN[0]	PLL100500 Differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	G24	CFG[57]	Configurable I/O
Right	Bottom	VDDR[3]	H23	CFG[58]	Configurable I/O
Right	Bottom	VDDR[3]	C28	CFG[59]	Configurable I/O
Right	Bottom	VDDR[3]	D27	CFG[60]	Configurable I/O
Right	Bottom	VDDR[3]	E27	CFG[61]	Configurable I/O
Right	Bottom	VDDR[3]	F26	CFG[62]	Configurable I/O
Right	Bottom	VDDR[3]	B30	CFG[63]	Configurable I/O
Right	Bottom	VDDR[3]	G25	CFG[64]	Configurable I/O
Right	Bottom	VDDR[3]	D29	CFG[65]	Configurable I/O
Right	Bottom	VDDR[3]	C29	CFG[66]	Configurable I/O
Right	Bottom	VDDR[3]	J23	CFG[67]	Configurable I/O
Right	Bottom	VDDR[3]	H25	CFG[68]	Configurable I/O
Right	Bottom	VDDR[3]	G26	CFG[69]	Configurable I/O
(Sheet 8 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[3]	J24	CFG[70]	Configurable I/O
Right	Bottom	VDDR[3]	F27	CFG[71]	Configurable I/O
Right	Bottom	VDDR[3]	K23	CFG[72]	Configurable I/O
Right	Bottom	VDDR[3]	E28	CFG[73]	Configurable I/O
Right	Bottom	VDDR[3]	K22	CFG[74]	Configurable I/O
Right	Bottom	VDDR[3]	L22	CFG[75]	Configurable I/O
Right	Bottom	VDDR[3]	E29	CFG[76]	Configurable I/O
Right	Bottom	VDDR[3]	C30	CFG[77]	Configurable I/O
Right	Bottom	VDDR[3]	D30	CFG[78]	Configurable I/O
Right	Bottom	VDDR[3]	F28	CFG[79]	Configurable I/O
Right	Bottom	VDDR[3]	H26	CFG[80]	Configurable I/O
Right	Bottom	VDDR[3]	K24	CFG[81]	Configurable I/O
Right	Bottom	VDDR[3]	L21	CFG[82]	Configurable I/O
Right	Bottom	VDDR[3]	M21	CFG[83]	Configurable I/O
Right	Bottom	VDDR[3]	G28	CFG[84]	Configurable I/O
Right	Bottom	VDDR[3]	J25	CFG[85]	Configurable I/O
Right	Bottom	VDDR[3]	H27	CFG[86]	Configurable I/O
Right	Bottom	VDDR[3]	F30	CFG[87]	Configurable I/O
Right	Bottom	VDDR[3]	L24	CFG[88]	Configurable I/O
Right	Bottom	VDDR[3]	G29	CFG[89]	Configurable I/O
Right	Bottom	VDDR[3]	M22	CFG[90]	Configurable I/O
Right	Bottom	VDDR[3]	N21	CFG[91]	Configurable I/O
Right	Bottom	VDDR[3]	H29	CFG[92]	Configurable I/O
(Sheet 9 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[3]	G30	CFG[93]	Configurable I/O
Right	Bottom	VDDR[3]	J27	CFG[94]	Configurable I/O
Right	Bottom	VDDR[3]	J28	CFG[95]	Configurable I/O
Right	Bottom	VDDR[3]	K26	CFG[96]	Configurable I/O
Right	Bottom	VDDR[3]	L25	CFG[97]	Configurable I/O
Right	Bottom	VDDR[3]	N20	CFG[98]	Configurable I/O
Right	Bottom	VDDR[3]	M23	CFG[99]	Configurable I/O
Right	Bottom	VDDR[4]	K27	CFG[100]	Configurable I/O
Right	Bottom	VDDR[4]	L26	CFG[101]	Configurable I/O
Right	Bottom	VDDR[4]	H30	CFG[102]	Configurable I/O
Right	Bottom	VDDR[4]	M25	CFG[103]	Configurable I/O
Right	Bottom	VDDR[4]	J29	CFG[104]	Configurable I/O
Right	Bottom	VDDR[4]	N24	CFG[105]	Configurable I/O
Right	Bottom	VDDR[4]	N23	CFG[106]	Configurable I/O
Right	Bottom	VDDR[4]	P20	CFG[107]	Configurable I/O
Right	Bottom	VDDR[4]	K28	CFG[108]	Configurable I/O
Right	Bottom	VDDR[4]	J30	CFG[109]	Configurable I/O
Right	Bottom	VDDR[4]	K30	CFG[110]	Configurable I/O
Right	Bottom	VDDR[4]	L28	CFG[111]	Configurable I/O
Right	Bottom	VDDR[4]	M26	CFG[112]	Configurable I/O
Right	Bottom	VDDR[4]	M27	CFG[113]	Configurable I/O
Right	Bottom	VDDR[4]	P19	CFG[114]	Configurable I/O
Right	Bottom	VDDR[4]	P22	CFG[115]	Configurable I/O
(Sheet 10 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[4]	P24	CFG[116]	Configurable I/O
Right	Bottom	VDDR[4]	N25	CFG[117]	Configurable I/O
Right	Bottom	VDDR[4]	L29	CFG[118]	Configurable I/O
Right	Bottom	VDDR[4]	L30	CFG[119]	Configurable I/O
Right	Bottom	VDDR[4]	M29	CFG[120]	Configurable I/O
Right	Bottom	VDDR[4]	M30	CFG[121]	Configurable I/O
Right	Bottom	VDDR[4]	P23	CFG[122]	Configurable I/O
Right	Bottom	VDDR[4]	R24	CFG[123]	Configurable I/O
Right	Bottom	VDDR[4]	N28	CFG[124]	Configurable I/O
Right	Bottom	VDDR[4]	N27	CFG[125]	Configurable I/O
Right	Bottom	VDDR[4]	P26	CFG[126]	Configurable I/O
Right	Bottom	VDDR[4]	N29	CFG[127]	Configurable I/O
Right	Bottom	VDDR[4]	P27	CFG[128]	Configurable I/O
Right	Bottom	VDDR[4]	P28	CFG[129]	Configurable I/O
Right	Bottom	VDDR[4]	R21	CFG[130]	Configurable I/O
Right	Bottom	VDDR[4]	R22	CFG[131]	Configurable I/O
Right	Bottom	VDDR[4]	N30	CFG[132]	Configurable I/O
Right	Bottom	VDDR[4]	R26	CFG[133]	Configurable I/O
Right	Bottom	VDDR[4]	P30	CFG[134]	Configurable I/O
Right	Bottom	VDDR[4]	R30	CFG[135]	Configurable I/O
Right	Bottom	VDDR[4]	R29	CFG[136]	Configurable I/O
Right	Bottom	VDDR[4]	T30	CFG[137]	Configurable I/O
Right	Bottom	VDDR[4]	T21	CFG[138]	Configurable I/O
(Sheet 11 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[4]	T22	CFG[139]	Configurable I/O
Right	Bottom	VDDR[5]	T29	CFG[140]	Configurable I/O
Right	Bottom	VDDR[5]	T26	CFG[141]	Configurable I/O
Right	Bottom	VDDR[5]	U30	CFG[142]	Configurable I/O
Right	Bottom	VDDR[5]	V30	CFG[143]	Configurable I/O
Right	Bottom	VDDR[5]	U28	CFG[144]	Configurable I/O
Right	Bottom	VDDR[5]	U27	CFG[145]	Configurable I/O
Right	Bottom	VDDR[5]	U23	CFG[146]	Configurable I/O
Right	Bottom	VDDR[5]	T24	CFG[147]	Configurable I/O
Right	Bottom	VDDR[5]	V29	CFG[148]	Configurable I/O
Right	Bottom	VDDR[5]	U26	CFG[149]	Configurable I/O
Right	Bottom	VDDR[5]	V28	CFG[150]	Configurable I/O
Right	Bottom	VDDR[5]	V27	CFG[151]	Configurable I/O
Right	Bottom	VDDR[5]	W30	CFG[152]	Configurable I/O
Right	Bottom	VDDR[5]	W29	CFG[153]	Configurable I/O
Right	Bottom	VDDR[5]	U22	CFG[154]	Configurable I/O
Right	Bottom	VDDR[5]	V23	CFG[155]	Configurable I/O
Right	Bottom	VDDR[5]	Y30	CFG[156]	Configurable I/O
Right	Bottom	VDDR[5]	U24	CFG[157]	Configurable I/O
Right	Bottom	VDDR[5]	Y29	CFG[158]	Configurable I/O
Right	Bottom	VDDR[5]	V25	CFG[159]	Configurable I/O
Right	Bottom	VDDR[5]	W27	CFG[160]	Configurable I/O
Right	Bottom	VDDR[5]	W26	CFG[161]	Configurable I/O
(Sheet 12 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[5]	U20	CFG[162]	Configurable I/O
Right	Bottom	VDDR[5]	U19	CFG[163]	Configurable I/O
Right	Bottom	VDDR[5]	AA30	CFG[164]	Configurable I/O
Right	Bottom	VDDR[5]	Y28	CFG[165]	Configurable I/O
Right	Bottom	VDDR[5]	V24	CFG[166]	Configurable I/O
Right	Bottom	VDDR[5]	AA28	CFG[167]	Configurable I/O
Right	Bottom	VDDR[5]	AB30	CFG[168]	Configurable I/O
Right	Bottom	VDDR[5]	AB29	CFG[169]	Configurable I/O
Right	Bottom	VDDR[5]	V21	CFG[170]	Configurable I/O
Right	Bottom	VDDR[5]	W23	CFG[171]	Configurable I/O
Right	Bottom	VDDR[5]	AC30	CFG[172]	Configurable I/O
Right	Bottom	VDDR[5]	W25	CFG[173]	Configurable I/O
Right	Bottom	VDDR[5]	Y26	CFG[174]	Configurable I/O
Right	Bottom	VDDR[5]	AA27	CFG[175]	Configurable I/O
Right	Bottom	VDDR[5]	AA26	CFG[176]	Configurable I/O
Right	Bottom	VDDR[5]	Y25	CFG[177]	Configurable I/O
Right	Bottom	VDDR[5]	V20	CFG[178]	Configurable I/O
Right	Bottom	VDDR[5]	W22	CFG[179]	Configurable I/O
Right	Bottom	VDDR[6]	AB28	CFG[180]	Configurable I/O
Right	Bottom	VDDR[6]	Y24	CFG[181]	Configurable I/O
Right	Bottom	VDDR[6]	AB27	CFG[182]	Configurable I/O
Right	Bottom	VDDR[6]	AC29	CFG[183]	Configurable I/O
Right	Bottom	VDDR[6]	AD30	CFG[184]	Configurable I/O
(Sheet 13 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[6]	AD29	CFG[185]	Configurable I/O
Right	Bottom	VDDR[6]	W21	CFG[186]	Configurable I/O
Right	Bottom	VDDR[6]	Y22	CFG[187]	Configurable I/O
Right	Bottom	VDDR[6]	AC27	CFG[188]	Configurable I/O
Right	Bottom	VDDR[6]	AE30	CFG[189]	Configurable I/O
Right	Bottom	VDDR[6]	AD28	CFG[190]	Configurable I/O
Right	Bottom	VDDR[6]	AA24	CFG[191]	Configurable I/O
Right	Bottom	VDDR[6]	AB25	CFG[192]	Configurable I/O
Right	Bottom	VDDR[6]	AC26	CFG[193]	Configurable I/O
Right	Bottom	VDDR[6]	W19	CFG[194]	Configurable I/O
Right	Bottom	VDDR[6]	Y21	CFG[195]	Configurable I/O
Right	Bottom	VDDR[6]	AF30	CFG[196]	Configurable I/O
Right	Bottom	VDDR[6]	AE28	CFG[197]	Configurable I/O
Right	Bottom	VDDR[6]	AF29	CFG[198]	Configurable I/O
Right	Bottom	VDDR[6]	AG30	CFG[199]	Configurable I/O
Right	Bottom	VDDR[6]	AB24	CFG[200]	Configurable I/O
Right	Bottom	VDDR[6]	AA23	CFG[201]	Configurable I/O
Right	Bottom	VDDR[6]	Y20	CFG[202]	Configurable I/O
Right	Bottom	VDDR[6]	AB23	CFG[203]	Configurable I/O
Right	Bottom	VDDR[6]	AE27	CFG[204]	Configurable I/O
Right	Bottom	VDDR[6]	AF28	CFG[205]	Configurable I/O
Right	Bottom	VDDR[6]	AC25	CFG[206]	Configurable I/O
Right	Bottom	VDDR[6]	AD26	CFG[207]	Configurable I/O
(Sheet 14 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[6]	AH30	CFG[208]	Configurable I/O
Right	Bottom	VDDR[6]	AG29	CFG[209]	Configurable I/O
Right	Bottom	VDDR[6]	AA22	CFG[210]	Configurable I/O
Right	Bottom	VDDR[6]	AH29	CFG[211]	Configurable I/O
Right	Bottom	VDDR[6]	AE26	CFG[212]	Configurable I/O
Right	Bottom	VDDR[6]	AD25	CFG[213]	Configurable I/O
Right	Bottom	VDDR[6]	AJ30	CFG[214]	Configurable I/O
Right	Bottom	VDDR[6]	AF27	CFG[215]	Configurable I/O
Right	Bottom	VDDR[6]	AG27	CFG[216]	Configurable I/O
Right	Bottom	VDDR[6]	AH28	CFG[217]	Configurable I/O
Right	Bottom	VDDR[6]	AK29	CFG[218]	Configurable I/O
Right	Bottom	VDDR[6]	AC23	CFG[219]	Configurable I/O
Right	Bottom	VDDR[6]	AD24	CFG[220]	Configurable I/O
Bottom	Right	VDDR[7]	AD21	PCKP[1]	PLL601250 Differential clock input / Configurable I/O
Bottom	Right	VDDR[7]	AC21	PCKN[1]	PLL601250 Differential clock input / Configurable I/O
Bottom	Right	VDDR[7]	AJ28	CFG[221]	Configurable I/O
Bottom	Right	VDDR[7]	AG26	CFG[222]	Configurable I/O
Bottom	Right	VDDR[7]	AF25	CFG[223]	Configurable I/O
Bottom	Right	VDDR[7]	AK28	CFG[224]	Configurable I/O
Bottom	Right	VDDR[7]	AE24	CFG[225]	Configurable I/O
Bottom	Right	VDDR[7]	AE23	CFG[226]	Configurable I/O
(Sheet 15 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDR[7]	AF24	CFG[227]	Configurable I/O
Bottom	Right	VDDR[7]	AJ27	CFG[228]	Configurable I/O
Bottom	Right	VDDR[7]	AG25	CFG[229]	Configurable I/O
Bottom	Right	VDDR[7]	AA20	CFG[230]	Configurable I/O
Bottom	Right	VDDR[7]	AB20	CFG[231]	Configurable I/O
Bottom	Right	VDDR[7]	AH26	CFG[232]	Configurable I/O
Bottom	Right	VDDR[7]	AE22	CFG[233]	Configurable I/O
Bottom	Right	VDDR[7]	AK27	CFG[234]	Configurable I/O
Bottom	Right	VDDR[7]	AJ26	CFG[235]	Configurable I/O
Bottom	Right	VDDR[7]	AK26	CFG[236]	Configurable I/O
Bottom	Right	VDDR[7]	AH25	CFG[237]	Configurable I/O
Bottom	Right	VDDR[7]	AF21	CFG[238]	Configurable I/O
Bottom	Right	VDDR[7]	AD20	CFG[239]	Configurable I/O
Bottom	Right	VDDR[7]	AH24	CFG[240]	Configurable I/O
Bottom	Right	VDDR[7]	AF23	CFG[241]	Configurable I/O
Bottom	Right	VDDR[7]	AG23	CFG[242]	Configurable I/O
Bottom	Right	VDDR[7]	AK25	CFG[243]	Configurable I/O
Bottom	Right	VDDR[7]	AJ24	CFG[244]	Configurable I/O
Bottom	Right	VDDR[7]	AK24	CFG[245]	Configurable I/O
Bottom	Right	VDDR[7]	AA19	CFG[246]	Configurable I/O
Bottom	Right	VDDR[7]	AE20	CFG[247]	Configurable I/O
Bottom	Right	VDDGCK[3]	AG22	RSVD[2]	Reserved
Bottom	Right	VDDGCK[3]	AH22	RSVD[3]	Reserved
(Sheet 16 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDGCK[3]	AJ23	GCKP[2]	GigaBlaze differential TX reference clock
Bottom	Right	VDDGCK[3]	AJ22	GCKN[2]	GigaBlaze differential TX reference clock
Bottom	Right	VDDG[5]	AK20	GRXN[16]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AK21	GRXP[16]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AA18	GTXP[16]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	Y18	GTXN[16]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	AB19	GTXN[17]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	AC19	GTXP[17]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	AJ20	GRXP[17]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AH20	GRXN[17]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AJ18	GRXN[18]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AJ19	GRXP[18]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AE18	GTXP[18]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	AE19	GTXN[18]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	Y17	GTXN[19]	GigaBlaze TX differential pair
(Sheet 17 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDG[5]	W17	GTXP[19]	GigaBlaze TX differential pair
Bottom	Right	VDDG[5]	AK19	GRXP[19]	GigaBlaze RX differential pair
Bottom	Right	VDDG[5]	AK18	GRXN[19]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AG17	GRXN[20]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AH17	GRXP[20]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AC18	GTXP[20]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AD18	GTXN[20]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AB17	GTXN[21]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AC17	GTXP[21]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AJ15	GRXP[21]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AJ16	GRXN[21]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AK16	GRXN[22]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AK15	GRXP[22]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AA16	GTXP[22]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AB16	GTXN[22]	GigaBlaze TX differential pair
(Sheet 18 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDG[6]	AD17	GTXN[23]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AD16	GTXP[23]	GigaBlaze TX differential pair
Bottom	Right	VDDG[6]	AF16	GRXP[23]	GigaBlaze RX differential pair
Bottom	Right	VDDG[6]	AF15	GRXN[23]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AK12	GRXN[24]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AK13	GRXP[24]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AD15	GTXP[24]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AD14	GTXN[24]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AA15	GTXN[25]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AB15	GTXP[25]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AH13	GRXP[25]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AH14	GRXN[25]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AJ12	GRXN[26]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AJ13	GRXP[26]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AC14	GTXP[26]	GigaBlaze TX differential pair
(Sheet 19 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDG[7]	AB14	GTXN[26]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AC13	GTXN[27]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AD13	GTXP[27]	GigaBlaze TX differential pair
Bottom	Right	VDDG[7]	AG14	GRXP[27]	GigaBlaze RX differential pair
Bottom	Right	VDDG[7]	AG13	GRXN[27]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AK10	GRXN[28]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AK09	GRXP[28]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AE13	GTXP[28]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	AE12	GTXN[28]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	AC12	GTXN[29]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	AB12	GTXP[29]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	AH10	GRXP[29]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AH11	GRXN[29]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AJ09	GRXN[30]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AH09	GRXP[30]	GigaBlaze RX differential pair
(Sheet 20 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDG[8]	AA13	GTXP[30]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	Y13	GTXN[30]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	Y14	GTXN[31]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	W14	GTXP[31]	GigaBlaze TX differential pair
Bottom	Right	VDDG[8]	AG10	GRXP[31]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AF10	GRXN[31]	GigaBlaze RX differential pair
Bottom	Right	VDDG[8]	AF11	GBRTRIM	GigaBlaze RTRIM
Bottom	Right	VDDGCK[4]	AH07	GCKP[3]	GigaBlaze differential TX reference clock
Bottom	Right	VDDGCK[4]	AJ07	GCKN[3]	GigaBlaze differential TX reference clock
Bottom	Right	VDDR[8]	AG08	CFG[248]	Configurable I/O
Bottom	Right	VDDR[8]	AK07	CFG[249]	Configurable I/O
Bottom	Right	VDDR[8]	AD11	CFG[250]	Configurable I/O
Bottom	Right	VDDR[8]	AA12	CFG[251]	Configurable I/O
Bottom	Right	VDDR[8]	AD10	CFG[252]	Configurable I/O
Bottom	Right	VDDR[8]	AK06	CFG[253]	Configurable I/O
Bottom	Right	VDDR[8]	AE09	CFG[254]	Configurable I/O
Bottom	Right	VDDR[8]	AF08	CFG[255]	Configurable I/O
Bottom	Right	VDDR[8]	AH06	CFG[256]	Configurable I/O
Bottom	Right	VDDR[8]	AK05	CFG[257]	Configurable I/O
(Sheet 21 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDR[8]	W12	CFG[258]	Configurable I/O
Bottom	Right	VDDR[8]	AB11	CFG[259]	Configurable I/O
Bottom	Right	VDDR[8]	AK04	CFG[260]	Configurable I/O
Bottom	Right	VDDR[8]	AJ05	CFG[261]	Configurable I/O
Bottom	Right	VDDR[8]	AG06	CFG[262]	Configurable I/O
Bottom	Right	VDDR[8]	AF07	CFG[263]	Configurable I/O
Bottom	Right	VDDR[8]	AE08	CFG[264]	Configurable I/O
Bottom	Right	VDDR[8]	AD09	CFG[265]	Configurable I/O
Bottom	Right	VDDR[8]	AA11	CFG[266]	Configurable I/O
Bottom	Right	VDDR[8]	Y11	CFG[267]	Configurable I/O
Bottom	Right	VDDR[9]	AJ04	TMS	Reserved Test
Bottom	Right	VDDR[9]	AH05	TDI	Reserved Test
Bottom	Right	VDDR[9]	AF06	TCK	Reserved Test
Bottom	Right	VDDR[9]	AE07	TRSTN	Reserved Test
Bottom	Right	VDDR[9]	AG05	TN	Reserved Test
Bottom	Right	VDDR[9]	AK03	IDDT	Reserved Test
Bottom	Right	VDDR[9]	AK02	TDO	Reserved Test
Bottom	Right	VDDR[9]	AJ03	SEN	Reserved Test
Bottom	Right	VDDR[9]	AH03	PMON	Reserved Test
Left	Top	VDDR[10]	AB08	PCKP[2]	PLL100500 Differential clock input / Configurable I/O
Left	Top	VDDR[10]	AC08	PCKN[2]	PLL100500 Differential clock input / Configurable I/O
(Sheet 22 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[10]	AG04	CFG[268]	Configurable I/O
Left	Top	VDDR[10]	AD07	CFG[269]	Configurable I/O
Left	Top	VDDR[10]	AH02	CFG[270]	Configurable I/O
Left	Top	VDDR[10]	AJ01	CFG[271]	Configurable I/O
Left	Top	VDDR[10]	AF04	CFG[272]	Configurable I/O
Left	Top	VDDR[10]	AD06	CFG[273]	Configurable I/O
Left	Top	VDDR[10]	AE05	CFG[274]	Configurable I/O
Left	Top	VDDR[10]	AE04	CFG[275]	Configurable I/O
Left	Top	VDDR[10]	AA08	CFG[276]	Configurable I/O
Left	Top	VDDR[10]	AH01	CFG[277]	Configurable I/O
Left	Top	VDDR[10]	AB07	CFG[278]	Configurable I/O
Left	Top	VDDR[10]	AC06	CFG[279]	Configurable I/O
Left	Top	VDDR[10]	AD05	CFG[280]	Configurable I/O
Left	Top	VDDR[10]	AG02	CFG[281]	Configurable I/O
Left	Top	VDDR[10]	AF03	CFG[282]	Configurable I/O
Left	Top	VDDR[10]	AG01	CFG[283]	Configurable I/O
Left	Top	VDDR[10]	AF02	CFG[284]	Configurable I/O
Left	Top	VDDR[10]	Y10	CFG[285]	Configurable I/O
Left	Top	VDDR[10]	AA09	CFG[286]	Configurable I/O
Left	Top	VDDR[10]	AE03	CFG[287]	Configurable I/O
Left	Top	VDDR[10]	AF01	CFG[288]	Configurable I/O
Left	Top	VDDR[10]	AC05	CFG[289]	Configurable I/O
Left	Top	VDDR[10]	AB06	CFG[290]	Configurable I/O
(Sheet 23 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[10]	AA07	CFG[291]	Configurable I/O
Left	Top	VDDR[10]	AE01	CFG[292]	Configurable I/O
Left	Top	VDDR[10]	W10	CFG[293]	Configurable I/O
Left	Top	VDDR[10]	Y09	CFG[294]	Configurable I/O
Left	Top	VDDR[10]	AC04	CFG[295]	Configurable I/O
Left	Top	VDDR[10]	AD03	CFG[296]	Configurable I/O
Left	Top	VDDR[10]	W09	CFG[297]	Configurable I/O
Left	Top	VDDR[10]	AD01	CFG[298]	Configurable I/O
Left	Top	VDDR[10]	Y07	CFG[299]	Configurable I/O
Left	Top	VDDR[10]	AD02	CFG[300]	Configurable I/O
Left	Top	VDDR[10]	V10	CFG[301]	Configurable I/O
Left	Top	VDDR[10]	V11	CFG[302]	Configurable I/O
Left	Top	VDDR[10]	AB04	CFG[303]	Configurable I/O
Left	Top	VDDR[10]	AC02	CFG[304]	Configurable I/O
Left	Top	VDDR[10]	AB03	CFG[305]	Configurable I/O
Left	Top	VDDR[10]	AA05	CFG[306]	Configurable I/O
Left	Top	VDDR[10]	Y06	CFG[307]	Configurable I/O
Left	Top	VDDR[11]	Y05	CFG[308]	Configurable I/O
Left	Top	VDDR[11]	V08	CFG[309]	Configurable I/O
Left	Top	VDDR[11]	W08	CFG[310]	Configurable I/O
Left	Top	VDDR[11]	AC01	CFG[311]	Configurable I/O
Left	Top	VDDR[11]	AA04	CFG[312]	Configurable I/O
Left	Top	VDDR[11]	W06	CFG[313]	Configurable I/O
(Sheet 24 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[11]	AB02	CFG[314]	Configurable I/O
Left	Top	VDDR[11]	AA03	CFG[315]	Configurable I/O
Left	Top	VDDR[11]	V07	CFG[316]	Configurable I/O
Left	Top	VDDR[11]	U11	CFG[317]	Configurable I/O
Left	Top	VDDR[11]	U07	CFG[318]	Configurable I/O
Left	Top	VDDR[11]	Y03	CFG[319]	Configurable I/O
Left	Top	VDDR[11]	AB01	CFG[320]	Configurable I/O
Left	Top	VDDR[11]	W05	CFG[321]	Configurable I/O
Left	Top	VDDR[11]	Y02	CFG[322]	Configurable I/O
Left	Top	VDDR[11]	W04	CFG[323]	Configurable I/O
Left	Top	VDDR[11]	V06	CFG[324]	Configurable I/O
Left	Top	VDDR[11]	U09	CFG[325]	Configurable I/O
Left	Top	VDDR[11]	V04	CFG[326]	Configurable I/O
Left	Top	VDDR[11]	W02	CFG[327]	Configurable I/O
Left	Top	VDDR[11]	Y01	CFG[328]	Configurable I/O
Left	Top	VDDR[11]	W01	CFG[329]	Configurable I/O
Left	Top	VDDR[11]	U12	CFG[330]	Configurable I/O
Left	Top	VDDR[11]	U08	CFG[331]	Configurable I/O
Left	Top	VDDR[11]	U04	CFG[332]	Configurable I/O
Left	Top	VDDR[11]	V02	CFG[333]	Configurable I/O
Left	Top	VDDR[11]	V03	CFG[334]	Configurable I/O
Left	Top	VDDR[11]	T07	CFG[335]	Configurable I/O
Left	Top	VDDR[11]	U05	CFG[336]	Configurable I/O
(Sheet 25 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[11]	V01	CFG[337]	Configurable I/O
Left	Top	VDDR[11]	U03	CFG[338]	Configurable I/O
Left	Top	VDDR[11]	T10	CFG[339]	Configurable I/O
Left	Top	VDDR[11]	T09	CFG[340]	Configurable I/O
Left	Top	VDDR[11]	T05	CFG[341]	Configurable I/O
Left	Top	VDDR[11]	U01	CFG[342]	Configurable I/O
Left	Top	VDDR[11]	T01	CFG[343]	Configurable I/O
Left	Top	VDDR[11]	T02	CFG[344]	Configurable I/O
Left	Top	VDDR[11]	R01	CFG[345]	Configurable I/O
Left	Top	VDDR[11]	R02	CFG[346]	Configurable I/O
Left	Top	VDDR[11]	R09	CFG[347]	Configurable I/O
Left	Top	VDDR[11]	R10	CFG[348]	Configurable I/O
Left	Top	VDDR[11]	P01	CFG[349]	Configurable I/O
Left	Top	VDDR[11]	R05	CFG[350]	Configurable I/O
Left	Top	VDDR[11]	N01	CFG[351]	Configurable I/O
Left	Top	VDDR[11]	P03	CFG[352]	Configurable I/O
Left	Top	VDDR[11]	P05	CFG[353]	Configurable I/O
Left	Top	VDDR[11]	P04	CFG[354]	Configurable I/O
Left	Top	VDDR[11]	P08	CFG[355]	Configurable I/O
Left	Top	VDDR[11]	R07	CFG[356]	Configurable I/O
Left	Top	VDDR[11]	N03	CFG[357]	Configurable I/O
Left	Top	VDDR[11]	N02	CFG[358]	Configurable I/O
Left	Top	VDDR[11]	N04	CFG[359]	Configurable I/O
(Sheet 26 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[11]	M01	CFG[360]	Configurable I/O
Left	Top	VDDR[11]	M02	CFG[361]	Configurable I/O
Left	Top	VDDR[11]	P07	CFG[362]	Configurable I/O
Left	Top	VDDR[11]	P09	CFG[363]	Configurable I/O
Left	Top	VDDR[11]	N08	CFG[364]	Configurable I/O
Left	Top	VDDR[11]	L02	CFG[365]	Configurable I/O
Left	Top	VDDR[11]	L01	CFG[366]	Configurable I/O
Left	Top	VDDR[11]	N06	CFG[367]	Configurable I/O
Left	Top	VDDR[11]	M04	CFG[368]	Configurable I/O
Left	Top	VDDR[11]	M05	CFG[369]	Configurable I/O
Left	Top	VDDR[11]	L03	CFG[370]	Configurable I/O
Left	Top	VDDR[11]	P11	CFG[371]	Configurable I/O
Left	Top	VDDR[11]	P12	CFG[372]	Configurable I/O
Left	Top	VDDR[11]	N07	CFG[373]	Configurable I/O
Left	Top	VDDR[11]	K03	CFG[374]	Configurable I/O
Left	Top	VDDR[11]	J01	CFG[375]	Configurable I/O
Left	Top	VDDR[11]	M06	CFG[376]	Configurable I/O
Left	Top	VDDR[11]	J02	CFG[377]	Configurable I/O
Left	Top	VDDR[11]	H01	CFG[378]	Configurable I/O
Left	Top	VDDR[11]	M09	CFG[379]	Configurable I/O
Left	Top	VDDR[11]	M08	CFG[380]	Configurable I/O
Left	Top	VDDR[11]	L06	CFG[381]	Configurable I/O
Left	Top	VDDR[11]	L05	CFG[382]	Configurable I/O
(Sheet 27 of 29)					

Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[11]	K04	CFG[383]	Configurable I/O
Left	Top	VDDR[11]	K05	CFG[384]	Configurable I/O
Left	Top	VDDR[11]	N10	CFG[385]	Configurable I/O
Left	Top	VDDR[11]	N11	CFG[386]	Configurable I/O
Left	Top	VDDR[11]	J03	CFG[387]	Configurable I/O
Left	Top	VDDR[11]	H02	CFG[388]	Configurable I/O
Left	Top	VDDR[11]	J04	CFG[389]	Configurable I/O
Left	Top	VDDR[11]	G01	CFG[390]	Configurable I/O
Left	Top	VDDR[11]	G02	CFG[391]	Configurable I/O
Left	Top	VDDR[11]	E01	CFG[392]	Configurable I/O
Left	Top	VDDR[11]	M10	CFG[393]	Configurable I/O
Left	Top	VDDR[11]	L09	CFG[394]	Configurable I/O
Left	Top	VDDR[11]	L07	CFG[395]	Configurable I/O
Left	Top	VDDR[11]	F01	CFG[396]	Configurable I/O
Left	Top	VDDR[11]	G03	CFG[397]	Configurable I/O
Left	Top	VDDR[11]	K07	CFG[398]	Configurable I/O
Left	Top	VDDR[11]	J06	CFG[399]	Configurable I/O
Left	Top	VDDR[11]	E02	CFG[400]	Configurable I/O
Left	Top	VDDR[11]	M12	CFG[401]	Configurable I/O
Left	Top	VDDR[11]	K08	CFG[402]	Configurable I/O
Left	Top	VDDR[11]	H04	CFG[403]	Configurable I/O
Left	Top	VDDR[11]	D01	CFG[404]	Configurable I/O
Left	Top	VDDR[11]	H05	CFG[405]	Configurable I/O
(Sheet 28 of 29)					

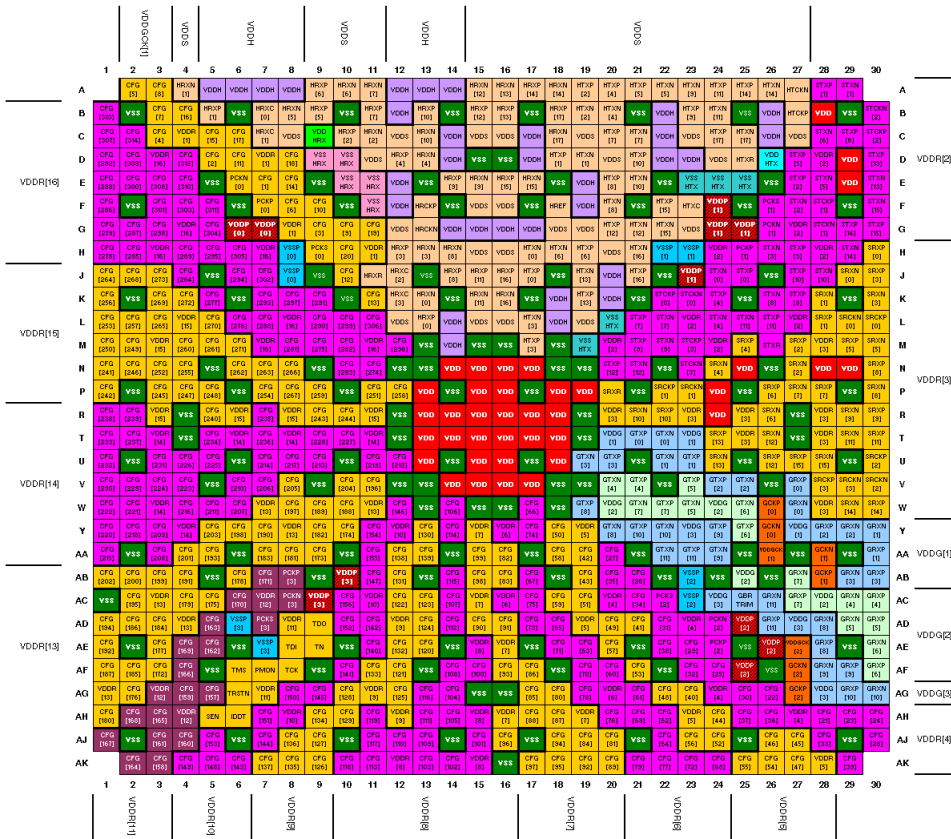
Table A.10 FC896 Package I/O Signals (RC11XT432) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[11]	F03	CFG[406]	Configurable I/O
Left	Top	VDDR[11]	J07	CFG[407]	Configurable I/O
Left	Top	VDDR[11]	K09	CFG[408]	Configurable I/O
Left	Top	VDDR[12]	L11	CFG[409]	Configurable I/O
Left	Top	VDDR[12]	L10	CFG[410]	Configurable I/O
Left	Top	VDDR[12]	E03	CFG[411]	Configurable I/O
Left	Top	VDDR[12]	H06	CFG[412]	Configurable I/O
Left	Top	VDDR[12]	F04	CFG[413]	Configurable I/O
Left	Top	VDDR[12]	G05	CFG[414]	Configurable I/O
Left	Top	VDDR[12]	D02	CFG[415]	Configurable I/O
Left	Top	VDDR[12]	C01	CFG[416]	Configurable I/O
Left	Top	VDDR[12]	J08	CFG[417]	Configurable I/O
Left	Top	VDDR[12]	C02	CFG[418]	Configurable I/O
Left	Top	VDDR[12]	F05	CFG[419]	Configurable I/O
Left	Top	VDDR[12]	G06	CFG[420]	Configurable I/O
Left	Top	VDDR[12]	B01	CFG[421]	Configurable I/O
Left	Top	VDDR[12]	E04	CFG[422]	Configurable I/O
Left	Top	VDDR[12]	D04	CFG[423]	Configurable I/O
Left	Top	VDDR[12]	C03	CFG[424]	Configurable I/O
Left	Top	VDDR[12]	A02	CFG[425]	Configurable I/O
Left	Top	VDDR[12]	H08	CFG[426]	Configurable I/O
Left	Top	VDDR[12]	G07	CFG[427]	Configurable I/O
(Sheet 29 of 29)					

A.3.3 RC11XT531 in the FC896 Package

Figure A.6 is a color-coded diagram of the RC11XT531 in the FC896 package. It shows the location of each ball in the ball field and the power domains. If you are viewing this document on a computer monitor, you can zoom in to see more detail.

Figure A.6 RC11XT531 in the FC896 Package Diagram



VSS Global VSS Ground Plane for Core Logic and Configurable I/O

VDD VDD Power Supply for Core Logic

VDDP[2] Independent VDD Power Supply for PLL

VSSP[2] Independent VSS Power Supply for PLL

VDDR[3] VDDR Power Supply Split Region for Configurable I/O

VDDR[4] VDDR Power Supply Split Region for Configurable I/O

VDDR[12] VDDR Power Supply Split Region for Configurable I/O

Note: To help distinguish between adjacent VDDR Splits, 2 alternating colors for VDD are used for consecutive Splits. A third color is used for Split 1+2 to distinguish it from Split 10. All Splits are electrically independent of each other.

VDDH 1.2V Power Supply Region for HyperPHY hardmac

VDDGOK [x] 3.3V I/O Power Supply Region for GigaBlaze Clock Input Receiver

VDDG[1] Power Supply Split Region for GigaBlaze Differential Pairs

VDDG[2] Power Supply Split Region for GigaBlaze Differential Pairs

Note: To help distinguish between adjacent Power Supply Splits for the GigaBlaze differential pairs, 2 alternating colors are used for Splits VDDG[1] through VDDG[3]. All Splits are electrically independent of each other.

VDDOS 1.8V I/O Power Supply Region for HyperPHY LVDS

VDDH-RX 1.2V Power Supply for HyperPHY Receive PLL

VDDH-TX 1.2V Power Supply for HyperPHY Transmit PLL

VSSHRX Ground for HyperPHY Receive PLL

VSSHTX Ground for HyperPHY Transmit PLL

[Table A.11](#) lists the RC11XT531 FC896 package power connections. The core logic and I/Os share a common ground (V_{SS}). All the core logic is powered from a single power domain (V_{DD}). The I/Os are distributed across 16 separate power domains ($V_{DDR}[1:16]$). The four PLLs are isolated; each PLL has its own dedicated power ($V_{DDP}[0:3]$) and ground ($V_{SSP}[0:3]$) connection.

Table A.11 FC896 Package Power Connections (RC11XT531)

VDD Plane	Package Ball Location(s)	Description
VDD	B28, D29, E29, N14, N15, N16, N17, N25, N28, N29, P13, P15, P16, P18, P19, P24, R13, R14, R15, R16, R17, R18, R24, T13, T14, T15, T16, T17, T18, U13, U15, U16, U18, V14, V15, V16, V17	Core Logic VDD
VSS	B02, B06, B10, B14, B17, B21, B25, B29, D15, D16, E05, E09, E13, E18, E22, E26, F02, F06, F10, F14, F17, F21, F25, F29, J05, J09, J13, J18, J22, J26, K02, K06, K10, K14, K17, K21, K25, K29, M13, M15, M16, M18, N05, N09, N12, N13, N18, N19, N22, N26, P02, P06, P10, P14, P17, P21, P25, P29, R04, R12, R19, R27, T04, T12, T19, T27, U02, U06, U10, U14, U17, U21, U25, U29, V05, V09, V12, V13, V18, V19, V22, V26, W13, W15, W16, W18, AA02, AA06, AA10, AA14, AA17, AA21, AA25, AA27, AA29, AB05, AB09, AB13, AB18, AB22, AB24, AB26, AC01, AE02, AE06, AE10, AE14, AE17, AE21, AE25, AE29, AF05, AF09, AF13, AF18, AF22, AF26, AG15, AG16, AJ02, AJ06, AJ10, AJ14, AJ17, AJ21, AJ25, AJ29, AK16	Core Logic & Configurable I/O Ground
VDDG[1]	T20, T23, Y27	1.2V GigaBlaze VDD
VDDG[2]	W20, W24, AB25, AC28	1.2V GigaBlaze VDD
VDDG[3]	Y23, AC24, AD27, AG28	1.2V GigaBlaze VDD
VDDH	A05, A06, A07, A08, A12, A13, A14, B12, B22, B26, C14, C17, C22, C26, D14, D17, D22, D23, E12, E19, F12, F19, G14, G15, G16, G17, J20, K18, K20, L14, L18, M14	HyperPHY 1.2V VDD
VDDHRX	C09	1.2V VDD for HyperPHY RX PLL
(Sheet 1 of 3)		

Table A.11 FC896 Package Power Connections (RC11XT531) (Cont.)

VDD Plane	Package Ball Location(s)	Description
VDDHTX	D26	1.2V VDD for HyperPHY TX PLL
VDDS	C08, C12, C15, C16, C19, C23, C27, D11, D20, D24, F15, F16, G12, G18, G19, G23, H15, H16, H20, L12, L15, L16, L19	Dedicated 1.8V VDD for HyperPHY LVDS I/Os
VDDGCK[1]	AA26	Dedicated 3.3V VDD for GigaBlaze TX clock input
VDDGCK[2]	AE27	Dedicated 3.3V VDD for GigaBlaze TX clock input
VDDR[1]	C04, D07, G08, H11	Configurable I/O VDD
VDDR[2]	D28, G27, H24, H28, L23, L27, M20, M24	Configurable I/O VDD
VDDR[3]	M28, R20, R23, R25, R28, T25, T28, W28	Configurable I/O VDD
VDDR[4]	AC20, AD23, AG24, AH27	Configurable I/O VDD
VDDR[5]	Y19, AD19, AH23, AK28	Configurable I/O VDD
VDDR[6]	Y16, AC16, AG20	Configurable I/O VDD
VDDR[7]	Y15, AC15, AE16, AH16, AH19	Configurable I/O VDD
VDDR[8]	AE15, AH15, AK12, AK15	Configurable I/O VDD
VDDR[9]	AD12, AG11, AH12	Configurable I/O VDD
VDDR[10]	Y12, AC11, AH08	Configurable I/O VDD
VDDR[11]	AD08, AG07	Configurable I/O VDD
VDDR[12]	AC07, AG03, AH04	Configurable I/O VDD
VDDR[13]	W07, W11, Y08, AC03, AD04, AG01	Configurable I/O VDD
VDDR[14]	T03, T06, T08, T11, W03, Y04	Configurable I/O VDD
VDDR[15]	L04, M03, R03, R06, R08, R11	Configurable I/O VDD
VDDR[16]	D03, G04, H03, H07, L08, M07, M11	Configurable I/O VDD
VDDP[0]	G06, G07	PLL VDD
VDDP[1]	F24, G24, G25, J23	PLL VDD
(Sheet 2 of 3)		

Table A.11 FC896 Package Power Connections (RC11XT531) (Cont.)

VDD Plane	Package Ball Location(s)	Description
VDDP[2]	AD25, AE26, AF25	PLL VDD
VDDP[3]	AB10, AC09	PLL VDD
VSSHRX	D09, D10, E10, E11, F11	Ground for HyperPHY Receive PLL
VSSHTX	E23, E24, E25, L20, M19	Ground for HyperPHY Transmit PLL
VSSP[0]	H08, J08	PLL Ground
VSSP[1]	H22, H23	PLL Ground
VSSP[2]	AB23, AC23	PLL Ground
VSSP[3]	AD06, AE07	PLL Ground
(Sheet 3 of 3)		

[Table A.12](#) lists the RC11XT531 in the FC896 package I/O assignments.

Table A.12 FC896 Package I/O Assignments (RC11XT531)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDR[1]	F07	PCKP[0]	PLL601250 Differential clock input / Configurable I/O
Top	Left	VDDR[1]	E06	PCKN[0]	PLL601250 Differential clock input / Configurable I/O
Top	Left	VDDR[1]	H09	PCKS[0]	PLL601250 Single-ended clock input / Configurable I/O
Top	Left	VDDR[1]	E07	CFG[1]	Configurable I/O
Top	Left	VDDR[1]	D05	CFG[2]	Configurable I/O
Top	Left	VDDR[1]	G09	CFG[3]	Configurable I/O
Top	Left	VDDR[1]	C03	CFG[4]	Configurable I/O
Top	Left	VDDR[1]	A02	CFG[5]	Configurable I/O
(Sheet 1 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDR[1]	F08	CFG[6]	Configurable I/O
Top	Left	VDDR[1]	B03	CFG[7]	Configurable I/O
Top	Left	VDDR[1]	A03	CFG[8]	Configurable I/O
Top	Left	VDDR[1]	G10	CFG[9]	Configurable I/O
Top	Left	VDDR[1]	F09	CFG[10]	Configurable I/O
Top	Left	VDDR[1]	D06	CFG[11]	Configurable I/O
Top	Left	VDDR[1]	J10	CFG[12]	Configurable I/O
Top	Left	VDDR[1]	K11	CFG[13]	Configurable I/O
Top	Left	VDDR[1]	E08	CFG[14]	Configurable I/O
Top	Left	VDDR[1]	C05	CFG[15]	Configurable I/O
Top	Left	VDDR[1]	B04	CFG[16]	Configurable I/O
Top	Left	VDDR[1]	C06	CFG[17]	Configurable I/O
Top	Left	VDDR[1]	D08	CFG[18]	Configurable I/O
Top	Left	VDDR[1]	G11	CFG[19]	Configurable I/O
Top	Left	VDDR[1]	H10	CFG[20]	Configurable I/O
Top	Left	VDDS	J11	HRXR	HyperPHY RX PLL voltage regulator 1.2V reference
Top	Left	VDDS	K12	HRXC[3]	HyperPHY RX LVDS buffer CTAP input
Top	Left	VDDS	J12	HRXC[2]	HyperPHY RX LVDS buffer CTAP input
Top	Left	VDDS	C07	HRXC[1]	HyperPHY RX LVDS buffer CTAP input
Top	Left	VDDS	B07	HRXC[0]	HyperPHY RX LVDS buffer CTAP input
Top	Left	VDDS	F13	HRCKP	HyperPHY RX differential clock input
Top	Left	VDDS	G13	HRCKN	HyperPHY RX differential clock input
(Sheet 2 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDS	L13	HRXP[0]	HyperPHY RX differential data input
Top	Left	VDDS	K13	HRXN[0]	HyperPHY RX differential data input
Top	Left	VDDS	B05	HRXP[1]	HyperPHY RX differential data input
Top	Left	VDDS	A04	HRXN[1]	HyperPHY RX differential data input
Top	Left	VDDS	C10	HRXP[2]	HyperPHY RX differential data input
Top	Left	VDDS	C11	HRXN[2]	HyperPHY RX differential data input
Top	Left	VDDS	H12	HRXP[3]	HyperPHY RX differential data input
Top	Left	VDDS	H13	HRXN[3]	HyperPHY RX differential data input
Top	Left	VDDS	D12	HRXP[4]	HyperPHY RX differential data input
Top	Left	VDDS	D13	HRXN[4]	HyperPHY RX differential data input
Top	Left	VDDS	B09	HRXP[5]	HyperPHY RX differential data input
Top	Left	VDDS	B08	HRXN[5]	HyperPHY RX differential data input
Top	Left	VDDS	A09	HRXP[6]	HyperPHY RX differential data input
Top	Left	VDDS	A10	HRXN[6]	HyperPHY RX differential data input
Top	Left	VDDS	B11	HRXP[7]	HyperPHY RX differential data input
Top	Left	VDDS	A11	HRXN[7]	HyperPHY RX differential data input
Top	Left	VDDS	J14	HRXP[8]	HyperPHY RX differential data input
Top	Left	VDDS	H14	HRXN[8]	HyperPHY RX differential data input
Top	Left	VDDS	E14	HRXP[9]	HyperPHY RX differential data input
Top	Left	VDDS	E15	HRXN[9]	HyperPHY RX differential data input
Top	Left	VDDS	B13	HRXP[10]	HyperPHY RX differential data input
Top	Left	VDDS	C13	HRXN[10]	HyperPHY RX differential data input
Top	Left	VDDS	J15	HRXP[11]	HyperPHY RX differential data input
(Sheet 3 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDS	K15	HRXN[11]	HyperPHY RX differential data input
Top	Left	VDDS	B15	HRXP[12]	HyperPHY RX differential data input
Top	Left	VDDS	A15	HRXN[12]	HyperPHY RX differential data input
Top	Left	VDDS	B16	HRXP[13]	HyperPHY RX differential data input
Top	Left	VDDS	A16	HRXN[13]	HyperPHY RX differential data input
Top	Left	VDDS	A17	HRXP[14]	HyperPHY RX differential data input
Top	Left	VDDS	A18	HRXN[14]	HyperPHY RX differential data input
Top	Left	VDDS	E16	HRXP[15]	HyperPHY RX differential data input
Top	Left	VDDS	E17	HRXN[15]	HyperPHY RX differential data input
Top	Left	VDDS	J16	HRXP[16]	HyperPHY RX differential data input
Top	Left	VDDS	K16	HRXN[16]	HyperPHY RX differential data input
Top	Left	VDDS	B18	HRXP[17]	HyperPHY RX differential data input
Top	Left	VDDS	C18	HRXN[17]	HyperPHY RX differential data input
Top	Left	VDDS	F18	HREF	HyperPHY LVDS bias cell reference
Top	Left	VDDS	J17	HTXP[0]	HyperPHY TX differential data output
Top	Left	VDDS	H17	HTXN[0]	HyperPHY TX differential data output
Top	Left	VDDS	D18	HTXP[1]	HyperPHY TX differential data output
Top	Left	VDDS	D19	HTXN[1]	HyperPHY TX differential data output
Top	Left	VDDS	A19	HTXP[2]	HyperPHY TX differential data output
Top	Left	VDDS	B19	HTXN[2]	HyperPHY TX differential data output
Top	Left	VDDS	M17	HTXP[3]	HyperPHY TX differential data output
Top	Left	VDDS	L17	HTXN[3]	HyperPHY TX differential data output
Top	Left	VDDS	A20	HTXP[4]	HyperPHY TX differential data output
(Sheet 4 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDS	B20	HTXN[4]	HyperPHY TX differential data output
Top	Left	VDDS	A21	HTXP[5]	HyperPHY TX differential data output
Top	Left	VDDS	A22	HTXN[5]	HyperPHY TX differential data output
Top	Left	VDDS	H19	HTXP[6]	HyperPHY TX differential data output
Top	Left	VDDS	H18	HTXN[6]	HyperPHY TX differential data output
Top	Left	VDDS	C20	HTXP[7]	HyperPHY TX differential data output
Top	Left	VDDS	C21	HTXN[7]	HyperPHY TX differential data output
Top	Left	VDDS	E20	HTXP[8]	HyperPHY TX differential data output
Top	Left	VDDS	F20	HTXN[8]	HyperPHY TX differential data output
Top	Left	VDDS	B23	HTXP[9]	HyperPHY TX differential data output
Top	Left	VDDS	A23	HTXN[9]	HyperPHY TX differential data output
Top	Left	VDDS	D21	HTXP[10]	HyperPHY TX differential data output
Top	Left	VDDS	E21	HTXN[10]	HyperPHY TX differential data output
Top	Left	VDDS	A24	HTXP[11]	HyperPHY TX differential data output
Top	Left	VDDS	B24	HTXN[11]	HyperPHY TX differential data output
Top	Left	VDDS	G20	HTXP[12]	HyperPHY TX differential data output
Top	Left	VDDS	G21	HTXN[12]	HyperPHY TX differential data output
Top	Left	VDDS	K19	HTXP[13]	HyperPHY TX differential data output
Top	Left	VDDS	J19	HTXN[13]	HyperPHY TX differential data output
Top	Left	VDDS	A25	HTXP[14]	HyperPHY TX differential data output
Top	Left	VDDS	A26	HTXN[14]	HyperPHY TX differential data output
Top	Left	VDDS	F22	HTXP[15]	HyperPHY TX differential data output
Top	Left	VDDS	G22	HTXN[15]	HyperPHY TX differential data output
(Sheet 5 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Top	Left	VDDS	J21	HTXP[16]	HyperPHY TX differential data output
Top	Left	VDDS	H21	HTXN[16]	HyperPHY TX differential data output
Top	Left	VDDS	C24	HTXP[17]	HyperPHY TX differential data output
Top	Left	VDDS	C25	HTXN[17]	HyperPHY TX differential data output
Top	Left	VDDS	B27	HTCKP	HyperPHY TX differential clock input
Top	Left	VDDS	A27	HTCKN	HyperPHY TX differential clock input
Top	Left	VDDS	F23	HTXC	HyperPHY TX LVDS buffer CTAP input
Top	Left	VDDS	D25	HTXR	HyperPHY TX PLL voltage regulator 1.2V reference
Right	Bottom	VDDR[2]	H25	PCKP[1]	PLL601250 Differential clock input / Configurable I/O
Right	Bottom	VDDR[2]	G26	PCKN[1]	PLL601250 Differential clock input / Configurable I/O
Right	Bottom	VDDR[2]	F26	PCKS[1]	PLL601250 Single-ended clock input / Configurable I/O
Right	Bottom	VDDR[2]	J25	STXP[0]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	J24	STXN[0]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	A28	STXP[1]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	A29	STXN[1]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	E27	STXP[2]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	F27	STXN[2]	SFI-4 TX differential data output / Configurable I/O
(Sheet 6 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[2]	H27	STXP[3]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	H26	STXN[3]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	K22	STCKP[0]	SFI-4 TX differential clock output / Configurable I/O
Right	Bottom	VDDR[2]	K23	STCKN[0]	SFI-4 TX differential clock output / Configurable I/O
Right	Bottom	VDDR[2]	K24	STXP[4]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	L24	STXN[4]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	D27	STXP[5]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	E28	STXN[5]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	C29	STXP[6]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	C28	STXN[6]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	L21	STXP[7]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	L22	STXN[7]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	F28	STCKP[1]	SFI-4 TX differential clock output / Configurable I/O
Right	Bottom	VDDR[2]	G28	STCKN[1]	SFI-4 TX differential clock output / Configurable I/O
Right	Bottom	VDDR[2]	K27	STXP[8]	SFI-4 TX differential data output / Configurable I/O
(Sheet 7 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[2]	K26	STXN[8]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	M21	STXP[9]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	M22	STXN[9]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	J27	STXP[10]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	J28	STXN[10]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	L26	STXP[11]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	L25	STXN[11]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	C30	STCKP[2]	SFI-4 TX differential clock output / Configurable I/O
Right	Bottom	VDDR[2]	B30	STCKN[2]	SFI-4 TX differential clock output / Configurable I/O
Right	Bottom	VDDR[2]	N20	STXP[12]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	N21	STXN[12]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	D30	STXP[13]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	E30	STXN[13]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	G29	STXP[14]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	H29	STXN[14]	SFI-4 TX differential data output / Configurable I/O
(Sheet 8 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[2]	G30	STXP[15]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	F30	STXN[15]	SFI-4 TX differential data output / Configurable I/O
Right	Bottom	VDDR[2]	M23	STCKP[3]	SFI-4 TX differential clock output / Configurable I/O
Right	Bottom	VDDR[2]	N23	STCKN[3]	SFI-4 TX differential clock output / Configurable I/O
Right	Bottom	VDDR[2]	M26	STXR	SFI-4 TX LVDS reference/Configurable I/O
Right	Bottom	VDDR[3]	P20	SRXR	SFI-4 RX LVDS reference/Configurable I/O
Right	Bottom	VDDR[3]	H30	SRXP[0]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	J29	SRXN[0]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	L28	SRXP[1]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	K28	SRXN[1]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	M27	SRXP[2]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	N27	SRXN[2]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	J30	SRXP[3]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	K30	SRXN[3]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	L30	SRCKP[0]	SFI-4 RX differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	L29	SRCKN[0]	SFI-4 RX differential clock input / Configurable I/O
(Sheet 9 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[3]	M25	SRXP[4]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	N24	SRXN[4]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	M29	SRXP[5]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	M30	SRXN[5]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	P26	SRXP[6]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	R26	SRXN[6]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	P28	SRXP[7]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	P27	SRXN[7]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	P22	SRCKP[1]	SFI-4 RX differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	P23	SRCKN[1]	SFI-4 RX differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	N30	SRXP[8]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	P30	SRXN[8]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	R30	SRXP[9]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	R29	SRXN[9]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	R22	SRXP[10]	SFI-4 RX differential data input / Configurable I/O
(Sheet 10 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDR[3]	R21	SRXN[10]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	T30	SRXP[11]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	T29	SRXN[11]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	U30	SRCKP[2]	SFI-4 RX differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	V30	SRCKN[2]	SFI-4 RX differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	U26	SRXP[12]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	T26	SRXN[12]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	T24	SRXP[13]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	U24	SRXN[13]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	W30	SRXP[14]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	W29	SRXN[14]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	U27	SRXP[15]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	U28	SRXN[15]	SFI-4 RX differential data input / Configurable I/O
Right	Bottom	VDDR[3]	V28	SRCKP[3]	SFI-4 RX differential clock input / Configurable I/O
Right	Bottom	VDDR[3]	V29	SRCKN[3]	SFI-4 RX differential clock input / Configurable I/O
(Sheet 11 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDG[1]	W27	GRXN[0]	GigaBlaze RX differential pair
Right	Bottom	VDDG[1]	V27	GRXP[0]	GigaBlaze RX differential pair
Right	Bottom	VDDG[1]	T21	GTXP[0]	GigaBlaze TX differential pair
Right	Bottom	VDDG[1]	T22	GTXN[0]	GigaBlaze TX differential pair
Right	Bottom	VDDG[1]	U22	GTXN[1]	GigaBlaze TX differential pair
Right	Bottom	VDDG[1]	U23	GTXP[1]	GigaBlaze TX differential pair
Right	Bottom	VDDG[1]	AA30	GRXP[1]	GigaBlaze RX differential pair
Right	Bottom	VDDG[1]	Y30	GRXN[1]	GigaBlaze RX differential pair
Right	Bottom	VDDG[1]	Y29	GRXN[2]	GigaBlaze RX differential pair
Right	Bottom	VDDG[1]	Y28	GRXP[2]	GigaBlaze RX differential pair
Right	Bottom	VDDG[1]	V24	GTXP[2]	GigaBlaze TX differential pair
Right	Bottom	VDDG[1]	V25	GTXN[2]	GigaBlaze TX differential pair
Right	Bottom	VDDG[1]	U19	GTXN[3]	GigaBlaze TX differential pair
Right	Bottom	VDDG[1]	U20	GTXP[3]	GigaBlaze TX differential pair
Right	Bottom	VDDG[1]	AB30	GRXP[3]	GigaBlaze RX differential pair
Right	Bottom	VDDG[1]	AB29	GRXN[3]	GigaBlaze RX differential pair
Right	Bottom	VDDGCK[1]	W26	GCKP[0]	GigaBlaze differential TX reference clock
Right	Bottom	VDDGCK[1]	Y26	GCKN[0]	GigaBlaze differential TX reference clock
Right	Bottom	VDDGCK[1]	AB28	GCKP[1]	GigaBlaze differential TX reference clock
Right	Bottom	VDDGCK[1]	AA28	GCKN[1]	GigaBlaze differential TX reference clock
Right	Bottom	VDDG[2]	AC29	GRXN[4]	GigaBlaze RX differential pair
Right	Bottom	VDDG[2]	AC30	GRXP[4]	GigaBlaze RX differential pair
Right	Bottom	VDDG[2]	V21	GTXP[4]	GigaBlaze TX differential pair
(Sheet 12 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDG[2]	V20	GTXN[4]	GigaBlaze TX differential pair
Right	Bottom	VDDG[2]	W23	GTXN[5]	GigaBlaze TX differential pair
Right	Bottom	VDDG[2]	V23	GTXP[5]	GigaBlaze TX differential pair
Right	Bottom	VDDG[2]	AD30	GRXP[5]	GigaBlaze RX differential pair
Right	Bottom	VDDG[2]	AD29	GRXN[5]	GigaBlaze RX differential pair
Right	Bottom	VDDG[2]	AE30	GRXN[6]	GigaBlaze RX differential pair
Right	Bottom	VDDG[2]	AF30	GRXP[6]	GigaBlaze RX differential pair
Right	Bottom	VDDG[2]	Y25	GTXP[6]	GigaBlaze TX differential pair
Right	Bottom	VDDG[2]	W25	GTXN[6]	GigaBlaze TX differential pair
Right	Bottom	VDDG[2]	W21	GTXN[7]	GigaBlaze TX differential pair
Right	Bottom	VDDG[2]	W22	GTXP[7]	GigaBlaze TX differential pair
Right	Bottom	VDDG[2]	AC27	GRXP[7]	GigaBlaze RX differential pair
Right	Bottom	VDDG[2]	AB27	GRXN[7]	GigaBlaze RX differential pair
Right	Bottom	VDDG[3]	AD28	GRXN[8]	GigaBlaze RX differential pair
Right	Bottom	VDDG[3]	AE28	GRXP[8]	GigaBlaze RX differential pair
Right	Bottom	VDDG[3]	W19	GTXP[8]	GigaBlaze TX differential pair
Right	Bottom	VDDG[3]	Y20	GTXN[8]	GigaBlaze TX differential pair
Right	Bottom	VDDG[3]	AA24	GTXN[9]	GigaBlaze TX differential pair
Right	Bottom	VDDG[3]	Y24	GTXP[9]	GigaBlaze TX differential pair
Right	Bottom	VDDG[3]	AF29	GRXP[9]	GigaBlaze RX differential pair
Right	Bottom	VDDG[3]	AF28	GRXN[9]	GigaBlaze RX differential pair
Right	Bottom	VDDG[3]	AG30	GRXN[10]	GigaBlaze RX differential pair
Right	Bottom	VDDG[3]	AG29	GRXP[10]	GigaBlaze RX differential pair
(Sheet 13 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Right	Bottom	VDDG[3]	Y21	GTXP[10]	GigaBlaze TX differential pair
Right	Bottom	VDDG[3]	Y22	GTXN[10]	GigaBlaze TX differential pair
Right	Bottom	VDDG[3]	AA22	GTXN[11]	GigaBlaze TX differential pair
Right	Bottom	VDDG[3]	AA23	GTXP[11]	GigaBlaze TX differential pair
Right	Bottom	VDDG[3]	AD26	GRXP[11]	GigaBlaze RX differential pair
Right	Bottom	VDDG[3]	AC26	GRXN[11]	GigaBlaze RX differential pair
Right	Bottom	VDDG[3]	AC25	GBRTRIM	GigaBlaze RTRIM
Right	Bottom	VDDGCK[2]	AG27	GCKP[2]	GigaBlaze differential TX reference clock
Right	Bottom	VDDGCK[2]	AF27	GCKN[2]	GigaBlaze differential TX reference clock
Bottom	Right	VDDR[4]	AE24	PCKP[2]	PLL601250 Differential clock input / Configurable I/O
Bottom	Right	VDDR[4]	AD24	PCKN[2]	PLL601250 Differential clock input / Configurable I/O
Bottom	Right	VDDR[4]	AC22	PCKS[2]	PLL601250 Single-ended clock input / Configurable I/O
Bottom	Right	VDDR[4]	AH28	CFG[21]	Configurable I/O
Bottom	Right	VDDR[4]	AG26	CFG[22]	Configurable I/O
Bottom	Right	VDDR[4]	AH29	CFG[23]	Configurable I/O
Bottom	Right	VDDR[4]	AH30	CFG[24]	Configurable I/O
Bottom	Right	VDDR[4]	AF24	CFG[25]	Configurable I/O
Bottom	Right	VDDR[4]	AB21	CFG[26]	Configurable I/O
Bottom	Right	VDDR[4]	AA20	CFG[27]	Configurable I/O
Bottom	Right	VDDR[4]	AJ30	CFG[28]	Configurable I/O
Bottom	Right	VDDR[4]	AE23	CFG[29]	Configurable I/O
(Sheet 14 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDR[4]	AG25	CFG[30]	Configurable I/O
Bottom	Right	VDDR[4]	AD22	CFG[31]	Configurable I/O
Bottom	Right	VDDR[4]	AF23	CFG[32]	Configurable I/O
Bottom	Right	VDDR[4]	AJ28	CFG[33]	Configurable I/O
Bottom	Right	VDDR[4]	AC21	CFG[34]	Configurable I/O
Bottom	Right	VDDR[4]	AB20	CFG[35]	Configurable I/O
Bottom	Right	VDDR[4]	AH26	CFG[36]	Configurable I/O
Bottom	Right	VDDR[4]	AH25	CFG[37]	Configurable I/O
Bottom	Right	VDDR[4]	AE22	CFG[38]	Configurable I/O
Bottom	Right	VDDR[4]	AK29	CFG[39]	Configurable I/O
Bottom	Right	VDDR[5]	AG23	CFG[40]	Configurable I/O
Bottom	Right	VDDR[5]	AD21	CFG[41]	Configurable I/O
Bottom	Right	VDDR[5]	AA19	CFG[42]	Configurable I/O
Bottom	Right	VDDR[5]	AB19	CFG[43]	Configurable I/O
Bottom	Right	VDDR[5]	AH24	CFG[44]	Configurable I/O
Bottom	Right	VDDR[5]	AJ27	CFG[45]	Configurable I/O
Bottom	Right	VDDR[5]	AJ26	CFG[46]	Configurable I/O
Bottom	Right	VDDR[5]	AK27	CFG[47]	Configurable I/O
Bottom	Right	VDDR[5]	AG22	CFG[48]	Configurable I/O
Bottom	Right	VDDR[5]	AD20	CFG[49]	Configurable I/O
Bottom	Right	VDDR[5]	Y18	CFG[50]	Configurable I/O
Bottom	Right	VDDR[5]	AC19	CFG[51]	Configurable I/O
Bottom	Right	VDDR[5]	AJ24	CFG[52]	Configurable I/O
(Sheet 15 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDR[5]	AF21	CFG[53]	Configurable I/O
Bottom	Right	VDDR[5]	AK26	CFG[54]	Configurable I/O
Bottom	Right	VDDR[5]	AK25	CFG[55]	Configurable I/O
Bottom	Right	VDDR[5]	AJ23	CFG[56]	Configurable I/O
Bottom	Right	VDDR[5]	AE20	CFG[57]	Configurable I/O
Bottom	Right	VDDR[5]	AA18	CFG[58]	Configurable I/O
Bottom	Right	VDDR[5]	AC18	CFG[59]	Configurable I/O
Bottom	Right	VDDR[6]	AF20	CFG[60]	Configurable I/O
Bottom	Right	VDDR[6]	AG21	CFG[61]	Configurable I/O
Bottom	Right	VDDR[6]	AH22	CFG[62]	Configurable I/O
Bottom	Right	VDDR[6]	AE19	CFG[63]	Configurable I/O
Bottom	Right	VDDR[6]	AJ22	CFG[64]	Configurable I/O
Bottom	Right	VDDR[6]	AD18	CFG[65]	Configurable I/O
Bottom	Right	VDDR[6]	W17	CFG[66]	Configurable I/O
Bottom	Right	VDDR[6]	AB17	CFG[67]	Configurable I/O
Bottom	Right	VDDR[6]	AK24	CFG[68]	Configurable I/O
Bottom	Right	VDDR[6]	AH21	CFG[69]	Configurable I/O
Bottom	Right	VDDR[6]	AF19	CFG[70]	Configurable I/O
Bottom	Right	VDDR[6]	AE18	CFG[71]	Configurable I/O
Bottom	Right	VDDR[6]	AK23	CFG[72]	Configurable I/O
Bottom	Right	VDDR[6]	AD17	CFG[73]	Configurable I/O
Bottom	Right	VDDR[6]	Y17	CFG[74]	Configurable I/O
Bottom	Right	VDDR[6]	AC17	CFG[75]	Configurable I/O
(Sheet 16 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDR[6]	AH20	CFG[76]	Configurable I/O
Bottom	Right	VDDR[6]	AK22	CFG[77]	Configurable I/O
Bottom	Right	VDDR[6]	AG19	CFG[78]	Configurable I/O
Bottom	Right	VDDR[6]	AK21	CFG[79]	Configurable I/O
Bottom	Right	VDDR[7]	AG18	CFG[80]	Configurable I/O
Bottom	Right	VDDR[7]	AJ20	CFG[81]	Configurable I/O
Bottom	Right	VDDR[7]	AA16	CFG[82]	Configurable I/O
Bottom	Right	VDDR[7]	AB16	CFG[83]	Configurable I/O
Bottom	Right	VDDR[7]	AJ19	CFG[84]	Configurable I/O
Bottom	Right	VDDR[7]	AG17	CFG[85]	Configurable I/O
Bottom	Right	VDDR[7]	AF17	CFG[86]	Configurable I/O
Bottom	Right	VDDR[7]	AH18	CFG[87]	Configurable I/O
Bottom	Right	VDDR[7]	AH17	CFG[88]	Configurable I/O
Bottom	Right	VDDR[7]	AK20	CFG[89]	Configurable I/O
Bottom	Right	VDDR[7]	AD15	CFG[90]	Configurable I/O
Bottom	Right	VDDR[7]	AD16	CFG[91]	Configurable I/O
Bottom	Right	VDDR[7]	AK19	CFG[92]	Configurable I/O
Bottom	Right	VDDR[7]	AF16	CFG[93]	Configurable I/O
Bottom	Right	VDDR[7]	AJ18	CFG[94]	Configurable I/O
Bottom	Right	VDDR[7]	AK18	CFG[95]	Configurable I/O
Bottom	Right	VDDR[7]	AJ16	CFG[96]	Configurable I/O
Bottom	Right	VDDR[7]	AK17	CFG[97]	Configurable I/O
Bottom	Right	VDDR[7]	AB15	CFG[98]	Configurable I/O
(Sheet 17 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDR[7]	AA15	CFG[99]	Configurable I/O
Bottom	Right	VDDR[8]	AF15	CFG[100]	Configurable I/O
Bottom	Right	VDDR[8]	AJ15	CFG[101]	Configurable I/O
Bottom	Right	VDDR[8]	AK14	CFG[102]	Configurable I/O
Bottom	Right	VDDR[8]	AK13	CFG[103]	Configurable I/O
Bottom	Right	VDDR[8]	AG14	CFG[104]	Configurable I/O
Bottom	Right	VDDR[8]	AH14	CFG[105]	Configurable I/O
Bottom	Right	VDDR[8]	W14	CFG[106]	Configurable I/O
Bottom	Right	VDDR[8]	AC14	CFG[107]	Configurable I/O
Bottom	Right	VDDR[8]	AF14	CFG[108]	Configurable I/O
Bottom	Right	VDDR[8]	AJ13	CFG[109]	Configurable I/O
Bottom	Right	VDDR[8]	AJ12	CFG[110]	Configurable I/O
Bottom	Right	VDDR[8]	AH13	CFG[111]	Configurable I/O
Bottom	Right	VDDR[8]	AD14	CFG[112]	Configurable I/O
Bottom	Right	VDDR[8]	AK11	CFG[113]	Configurable I/O
Bottom	Right	VDDR[8]	Y14	CFG[114]	Configurable I/O
Bottom	Right	VDDR[8]	AB14	CFG[115]	Configurable I/O
Bottom	Right	VDDR[8]	AG13	CFG[116]	Configurable I/O
Bottom	Right	VDDR[8]	AJ11	CFG[117]	Configurable I/O
Bottom	Right	VDDR[8]	AK10	CFG[118]	Configurable I/O
Bottom	Right	VDDR[8]	AH11	CFG[119]	Configurable I/O
Bottom	Right	VDDR[9]	AE13	CFG[120]	Configurable I/O
Bottom	Right	VDDR[9]	AF12	CFG[121]	Configurable I/O
(Sheet 18 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDR[9]	AC12	CFG[122]	Configurable I/O
Bottom	Right	VDDR[9]	AC13	CFG[123]	Configurable I/O
Bottom	Right	VDDR[9]	AD13	CFG[124]	Configurable I/O
Bottom	Right	VDDR[9]	AG12	CFG[125]	Configurable I/O
Bottom	Right	VDDR[9]	AK09	CFG[126]	Configurable I/O
Bottom	Right	VDDR[9]	AJ09	CFG[127]	Configurable I/O
Bottom	Right	VDDR[9]	AG10	CFG[128]	Configurable I/O
Bottom	Right	VDDR[9]	AH10	CFG[129]	Configurable I/O
Bottom	Right	VDDR[9]	Y13	CFG[130]	Configurable I/O
Bottom	Right	VDDR[9]	AB12	CFG[131]	Configurable I/O
Bottom	Right	VDDR[9]	AE12	CFG[132]	Configurable I/O
Bottom	Right	VDDR[9]	AF11	CFG[133]	Configurable I/O
Bottom	Right	VDDR[9]	AH09	CFG[134]	Configurable I/O
Bottom	Right	VDDR[9]	AK08	CFG[135]	Configurable I/O
Bottom	Right	VDDR[9]	AJ08	CFG[136]	Configurable I/O
Bottom	Right	VDDR[9]	AK07	CFG[137]	Configurable I/O
Bottom	Right	VDDR[9]	AA12	CFG[138]	Configurable I/O
Bottom	Right	VDDR[9]	AA13	CFG[139]	Configurable I/O
Bottom	Right	VDDR[10]	AE11	CFG[140]	Configurable I/O
Bottom	Right	VDDR[10]	AF10	CFG[141]	Configurable I/O
Bottom	Right	VDDR[10]	AD11	CFG[142]	Configurable I/O
Bottom	Right	VDDR[10]	AK06	CFG[143]	Configurable I/O
Bottom	Right	VDDR[10]	AJ07	CFG[144]	Configurable I/O
(Sheet 19 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Bottom	Right	VDDR[10]	AG09	CFG[145]	Configurable I/O
Bottom	Right	VDDR[10]	W12	CFG[146]	Configurable I/O
Bottom	Right	VDDR[10]	AB11	CFG[147]	Configurable I/O
Bottom	Right	VDDR[10]	AK05	CFG[148]	Configurable I/O
Bottom	Right	VDDR[10]	AK04	CFG[149]	Configurable I/O
Bottom	Right	VDDR[10]	AG08	CFG[150]	Configurable I/O
Bottom	Right	VDDR[10]	AH07	CFG[151]	Configurable I/O
Bottom	Right	VDDR[10]	AD10	CFG[152]	Configurable I/O
Bottom	Right	VDDR[10]	AJ05	CFG[153]	Configurable I/O
Bottom	Right	VDDR[10]	Y11	CFG[154]	Configurable I/O
Bottom	Right	VDDR[10]	AA11	CFG[155]	Configurable I/O
Bottom	Right	VDDR[10]	AC10	CFG[156]	Configurable I/O
Bottom	Right	VDDR[11]	AE09	TN	Reserved Test
Bottom	Right	VDDR[11]	AD09	TDO	Reserved Test
Bottom	Right	VDDR[11]	AF08	TCK	Reserved Test
Bottom	Right	VDDR[11]	AG06	TRSTN	Reserved Test
Bottom	Right	VDDR[11]	AH06	IDDT	Reserved Test
Bottom	Right	VDDR[11]	AE08	TDI	Reserved Test
Bottom	Right	VDDR[11]	AF06	TMS	Reserved Test
Bottom	Right	VDDR[11]	AH05	SEN	Reserved Test
Bottom	Right	VDDR[11]	AF07	PMON	Reserved Test
Left	Top	VDDR[12]	AB08	PCKP[3]	PLL601250 Differential clock input / Configurable I/O
(Sheet 20 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[12]	AC08	PCKN[3]	PLL601250 Differential clock input / Configurable I/O
Left	Top	VDDR[12]	AD07	PCKS[3]	PLL601250 Single-ended clock input / Configurable I/O
Left	Top	VDDR[12]	AG05	CFG[157]	Configurable I/O
Left	Top	VDDR[12]	AK03	CFG[158]	Configurable I/O
Left	Top	VDDR[12]	AG04	CFG[159]	Configurable I/O
Left	Top	VDDR[12]	AJ04	CFG[160]	Configurable I/O
Left	Top	VDDR[12]	AJ03	CFG[161]	Configurable I/O
Left	Top	VDDR[12]	AE05	CFG[162]	Configurable I/O
Left	Top	VDDR[12]	AD05	CFG[163]	Configurable I/O
Left	Top	VDDR[12]	AK02	CFG[164]	Configurable I/O
Left	Top	VDDR[12]	AH03	CFG[165]	Configurable I/O
Left	Top	VDDR[12]	AF04	CFG[166]	Configurable I/O
Left	Top	VDDR[12]	AJ01	CFG[167]	Configurable I/O
Left	Top	VDDR[12]	AH02	CFG[168]	Configurable I/O
Left	Top	VDDR[12]	AE04	CFG[169]	Configurable I/O
Left	Top	VDDR[12]	AC06	CFG[170]	Configurable I/O
Left	Top	VDDR[12]	AB07	CFG[171]	Configurable I/O
Left	Top	VDDR[13]	AF03	CFG[172]	Configurable I/O
Left	Top	VDDR[13]	AA09	CFG[173]	Configurable I/O
Left	Top	VDDR[13]	Y10	CFG[174]	Configurable I/O
Left	Top	VDDR[13]	AC05	CFG[175]	Configurable I/O
Left	Top	VDDR[13]	AG02	CFG[176]	Configurable I/O
(Sheet 21 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[13]	AE03	CFG[177]	Configurable I/O
Left	Top	VDDR[13]	AB06	CFG[178]	Configurable I/O
Left	Top	VDDR[13]	AC04	CFG[179]	Configurable I/O
Left	Top	VDDR[13]	AH01	CFG[180]	Configurable I/O
Left	Top	VDDR[13]	AA08	CFG[181]	Configurable I/O
Left	Top	VDDR[13]	Y09	CFG[182]	Configurable I/O
Left	Top	VDDR[13]	AA07	CFG[183]	Configurable I/O
Left	Top	VDDR[13]	AD03	CFG[184]	Configurable I/O
Left	Top	VDDR[13]	AF02	CFG[185]	Configurable I/O
Left	Top	VDDR[13]	AD02	CFG[186]	Configurable I/O
Left	Top	VDDR[13]	AF01	CFG[187]	Configurable I/O
Left	Top	VDDR[13]	W10	CFG[188]	Configurable I/O
Left	Top	VDDR[13]	W09	CFG[189]	Configurable I/O
Left	Top	VDDR[13]	Y07	CFG[190]	Configurable I/O
Left	Top	VDDR[13]	AB04	CFG[191]	Configurable I/O
Left	Top	VDDR[13]	AE01	CFG[192]	Configurable I/O
Left	Top	VDDR[13]	AA05	CFG[193]	Configurable I/O
Left	Top	VDDR[13]	AD01	CFG[194]	Configurable I/O
Left	Top	VDDR[13]	AC02	CFG[195]	Configurable I/O
Left	Top	VDDR[13]	V11	CFG[196]	Configurable I/O
Left	Top	VDDR[13]	W08	CFG[197]	Configurable I/O
Left	Top	VDDR[13]	Y06	CFG[198]	Configurable I/O
Left	Top	VDDR[13]	AB03	CFG[199]	Configurable I/O
(Sheet 22 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[13]	AB02	CFG[200]	Configurable I/O
Left	Top	VDDR[13]	AA04	CFG[201]	Configurable I/O
Left	Top	VDDR[13]	AB01	CFG[202]	Configurable I/O
Left	Top	VDDR[13]	Y05	CFG[203]	Configurable I/O
Left	Top	VDDR[13]	V10	CFG[204]	Configurable I/O
Left	Top	VDDR[13]	V08	CFG[205]	Configurable I/O
Left	Top	VDDR[14]	V07	CFG[206]	Configurable I/O
Left	Top	VDDR[14]	W06	CFG[207]	Configurable I/O
Left	Top	VDDR[14]	AA03	CFG[208]	Configurable I/O
Left	Top	VDDR[14]	Y03	CFG[209]	Configurable I/O
Left	Top	VDDR[14]	V06	CFG[210]	Configurable I/O
Left	Top	VDDR[14]	W05	CFG[211]	Configurable I/O
Left	Top	VDDR[14]	U12	CFG[212]	Configurable I/O
Left	Top	VDDR[14]	U09	CFG[213]	Configurable I/O
Left	Top	VDDR[14]	U07	CFG[214]	Configurable I/O
Left	Top	VDDR[14]	AA01	CFG[215]	Configurable I/O
Left	Top	VDDR[14]	W04	CFG[216]	Configurable I/O
Left	Top	VDDR[14]	U08	CFG[217]	Configurable I/O
Left	Top	VDDR[14]	Y02	CFG[218]	Configurable I/O
Left	Top	VDDR[14]	U11	CFG[219]	Configurable I/O
Left	Top	VDDR[14]	Y01	CFG[220]	Configurable I/O
Left	Top	VDDR[14]	W02	CFG[221]	Configurable I/O
Left	Top	VDDR[14]	W01	CFG[222]	Configurable I/O
(Sheet 23 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[14]	V04	CFG[223]	Configurable I/O
Left	Top	VDDR[14]	V03	CFG[224]	Configurable I/O
Left	Top	VDDR[14]	U05	CFG[225]	Configurable I/O
Left	Top	VDDR[14]	U04	CFG[226]	Configurable I/O
Left	Top	VDDR[14]	T10	CFG[227]	Configurable I/O
Left	Top	VDDR[14]	T09	CFG[228]	Configurable I/O
Left	Top	VDDR[14]	V02	CFG[229]	Configurable I/O
Left	Top	VDDR[14]	V01	CFG[230]	Configurable I/O
Left	Top	VDDR[14]	U03	CFG[231]	Configurable I/O
Left	Top	VDDR[14]	U01	CFG[232]	Configurable I/O
Left	Top	VDDR[14]	T01	CFG[233]	Configurable I/O
Left	Top	VDDR[14]	T05	CFG[234]	Configurable I/O
Left	Top	VDDR[14]	R07	CFG[235]	Configurable I/O
Left	Top	VDDR[14]	T07	CFG[236]	Configurable I/O
Left	Top	VDDR[14]	T02	CFG[237]	Configurable I/O
Left	Top	VDDR[14]	R01	CFG[238]	Configurable I/O
Left	Top	VDDR[14]	R02	CFG[239]	Configurable I/O
Left	Top	VDDR[15]	R05	CFG[240]	Configurable I/O
Left	Top	VDDR[15]	N01	CFG[241]	Configurable I/O
Left	Top	VDDR[15]	P01	CFG[242]	Configurable I/O
Left	Top	VDDR[15]	R09	CFG[243]	Configurable I/O
Left	Top	VDDR[15]	R10	CFG[244]	Configurable I/O
Left	Top	VDDR[15]	P03	CFG[245]	Configurable I/O
(Sheet 24 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[15]	N02	CFG[246]	Configurable I/O
Left	Top	VDDR[15]	P04	CFG[247]	Configurable I/O
Left	Top	VDDR[15]	P05	CFG[248]	Configurable I/O
Left	Top	VDDR[15]	M02	CFG[249]	Configurable I/O
Left	Top	VDDR[15]	M01	CFG[250]	Configurable I/O
Left	Top	VDDR[15]	P11	CFG[251]	Configurable I/O
Left	Top	VDDR[15]	N03	CFG[252]	Configurable I/O
Left	Top	VDDR[15]	L01	CFG[253]	Configurable I/O
Left	Top	VDDR[15]	P07	CFG[254]	Configurable I/O
Left	Top	VDDR[15]	N04	CFG[255]	Configurable I/O
Left	Top	VDDR[15]	K01	CFG[256]	Configurable I/O
Left	Top	VDDR[15]	L02	CFG[257]	Configurable I/O
Left	Top	VDDR[15]	P12	CFG[258]	Configurable I/O
Left	Top	VDDR[15]	P09	CFG[259]	Configurable I/O
Left	Top	VDDR[15]	M04	CFG[260]	Configurable I/O
Left	Top	VDDR[15]	M05	CFG[261]	Configurable I/O
Left	Top	VDDR[15]	N06	CFG[262]	Configurable I/O
Left	Top	VDDR[15]	N07	CFG[263]	Configurable I/O
Left	Top	VDDR[15]	J01	CFG[264]	Configurable I/O
Left	Top	VDDR[15]	L03	CFG[265]	Configurable I/O
Left	Top	VDDR[15]	N08	CFG[266]	Configurable I/O
Left	Top	VDDR[15]	P08	CFG[267]	Configurable I/O
Left	Top	VDDR[15]	J02	CFG[268]	Configurable I/O
(Sheet 25 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[15]	K03	CFG[269]	Configurable I/O
Left	Top	VDDR[15]	L05	CFG[270]	Configurable I/O
Left	Top	VDDR[15]	M06	CFG[271]	Configurable I/O
Left	Top	VDDR[15]	K04	CFG[272]	Configurable I/O
Left	Top	VDDR[15]	J03	CFG[273]	Configurable I/O
Left	Top	VDDR[16]	N11	CFG[274]	Configurable I/O
Left	Top	VDDR[16]	M09	CFG[275]	Configurable I/O
Left	Top	VDDR[16]	L06	CFG[276]	Configurable I/O
Left	Top	VDDR[16]	K05	CFG[277]	Configurable I/O
Left	Top	VDDR[16]	H01	CFG[278]	Configurable I/O
Left	Top	VDDR[16]	G01	CFG[279]	Configurable I/O
Left	Top	VDDR[16]	L07	CFG[280]	Configurable I/O
Left	Top	VDDR[16]	M08	CFG[281]	Configurable I/O
Left	Top	VDDR[16]	M10	CFG[282]	Configurable I/O
Left	Top	VDDR[16]	N10	CFG[283]	Configurable I/O
Left	Top	VDDR[16]	J04	CFG[284]	Configurable I/O
Left	Top	VDDR[16]	H02	CFG[285]	Configurable I/O
Left	Top	VDDR[16]	F01	CFG[286]	Configurable I/O
Left	Top	VDDR[16]	G02	CFG[287]	Configurable I/O
Left	Top	VDDR[16]	E01	CFG[288]	Configurable I/O
Left	Top	VDDR[16]	H04	CFG[289]	Configurable I/O
Left	Top	VDDR[16]	L09	CFG[290]	Configurable I/O
Left	Top	VDDR[16]	K09	CFG[291]	Configurable I/O
(Sheet 26 of 27)					

Table A.12 FC896 Package I/O Assignments (RC11XT531) (Cont.)

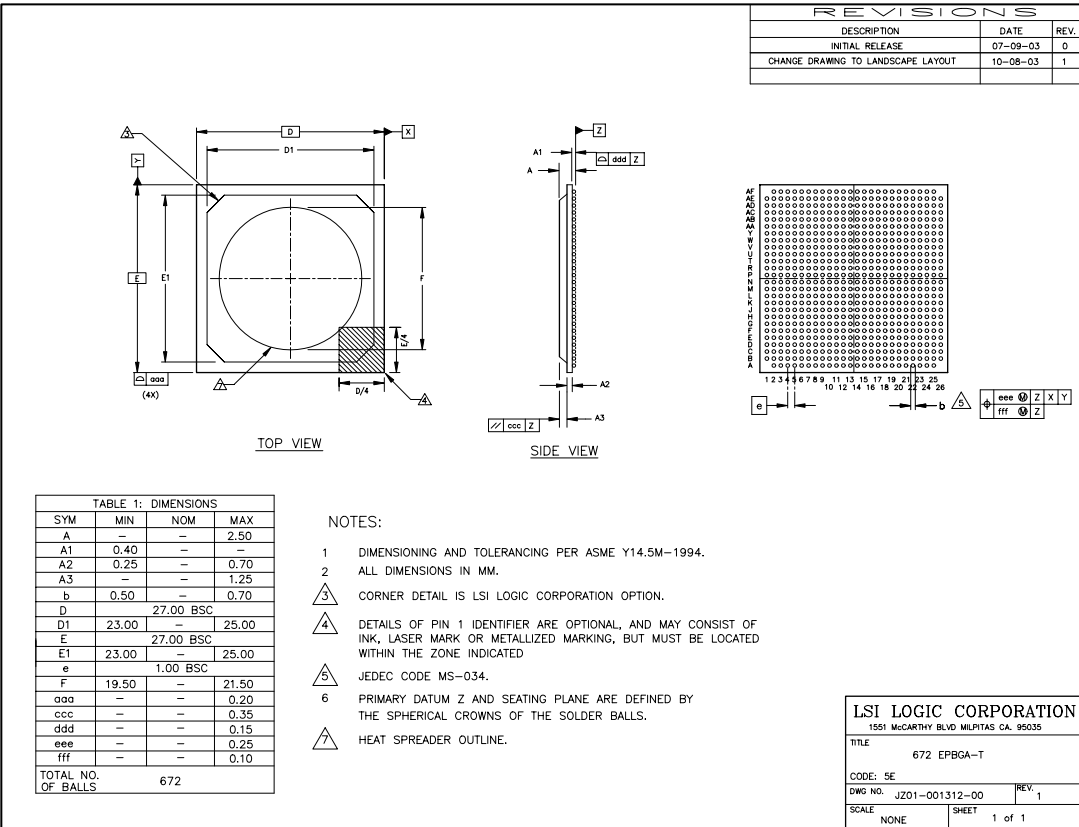
Package Edge	Die Edge	Domain	FC896 Package Ball	Signal	Description
Left	Top	VDDR[16]	D01	CFG[292]	Configurable I/O
Left	Top	VDDR[16]	K07	CFG[293]	Configurable I/O
Left	Top	VDDR[16]	J06	CFG[294]	Configurable I/O
Left	Top	VDDR[16]	H05	CFG[295]	Configurable I/O
Left	Top	VDDR[16]	M12	CFG[296]	Configurable I/O
Left	Top	VDDR[16]	K08	CFG[297]	Configurable I/O
Left	Top	VDDR[16]	G03	CFG[298]	Configurable I/O
Left	Top	VDDR[16]	L10	CFG[299]	Configurable I/O
Left	Top	VDDR[16]	E02	CFG[300]	Configurable I/O
Left	Top	VDDR[16]	F03	CFG[301]	Configurable I/O
Left	Top	VDDR[16]	J07	CFG[302]	Configurable I/O
Left	Top	VDDR[16]	F04	CFG[303]	Configurable I/O
Left	Top	VDDR[16]	G05	CFG[304]	Configurable I/O
Left	Top	VDDR[16]	H06	CFG[305]	Configurable I/O
Left	Top	VDDR[16]	L11	CFG[306]	Configurable I/O
Left	Top	VDDR[16]	C01	CFG[307]	Configurable I/O
Left	Top	VDDR[16]	E03	CFG[308]	Configurable I/O
Left	Top	VDDR[16]	D02	CFG[309]	Configurable I/O
Left	Top	VDDR[16]	E04	CFG[310]	Configurable I/O
Left	Top	VDDR[16]	F05	CFG[311]	Configurable I/O
Left	Top	VDDR[16]	D04	CFG[312]	Configurable I/O
Left	Top	VDDR[16]	B01	CFG[313]	Configurable I/O
Left	Top	VDDR[16]	C02	CFG[314]	Configurable I/O
(Sheet 27 of 27)					

A.4 Package Mechanical Drawings

This section provides mechanical drawings of the packages that are used for the RapidChip Xtreme platform ASICs. It includes the following drawings:

- [Figure A.7, 672-Ball Count EPBGA-T \(5E\) Mechanical Drawing](#)
- [Figure A.8, 672-Ball Count FCBGA Mechanical Drawing](#)
- [Figure A.9, 896-Ball Count FCBGA \(9P\) Mechanical Drawing](#)

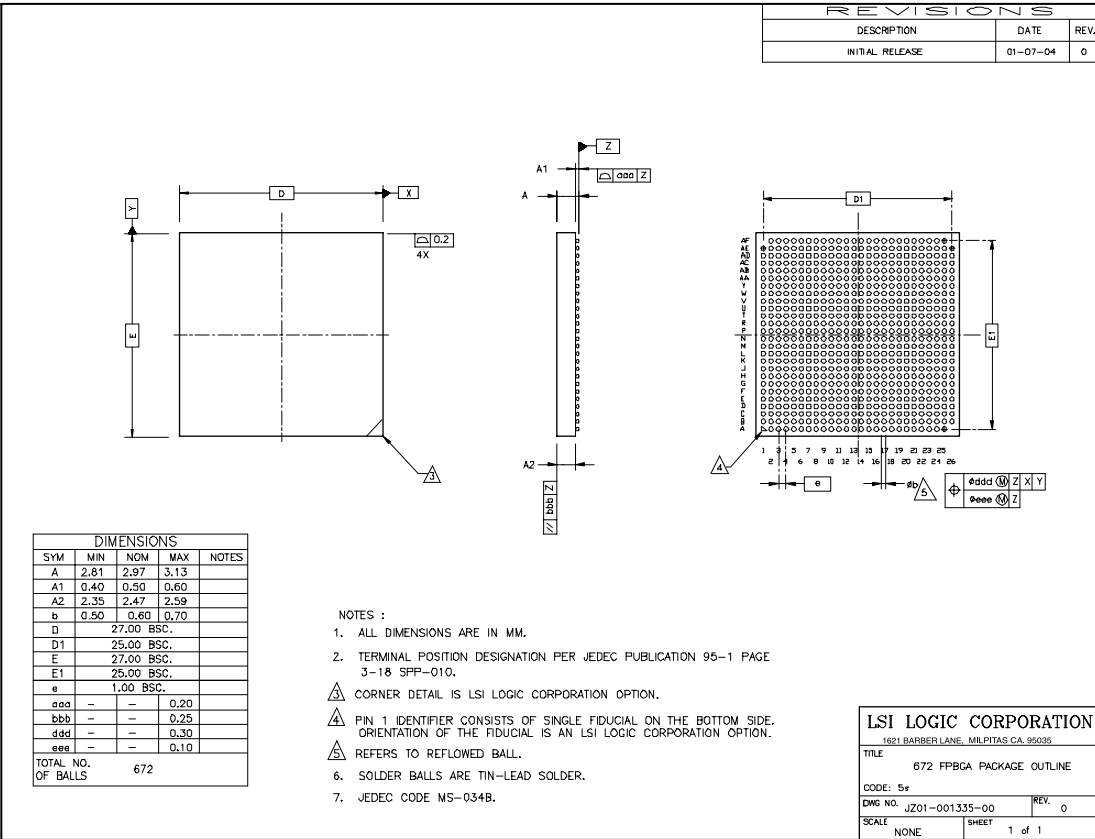
Figure A.7 672-Ball Count EPBGA-T (5E) Mechanical Drawing



Important:

This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative.

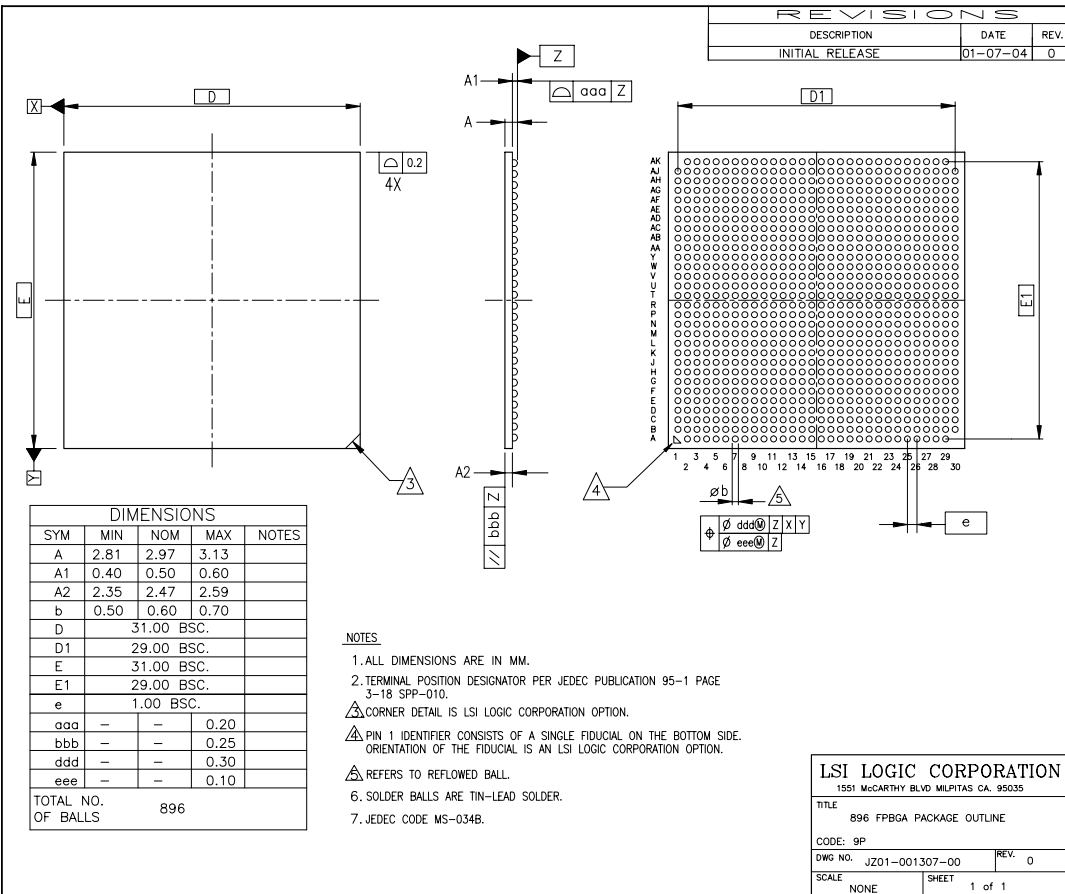
Figure A.8 672-Ball Count FCBGA Mechanical Drawing



Important:

This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative.

Figure A.9 896-Ball Count FCBGA (9P) Mechanical Drawing



Important:

This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative.