LSI LOGIC

Full Duplex

80C26

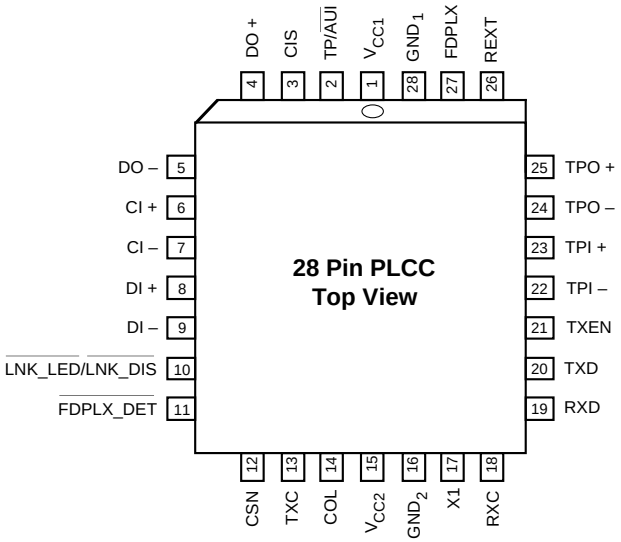
CMOS Ethernet Interface Adapter in 28L Package

96346

Functional Features

- Low Power CMOS Technology Ethernet Serial Interface Adapter with Integrated Manchester Code Converter (MCC™), AUI and 10Base-T Transceiver with Output Wave Shaping and on chip filters.
- Meets IEEE 802.3 10Base-5, 10Base-2, 10Base-T Standards
- Direct Interface to NSC & AMD Controllers, See the 80C25 Data Sheet for Direct Interface to SEEQ and Intel Controllers
- Automatic or Manual Selection of AUI/10Base-T Interface
- Provides AutoDUPLEX™ Detect Function for Full Duplex LAN Controllers, Doubling Bandwidth to 20 MBits/sec for Switched Networks
- Separate Analog/Digital Power and Ground Pins to Minimize Noise

Pin Configuration



Note: Check for latest Data Sheet revision before starting any designs.

SEEQ Data Sheets are now on the Web, at www.lsilogic.com.

This document is an LSI Logic document. Any reference to SEEQ Technology should be considered LSI Logic.

Interface Features

- Meets IEEE 10Base-T Standards and IEEE 802.3 standards for AUI.
- On Chip Transmit Wave Shaping and Low Pass Filter Circuits - No External Filters Required
- Link Integrity Test Disable, Selectable Coded Link Pulse for AutoDUPLEX Mode
- Automatic Polarity Correction
- Low differential and common mode noise on TP transmit outputs.
- Differential Transmit Drivers to support 50 Meters of AUI Cable Lengths.
- Direct AUI interface to the Manchester Code Converter.

General Description

The SEEQ 80C26 is a CMOS single chip Ethernet serial interface adapter with a integrated Manchester Code Converter (MCC), AUI & 10Base-T transceiver with wave shaping & filters eliminating the need for external filters. The 80C26 is designed to interface directly with National and AMD Ethernet controllers. The chip provides automatic polarity correction, automatic port selection, separate analog & digital ground pins & a link disable feature. It also provides a selectable coded link pulse to implement AutoDUPLEX function together with a Full Duplex controller allowing seamless full duplex operation in switched network implementations doubling network bandwidth to 20 Mbps in 10Base-T. The 80C26 is typically suitable for adapter boards, motherboards and stand-alone TP transceiver designs & switching hubs.

MCC and AutoDUPLEX are trademarks of SEEQ Technology, Inc.

80C26 Pin Description

Pin	Name	I/O	Description
1	V_{CC1}	—	Power Supply. +5 Volts.
2	TP/AUI	I Pullup To $V_{CC}/2$	TP or AUI or Autoport Select Input. This pin selects the interface to the ENDEC. This pin is a three state input that is internally biased at $V_{CC}/2$. TP/$\overline{\text{AUI}}$ 1 TP Port float Autoport 0 AUI Port
3	CIS	I Pulldown	Controller Interface Select Input. CIS 0 NSC 1 AMD The 80C25 Provides interface to SEEQ and Intel Controllers.
4	DO +	O	AUI Transmit Output, Positive.
5	DO –	O	AUI Transmit Output, Negative.
6	CI +	I	AUI Collision Input, Positive.
7	CI –	I	AUI Collision Input, Negative.
8	DI +	I	AUI Receive Input, Positive.
9	DI –	I	AUI Receive Input, Negative.
10	$\overline{\text{LNK\_LED}}$ /$\overline{\text{LNK\_DIS}}$	I/O	Link Detect Output and Link Disable Input. This pin consists of an open drain output transistor. If the pin is tied to D_{GND}, the link test function is disabled. Otherwise, the pin is a Link Pulse Detect output and can drive an LED. $\overline{\text{LNK\_LED}}$ = 1 Output Link Pulse Not Detected $\overline{\text{LNK\_LED}}$ = 0 Output Link Pulse Detected $\overline{\text{LNK\_LED}}$ = D_{GND} Input Link Test Function Disabled
11	$\overline{\text{FDPLX\_DET}}$	O	Full Duplex Detect Output. When $\overline{\text{FDPLX\_DET}}$ = 0, the device has been placed in the full duplex mode by either selection or by the AutoDUPLEX feature.
12	CSN	O	Carrier Sense Output. This controller interface output indicates valid data and collisions on the receive TP or AUI inputs.
13	TXC	O	Transmit Clock Output. This controller interface output provides a 10 MHz clock to the controller. Transmit data from the controller on TXD is clocked in on edges of TXC.

Pin Description cont'd

Pin	Name	I/O	Description
14	COL	O	Collision Output. This controller interface output is asserted when collision transmit and receive data occurs and during SQE test.
15	V_{CC2}	—	Power Supply. +5 Volts.
16	GND_2	—	Ground. 0 Volts.
17	X1	I	Crystal Oscillator Input. The master clock for the device is generated by either placing a crystal between X1 and DGND, or by applying an external clock to X1. If a crystal is used as the clock source, connect a 1M Ω resistor between X1 and GND. For external oscillator operation, connect a 470 Ω resistor in series between X1 and clock source.
18	RXC	O	Receive Clock Output. This controller interface output provides a 10 MHz clock to the controller. Receive data on RXD is clocked out on edges of RXC.
19	RXD	O	Receive Data Output. This controller interface output contains receive data decoded from the receive TP/AUI inputs and is clock out on edges of RXC.
20	TXD	I	Transmit Data Input. This controller interface input contains data to be transmitted on either TP or AUI transmit outputs and is clocked in on edges of TXC.
21	TXEN	I	Transmit Enable Input. This controller interface input has to be asserted when data on TXD is valid.
22	TPI–	I	Twisted Pair Receive Input, Negative.
23	TPI+	I	Twisted Pair Receive Input, Positive.
24	TPO–	O	Twisted Pair Transmit Output, Negative.
25	TPO+	O	Twisted Pair Transmit Output, Positive.
26	REXT	—	Transmit Current Set. An external resistor tied between this pin and A_{GND} sets the twisted pair transmit output current level on TPO±.
27	FDPLX	I Pullup to $V_{CC}/2$	Full Duplex/AutoDUPLEX Mode Select Input. This pin is a three state input that is internally biased to $V_{CC}/2$. $\overline{\text{FDPLX}}$ 1 — Full Duplex Mode float — AutoDUPLEX Mode 0 — Normal
28	GND_1	—	Ground. 0 Volts.

BLOCK DESCRIPTION

Functional Description

The 80C26 is an Ethernet adapter with a integrated Manchester Code Converter, 10Base-T transceiver with on chip filters. The device contains both 10Base-T and AUI interfaces compliant with IEEE 802.3 specifications. The chip is divided into four major blocks, namely (i) The controller interface (ii) The Encoder / Decoder (iii) The twisted pair interface and (iv) The AUI. The input signals are received on the TP or AUI receivers depending on which is selected. Both the twisted pair and AUI receivers contain a threshold comparator to validate the signal and a zero crossing comparator for checking the transitions. Then the data is sent to the PLL in the decoder to separate the data from the clock. On the other side, digital transmit data is clocked into the device via the controller interface. The data is then sent to the Manchester encoder to be encoded. Encoded data is then transmitted on the twisted pair or AUI based on the selected port.

The Controller Interface

The 80C26 is designed to interface directly to National and AMD Ethernet controllers, with the use of CIS Pin. The controller interface consists of the Transmit/Receive data (TXD/RXD), transmit/receive Clocks (TXC/RXC), the Transmit Enable (TXEN) input, the collision output (COLL), the Full Duplex acknowledgment (FDPLX_DET) and the Carrier Sense Output (CSN) pins. On the transmit side, data on TXD is clocked into the device on the edges of TXC clock output only when the data valid signal (TXEN) is asserted. On the receive side, data on RXD is clocked out on edges of RXC. RXC follows TXC for 1.5 µs and then switches to the recovered clock. The FDPLX_DET pin signifies to the controller that full duplex channels have been established.

The 80C26 supports NSC and AMD Controllers according to Table 1.

Table 1. CIS Pin Description

CIS	Controller Interface
0	NSC
1	AMD

The Encoder/Decoder

Manchester encoding is a process of combining the clock & the data stream together so that they can be transmitted on the twisted pair interface or AUI at the transceiver side. Once encoded, the first half contains the complement of the data and the second half contains the true data, so that a transition is always guaranteed at the middle of a bit cell. Data encoding and transmission begins with TXEN going active, and the subsequent data is clocked on the edges of TXC and then gets encoded. The end of a transmit packet occurs at a bit cell center if the last bit is a "ONE" or at a bit boundary if the last bit is a "ZERO".

The decoding is a process of recovering the encoded data stream coming from the receiver side and decoding it back into the clock and data outputs using the phase locked loop technique. The PLL is designed to lock into the preamble of the incoming signal at less than 15 bit times with a maximum jitter of ±13.5 ns at the TPI or AUI inputs and can also sample the incoming data with this amount of jitter. The ENDEC asserts the CSN signal to indicate to the controller that the data and clock received are valid and available. There is an inhibit period after the end of a frame after a node has finished transmitting for 4.4 µs during which CSN is deasserted irregardless of the state of the receiver and collision status.

Twisted Pair Interface

(a) The transmitter function

The transmitter transfers Manchester encoded data from the ENDEC to the twisted pair cable. The circuit consists of a set of functional blocks to provide pre-coded wave-shaped, pre-equalized and smoothed waveforms so that the outputs are made to appear as though it had passed through a 5-7th order external elliptic passive filter, thereby eliminating the need for an external filter. The waveform generator consists of a ROM, DAC, PLL, filter and a output driver to preshape the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE STD 802.3 and illustrated in figure 12. The DAC first converts the data pulse into a stair stepped representation of the desired output waveform, which goes through a second order low-pass filter. The DAC values are determined from the ROM addresses, which are chosen to have different values for long and short data bits so as to shape the pulse to meet the 10Base-T waveform template. The line driver takes the smoothed current waveform and converts it into an high current output that can drive the TP directly without any

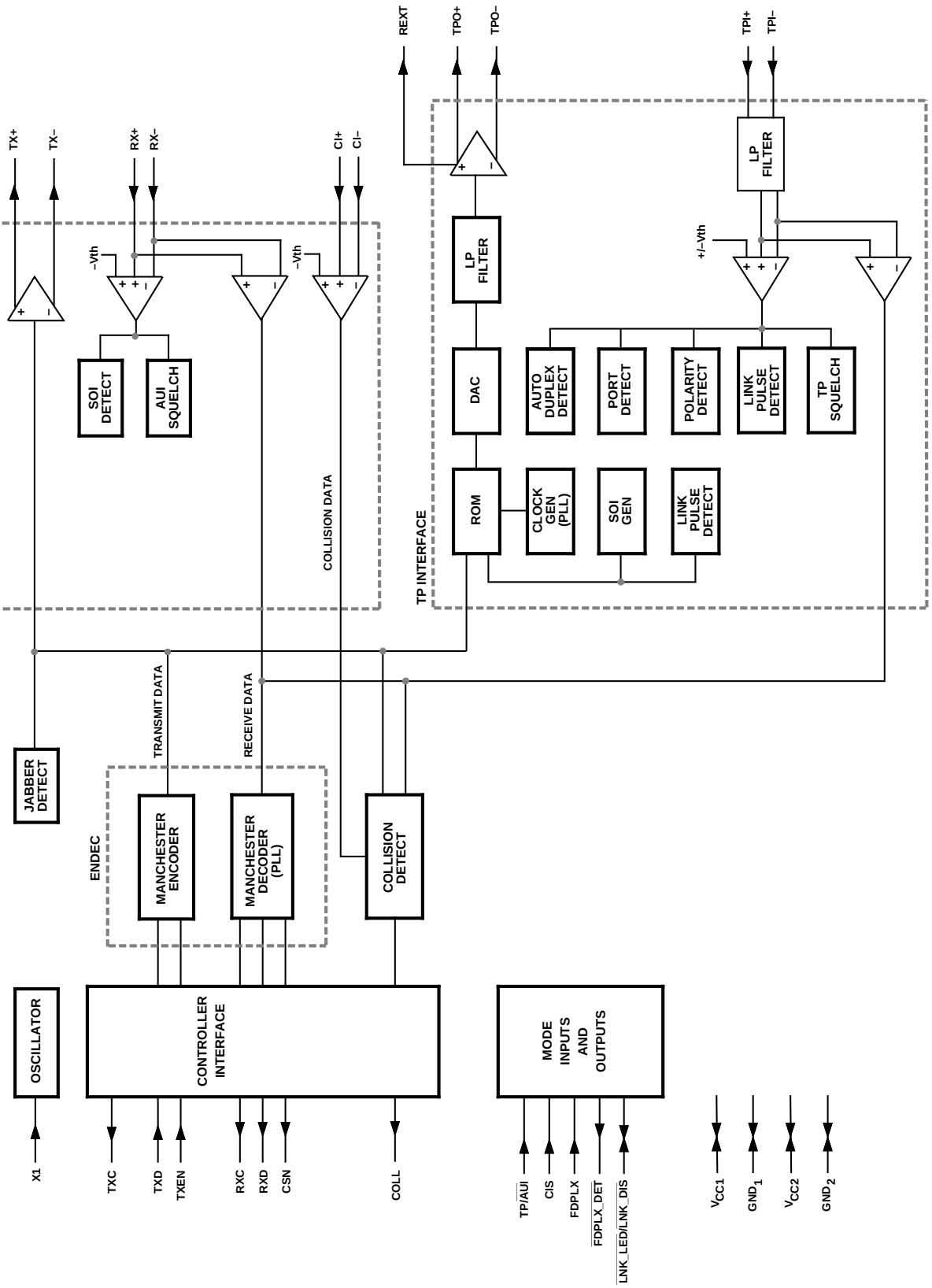


Figure 1. 80C26 Block Diagram

external filters. The current output is guaranteed to have a very low common mode and differential noise. The interface to the twisted pair cable requires a transformer with a ratio of 2:1 on transmit and a 1:1 on receive, with two 200 ohm resistors connected as shown in figure 2. The output driver is a current source. The output current level is set by the values of the resistor tied between the REXT and AGND. The current level is determined by the following equation.

$$I_{OUT} = (REXT/10K)* 50\ mA$$

Though a 10K resistor will meet the template requirements specified with a no load condition, a capacitive or inductive loading can influence the level, because the transmitter has a current source output. So, in a actual application, it might be necessary to adjust the value to compensate the loading involved. For example, the bias resistance value for a loading of 10 pf will be approximately 8K.

(b) The receiver function

The receiver receives the Manchester-encoded data from the twisted pair lines(TPI±) and passes it on to the ENDEC side, where it gets decoded back into the receive clock RXC and the receive data RXD. The inputs first go through a receive filter, which is a continuous time 3rd order low pass filter with a typical 3 dB cutoff frequency of 20-25 Mhz. The filter's output then passes through two different types of comparators, namely threshold and zero crossing. The threshold comparator compares the TPI± inputs with fixed positive and negative thresholds called the squelch levels. The zero crossing comparator senses the transition point on the TPI± inputs without introducing excess jitter and the outputs go to the PLL in the decoder. The receiver is transformer coupled and needs to be terminated with a 100Ω resistor or two 50Ω resistors and a capacitor as described in figure 2.

(c) Full Duplex Functions

The Full Duplex scheme allows the simultaneous transmission on the TPO± and simultaneous reception on the TPI± without interruption, effectively doubling the bandwidth to 20 MBPS in switched network implementations on 10Base-T. The 80C26 can be made to operate either in the AutoDUPLEX or in the Forced FullDuplex scheme according to Table 2.

Table 2. FDPLX Pin Description

FDPLX	MODE
1	Full Duplex Mode Enabled
float	AutoDUPLEX Enabled
0	Normal

The 80C26 is switched on to the AutoDUPLEX mode when FDPLX is left floating. In this configuration, Full duplex mode is automatically established by the successful detection of double pulses embedded within the regular link pulses. The 80C26 sends the double pulses in 16 pulse intervals constantly on the TPO± pins and continually monitors the TPI± pins for similar type of double pulses within a time window of 210 ± 6ms. Once the double pulses are detected, the FDPLX_DET will go low to acknowledge to the controller that the network will allow simultaneous transmission and reception on the TP port. The maximum distance between two consecutive pulses in a double pulse is 5.4 µs.

The Forced Full-Duplex mode can be established by setting FDPLX to high.

In this combination, forced full duplex is effectively established and Collision, SQE & the LoopBack functions are disabled.

(d) Squelch functions

The squelch function is used to discriminate noise from link test pulses and valid data to prevent the noise from activating the receiver. It is accomplished by a squelch comparator which compares the TPI± signals with a fixed positive and negative squelch value. The output from the comparator goes to a receive squelch circuit which determines whether the input data is valid or not. If the data is invalid, the transceiver enters into an squelched state. The input voltage should exceed ±300mV p-p for five bit times max. (with alternating polarity) for unsquelching to occur. In the Unsquelch state, the value of the threshold in the comparator is reduced to take care of hysteresis effects. While in the unsquelch state, the receive squelch circuit looks for the SOI (Start of Idle) signal at the end of the packet. When the SOI signal is detected, the receive squelch is turned on again.

(e) The Link integrity functions

The 80C26 monitors the TPI± pins continuously for valid data and link pulse activity. If neither data nor link test pulse is detected for a minimum time, the transceiver enters into a Link Test Fail State and disables the transmitter, receiver, collision presence and the SQE functions. For the transceiver to exit this state, it should receive three consecutive link pulses or valid data at the TPI± inputs to resume normal packet transmission and reception. Additionally the transmitter generates link pulses periodically when it's not transmitting data to indicate to the network that the link is intact. Please refer to figure 14 for the diagram illustrating the Transmit Link Pulse Voltage Tem-

plate as specified in the IEEE 802.3. The Link Pulse Detect Output and Link Pulse Disable Function are combined on one pin, LNK_LED/LNK_DIS according to Table 3.

Table 3. LNK_LED/LNK_DIS Pin Description

LNK_LED/LNK_DIS	I/O	Function
1	Output	Link Pulse Not Detected
0	Output	Link Pulse Detected
Tie to GND_2	Input	Link Test Function Disabled

(f) The Start of Idle (SOI) pulse

The transmit SOI pulse is a positive pulse inserted at the end of every transmission to signal the end and the start of idle period to corresponding receivers. The output pulse is also shaped by the transmit waveshaper to meet the pulse requirements specified in IEEE 802.3. Please refer to figure 13 for the Transmit Start Of Idle Pulse voltage template diagram. The receiver detects the SOI pulse by sensing the missing data transitions with the zero crossing comparator. Once the SOI pulse is detected, another SOI pulse is generated and sent to the Controller interface outputs.

(g) Automatic Polarity Correction

The 80C26 provides autopolarity detection and correction functions for the twisted pair receiver peak detectors to determine whether normal or inverted data is received over the TPI± pins. A polarity reversed condition is sensed and corrected when four opposite link pulses are detected without the expected polarity or if 3-4 frames are received with a reversed start-of-idle.

(h) Jabber functions

The jabber function detects abnormally long streams of Manchester-encoded data on the TXD input with the help of a Jabber detect circuit. The jabber circuit uses a Jabber timer, which monitors the TXEN pin. It starts counting at the beginning of each transmission. If the timer expires before TXEN goes inactive, the 80C26 enters a jabber state disabling the transmit/loopback functions and enabling the collision functions. If TXEN goes inactive before the timer expires, the timer is reset and becomes ready for the next transmission.

(i) Loopback functions

Loopback in the TP mode is internally enabled when Manchester encoded data is transmitted on TPO± and no data is received on the TPI± in order to simulate Coax Ethernet behavior. When internal loopback is enabled, the transmitted data is loopbacked into the RXD and sent to the controller. The loopback function is disabled during Link Fail State, Jabber State and during Full-Duplex Operation.

(l) Signal Quality Error Test

The Signal Quality Error test is used to indicate a successful transmission (i,e A transmission without interruptions such as Collision, jabber or Link failure) to the DTE. [1]

AUI Interface

The differential transmit output pair DO± sends the encoded data on to an external transceiver that is capable of driving 50 meters of 78 ohm shielded AUI cable directly with a jitter of 0.5 ns max. The receive input differential pair DI± goes through the AUI squelch comparator and the zero crossing comparator. The AUI squelch comparator compares the input signals with fixed minimum and maximum values of -175 mv and -325 mv respectively, and passes it on to the squelch circuit to determine data validity. The zero crossing comparator senses the transition point of the input pair without introducing excess jitter and passes the data to the phase locked loop of the decoder. The CI+/CI- are the collision input pair signals which expect a 5 Mhz or a 10 Mhz square wave from an external transceiver.

Collisions

Collisions are generated when two stations contend for the network at the same time, resulting in simultaneous activity detected on the TPO± and TPI±. When this happens, COLL will be asserted to indicating to the controller the simultaneous transmission of two or more stations on the network. CSN is also asserted during collision. For further details about timing, refer to figures 7 and 8.

Note:

1. Since SQE is internally enabled on the 80C26, on successful transmission, a collision signal is presented to the controller as an indication when the transmitter goes idle on the twisted pair network.

Oscillator

The internal clock generator is controlled either by an external parallel resonant crystal connected across X1 & GND_2 , or by connecting a clock to the input pin X1. This external 20 Mhz clock is used by the clock circuitry and the PLL to generate a 10 Mhz ± 0.01% transmit clock. The manchester encoding process uses both the 10Mhz and 20Mhz clocks.

Crystal Specification:

1. *Parallel resonant mode*
2. *Frequency ..... 20 MHz ±0.01% @ 0 – 70°C*
3. *Equivalent Series Resistance ..... 25 Ω max.*
4. *Load Capacitance ..... 20 pf max.*
5. *Case Capacitance ..... 7 pf max.*

Automatic Port Selection

The interface to the Manchester encoder can be selected to be either TP, AUI or Autoport. Port selection is done with the TP/$\overline{AUI}$ pin as described in Table 4.

Table 4. TP/$\overline{AUI}$ Pin Description

TP/AUI	Port
1	TP
float	Autoport
0	AUI

The Autoport mode automatically selects either the TP or AUI port by detecting the presence or absence of activity on the TPI± and DI± inputs. If autoport mode is selected, the device powers up with TP port active. If no packets or LINK pulses are detected on the TP port, the device switches to AUI port. The device will stay in AUI mode as long as no activity is detected on TP port.

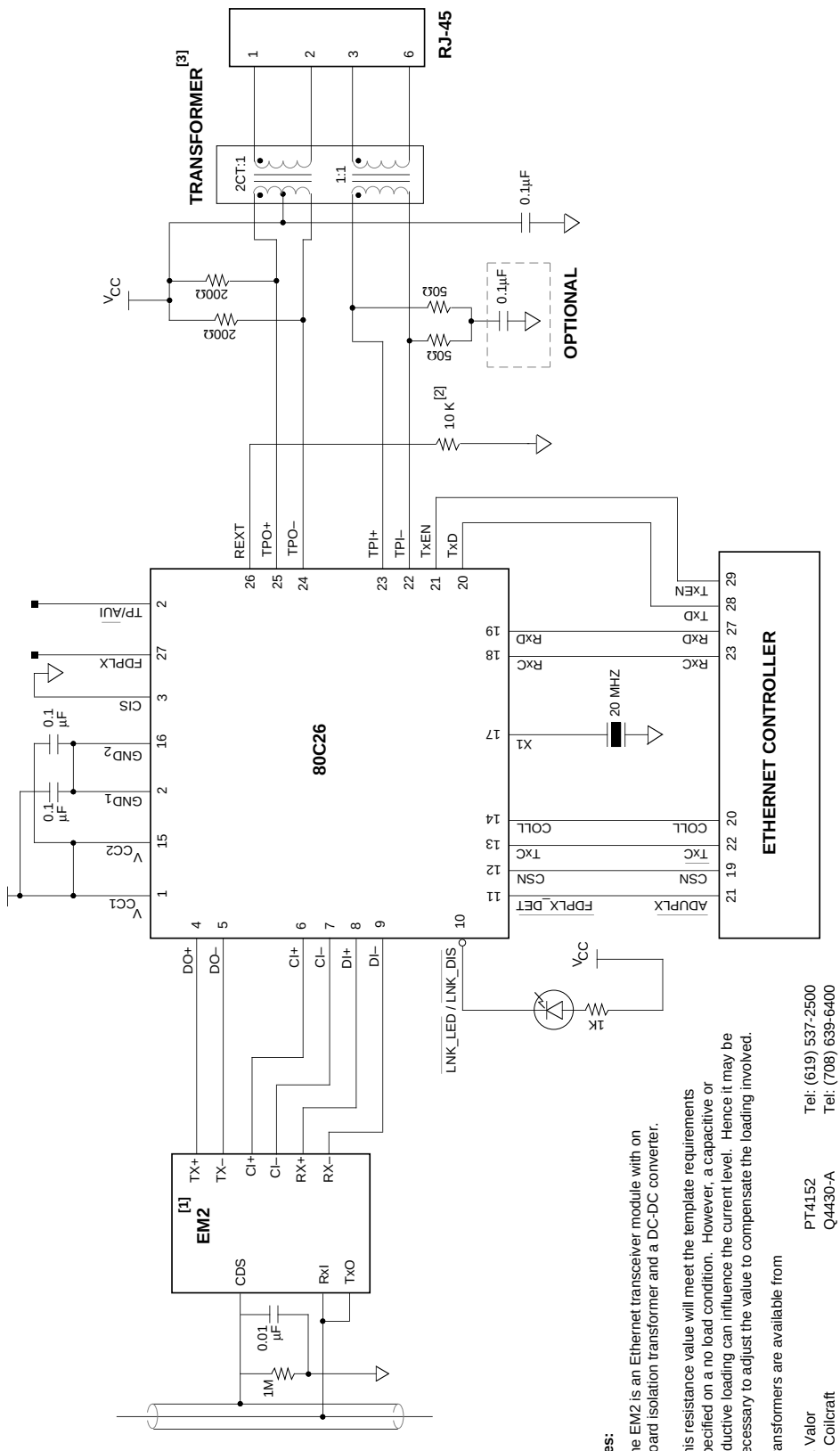
Power Supply Decoupling

There are two V_{CC}'s on the 80C26 (V_{CC1} and V_{CC2}) and two GND's (GND_1 and GND_2).

V_{CC1} and V_{CC2} should be connected together as close as possible to the device with a large V_{CC} plane.

GND_1 and GND_2 should also be connected together as close as possible to the device with a large ground plane.

A 0.1 µF decoupling capacitor should be connected between V_{CC1} and GND_1 as close as possible to the device pins, preferably within 0.5". The same should be repeated for V_{CC2} and GND_2.



Notes:

1. The EM2 is an Ethernet transceiver module with on board isolation transformer and a DC-DC converter.
2. This resistance value will meet the template requirements specified on a no load condition. However, a capacitive or inductive loading can influence the current level. Hence it may be necessary to adjust the value to compensate the loading involved.
3. Transformers are available from

a. Valor	PT4152	Tel: (619) 537-2500
b. Coilcraft	Q4430-A	Tel: (708) 639-6400
c. PCA	EPE6047S	Tel: (818) 892-0761
d. Bel Hybrids and Magnetics	A553-1084-01	Tel: (201) 432-0463
e. FEE Fil-mag	232435	Tel: (619) 569-6577
f. NANO Pulse	000-6115-00	Tel: (714) 529-2600

Figure 2. 80C26 in Typical TP/Coax Adapter Board Application

Absolute Maximum Ratings

V_{CC1}, V_{CC2} Supply Voltage ..... –0.3V to 7V
All Inputs and Outputs ..... –0.3 to V_{CC} + 0.3 V
Latchup Current ..... ±25 mA
Package Power Dissipation ..... 1 Watt @ 25°C
Storage Temperature ..... –65 to +150°C
Operating Temperature ..... –65 to +125°C
Lead Temperature (Soldering, 10 sec) ..... 250°C

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Power Supply Characteristics

Test conditions are as follows:

1. T = 0–70°C
2. V_{CC} = 5V ±5%
3. 20 MHZ ±.01%
4. REXT = 10K, with no load.

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
I_{CC}	V_{CC} Power Supply Current		110	150	mA	Transmitting, TP selected
			85	110	mA	Transmitting, AUI selected

DC Digital I/O Characteristics

Test conditions are as follows:

1. T = 0–70°C
2. V_{CC} = 5V ±5%
3. 20 MHZ ±.01%
4. REXT = 10K, with no load.

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
V_{IL}	Input Low Voltage			0.8	Volt	All except X1, TP/$\overline{AUI}$, FDPLX
				0.8	Volt	TP/$\overline{AUI}$, FDPLX
				1.5	Volt	X1
V_{IM}	Input Intermediate Voltage	V_{CC}/2 –0.5 V		V_{CC}/2 +0.5 V	Volt	TP/$\overline{AUI}$, FDPLX
V_{IH}	Input High Voltage	2			Volt	All except X1, TP/$\overline{AUI}$, FDPLX
		V_{CC}–0.8			Volt	TP/$\overline{AUI}$, FDPLX
		3.5			Volt	X1
I_{IH}	Input High Current	15	60	120	µA	V_{IN}= V_{CC} All Except $\overline{LNK\_LED}$/$\overline{LNK\_DIS}$
I_{IL}	Input Low Current	–15	–60	–120	µA	V_{IN}= GND All Except CIS[1]
V_{OL}	Output Low Voltage			0.4	Volt	I_{OL}= 2.1 mA $\overline{FDPLX\_DET}$, $\overline{LNK\_LED}$/$\overline{LNK\_DIS}$
				1.2	Volt	I_{OL}= –20 mA $\overline{LNK\_LED}$/$\overline{LNK\_DIS}$

DC Digital I/O Characteristics cont'd

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
V_{OH}	Output High Voltage			4	Volt	I_{OH}= –1 mA $\overline{\text{FDPLX\_DET}}$
C_{IN}	Input Capacitance		5		pF	
C_{OUT}	Output Capacitance		5		pF	

Notes
1. Not measured, due to internal pull-down to GND.

Twisted Pair Interface Characteristics

Unless otherwise specified, all test conditions are as follows:

1. T = 0–70°C
2. V_{CC} = 5V ±5%
3. 20MHZ ±.01%
4. REXT = 10K, with no load.
5. 50 ohm load from TPO± to V_{CC}
6. 10Mhz sine wave on TPI±

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
TOV	TPO± Differential Output Voltage	2.2	2.5	2.8	Vpk	
TOVT	TPO± Differential Output Voltage Template	See Figure 12				
TSOI	TPO± SOI Output Voltage Template	See Figure 13				
TLPT	TPO± Link Pulse Output Voltage Template	See Figure 14				
TOIV	TPO± Differential Output Idle Voltage			±50	mV	Measured on Secondary Side of XFMR on Figure 2.
TOIA	TPO± Output Current	44	50	56	mA pk	
TOIR	TPO± Output Current Adjustment Range	30	50	80	mA pk	V_{CC} = 5V Adjustable with REXT
TCMA	TPO± Common Mode AC Output Voltage		10	50	mV pk	
THD	TPO± Harmonic Distortion			–27	dB	
TOR	TPO± Output Resistance		10K		ohms	
TOC	TPO± Output Capacitance		15		pF	
RST	TPI± Squelch Threshold	310		540	mVpk	
RUT	TPI± Unsquelch Threshold	190		330	mVpk	
RZT	TPI± Zero Cross Switching Threshold			20	mVpk	
ROCV	TPI± Input Open Circuit Voltage	(V_{CC}/3)–0.25	V_{CC}/3	(V_{CC}/3)+0.25	Volt	
RCMR	TPI± Input Common Mode Voltage Range	V_{CC}/3–1.0		V_{CC}/3+1.0	Volt	

Twisted Pair Interface Characteristics cont'd

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
RDR	TPI+/– Input Differential Voltage Range			V_{cc}	Volt	
RCRR	TPI+/– Input Common Mode Rejection Ratio			–20	dB	0–10Mhz
RIR	TPI+/– Input Resistance	5K			ohm	
RIC	TPI+/– Input Capacitance		10		pF	

AUI Characteristics

Unless otherwise specified, all test conditions are as follows:

1. T = 0–70°C
2. V_{CC} = 5V ±5%
3. 20 MHZ ±.01%
4. REXT = 10K with no load.
5. 78 ohm, 27µH load on DO±
6. 10 Mhz sine wave on DI±, CI±

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
AOV	DO±, Differential Output Voltage	550		1200	mVpk	
AORF	DO±, Output Rise And Fall Time			5	ns	t_R, t_F measured at 10-90% points
AOIV	DO±, Differential Output Idle Voltage			±40	mV	
AOVU	DO±, Differential Output Voltage Undershoot During Idle			–100	mV	
AOCD	DO±, Common Mode DC Output Voltage	V_{CC}/3.5	V_{CC}/3.0	V_{CC}/2.1	Volt	
AOCA	DO±, Common Mode AC Output Voltage			40	mV pk	
AOR	DO±, Output Resistance			75	ohms	
AOC	DO±, Output Capacitance		15		pF	
AIST	DI±, CI± Squelch Threshold	-175		-325	mV	
AIUT	DI±, CI± Unsquelch Threshold	-100		-225	mV	
AIZT	DI±, CI± Zero Cross Switching Threshold			20	mVpk	
AIOC	DI±, CI± Input Open Circuit Voltage	(V_{CC}/2)–.25	V_{CC}/2	(V_{CC}/2)+.25	Volt	
AICR	DI±, CI± Input Common Mode Voltage Range	(V_{CC}/2)–1.0		(V_{CC}/2)+1.0	Volt	
AIVR	DI±, CI± Input Differential Voltage Range	0		V_{CC}	Volt	
AIR	DI±, CI± Input Resistance	5K	10K		ohm	
AIC	DI±, CI± Input Capacitance		10		pF	

AC Test Timing Conditions

Unless otherwise specified, all test conditions for timing characteristics are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5v ±5%
3. 20MHZ ±.01%
4. REXT = 10K, with no load.
5. Input Conditions
   - All Inputs: t_R, t_F< = 10ns from 20-80% points
6. Output Loading
   - TPO±: 50 ohms to V_{CC} on each output, 10pF
   - DO±: 78 ohms differentially, 10pF
   - Open Drain Digital Outputs: 1K pullup, 50pF
   - All Other Digital Outputs: 50pF
7. Measurement Points
   - TPO±, TPI±, DO±, DI±, CI±: Zero crossing during data and ±.3V point at start/end of signal
   - X1: V_{CC}/2
   - All other inputs and outputs: 1.5 Volts

20 MHZ Input Clock Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_1	X1 Cycle Time	49.995	50.000	50.005	ns	

Refer to Figure 3 for timing diagram.

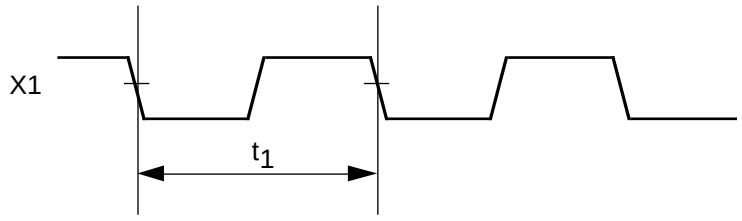
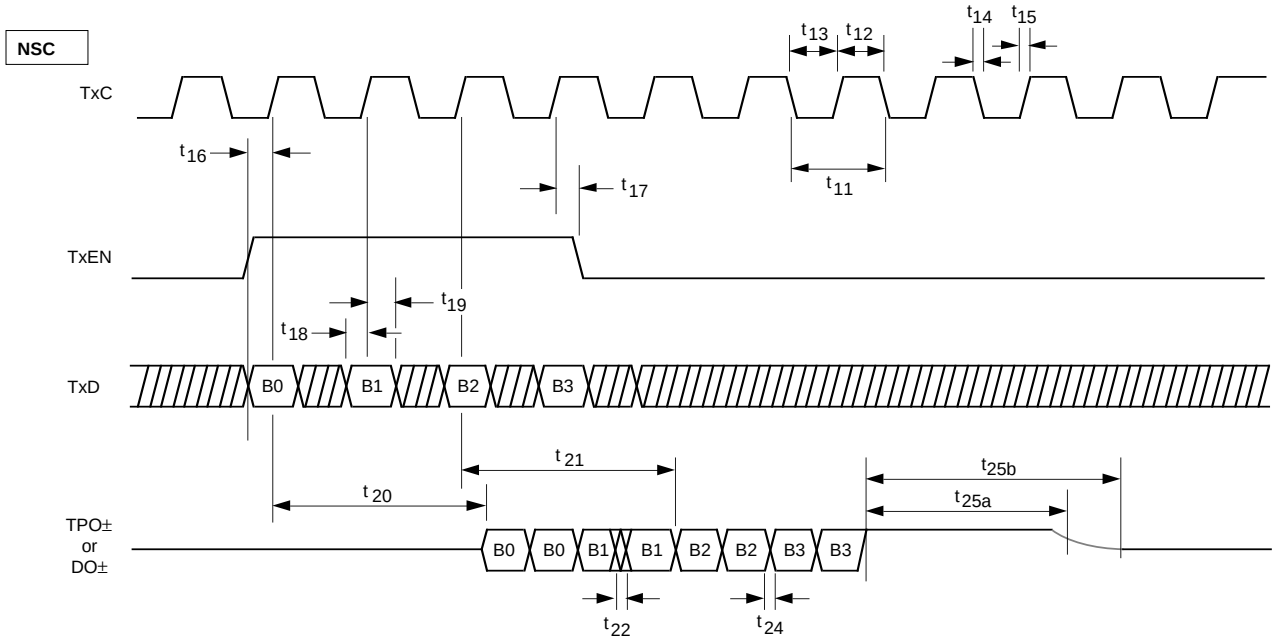


Figure 3. 20 MHZ Input Clock Timing

Transmit Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{11}	TXC Cycle Time	99.99	100	100.01	ns	
t_{12}	TXC High Time	40		60	ns	
t_{13}	TXC Low Time	40		60	ns	
t_{14}	TXC Rise Time			5	ns	
t_{15}	TXC Fall Time			5	ns	
t_{16}	TXEN Setup Time	30			ns	
t_{17}	TXEN Hold Time	0			ns	
t_{18}	TXD Setup Time	30			ns	
t_{19}	TXD Hold Time	0			ns	
t_{20}	Transmit Bit Loss			2	Bits	TP and AUI
t_{21}	Transmit Propagation Delay			2	Bits	TP and AUI
t_{22}	Transmit Output Jitter			8	ns	TP
				0.5	ns	AUI
t_{24}	Transmit Output Rise And Fall Time	See Figure 12			ns	TP
				5	ns	AUI
t_{25A}	Transmit SOI Pulse Width to 0.3V Point	250			ns	TP Measure TPO± from last zero cross to 0.3V point.
		200			ns	AUI Measure DO± from last zero cross to 0.3V point.
t_{25B}	Transmit SOI Pulse Width to 40 mV Point			4500	ns	TP Measure TPO± from last zero cross to 40mV point.
				7000	ns	AUI Measure DO± from last zero cross to 40 mV point.

Refer to Figure 4 for timing diagram.



AMD SAME AS NSC

Figure 4. Transmit Timing

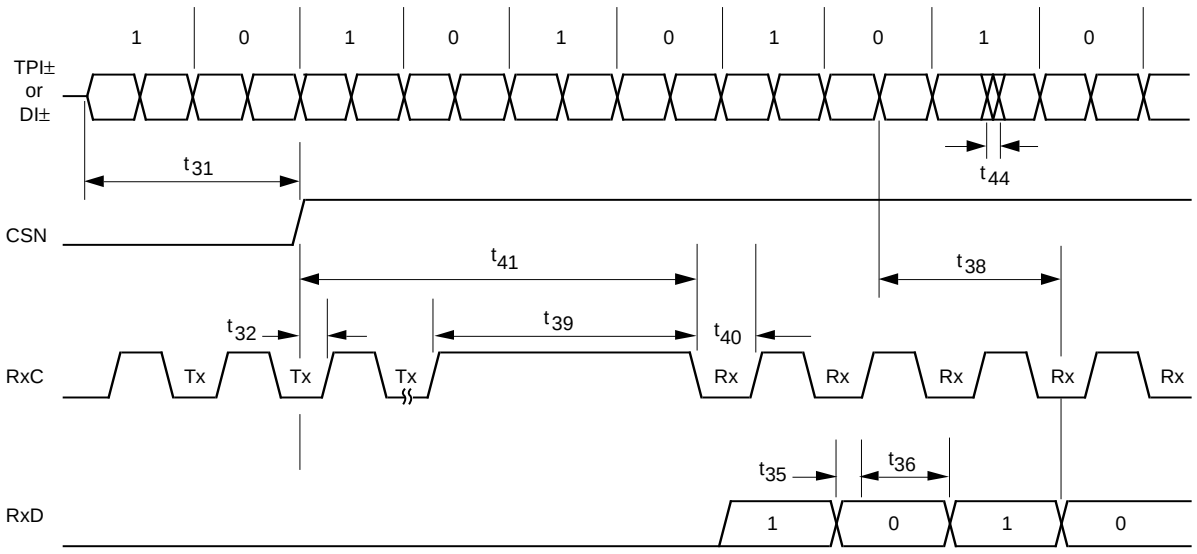
Receive Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{31}	CSN Assert Delay Time			600	ns	TP
				240	ns	AUI
t_{32}	CSN Assert Setup Time	30			ns	
t_{33}	CSN Deassert Hold Time	20		40	ns	
t_{35}	RXC to RXD Setup Time	40			ns	
t_{36}	RXC to RXD Hold Time	30			ns	
t_{38}	RXD Propagation Delay			200	ns	
t_{39}	RXC High Time	40		200	ns	
t_{40}	RXC Low Time	40		60	ns	
t_{41}	CSN Assert To RXC Switchover From TX Clock To RX Clock			1500	ns	TP
				1500	ns	AUI
t_{42}	CSN Deassert To RXC Switchover From Rx Clock To Tx Clock			200	ns	
t_{43}	SOI Pulse Width Required For Idle Detection	125		200	ns	TP Measure TPI± from last zero cross to .3v point.
		125		160	ns	AUI Measure RX± from last zero cross to .45v point.
t_{44}	Receive Input Jitter			±13.5	ns	Data
				±8.5	ns	Preamble
t_{49}	RXC, RXD, CSN Output Rise And Fall Times			10	ns	

Refer to Figures 5 and 6 for timing diagram.

NOTES:
1. CI+ and CI– asserts and deasserts COLL, asynchronously, and asserts and deasserts CSN synchronously with RxC.
2. If CI+ and CI– arrives within 4.5 µs from the time CSN was deasserted; CSN will not be reasserted (on transmission node only).
3. When CI+ and CI– terminates, CSN will not be deasserted if DI± are still active.
4. When the node finishes transmitting and CSN is deasserted, it cannot be asserted again for 4.5 µs.

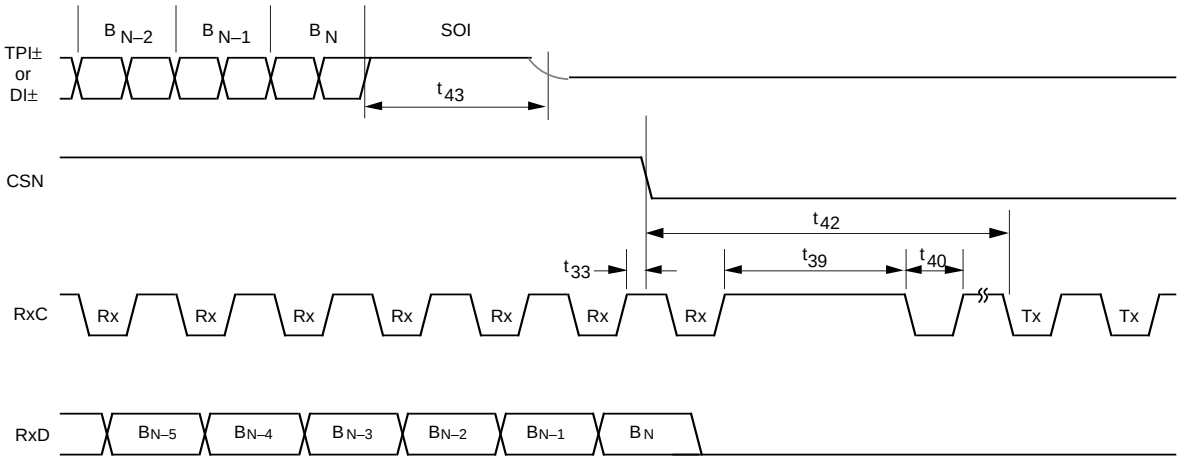
NSC



AMD SAME AS NSC EXCEPT RxC IS SHUTOFF DURING IDLE.

Figure 5. Receive Timing — Start of Packet

NSC



AMD SAME AS NSC EXCEPT RxC IS SHUTOFF DURING IDLE.

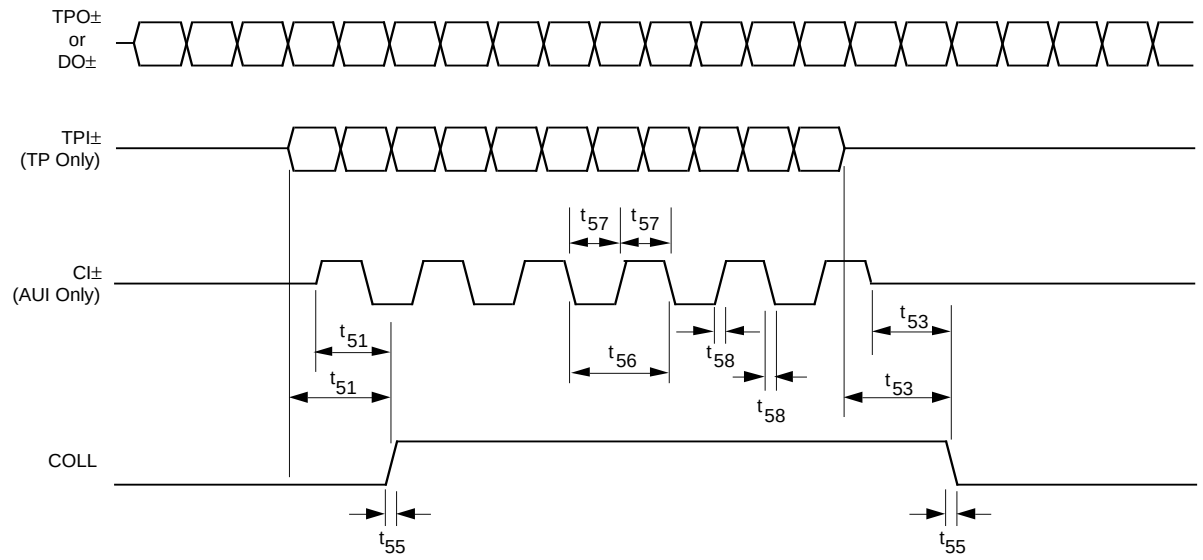
Figure 6. Receive Timing — End of Packet

Collision Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{51}	COLL Assert Delay Time - Rcv After Xmt			600	ns	TP TPI± to COLL
				300	ns	AUI CI± to COLL
t_{52}	COLL Assert Delay Time - Xmt After Rcv			600	ns	TP TPO± to COLL
				300	ns	AUI CI± to COLL
t_{53}	COLL Deassert Delay Time - Rcv After Xmt			500	ns	TP TPI± to COLL
				500	ns	AUI CI± to COLL
t_{54}	COLL Deassert Delay Time - Xmt After Rcv			500	ns	TP TPO± to COLL
				500	ns	AUI CI± to COLL
t_{55}	COLL Rise And Fall Time			10	ns	
t_{56}	CI± Cycle Time	80		117	ns	
t_{57}	CI± Low Or High Time	35		70	ns	
t_{58}	CI± Rise And Fall Time			10	ns	

Refer to Figures 7 and 8 for timing diagram.

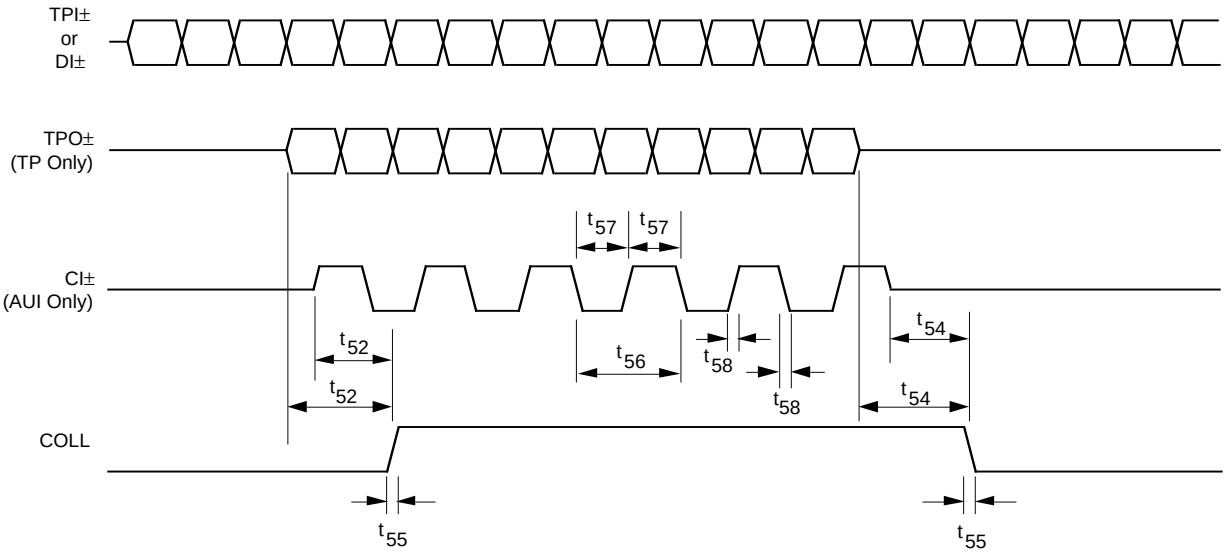
NSC



AMD SAME AS NSC

Figure 7. Collision Timing — Receive After Transmit

NSC



AMD SAME AS NSC

Figure 8. Collision Timing — Transmit After Receive

Link Pulse Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{61}	Transmit Link Pulse Width	75		125	ns	
t_{62}	Transmit Link Pulse Period	11		15	ms	
t_{63}	Transmit Link Pulse To Double Link Pulse Spacing	5.0	5.2	5.4	µs	Full Duplex Mode Signalling
t_{64}	Transmit Double Link Pulse Interval Spacing	16		16	Link Pulses	Full Duplex Mode Signalling
t_{65}	Receive Link Pulse Width Required For Detection	35		200	ns	
t_{66}	Receive Link Pulse Minimum Period Required For Detection	2	4	7	ms	Link_Test_Min
t_{67}	Receive Link Pulse Maximum Period Required For Detection	50		150	ms	Link_Loss and Link_Test_Max
t_{68}	Receive Link Pulse To Double Link Pulse Spacing Required For Full Duplex Mode Detection	4.8		5.6	µs	Full Duplex Mode Detection
t_{69}	Receive Double Link Pulse Minimum Period Required For Full Duplex Mode Detection	204	210	216	ms	Full Duplex Mode Detection
t_{70}	Receive Double Link Pulse Maximum Period Required for Full Duplex Detection	750		850	ms	Full Duplex Detection Mode
t_{71}	Receive Link Pulse Assert	2	3	10	Link Pulses	
t_{72}	Receive Full Duplex Assert			7	µs	Full Duplex Mode Detection

Refer to Figure 9 for timing diagram.

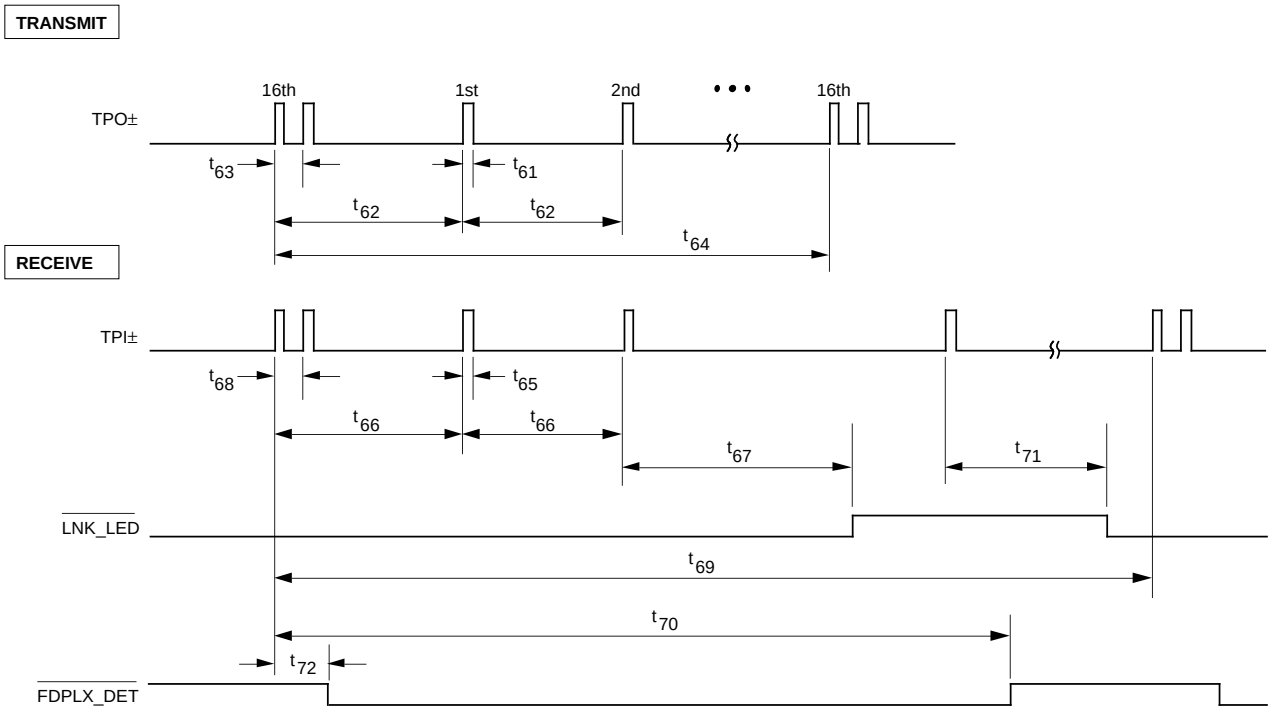


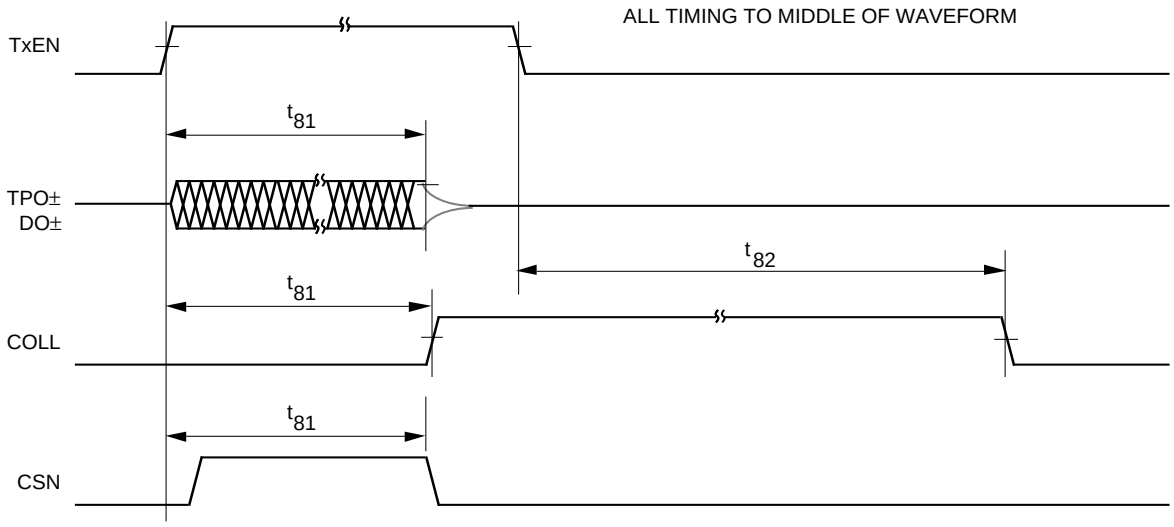
Figure 9. Link Pulse Timing

Jabber Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{81}	Jabber Activation Time	40		60	ms	TP and AUI
t_{82}	Jabber Deactivation Time	400		430	ms	TP and AUI

Refer to Figure 10 for timing diagram

NSC



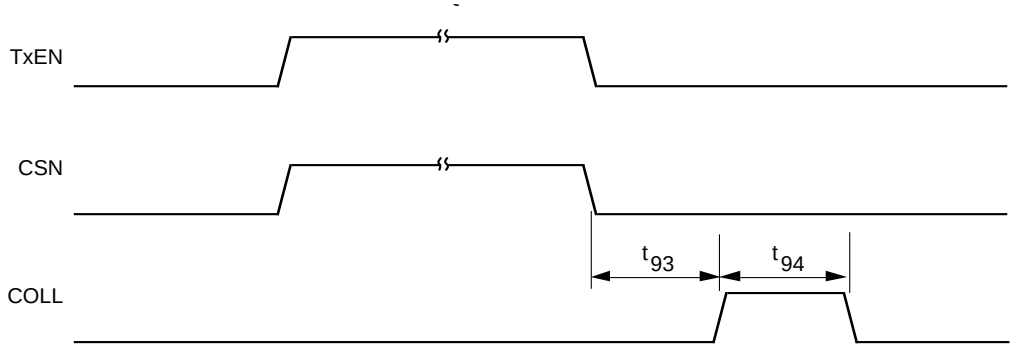
AMD SAME AS NSC

Figure 10. Jabber Timing

SQE Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{93}	SQE Pulse Delay	600		700	ns	
t_{94}	SQE Pulse Width	750		850	ns	

Refer to Figure 11 for timing diagram.



AMD SAME AS NSC

Figure 11. SQE Test Timing

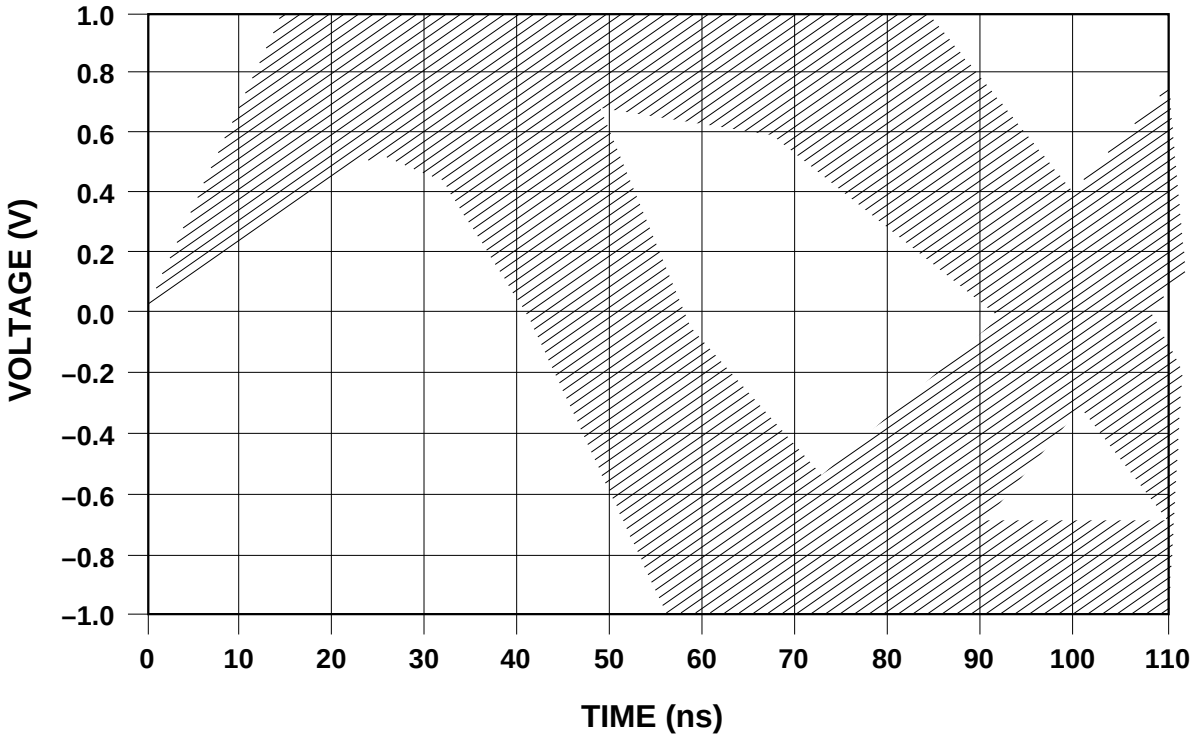
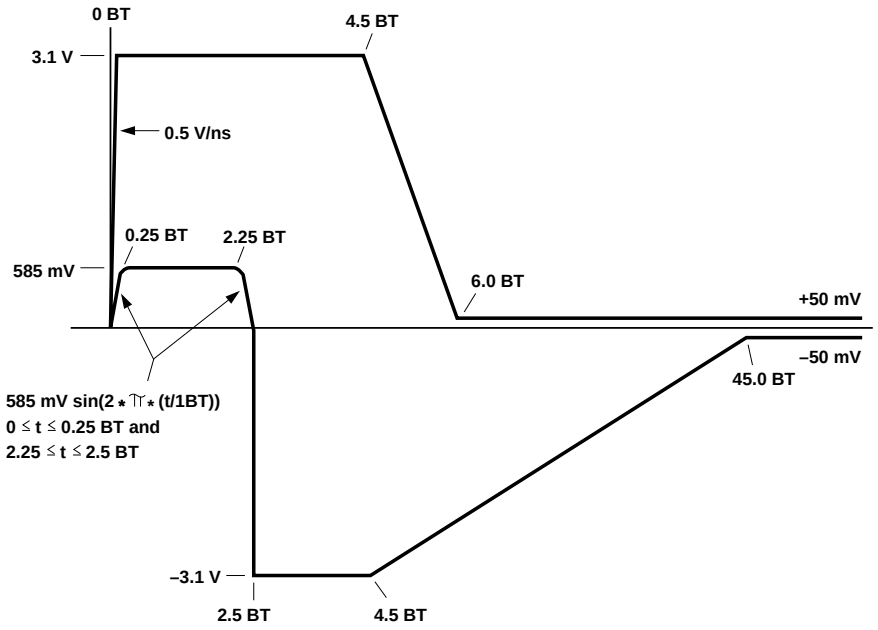
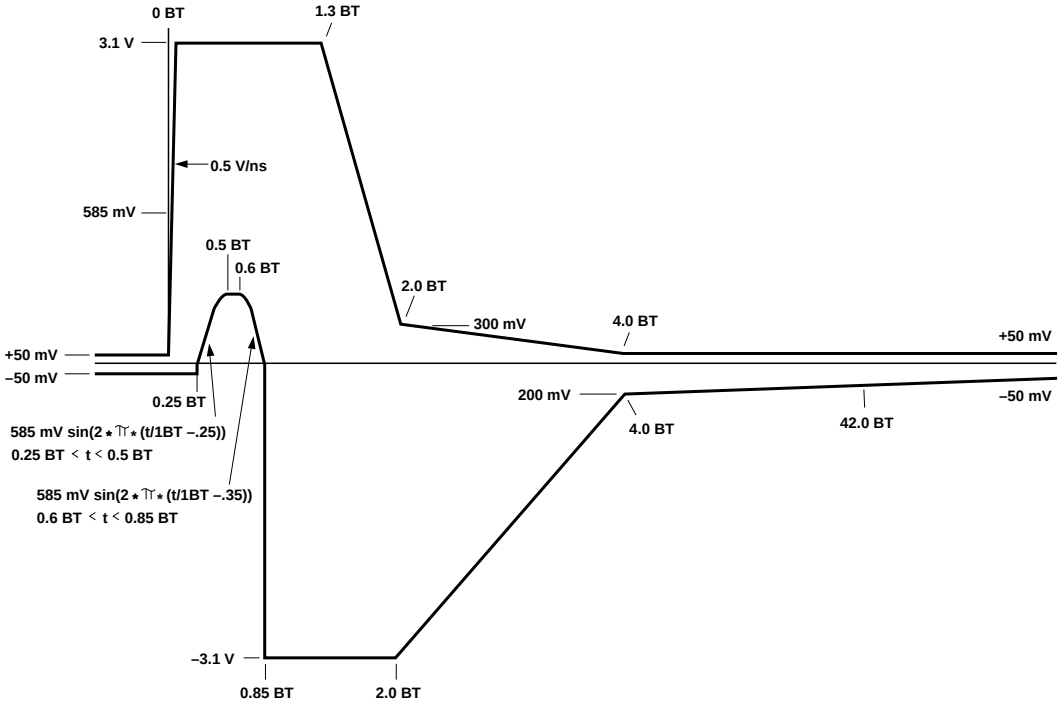


Figure 12. Twisted Pair Output Voltage Template with Line Model.



With and Without Line Model

Figure 13. Transmit Start of Idle Pulse Voltage Template

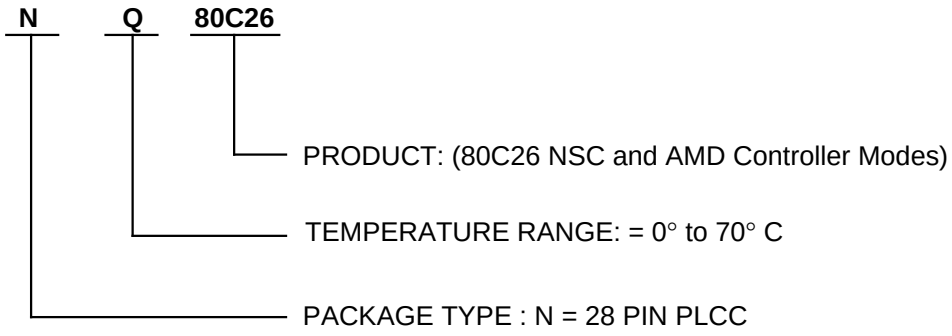


With and Without Line Model

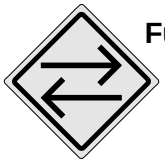
Figure 14. Transmit Link Pulse Voltage Template

Ordering Information

PART NUMBER



SEEQ Full Dulex Designation



Full Duplex

Symbol indentifies product as Full Duplex device.

Revision History

5/8/96

- All references to separate ‘digital’ and ‘analog’ power and grounds deleted.
- Page 3, Pin Descriptions: Pin 17 (X1) description clarified.
- Page 8, Added Power Supply Decoupling Suggestions.
- Page 10, Digital I/O Characteristics:
  - Added V_{IH} abd V_{IL} specifications for TP/$\overline{\text{AUI}}$ and FDPLX.
  - Added V_{IM} (Input Intermediate Voltage) specifications.
  - V_{OL} (max) changed to 1.2 V.
  - I_{IL} for CIS pin spec clarified (see note at table bottom).
  - I_{IH} (min) changed from 30 µA to 15 µA.
  - I_{IL} (min) changed from –30 µA to –15 µA.
- Page 14, AUI Characteristics:
  - AOCD (max) changed from V_{CC}/2.5 to V_{CC}/2.1.

9/9/96

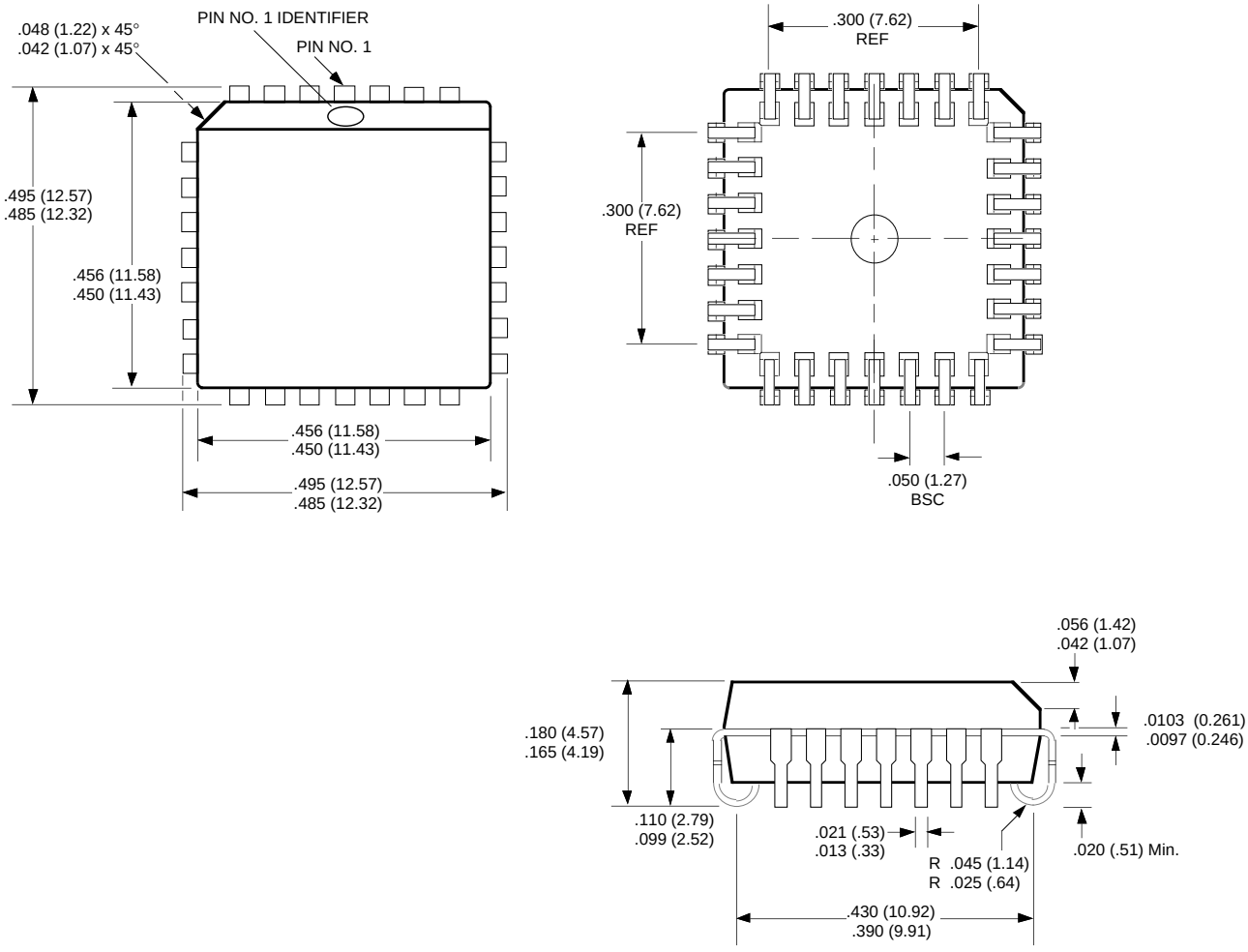
- Page 29, Dimension diagram has been added to this data sheet.

12/11/96

- Page 16, Transmit Timing Characteristics, TXEN Hold Time (min.) has been changed from 40 to 0.

Surface Mount Packages

28-Pin Plastic Leaded Chip Carrier Type N



Notes
1. All dimensions are in inches and (millimeters).
2. Dimensions do not include mold flash. Maximum allowable flash is .008 (.20).
3. Formed leads shall be planar with respect to one another within 0.004 inches.