

# LSI402Z Digital Signal Processor

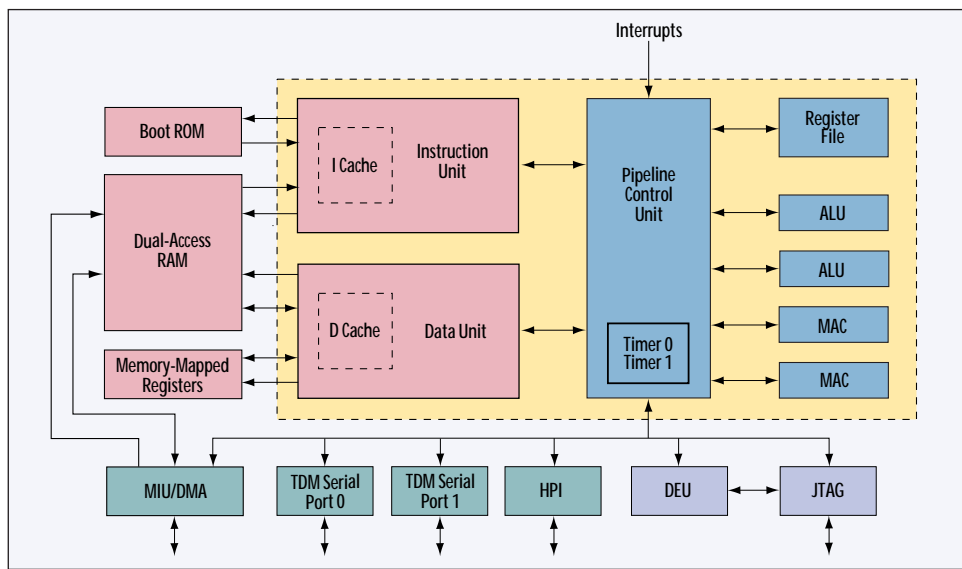
## ZSP Architecture Performance with High-End Integration

### Overview

The LSI402Z is a high-performance 16-bit fixed-point digital signal processor (DSP) based on the ZSP™ Architecture. This device has been designed for applications that require high data throughput capability coupled with high-speed I/O, such as communications infrastructure equipment, and offers enhanced I/O capabilities and large on-chip memory. The LSI402Z is capable of a maximum clock rate of 200 MHz for 800 MIPS peak performance and sustained effective throughput of 400 DSP MIPS (MACs).

### Memory

The internal memory structure of the LSI402Z comprises 62K words of dual-access RAM, 2K words of boot ROM and 2K words of data space dedicated to memory-mapped registers and external peripherals. Dual-access RAM can be freely used as both instruction and data memory. The boot ROM contains several routines, including internal self-test, and boot-loader routines. The Memory Interface Unit (MIU) provides a glueless interface to industry-standard 32-bit synchronous-burst SRAMs (SBSRAMs), and 16-bit asynchronous SRAMs and ROM devices. The total address range of the MIU is 20 bits, organized as sixteen 64K word pages which are selected by a software-controlled page register.



Functional Block Diagram

### Features

- 200 MHz operation at 1.8 V (5 ns cycle time)
- Two high-speed serial/TDM ports (T1/E1 framer, H.100/H.110 bit stream compatible)
- Low power dissipation (< 1 W at 200 MHz)
- 62K words RAM, 2K words ROM on-chip
- Eight-channel DMA support
- On-board PLL for clock generation
- 32-/16-bit external memory interface
- Two on-board timers
- 16-bit host processor interface
- IEEE 1149.1-compliant JTAG port for real-time emulation and system download
- 208 mBGA package

### Benefits

- 400 MMAC sustained DSP performance
- Direct interfacing to standard telecommunication interfaces, reducing system cost
- Very low power per channel
- Low or zero system memory cost
- High data throughput without processor overhead
- Flexibility to optimize power consumption
- High data bandwidth to off-chip devices
- RTOS support and increased system integration
- Simple interfacing to industry-standard micros
- Low overhead on chip debug
- Very high processing density per unit area

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## DMA

The DMA controller of the LSI402Z can support up to eight individual channels simultaneously, where all channels can access the entire 62K word dual-access RAM. Either instructions or data can be transferred to or from the internal memory space from the MIU, HPI, or either serial port. The eight DMA channels are segmented into four "indexed" and four "non-indexed" channels. Indexed channels have the ability to buffer data from either of the serial TDM interfaces. Non-indexed channels perform sequential accesses to or from internal memory.

## Timers

The LSI402Z has two identical 16-bit on-board timers for real-time interrupt generation. Each timer is fully programmable, and has a 6-bit pre-scaler and interrupt capability. The timers can automatically reload with the initial count so that periodic interrupts can be generated.

## TDM Serial Ports

The LSI402Z provides two identical synchronous serial ports that support 8- or 16-bit active or passive transfers, which can be either burst or continuous, with a maximum active mode transfer rate of 100 Mbps (with a 200 MHz processor clock). In passive mode, the maximum transfer rate is 200 Mbps. Both serial ports provide the programmable feature of a TDM (time division multiplex) mode that is compatible with T1/E1 framers or the local serial bus of H.100/ H.110 interface devices. The TDM mode can also be used to establish a serial multiprocessor communication link with only three signals.

## Host Processor Interface (HPI)

The Host Processor Interface, or HPI, is an asynchronous 16-bit parallel port that is compatible with both Motorola and Intel style interfaces, and supports word (16-bit) transfers. The maximum transfer rate for the HPI is half of the processor clock frequency (100M words per second given a processor operating frequency of 200 MHz).

## Development Tools

The ZSP Processor family is fully supported by a GNU-based compiler, linker and assembler, available for Windows 95/98/NT and Solaris 2 platforms. The ZSP Architecture enables the C compiler to produce code unrivaled in code density and execution speed by any DSP in its class, offering fast time to market with optimal performance and cost. An integrated debug environment is available for PC platforms.

An LSI402Z development platform is available, offering the following features:

- FLASH EPROM
- RS232C and JTAG-based host communication and code download
- 512K words SBSRAM expansion program/data memory
- 64K words asynchronous program/data memory
- Analog I/O interfaces

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