EZ4021 MiniRISC® EasyMACRO™

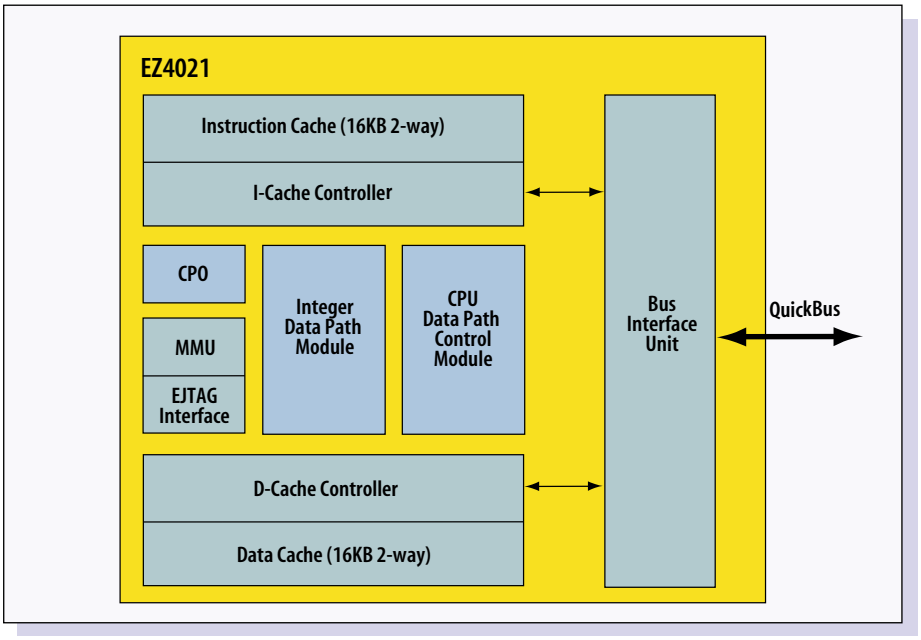
Integrated MiniRISC® MIPS Microprocessor Core

Overview

The EZ4021 extends the LSI Logic MIPS MiniRISC® family with a high performance 64-bit microprocessor. The EZ4021 EasyMACRO™ is an optimized implementation of a synthesizeable core that operates up to 250MHz under worst case conditions. With its 275 Dhrystone MIPS 2.1 performance, compact area, and low power consumption rating, the EZ4021 is well prepared to meet the embedded system designer's growing demand for high performance 64-bit applications.

The EZ4021 EasyMACRO physical implementation facilitates the re-use of the core in customers' designs. System designers do not require detailed knowledge of the core for use in a system-on-a-chip design. Optimized for frequency and size, the core is a highly integrated solution that is comprised of the MiniRISC EZ4021 64-bit CPU and CPU sub-system. Specifically designed using industry-standard, third party EDA tools (including simulation, synthesis, static timing analysis and ATPG), the EZ4021 further enhances LSI Logic's MIPS-based embedded processor line. The EZ4021 EasyMACRO is designed for rapid system on a chip ASIC integration through LSI Logic's CoreWare® design methodology.

With an operating frequency of 250MHz, the 64-bit EZ4021 microprocessor is ideally suited for performance driven applications such as set-top boxes, advanced networking systems, high-end printers and office systems.



EZ4021 Block Diagram

Features

- MIPS-III ISA Standard
- 250 MHz (under worst case conditions)
- 275 Dhrystone MIPS 2.1 Performance
- Harvard Cache Architecture
- Integrated 2 way set associative 16K Instruction Cache and 16K write-back or write-through Data Cache
- Bus Snooping enabling cache coherency in a multi-processing environment
- Compact EasyMACRO size: 12 square mm
  - includes 16K Instruction and 16K Data Caches
- Low power consumption: 2.6mW/MHz
- Integrated non-intrusive EJTAG Debug with enhanced break functions & PC Trace
- Low-operating voltage: 1.8V
- Future Options:
  - Integrated FPU
  - Code Compression
  - Configurable Cache
  - AMBA Interface
- EasyMacro: optimized for frequency and area
- Designed for Rapid SoC integration
- Support by Industry Standard Toolchains

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EZ4021 MiniRISC EasyMACRO

EZ4021 Description

The EZ4021 EasyMACRO is an optimized implementation of a synthesizeable core that operates up to 250MHz, under worst case conditions. The EZ4021 core integrates a complete CPU and CPU subsystem. The CPU implements the MIPS III instruction set architecture (ISA). The CPU subsystem is comprised of a memory management unit, multiply-divide unit, system-coprocessor, bus interface unit, separate 16K instruction and 16K data caches, non- intrusive EJTAG debug module. Both CPU and CPU subsystem are integrated into the compact 12-sq. mm EZ4021 core.

Performance features of the EasyMACRO include MAC instruction extensions, hardware instruction prefetch and streaming and a high-performance bus interface. The memory management unit, designed for Windows® CE compliance, includes dual 32 entry TLBs, supporting variable page sizes ranging from 4K-16M. The Bus Interface Unit controls the on-chip system bus. Operating up to 125MHz, the split transaction bus (32-bit address, 64 bit data), provides a glueless interface to optional external building blocks. These CoreWare library blocks, external to the EasyMACRO, include SDRAM controller, off-chip bus controller, and UART.

Support Products

The EZ4021 MiniRISC MIPS core supports MIPS-III instructions and leverages the widely available industry standard, low cost, third party tools developed in support of the MIPS architecture. In addition, the EZ4021 leverages both mature debug capability and third party tool chains that are supported by LSI Logic.

A complete evaluation and development kit is available for the EZ4021 EasyMACRO MIPS processor. The kit includes an EZ4021 development board, an EJTAG probe, third party tool chain, software examples and documentation.

CoreWare Design Program

The EZ4021 MiniRISC is a member of the LSI Logic CoreWare IP library. This CoreWare methodology provides an extensive selection of proven IP enabling rapid system-on-a-chip design integration. The EZ4021 deliverables include a Verilog compatible RTL model, a system verification environment (SVE), complete netlist, timing and example script files with layout to accelerate ASIC SoC development.

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