USER'S GUIDE

CODEC-5.1 Daughtercard

February 2003

Engineering Draft

LSI LOGIC®

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This document describes the version of LSI Logic Corporation's Codec 5.1 Daughter Card and will remain the official reference source for this product until rescinded by an update.

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Preface

This book is the primary reference for the CODEC-5.1 daughtercard. It contains detailed descriptions of the Card's features, design and how to use it with the EB402 and EB403 evaluation boards.

Audience

This document assumes that you have some familiarity with micro and/or digital signal processors and digital and analog audio electronics. The people who benefit from this book are:

- Engineers who are using the CODEC-5.1 card in conjunction with the EB402 and EB403 ZSP™ processor evaluation boards.

Organization

This document has the following chapters and appendixes:

- Chapter 1, "Introduction" provides an overview of the CODEC-5.1 card and its features.
- Chapter 2, "Installation," describes how to install the CODEC-5.1 card on an EB402 or EB403.
- Chapter 3, "Operation," describes the interfaces between the CODEC-5.1 card and the EB402/EB403 boards, and describes the operation of the CODEC-5.1 circuitry.

Related Publications

The following documents are available from LSI Logic Corporation.

- LSI402ZX User's Guide

- LSI403LP User's Guide
- LSI EB402 User's Guide
- LSI EB403 User's Guide
- EB402 Board Support Package Technical Manual
- EB403 Board Support Package Technical Manual

This document is intended to provide information to help the reader install and use the CODEC-5.1 board to AKM Corporation AK4586 DataSheet http://www.akm.com/datasheets/ek4586.pdf

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end in an "n."

Hexadecimal numbers are indicated by the prefix "0x" —for example, 0x32CF. Binary numbers are indicated by the prefix "0b" —for example, 0b0011.0010.1100.1111.

Contents

Chapter 1
Introduction

This section introduces the features of the CODEC-5.1 card and describes the purpose for which it has been designed. It contains the following sections:

1.1 Introduction

This document is the primary reference and user’s guide for the Multi-Channel Audio Codec (CODEC-5.1) daughtercard. This daughtercard interfaces with the LSI Logic ZSP400-based standard product evaluation boards, EB402 and EB403.

The daughtercard allows applications development for a 6-channel output codec for multi-channel audio applications. The codec used on board is an AKM AK4586, featuring 2x24-bit input channels, 6x24-bit output channels, with sampling rates up to 96KHz.

The daughtercard provides 6 line-level outputs. These outputs are available on both RCA-style connectors and 3.5mm phonojacks for ease of connecting to an external amplifier or powered speakers.

The daughtercard has 2 line-level analog inputs which support both RCA-style and a 35mm phonojack. In addition to these inputs, a separate 3.5mm phonojack input is connected to a circuit to support a Electret microphone input. A potentiometer is mounted on the board to adjust the gain of the microphone input circuit.

The analog section of the daughtercard can be powered from an external source for improved noise performance. For ease of use, the power

supplies can also be derived from the EB402/EB403 thus eliminating the need for separate power supplies.

The CODEC-5.1 daughtercard plugs into both of the SPORT connectors on the EB402 or EB403 evaluation board. All connections are made through the use of these 2 connectors.

This manual describes all the steps necessary to interface the CODEC-5.1 daughtercard to the LSI Logic ZSP processor evaluation boards (either EB402 or EB403).

1.2 Product Features

The CODEC-5.1 daughtercard provides the following features:

- AKM AK4586 codec chip
- SPDIF input
- SPDIF output
- 6 line-level output channels at 24-bits each
- 2 line-level input channels at 24-bits each
- Mono Electret microphone input
- Optional external power supplies for amplifiers
- Optional internal power supplies
- EB402/EB403 TDM serial port for data
- EB402/EB403 GPIO lines for configuration and control
- Interrupt lines to EB402/EB403

The codec analog outputs are limited to driving high-impedance loads. They should only be used to drive amplified speakers that accept line-level inputs. Do not connect passive, low-impedance (8 ohm) speakers to these outputs. The analog inputs must also be line-level signals.

The CODEC-5.1 is fully supported by the EB402 and EB403 Board Support Packages that are available as part of the LSI402ZX and LSI403LP Development Kits. Please refer to the *EB402 Board Support Package User Guide* or *EB403 Board Support Package User Guide* for further information.

Chapter 2
Installation

This chapter describes installation of the CODEC-5.1 card. It contains the following sections:

2.1 Hardware Equipment Required

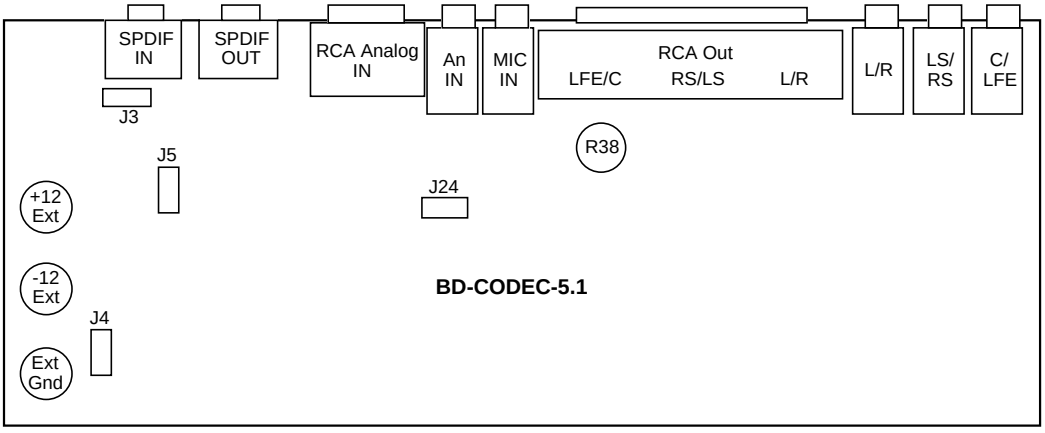
The following is the minimum recommended list of hardware required to evaluate and/or use the CODEC-5.1 daughtercard:

- LSI Logic EB402 or EB403 evaluation board.
- Host computer with SDK tools and debugger interface
- CODEC-5.1 Daughtercard
- Audio output devices
  - Line powered speakers, or
  - Amplifier with speakers, or
  - Analyzer
- Input Sources
  - DVD player or other SPDIF generating device
  - Stereo line-level inputs
  - Electret microphone

2.2 Hardware Setup for the CODEC-5.1 Daughtercard

The CODEC-5.1 daughtercard may be used with either the LSI Logic EB402 or the EB403 evaluation boards. The daughtercard is installed onto the SPORT0 and SPORT1 TDM interface connectors provided on the ZSP evaluation boards. Figure 2.1 shows an illustration of the CODEC-5.1 indicating locations of the various connectors and jumpers on the board.

Figure 2.1 CODEC-5.1 Connectors



2.3 Installation

The installation procedure is as follows:

1. Set jumpers J3, J4, and J5 for either internal or external power as shown in Table 2.1

Table 2.1 Power connections

Jumper	Power from EB40X	External Power
J5	Open	Installed
J3	2-3	1-2
J4	2-3	1-2
J6	Open	Analog Ground
J7	Open	-12V DC (Acceptable range is -7Vdc to _15Vdc)
J8	Open	+12V DC (Acceptable range is +7Vdc to +15Vdc)

2. Install J24 for input selection as shown in Table 2.2

Table 2.2 Input Selection

Jumper	SPDIF Input	Stereo Line Input	Microphone Input
J24	2-3	2-3	1-2

3. Plug the CODEC-5.1 daughtercard into the motherboard. The connectors are keyed and can only be installed in one orientation.
4. Connect an external power source to the CODEC-5.1 daughtercard if configured from step 1. The external supply should be turned off during connection and only turned on after the connections have been made.
5. Connect an input source to one of the following locations as shown in Table 2.3.

Table 2.3 Input Source Connector selection

Type	Input Connection - RCA	Input Connection - PhonoJack	Jumpers
Digital Audio	J19	NA	NA
Analog In	J20 - Bottom- Left J20 - Top - Right	J25 - TIP - Left J25 - RING - Right	J24 2-3
Microphone In	NA	J21 - TIP	J24 2-3

6. When using a microphone input, Potentiometer RX can be adjusted to increase or decrease the gain of the microphone amplifier.
7. Connect a destination to the output channels as shown in Table 2.4.

Table 2.4 Output Channel Connectors

Channel	RCA	PhonoJack
Left	J10-CH3-Bottom	J18-Tip
Right	J10-CH3-Top	J18-Ring
Left Surround	J10-CH2-Bottom	J15-Tip
Right Surround	J10-CH2-Top	J15-Ring
Center	J10-CH1-Bottom	J12-Tip
Base	J10-CH1-Top	J12-Ring

8. Note that all output channels are line-level outputs and require an amplifier or powered speakers.
9. Turn the EB402/EB403 evaluation board power on.
10. Turn on the external power supply if one is being used.

A software driver for the CODEC-5.1 daughtercard is provided in the EB402 and EB403 Board Support Packages. These BSPs are included on the ZSP Development Kit (ZDK) CDROM supplied with the EB402 and EB403. For details of the CODEC-5.1 driver, please refer to the EB402 Board Support Package Technical Manual or EB403 Board Support Package Technical Manual.

Chapter 3
Operation

This chapter describes the CODEC-5.1 interfaces to the EB402/EB403 cards and the operation of its circuitry. It contains the following sections:

3.1 Interface to LSI402ZX/LSI403LP

The AK4586 has two interfaces: a control interface and a data interface. The control interface is used to set the operating mode of the Codec chip and to read status information back. The data interface is used to read data, either digital audio or digitized analog inputs, and to write the 6 output channels.

Four GPIOs on the LSI402ZX/LSI403LP are used for the control interface. These signals comprise a clock, chip select, data in, and data out. All data is read and written from/to the control interface by manipulating individual bits in the PIO register.

Serial port 0 is used for the data interface to the codec. The AK4586 codec can be configured for TDM mode. This puts all three output pairs on a single serial port output wire and the input data on a single input wire.

Serial port 1 is used to provide a clock input to the AK4586 when in non-digital audio mode. By setting the clock rate of the serial port, the sample rate of the codec can be controlled. The sample rate of the codec is equal to the SP1 Clock Rate divided by 256. For example, to achieve a 44.1 kHz sample rate, the serial port clock rate should be 44.1K x 256 or 11.2896 MHz. Setting the EB402 clock rate at 170 MHz and using a

clock divider of 15 would yield a sample rate of 170 MHz/12/256 or 44.27 kHz, an error of 0.4%.

3.2 Circuit Description

This section describes the schematic for the audio daughtercard. The schematics for the CODEC-5.1 card are shown at the end of this manual. Figure A.1 shows the hierarchical connections between the various blocks.

Figure A.2 illustrates the connections to the EB402/3. Both SPORT0 and SPORT1 are used to provide access to the GPIO lines required. GPIO lines on the LSI402ZX/LSI403LP chip are used to control the 4-wire interface on the Codec. This four-wire interface is used to configure the codec and read back status information. SPORT0 contains the serial TDM interface between the AK4586 Codec and the ZSP processor. The TX clock from SPORT1 is routed to the clock input of the AK4586. When no external digital source is present, the AK4586 will automatically switch to the clock input signal to generate it's clock. This allows the codec rate to be set under program control. The codec produces 2 interrupts which are routed to the LSI402ZX/LSI403LP to pins INT2 and INT3. These interrupt lines are used to indicate operational status like the lock signal, non-PCM data stream, etc.

Figure A.3 contains the connections to the AK4586 Codec. A separate +5V regulator is used to provide the +5V rail required for the AK4586. U11 generates a reset pulse at powerup for the AK4586.

Figure A.4 shows the power supplies for the daughtercard. U2 is used to provide the +7V supply for the op-amps when using internal power. The analog power used by the amplifiers can either be produced on the CODEC-5.1 or through an external power supply. Jumpers J3, J4, and J5 are used to select either internally generated power or external power. J5, when installed, shuts down both U3 and U4. U3 generates a -9V rail from the +9V supplied from the EB402, and U4 generates -7V from the -9V supply. The use of external supplies helps to reduce noise in sensitive environments, while the internal supplies provide a level of convenience for development purposes. J9 provides the common connection between the analog and digital ground planes and must be always installed. The artwork includes a permanent connection across J9

on the top layer which can be cut for those applications requiring a separated ground system.

Figure A.5 shows the Audio connections on and off the board. J10 contains the 6 output channels in an RCA block connector. J12, J15, and J18 provide the same output connections in 3.5mm line-output jacks. J12 provides Left and Right channels for either 6 channel output or for stereo output. J15 provides Left Surround and Right Surround for 6 channel outputs. J18 provides Center and Base for 6 channel outputs. J19 is an RCA connector for the SPDIF input source, typically a DVD player. J23 is a SPDIF output pass through connection. J20 provides an RCA-style input connection for left and right stereo channels, and J25 provides the input connection using a phonojack input. J21 is a microphone input for a mono electret microphone.

Figure A.6 shows the amplifiers for each of the output DAC channels, the stereo line-inputs, and the microphone input. Figure A.7 shows one of the output DAC amplifiers. This amplifier will produce a +/- 3V signal suitable for driving line-level outputs.

Figure A.13 shows a line-input amplifier. This amplifier takes a line-level input signal and produces a valid analog input signal for the codec.

Figure A.14 shows the microphone amplifier circuit. This circuit provides power and amplification for an electret microphone. R38 is available on the board to adjust the gain of the amplifier.

Appendix A
Schematics

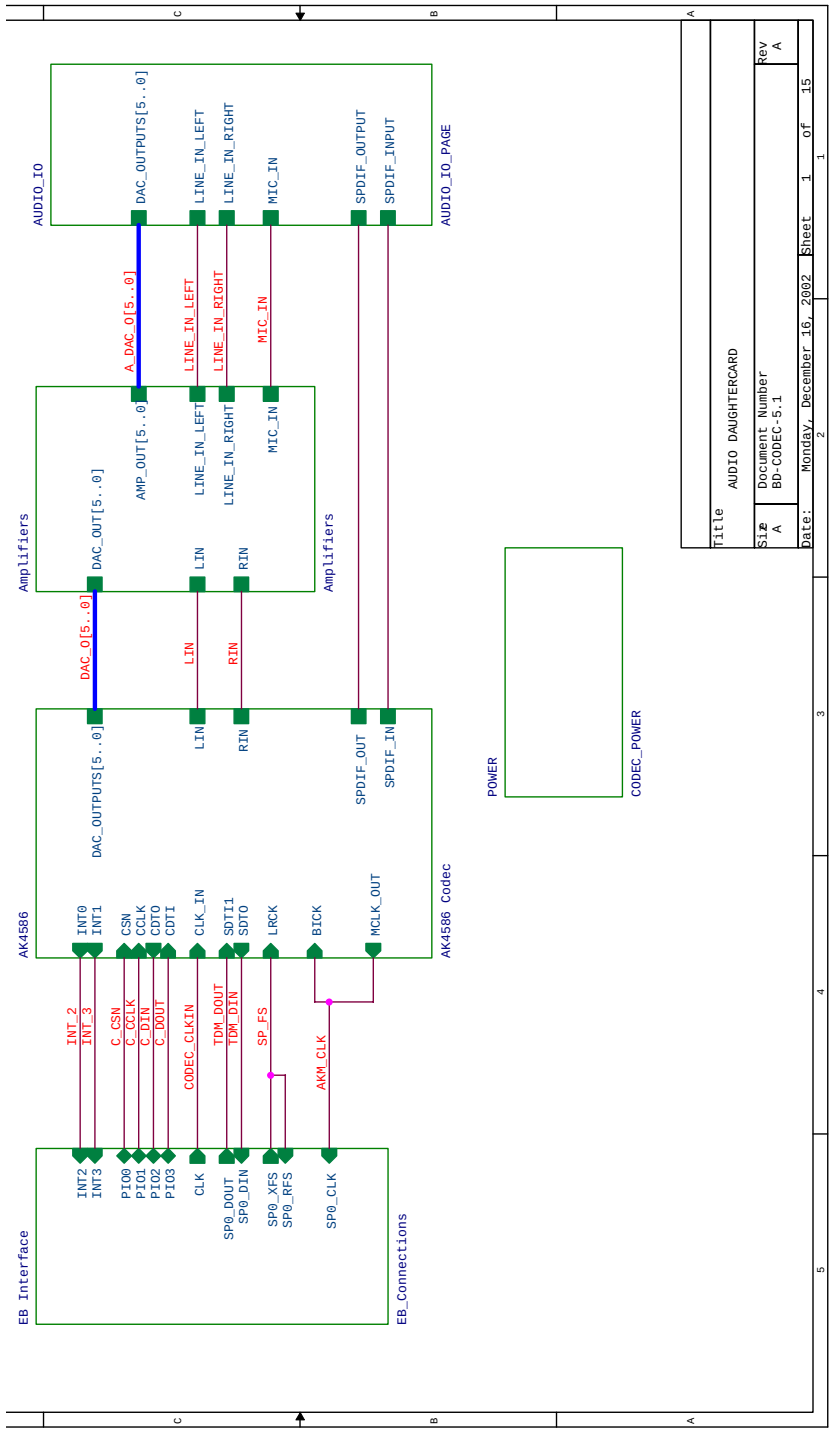


Figure A.1

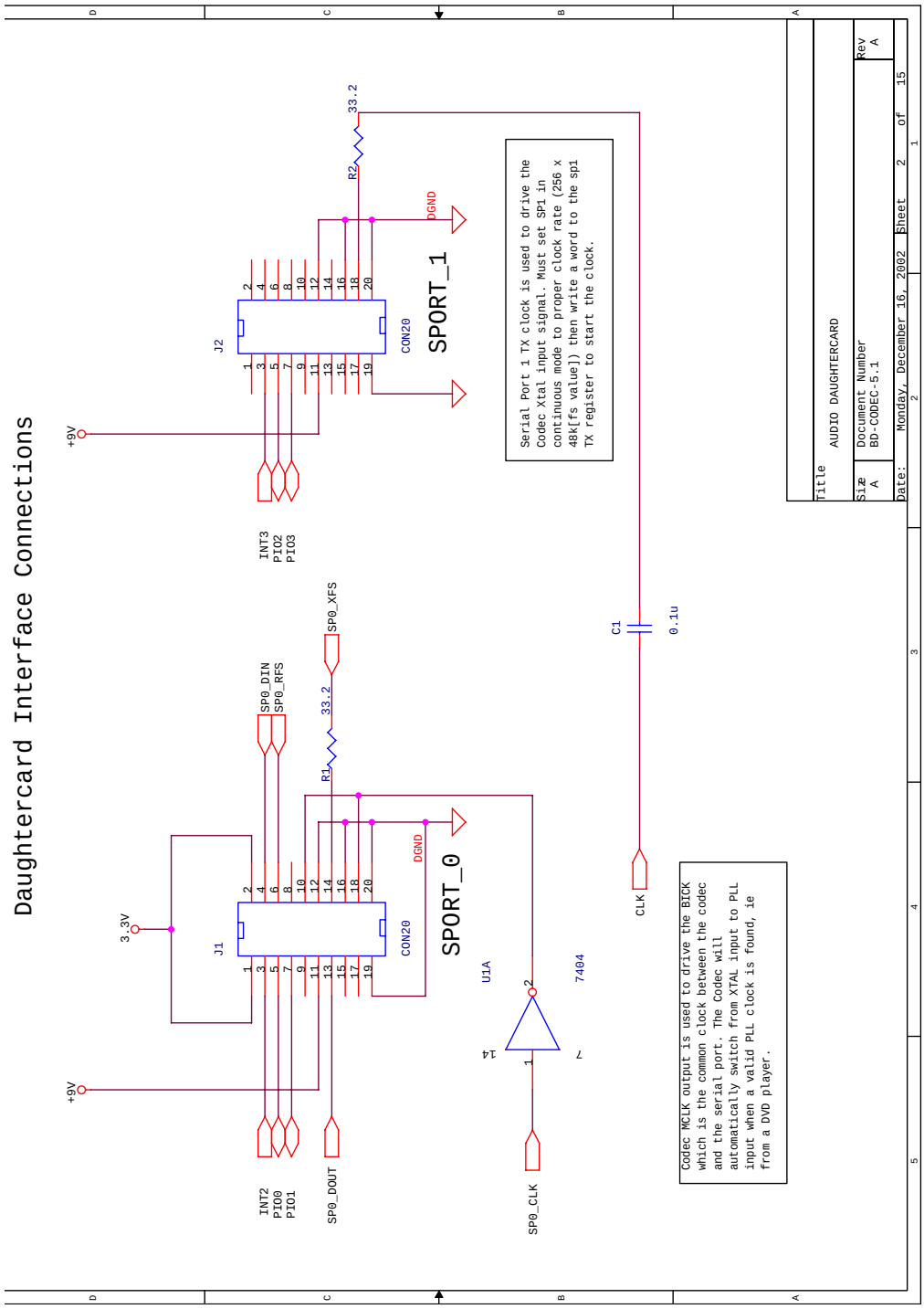


Figure A.2

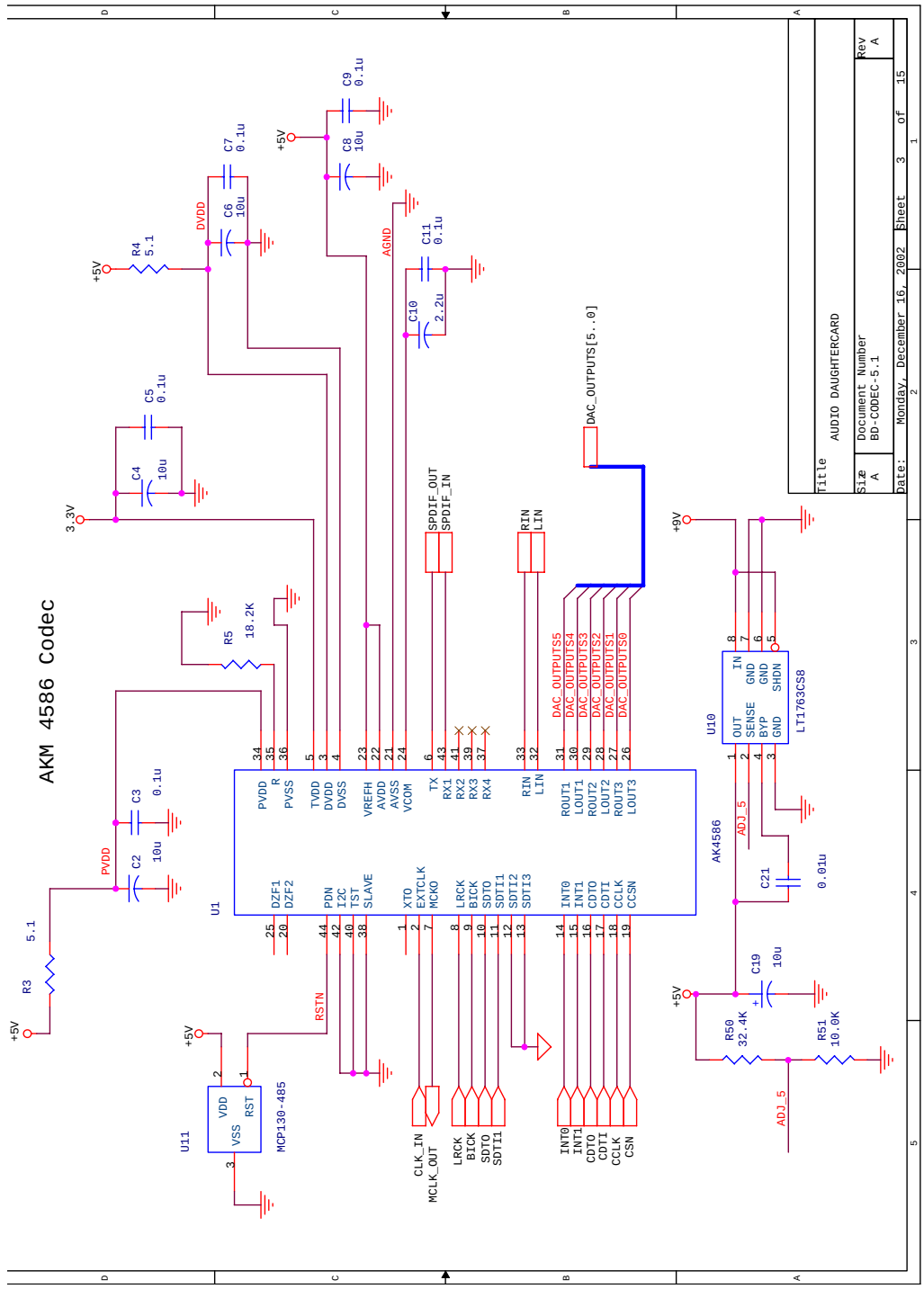


Figure A.3

Figure A.4

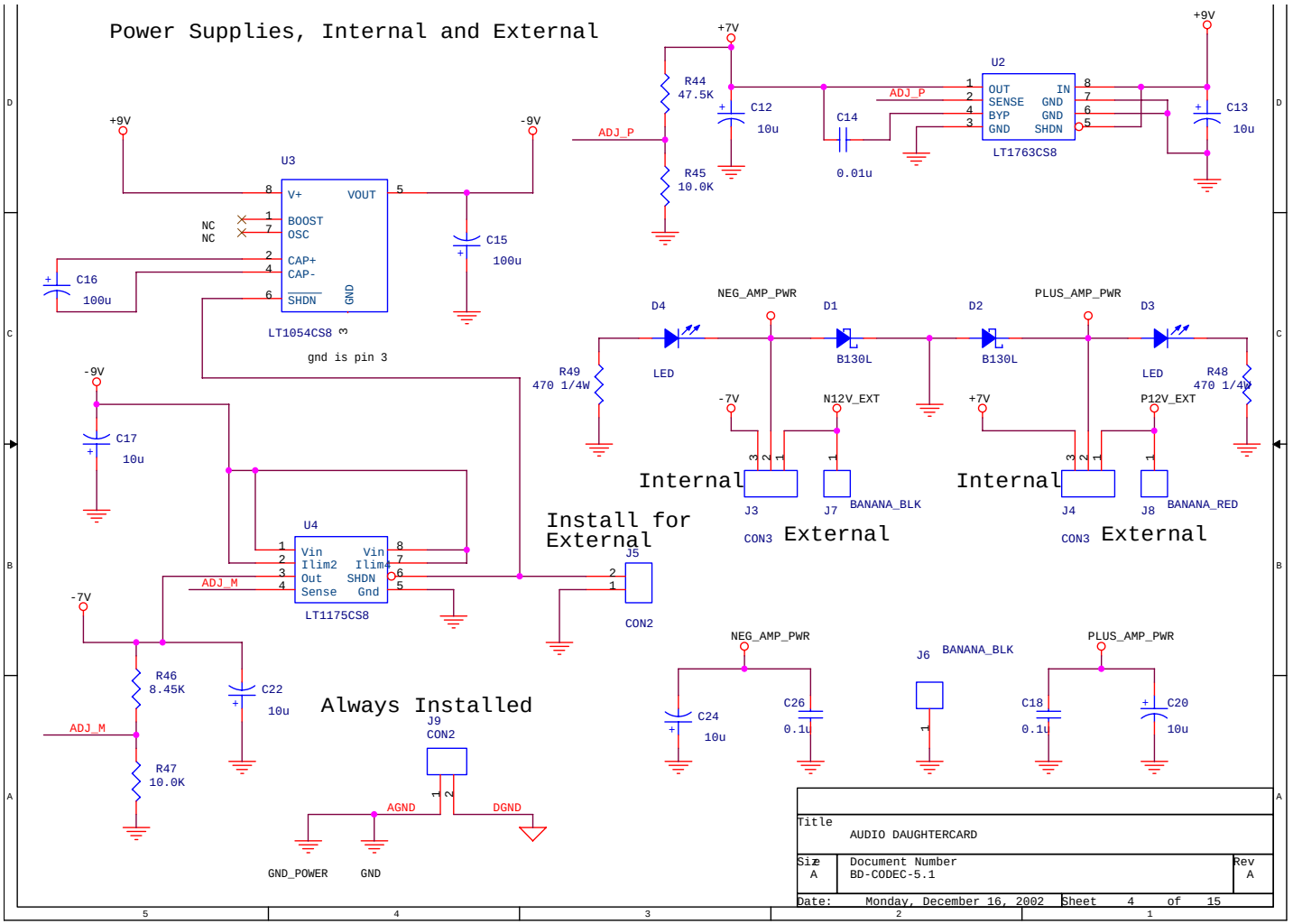


Figure A.5

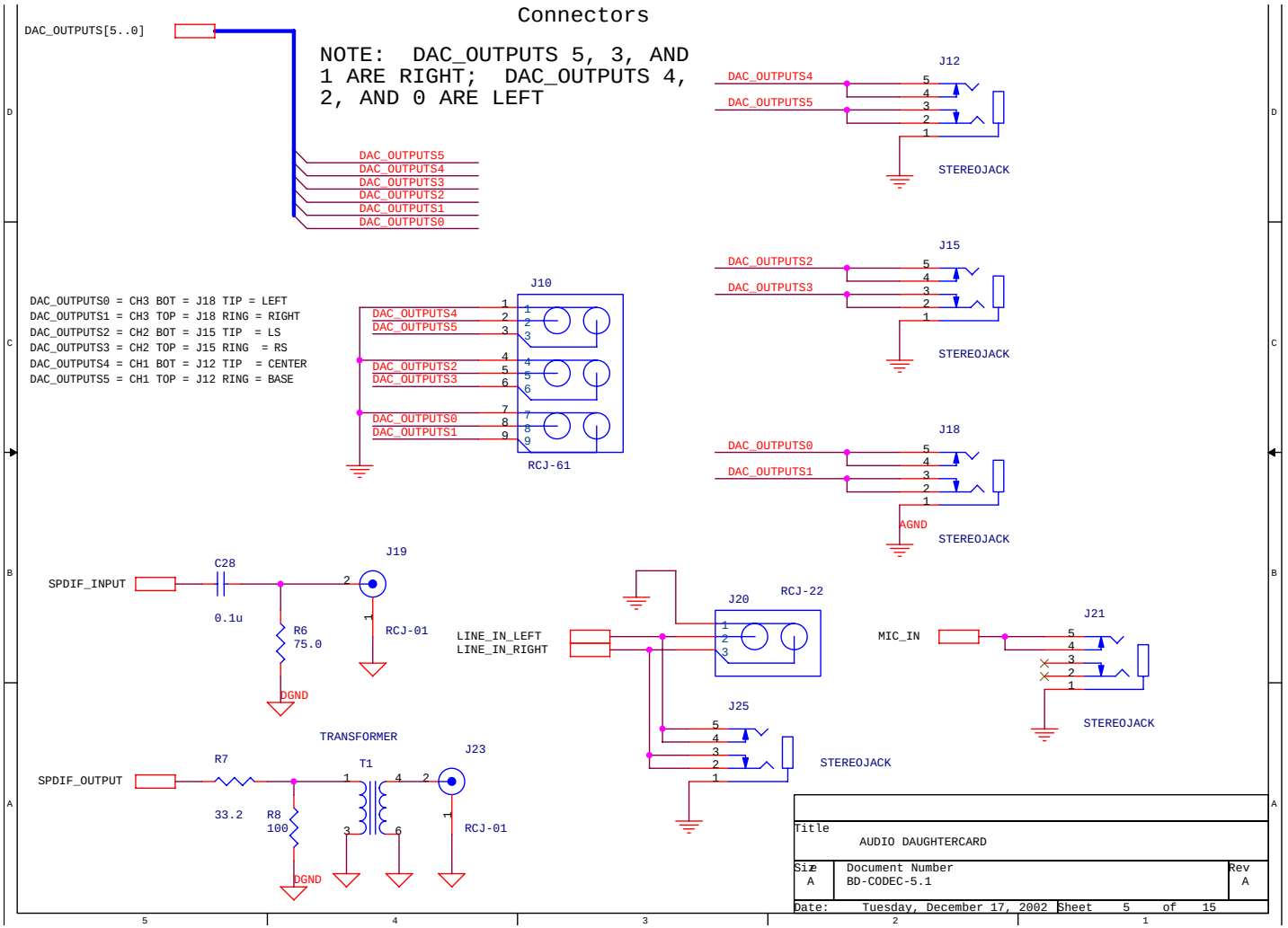
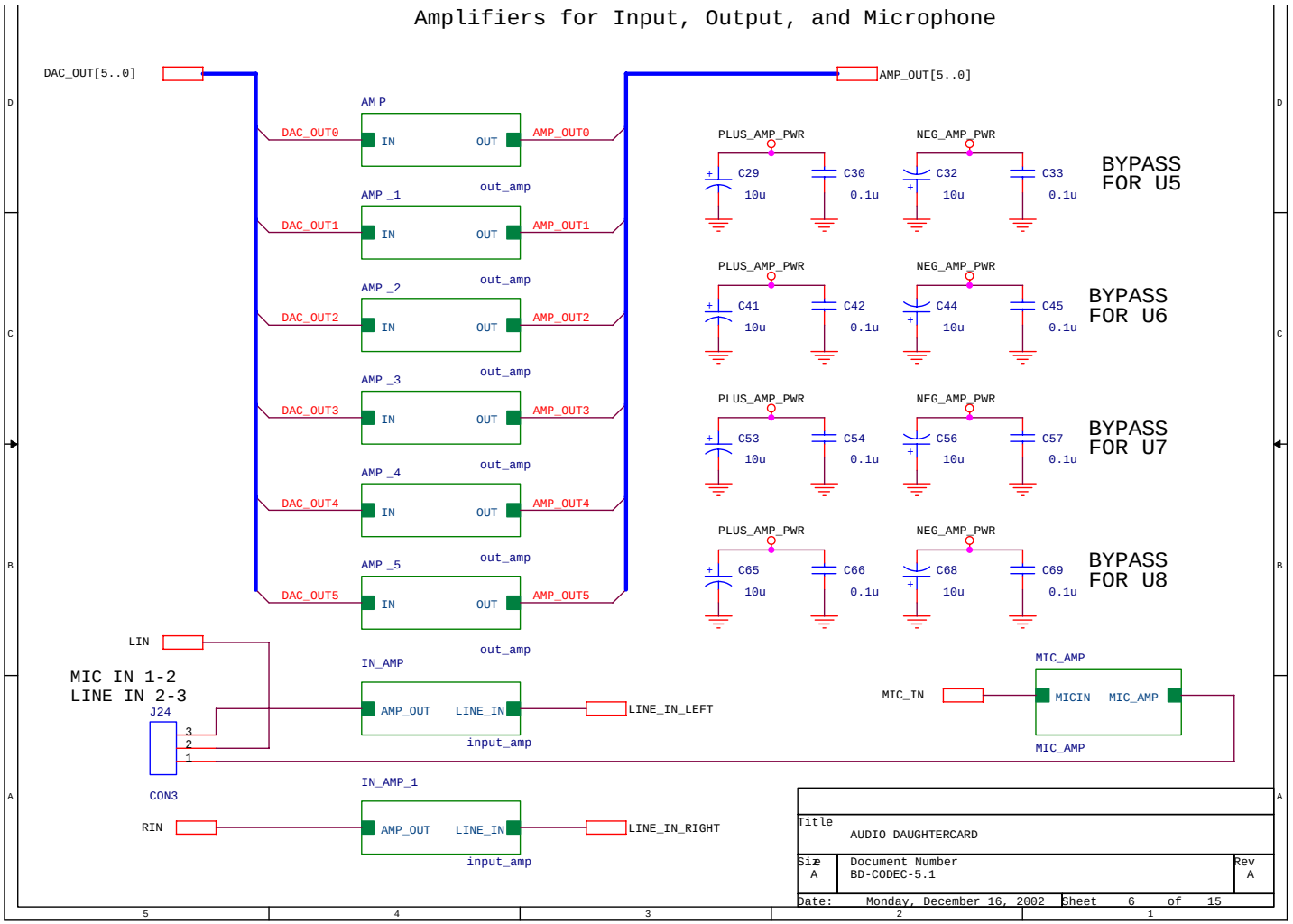


Figure A.6



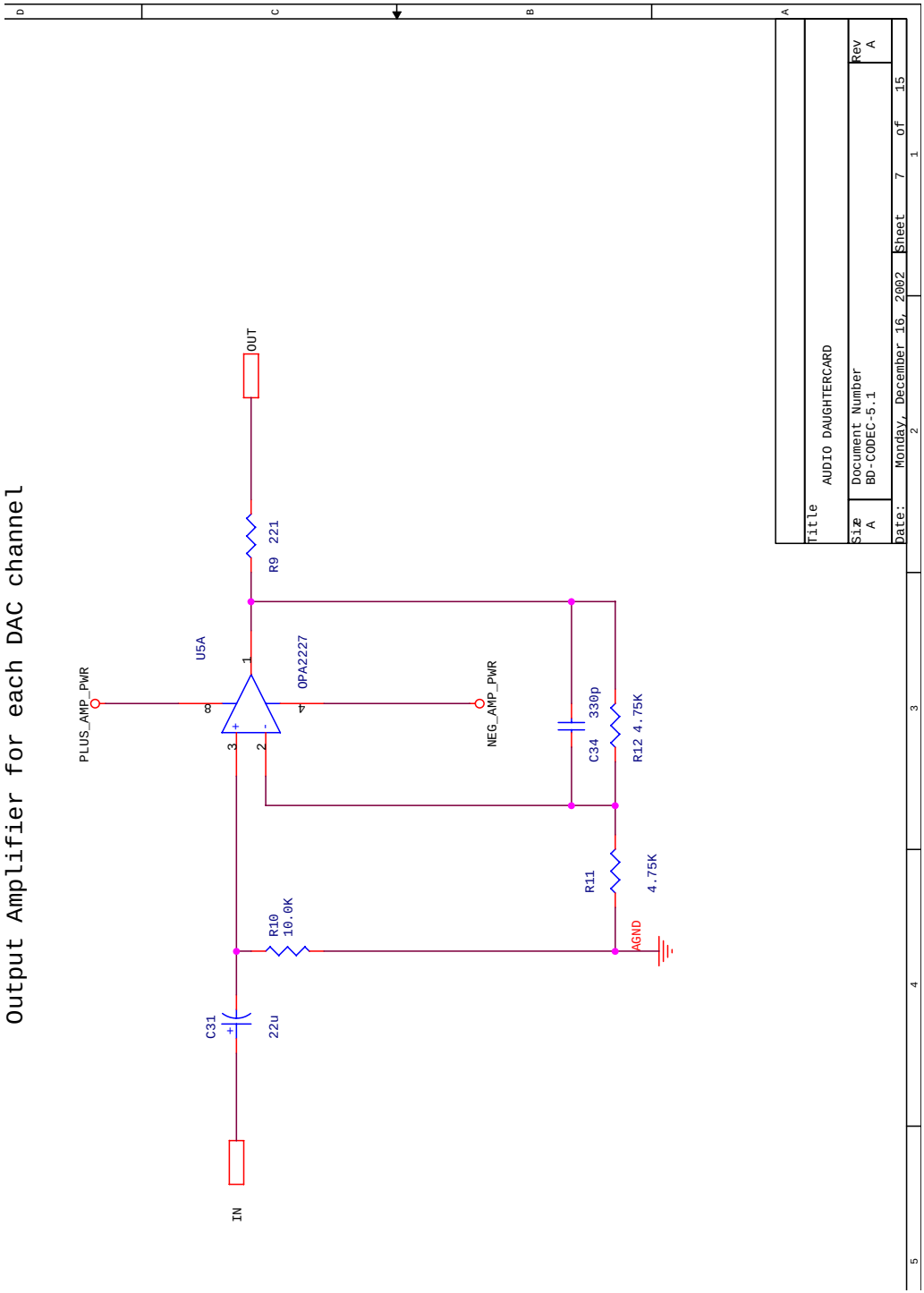


Figure A.7

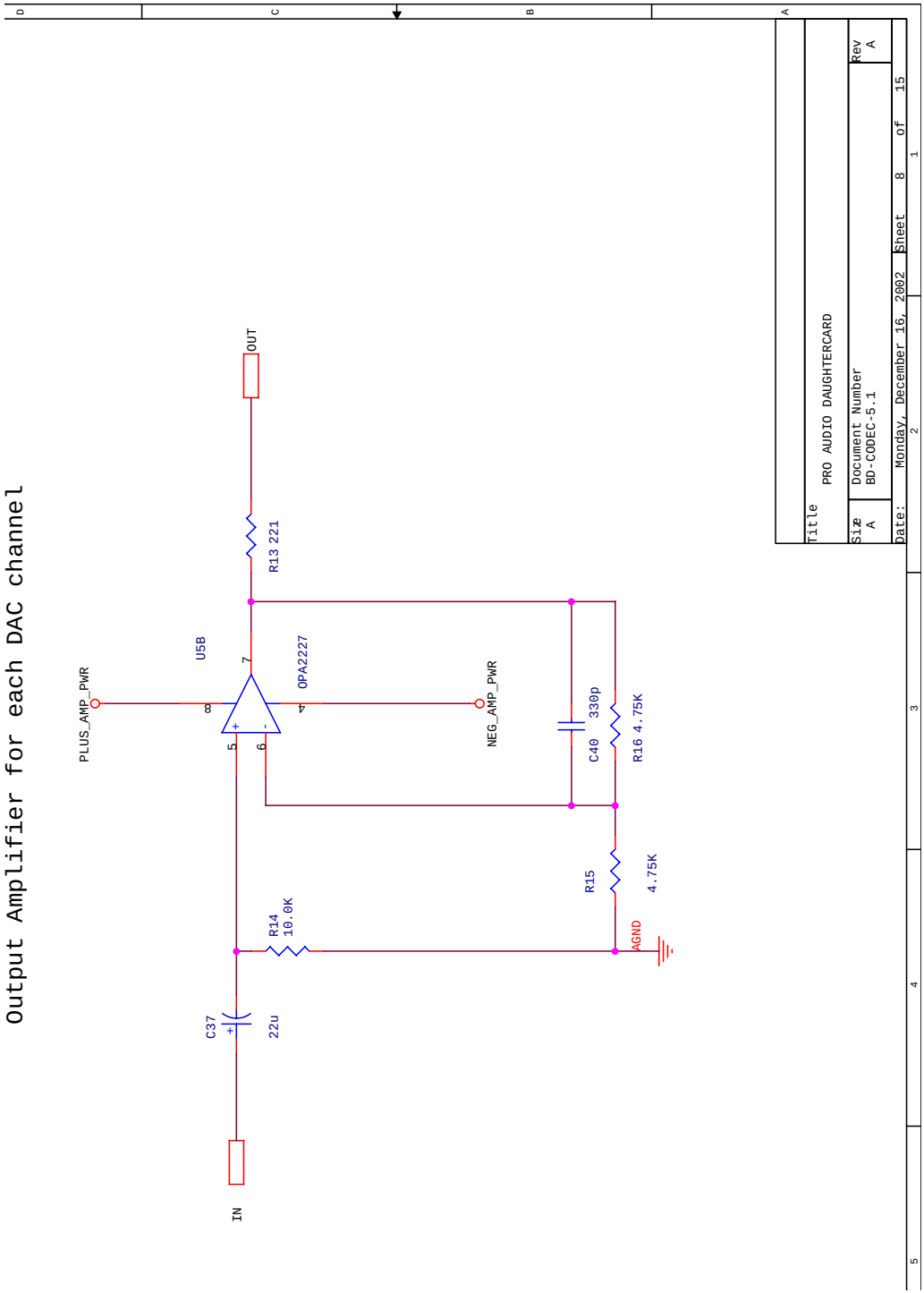


Figure A.8

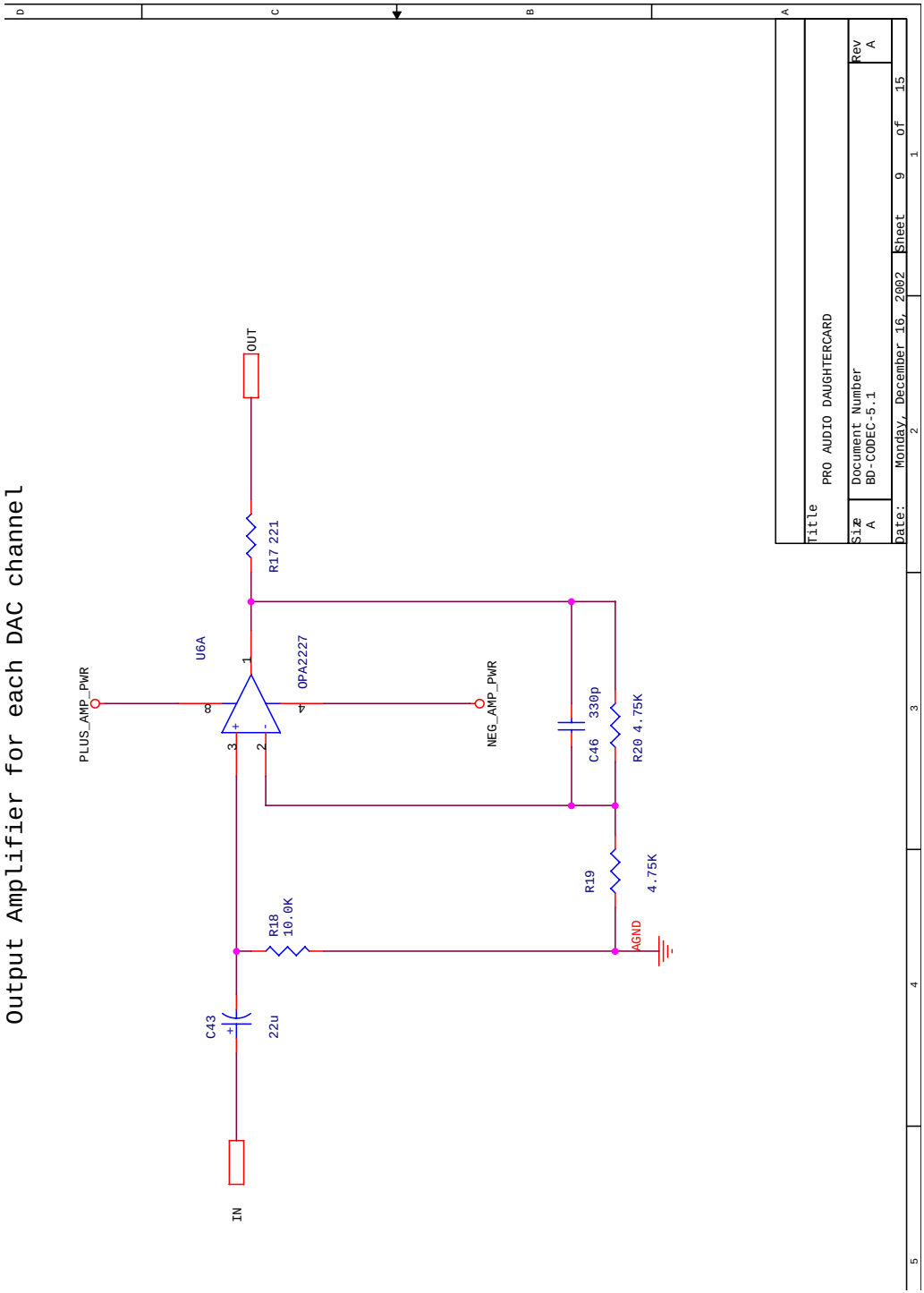


Figure A.9

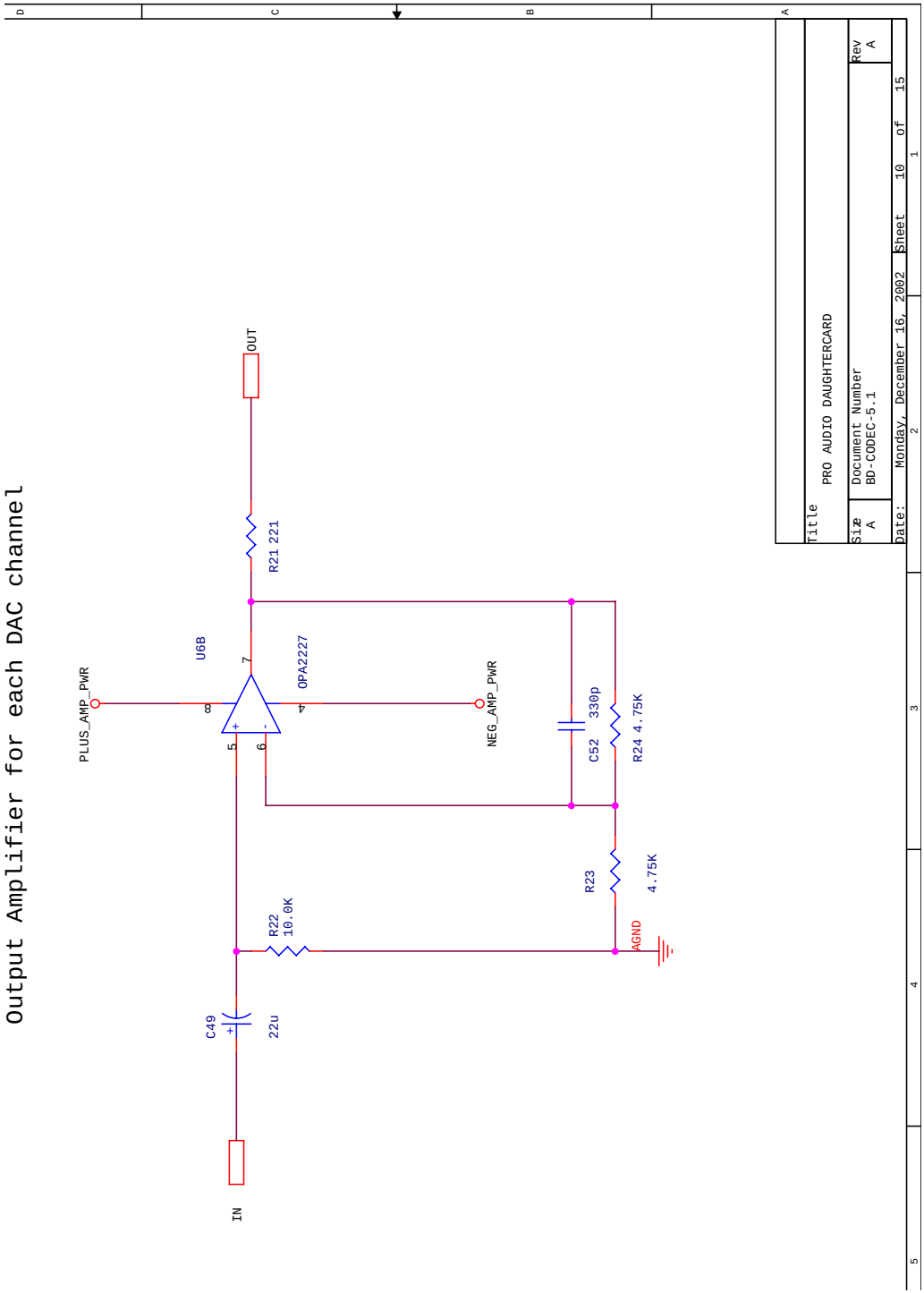


Figure A.10

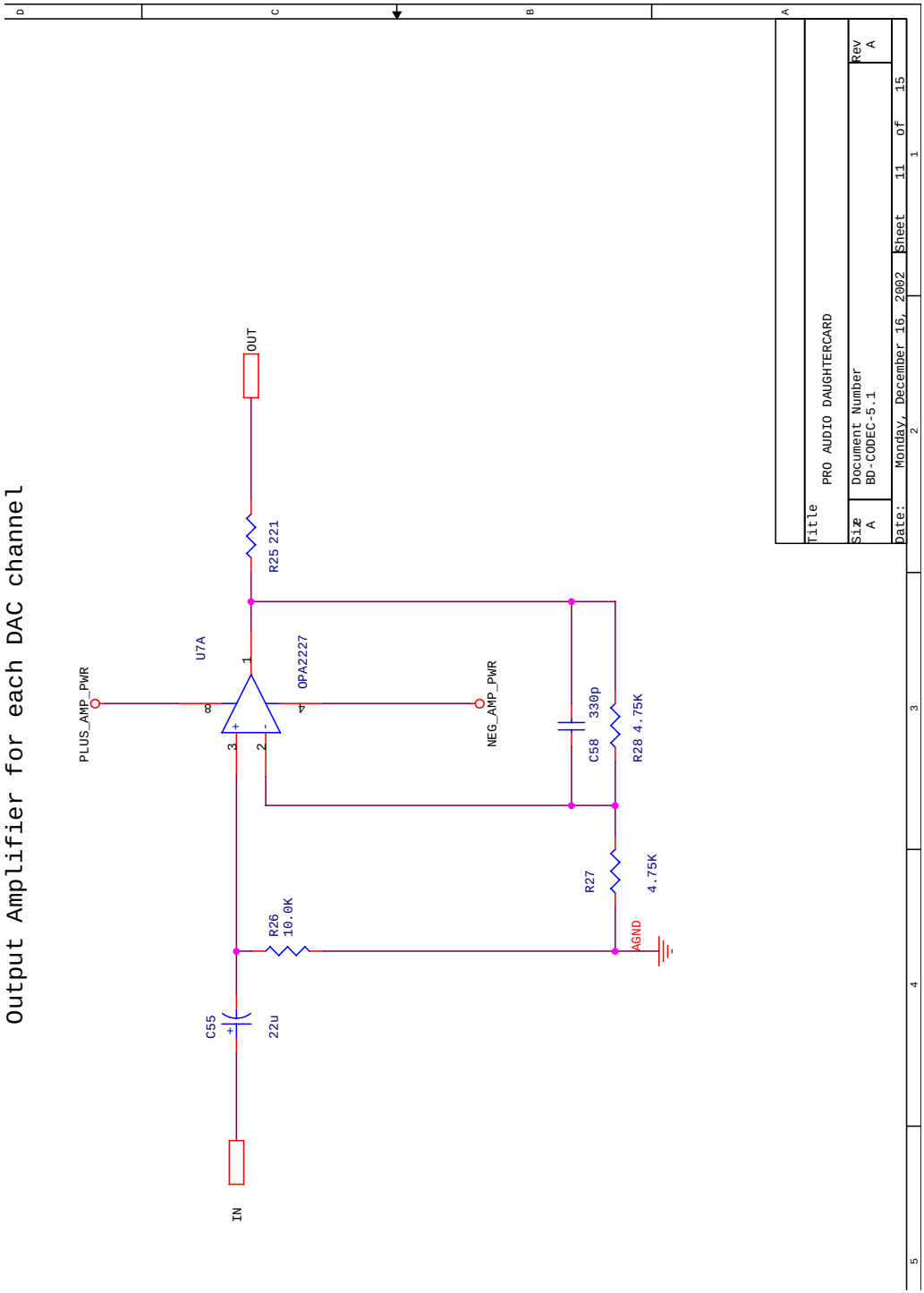


Figure A.11

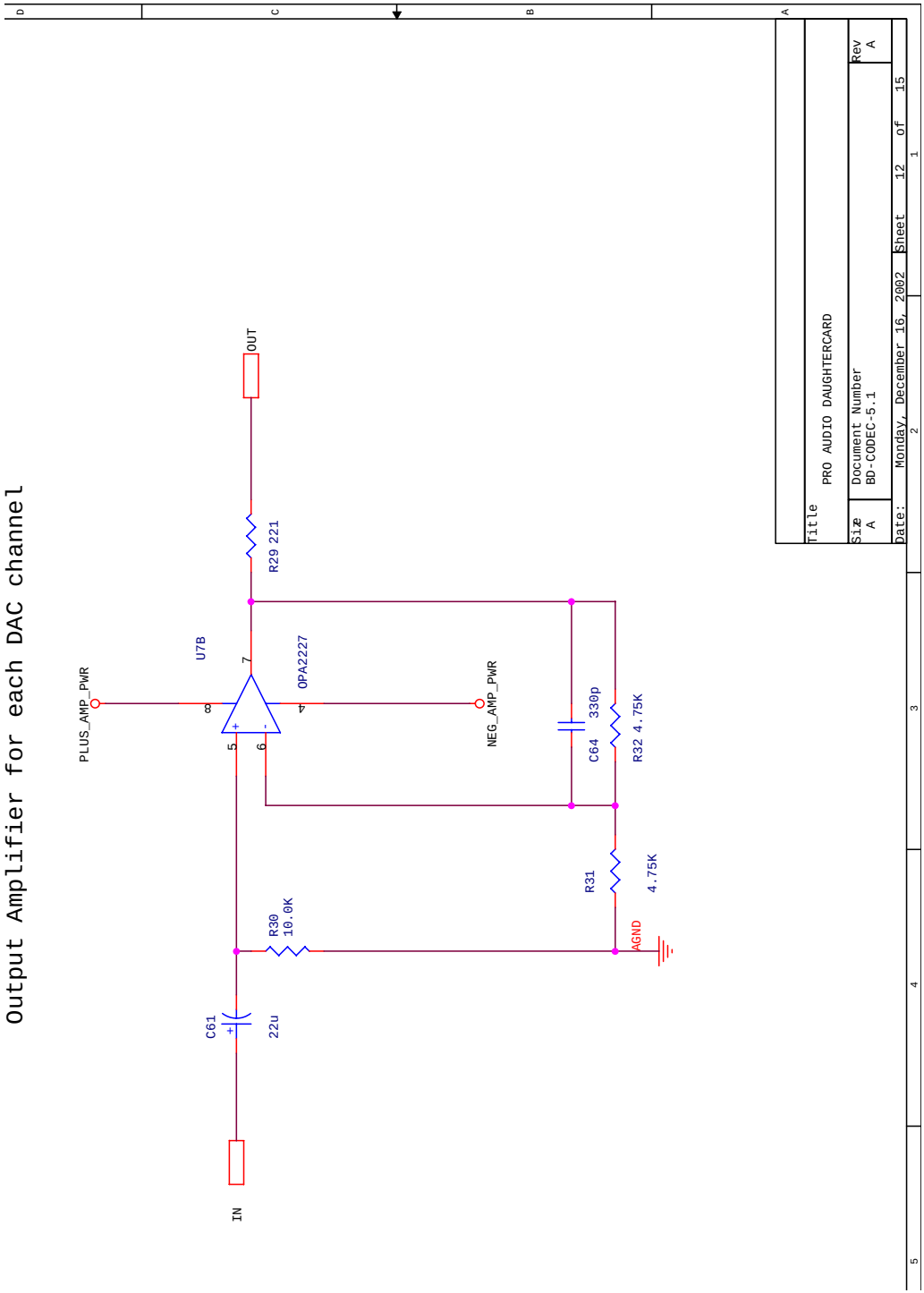


Figure A.12

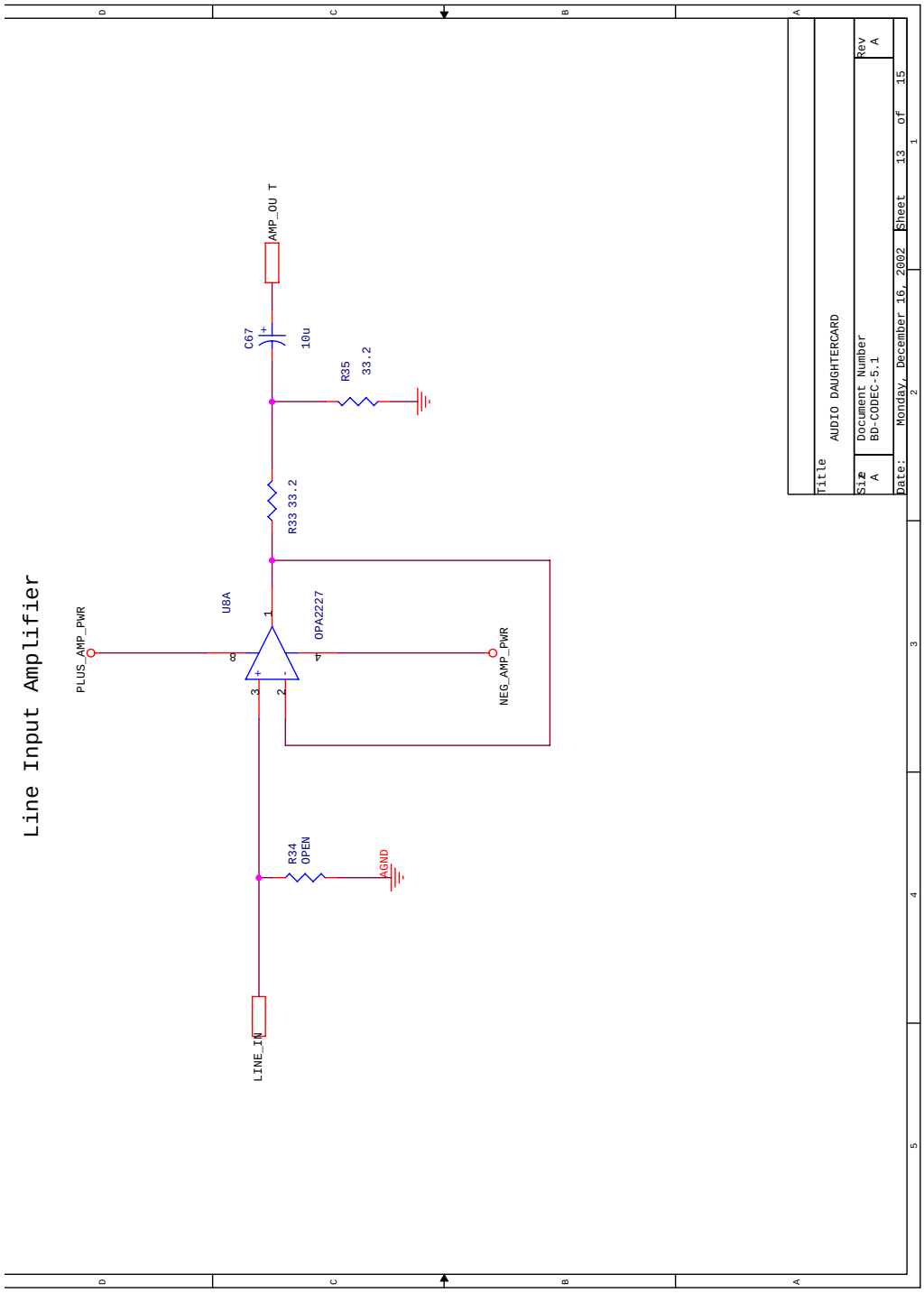


Figure A.13

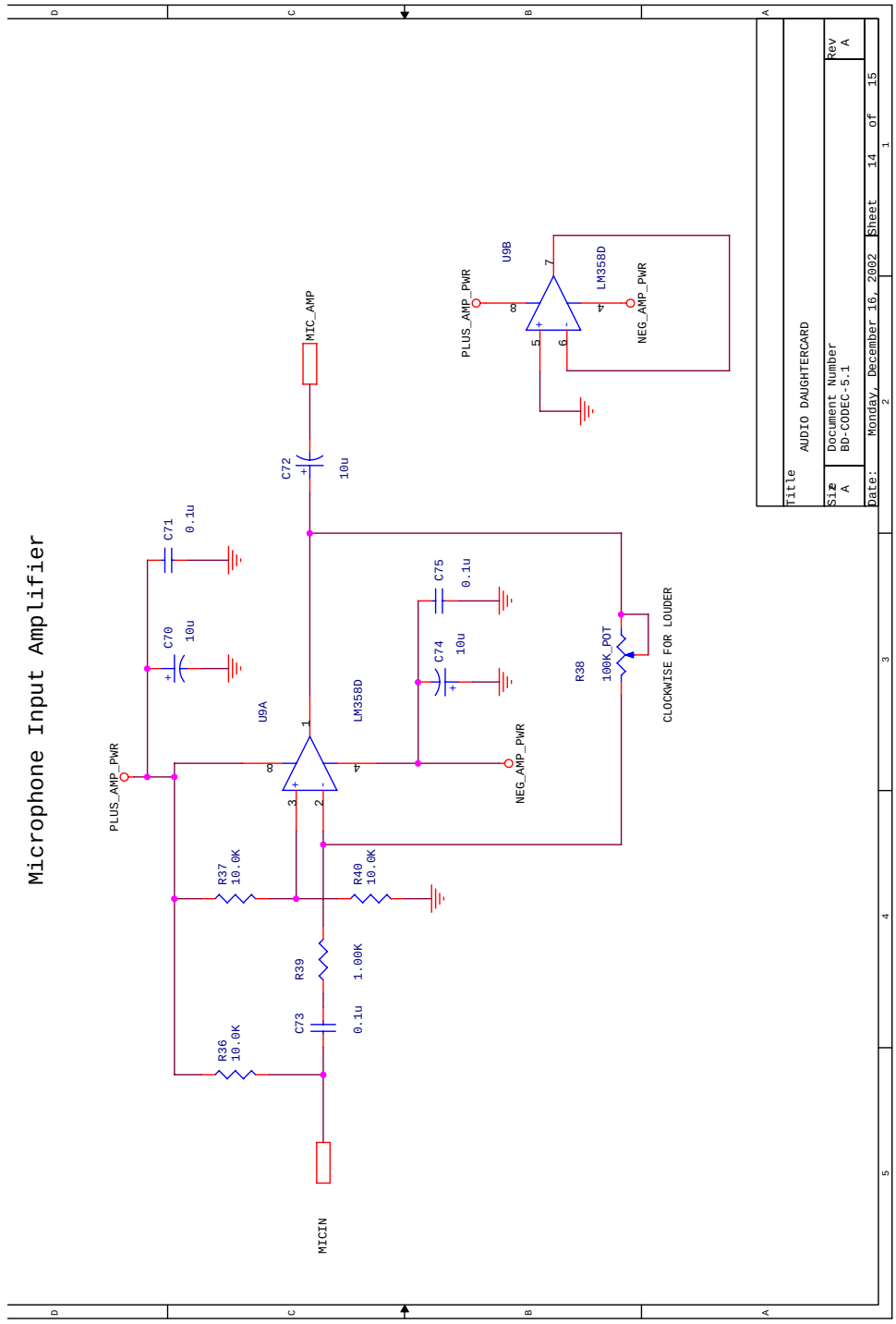


Figure A.14

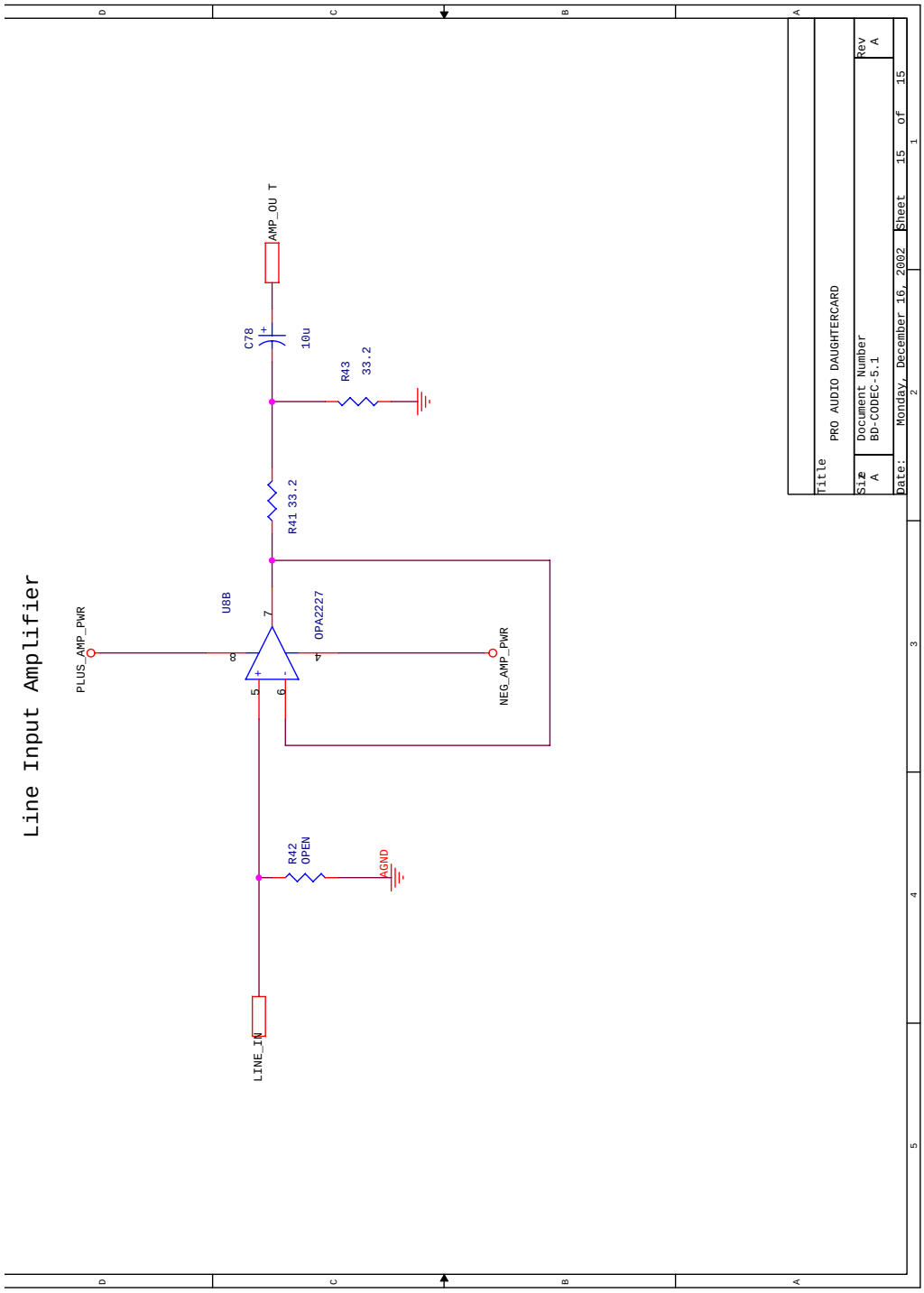


Figure A.15