

Picoamp Input Current, Microvolt Offset, Low Noise Op Amp

FEATURES

- OP-07 Type Performance:
at 1/8th of OP-07's Supply Current
at 1/20th of OP-07's Bias and Offset Currents
- *Guaranteed* Offset Voltage: 25 μ V Max
- *Guaranteed* Bias Current: 100pA Max
- *Guaranteed* Drift: 0.6 μ V/ $^{\circ}$ C Max
- Low Noise, 0.1Hz to 10Hz: 0.5 μ V_{P-P}
- *Guaranteed* Low Supply Current: 500 μ A Max
- *Guaranteed* CMRR: 114dB Min
- *Guaranteed* PSRR: 114dB Min
- *Guaranteed* Operation at ± 1.2 V Supplies

APPLICATIONS

- Replaces OP-07 While Saving Power
- Precision Instrumentation
- Charge Integrators
- Wide Dynamic Range Logarithmic Amplifiers
- Light Meters
- Low Frequency Active Filters
- Thermocouple Amplifiers

DESCRIPTION

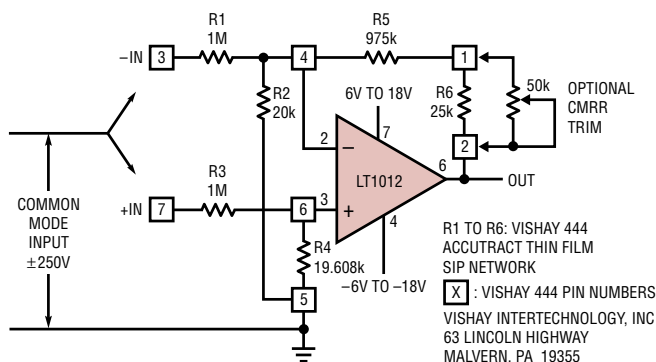
The LT[®]1012 is an internally compensated universal precision operational amplifier which can be used in practically all precision applications. The LT1012 combines picoampere bias currents (which are maintained over the full -55°C to 125°C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. The LT1012 achieves precision operation on two Ni-Cad batteries with 1mW of power dissipation. Extremely high common mode and power supply rejection ratios, practically unmeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of one million round out the LT1012's superb precision specifications.

The all around excellence of the LT1012 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1012 can be stocked as the universal internally compensated precision op amp.

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Protected by U. S. patents 4,575,685 and 4,775,884

TYPICAL APPLICATION

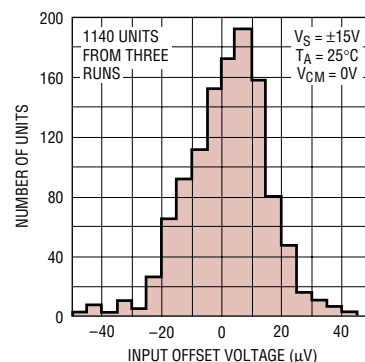
± 250 V Common Mode Range Instrumentation Amplifier ($A_V = 1$)



COMMON MODE REJECTION RATIO = 74dB (RESISTOR LIMITED)
WITH OPTIONAL TRIM = 130dB
OUTPUT OFFSET (TRIMMABLE TO ZERO) = 500 μ V
OUTPUT OFFSET DRIFT = 10 μ V/ $^{\circ}$ C
INPUT RESISTANCE = 1M

LT1012A • TA01

Typical Distribution of Input Offset Voltage



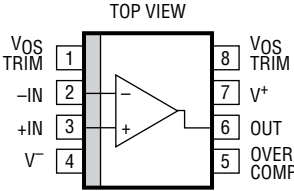
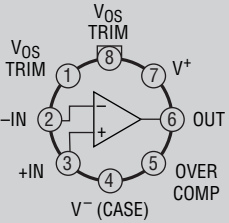
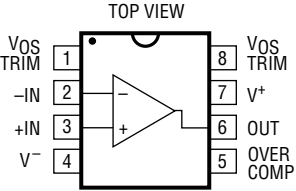
LT1012A • TA02

LT1012A/LT1012

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±20V	Operating Temperature Range	LT1012AM/LT1012M (OBSOLETE)....	–55°C to 125°C
Differential Input Current (Note 1)	±10mA		LT1012I/LT1012AI	–40°C to 85°C
Input Voltage	±20V		LT1012AC/LT1012C	
Output Short Circuit Duration	Indefinite		LT1012D/LT1012S8	0°C to 70°C
		Storage Temperature Range		–65°C to 150°C
		Lead Temperature (Soldering, 10 sec)		300°C

PACKAGE/ORDER INFORMATION

 <p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 100^{\circ}C$, $\theta_{JA} = 170^{\circ}C/W$</p>	 <p>H PACKAGE 8-LEAD TO-5 METAL CAN $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 150^{\circ}C/W$, $\theta_{JC} = 45^{\circ}C/W$</p>	 <p>N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 100^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$</p>
ORDER PART NUMBER	ORDER PART NUMBER	ORDER PART NUMBER
LT1012S8 LT1012IS8 LT1012ACS8 LT1012AIS8	LT1012AMH LT1012MH LT1012ACH LT1012CH LT1012DH	LT1012ACN8 LT1012AIN8 LT1012CN8 LT1012DN8 LT1012IN8
S8 PART MARKING	OBSOLETE PACKAGE Consider the S8 or N8 Packages for Alternate Source	
1012 1012I 1012A 1012AI		

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012AM/AC/AI			LT1012M/I			LT1012C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 3)		8 20	25 90		8 20	35 90		10 25	50 120	μV μV
	Long Term Input Offset Voltage Stability			0.3			0.3			0.3		$\mu V/month$
I_{OS}	Input Offset Current	(Note 3)		15 25	100 150		15 25	100 150		20 30	150 200	pA pA
I_B	Input Bias Current	(Note 3)		± 25 ± 35	± 100 ± 150		± 25 ± 35	± 100 ± 150		± 30 ± 40	± 150 ± 200	pA pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5			0.5		μV_{P-P}
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 4) $f_0 = 1000Hz$ (Note 5)		17 14	30 22		17 14	30 22		17 14	30 22	nV/\sqrt{Hz} nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_0 = 10Hz$		20			20			20		fA/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	300 300	2000 1000		300 200	2000 1000		200 200	2000 1000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	114	132		114	132		110	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2V$ to $\pm 20V$	114	132		114	132		110	132		dB
	Input Voltage Range		± 13.5	± 14		± 13.5	± 14		± 13.5	± 14		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	± 13	± 14		± 13	± 14		± 13	± 14		V
	Slew Rate		0.1	0.2		0.1	0.2		0.1	0.2		V/ μs
I_S	Supply Current	(Note 3)		370 380	500 600		380 380	600		380 380	600	μA μA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012D			LT1012S8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 3)		12 25	60		15 25	120 180	μV μV
	Long Term Input Offset Voltage Stability			0.3			0.4		$\mu V/month$
I_{OS}	Input Offset Current	(Note 3)		20 30	150		50 60	280 380	pA pA
I_B	Input Bias Current	(Note 3)		± 30 ± 40	± 150		± 80 ± 120	± 300 ± 400	pA pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μV_{P-P}
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 5) $f_0 = 1000Hz$ (Note 5)		17 14	30 22		17 14	30 22	nV/\sqrt{Hz} nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_0 = 10Hz$		20			20		fA/\sqrt{Hz}
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$ $V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	200 200	2000 1000		200 120	2000 1000		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	110	132		110	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2V$ to $\pm 20V$	110	132		110	132		dB
	Input Voltage Range		± 13.5	± 14.0		± 13.5	± 14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	± 13	± 14		± 13	± 14		V
	Slew Rate		0.1	0.2		0.1	0.2		V/ μs
I_S	Supply Current	(Note 3)		380	600		380	600	μA

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range of $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for LT1012AM and LT1012M, and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for LT1012AI and LT1012I. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1012AM/AI			LT1012M/I			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 3)	●	30	60		30	180		μV
			●	40	180		40	250		μV
	Average Temperature Coefficient of Input Offset Voltage		●	0.2	0.6		0.2	1.5		$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current	(Note 3)	●	30	250		30	250		pA
			●	70	350		70	350		pA
	Average Temperature Coefficient of Input Offset Current		●	0.3	2.5		0.3	2.5		$\text{pA}/^{\circ}\text{C}$
I_B	Input Bias Current	(Note 3)	●	± 80	± 600		± 80	± 600		pA
			●	± 150	± 800		± 150	± 800		pA
	Average Temperature Coefficient of Input Bias Current		●	0.6	6.0		0.6	6.0		$\text{pA}/^{\circ}\text{C}$
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L \geq 10\text{k}\Omega$	●	200	1000		150	1000		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L \geq 2\text{k}\Omega$	●	200	600		100	600		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5\text{V}$	●	110	128		108	128		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.5\text{V}$ to $\pm 20\text{V}$	●	110	126		108	126		dB
	Input Voltage Range		●	± 13.5			± 13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10\text{k}\Omega$	●	± 13	± 14		± 13	± 14		V
I_S	Supply Current		●	400	650		400	800		μA

LT1012A/LT1012

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1012AC			LT1012C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 3)	●	20	60		20	100		μV
			●	30	160		30	200		μV
	Average Temperature Coefficient of Input Offset Voltage		●	0.2	0.6		0.2	1.0		$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current	(Note 3)	●	25	230		35	230		pA
			●	40	300		45	300		pA
	Average Temperature Coefficient of Input Offset Current		●	0.3	2.5		0.3	2.5		$\text{pA}/^{\circ}\text{C}$
I_B	Input Bias Current	(Note 3)	●	± 35	± 230		± 35	± 230		pA
			●	± 50	± 300		± 50	± 300		pA
	Average Temperature Coefficient of Input Bias Current		●	0.3	2.5		0.3	2.5		$\text{pA}/^{\circ}\text{C}$
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L \geq 10\text{k}\Omega$	●	200	1500		150	1500		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L \geq 2\text{k}\Omega$	●	200	1000		150	800		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = 13.5\text{V}$	●	110	130		108	130		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.3\text{V}$ to $\pm 20\text{V}$	●	110	128		108	128		dB
	Input Voltage Range		●	± 13.5			± 13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10\text{k}\Omega$	●	± 13	± 14		± 13	± 14		V
I_S	Supply Current		●	400	600		400	800		μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1012D			LT1012S8			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 3)	●	25	140		30	200		μV
			●	40			45	270		μV
	Average Temperature Coefficient of Input Offset Voltage		●	0.3	1.7		0.3	1.8		$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current	(Note 3)	●	35	380		60	380		pA
			●	45			80	500		pA
	Average Temperature Coefficient of Input Offset Current		●	0.35	4.0		0.4	4.0		$\text{pA}/^{\circ}\text{C}$
I_B	Input Bias Current	(Note 3)	●	± 50	± 420		± 100	± 420		pA
			●	± 65			± 150	± 550		pA
	Average Temperature Coefficient of Input Bias Current		●	0.4	5.0		0.5	5.0		$\text{pA}/^{\circ}\text{C}$
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L \geq 10\text{k}\Omega$	●	150	1500		150	1500		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L \geq 2\text{k}\Omega$	●	150	800		100	800		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5\text{V}$	●	108	130		108	130		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.3\text{V}$ to $\pm 20\text{V}$	●	108	128		108	128		dB
	Input Voltage Range		●	± 13.5			± 13.5			V
V_{OUT}	Output Voltage Swing	$R_L = 10\text{k}\Omega$	●	± 13	± 14		± 13	± 14		V
I_S	Supply Current		●	400	800		400	800		μA

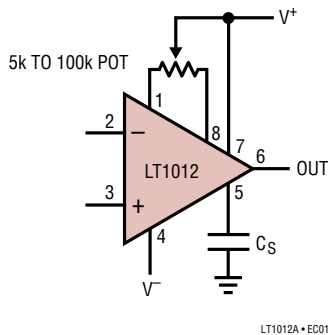
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 3: These specifications apply for $V_{MIN} \leq V_S \leq \pm 20\text{V}$ and $-13.5\text{V} \leq V_{CM} \leq 13.5\text{V}$ (for $V_S = \pm 15\text{V}$). $V_{MIN} = \pm 1.2\text{V}$ at 25°C , $\pm 1.3\text{V}$ from 0°C to 70°C , $\pm 1.5\text{V}$ from -55°C to 125°C .

Note 4: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 5: This parameter is tested on a sample basis only.



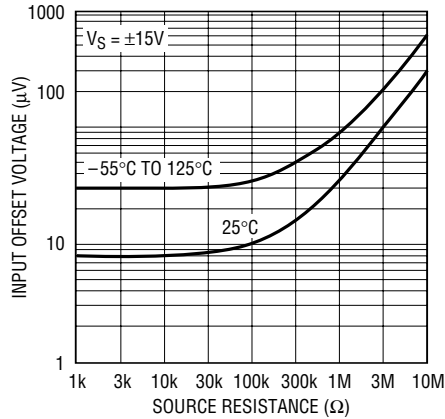
Optional Offset Nulling and Overcompensation Circuits

Input offset voltage can be adjusted over a $\pm 800\mu\text{V}$ range with a 5k to 100k potentiometer.

The LT1012 is internally compensated for unity gain stability. The overcompensation capacitor, C_S , can be used to improve capacitive load handling capability, to narrow noise bandwidth, or to stabilize circuits with gain in the feedback loop.

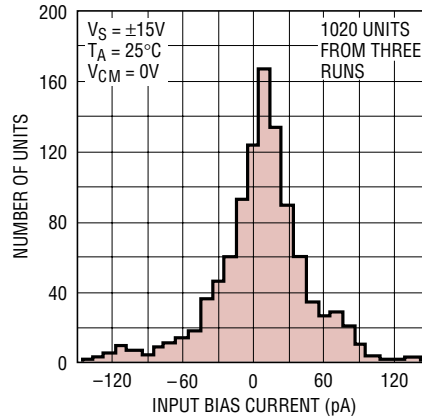
TYPICAL PERFORMANCE CHARACTERISTICS

Offset Voltage vs Source Resistance (Balanced or Unbalanced)



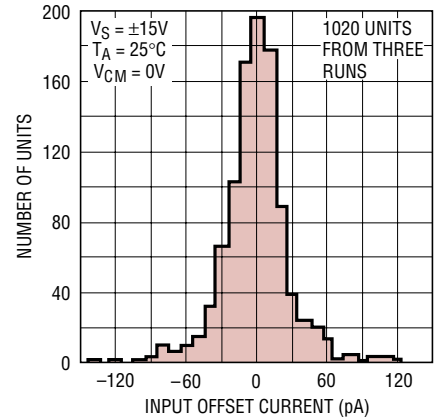
LT1012A • TPC01

Typical Distribution of Input Bias Current



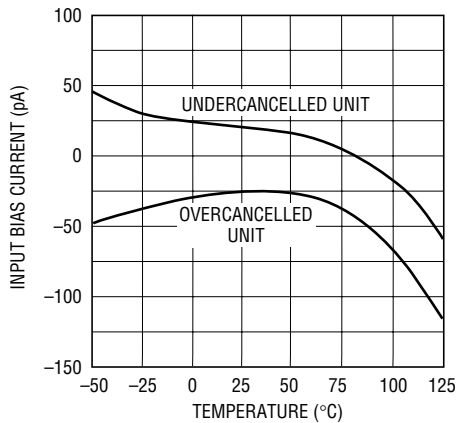
LT1012A • TPC02

Typical Distribution of Input Offset Current



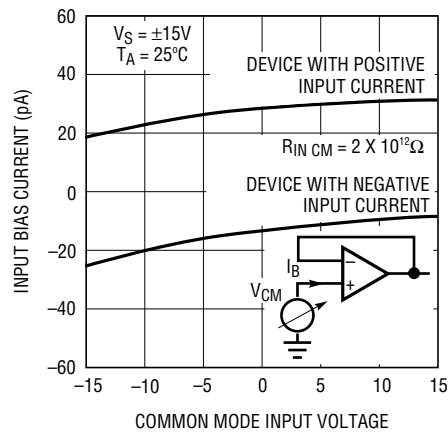
LT1012A • TPC03

Input Bias Current vs Temperature



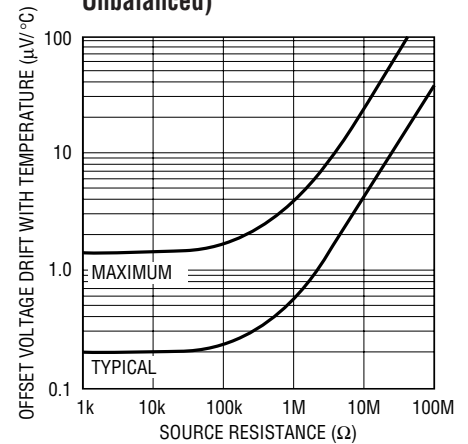
LT1012A • TPC04

Input Bias Current Over Common Mode Range



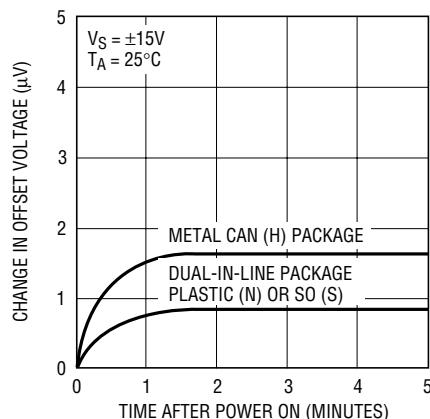
LT1012A • TPC5

Offset Voltage Drift vs Source Resistance (Balanced or Unbalanced)



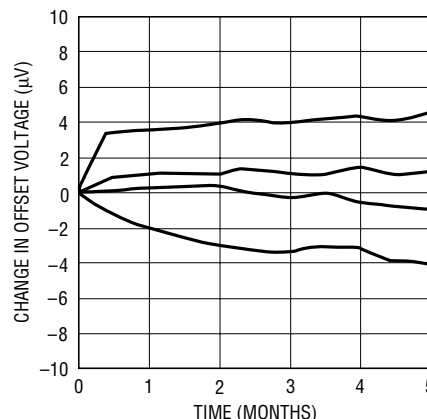
LT1012 • TPC06

Warm-Up Drift



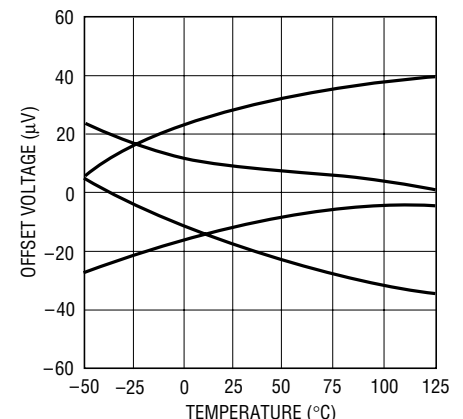
LT1012A • TPC07

Long Term Stability of Four Representative Units



LT1012A • TPC08

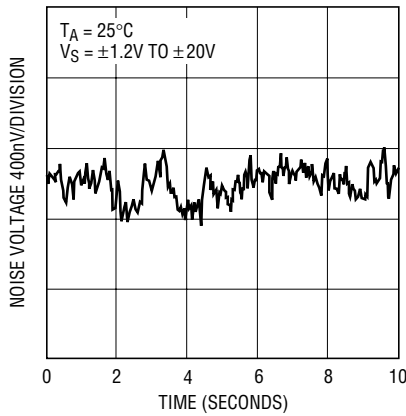
Offset Voltage Drift with Temperature of Four Representative Units



LT1012A • TPC09

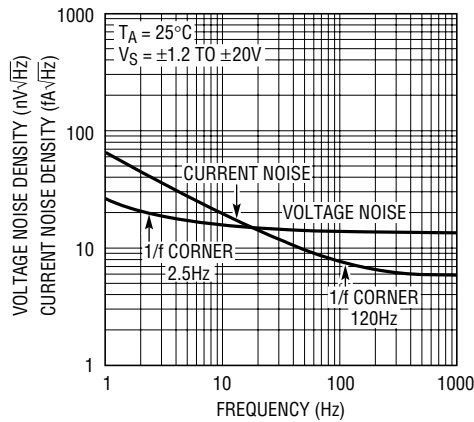
TYPICAL PERFORMANCE CHARACTERISTICS

0.1Hz to 10Hz Noise



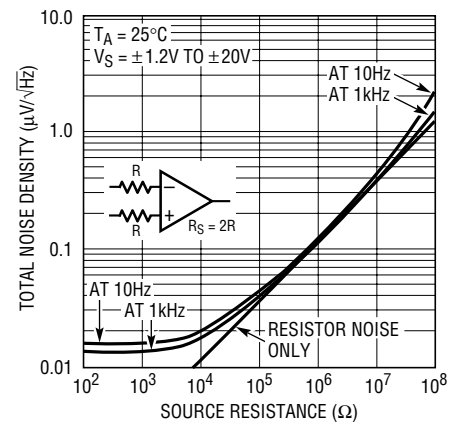
LT1012A • TPC10

Noise Spectrum



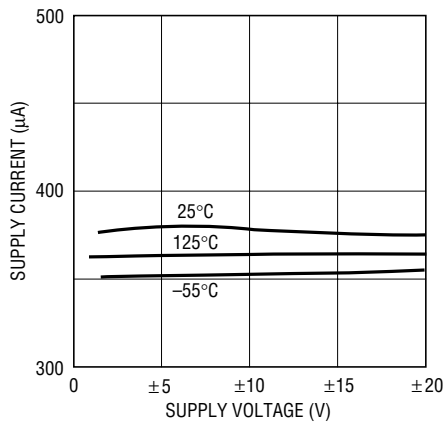
LT1012A • TPC11

Total Noise vs Source Resistance



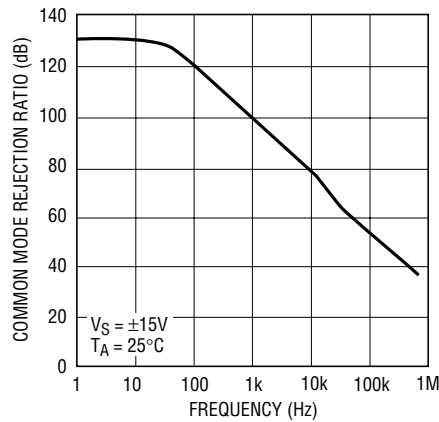
LT1012A • TPC12

Supply Current vs Supply Voltage



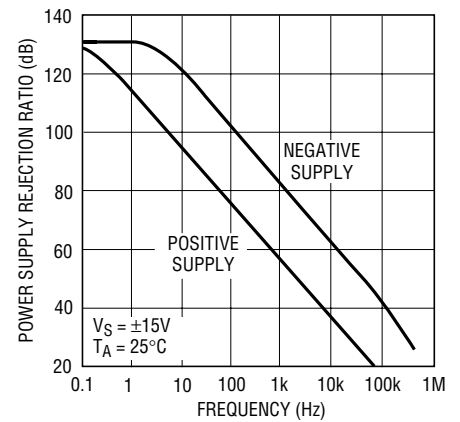
LT1012A • TPC13

Common Mode Rejection vs Frequency



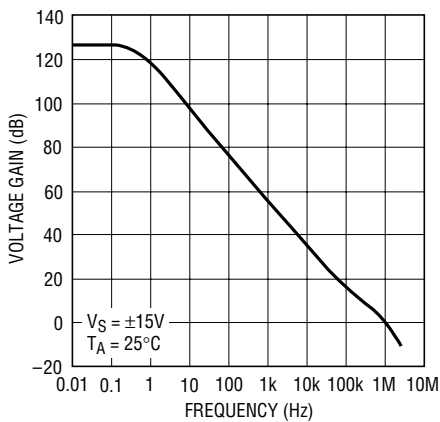
LT1012A • TPC14

Power Supply Rejection vs Frequency



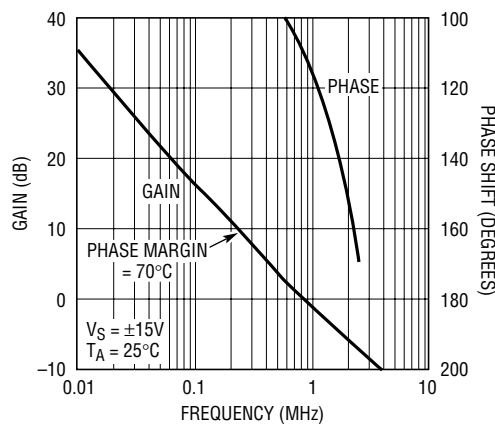
LT1012A • TPC15

Voltage Gain vs Frequency



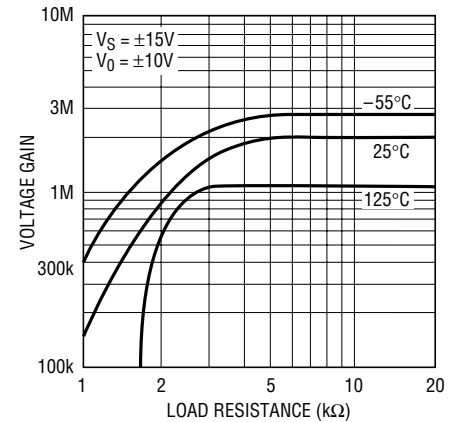
LT1012A • TPC16

Gain, Phase Shift vs Frequency



LT1012A • TPC17

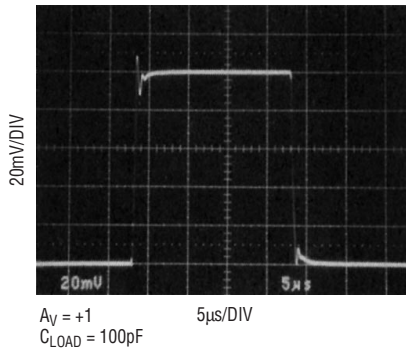
Voltage Gain vs Load Resistance



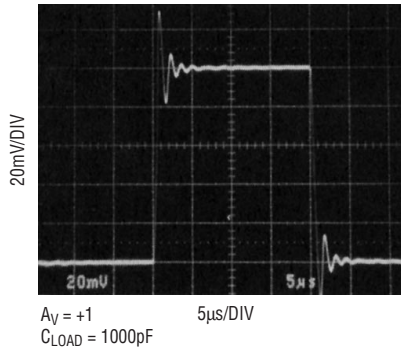
LT1012A • TPC18

TYPICAL PERFORMANCE CHARACTERISTICS

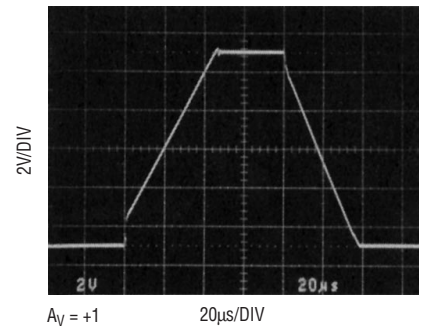
Small-Signal Transient Response



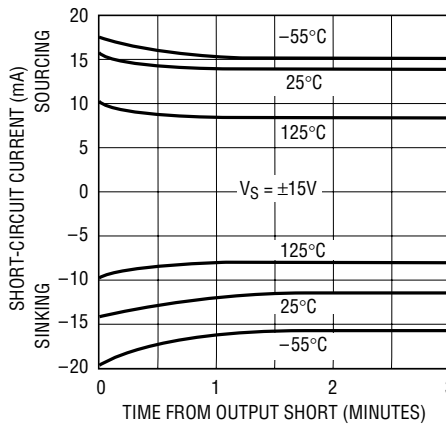
Small-Signal Transient Response



Large-Signal Transient Response

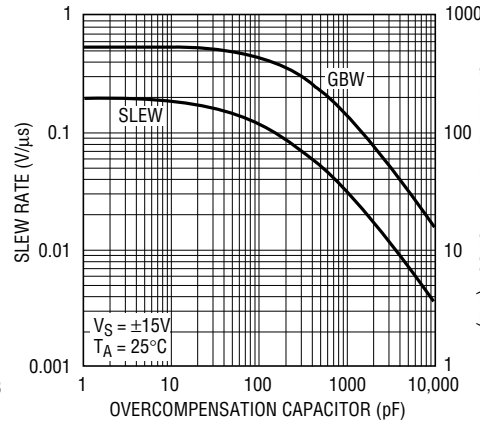


Output Short-Circuit Current vs Time



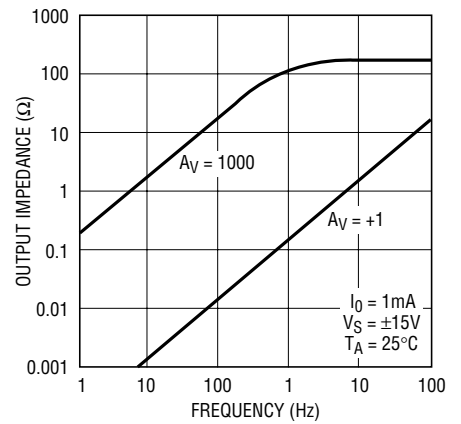
LT1012A • TPC19

Slew Rate, Gain Bandwidth Product vs Overcompensation Capacitor



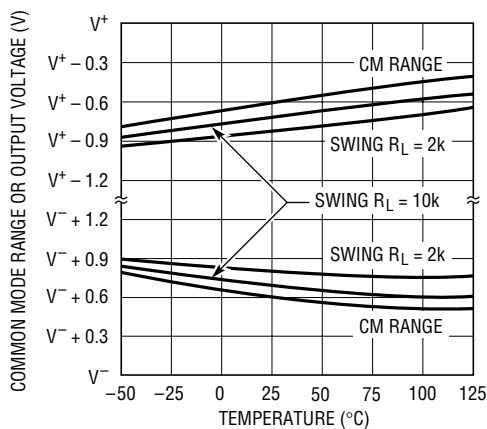
LT1012A • TPC20

Closed-Loop Output Impedance



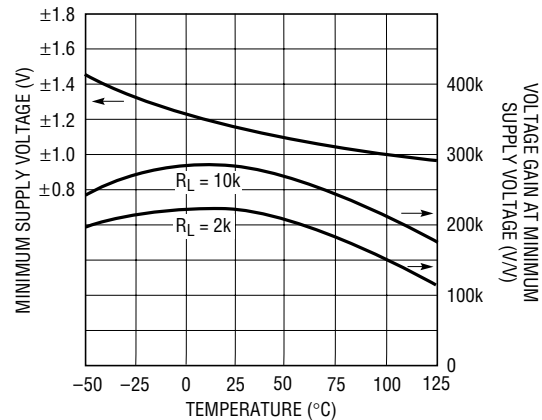
LT1012A • TPC21

Common Mode Range and Voltage Swing at Minimum Supply Voltage



LT1012A • TPC22

Minimum Supply Voltage, Voltage Gain at V_{MIN}



LT1012A • TPC23

APPLICATIONS INFORMATION

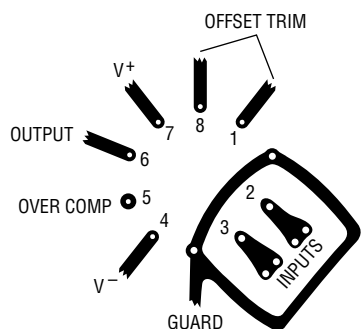
The LT1012 may be inserted directly into OP-07, LM11, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1012 can also be used in 741, LF411, LF156 or OP-15 applications provided that the nulling circuitry is removed.

Although the OP-97 is a copy of the LT1012, the LT1012 directly replaces and upgrades OP-97 applications. The LT1012C and D have lower offset voltage and drift than the OP-97F. The LT1012A has lower supply current than the OP-97A/E. In addition, all LT1012 grades guarantee operation at $\pm 1.2\text{V}$ supplies.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1012, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input at Pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the offset trim terminals can affect offset voltage and drift with temperature.



LT1012A * A101

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Noise Testing

For application information on noise testing and calculations, please see the LT1008 data sheet.

Frequency Compensation

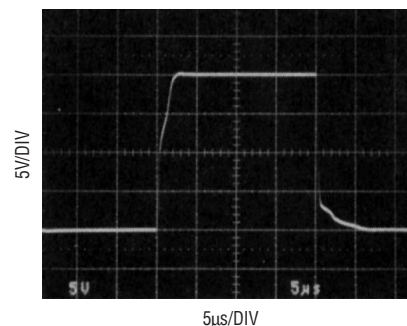
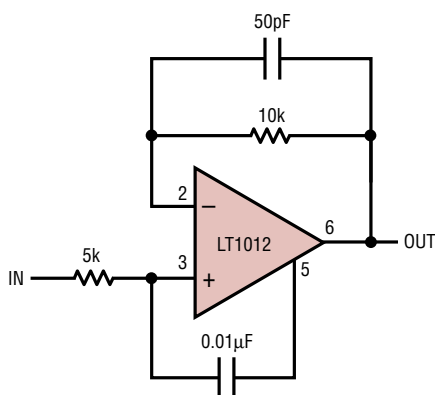
The LT1012 can be overcompensated to improve capacitive load handling capability or to narrow noise bandwidth. In many applications, the feedback loop around the amplifier has gain (e.g. logarithmic amplifiers); overcompensation can stabilize these circuits with a single capacitor.

The availability of the compensation terminal permits the use of feedforward frequency compensation to enhance slew rate. The voltage follower feedforward scheme bypasses the amplifier's gain stages and slews at nearly $10\text{V}/\mu\text{s}$.

The inputs of the LT1012 are protected with back-to-back diodes. Current limiting resistors are not used, because the leakage of these resistors would prevent the realization of picoampere level bias currents at elevated temperatures. In the voltage follower configuration, when the input is driven by a fast, large signal pulse ($>1\text{V}$), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short-circuit protection will flow through the diodes.

The use of a feedback resistor, as shown in the voltage follower feedforward diagram, is recommended because this resistor keeps the current below the short-circuit limit, resulting in faster recovery and settling of the output.

Pulse Response of Feedforward Compensation



IT1012A • AI02

LT1012A • AI03

TYPICAL APPLICATIONS

The circuit diagram illustrates a precision current-to-voltage converter. It features an LT1012 operational amplifier configured as a transimpedance amplifier. The non-inverting input (pin 3) is grounded, while the inverting input (pin 2) is connected to the 'CURRENT INPUT' through a 10kΩ resistor. A feedback path consisting of a 10kΩ resistor and a 0.1μF capacitor connects the output (pin 6) back to the inverting input. The op-amp is powered by a 15V supply (pin 7) and a -15V supply (pin 4). The output of the op-amp (pin 6) is connected to the base of a PNP transistor Q1. The emitter of Q1 is grounded, and its collector is connected to the base of an NPN transistor Q2. The emitter of Q2 is grounded, and its collector is connected to the base of another PNP transistor Q3. The emitter of Q3 is connected to a 15V supply through a 10kΩ resistor. The collector of Q3 is connected to a 100μA meter and a 2kΩ resistor R1. The wiper of R1 is connected to a 1.2kΩ resistor, which is in series with a 549Ω resistor. This 549Ω resistor is followed by a series of seven more 549Ω resistors, each connected to a current range terminal: 100pA, 1nA, 10nA, 100nA, 1μA, 10μA, and 100μA. The final 100μA terminal is connected to the 15V supply. A diode LT1004C is connected in parallel with the 100μA terminal to protect the meter. The entire circuit is powered by a 15V supply and a -15V supply. The RCA CA3146 transistor array provides the transistors Q1, Q2, Q3, and Q4, with pin 13 connected to ground.

Q1, Q2, Q3, Q4, RCA CA3146 TRANSISTOR ARRAY.
CALIBRATION: ADJUST R1 FOR FULL-SCALE DEFLECTION WITH 1μA INPUT CURRENT

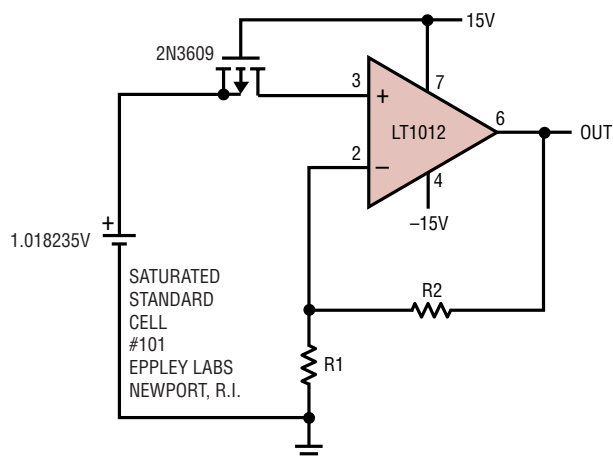
Q1, Q2, Q3, Q4, RCA CA3146 TRANSISTOR ARRAY.
CALIBRATION: ADJUST R1 FOR FULL-SCALE
DEFLECTION WITH 1 μ A INPUT CURRENT

AMP/MEETER MEASURES CURRENTS FROM 100pA TO 100μA WITHOUT THE USE OF EXPENSIVE HIGH VALUE RESISTORS. ACCURACY AT 100μA IS LIMITED BY THE OFFSET VOLTAGE BETWEEN Q1 AND Q2 AND, AT 100pA, BY THE INVERTING BIAS CURRENT OF THE LT1012

IT1012A • TA03

TYPICAL APPLICATIONS

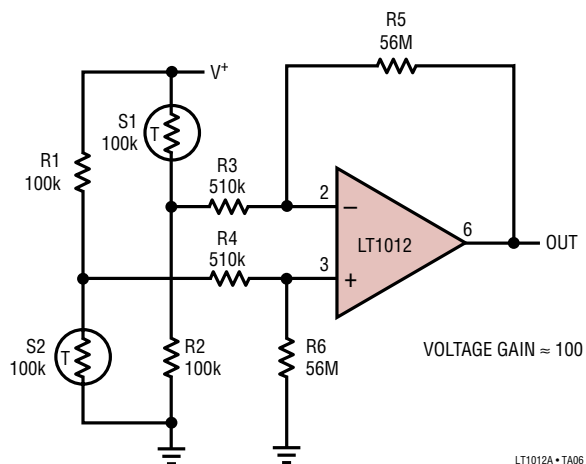
Saturated Standard Cell Amplifier



THE TYPICAL 30pA BIAS CURRENT OF THE LT1012 WILL DEGRADE THE STANDARD CELL BY ONLY 1ppm/YEAR. NOISE IS A FRACTION OF A ppm. UNPROTECTED GATE MOSFET ISOLATES STANDARD CELL ON POWER DOWN

LT1012A • TA05

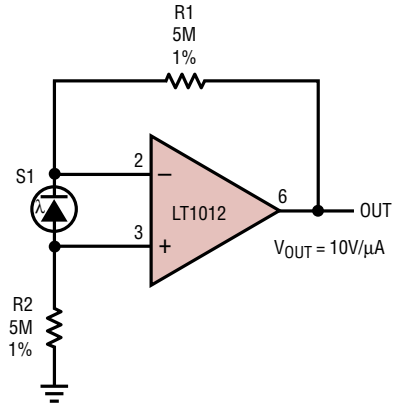
Amplifier for Bridge Transducers



LT1012A • TA06

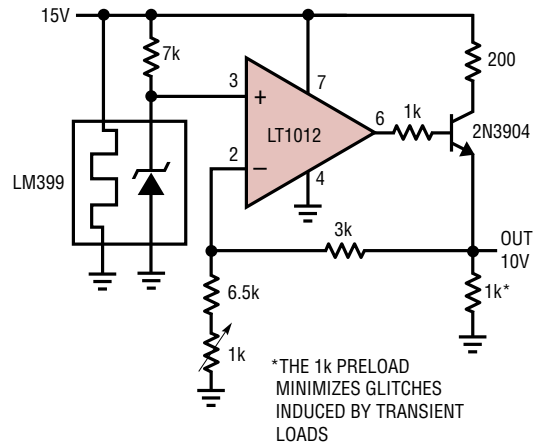
TYPICAL APPLICATIONS

Amplifier for Photodiode Sensor



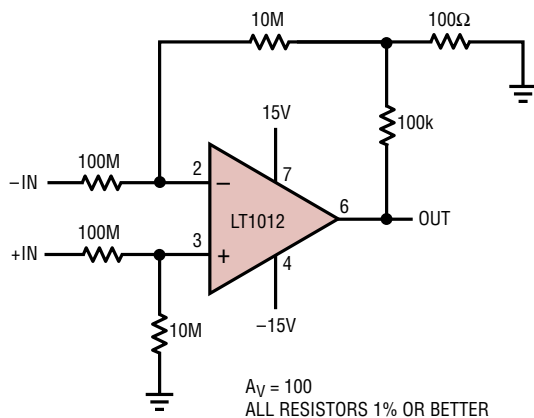
LT1012A • TA07

Buffered Reference for A-to-D Converters



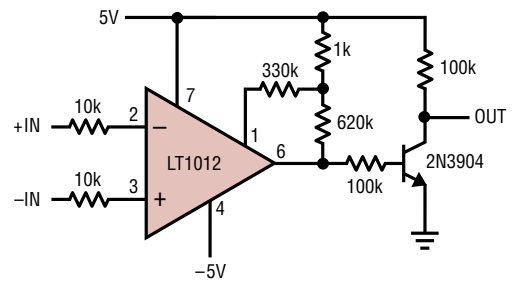
LT1012A • TA08

Instrumentation Amplifier with $\pm 100V$ Common Mode Range



LT1012A • TA09

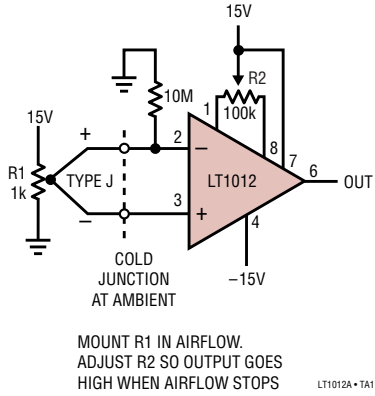
Low Power Comparator with $< 10\mu V$ Hysteresis



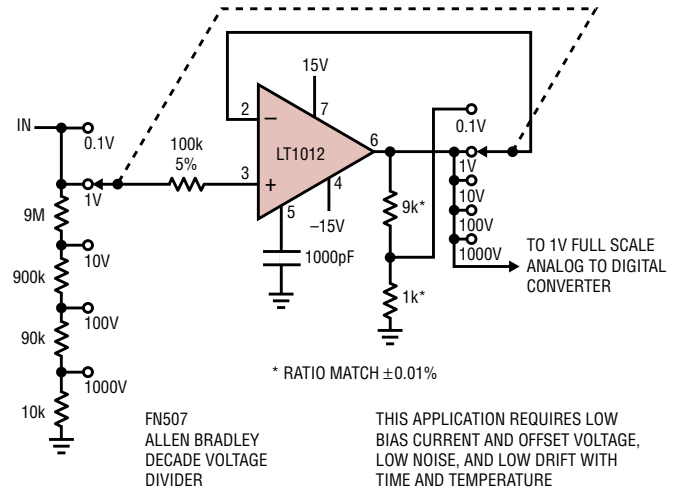
LT1012A • TA10

TYPICAL APPLICATIONS

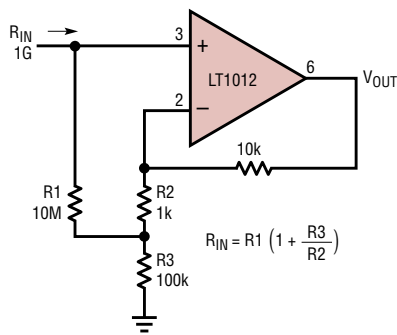
Air Flow Detector



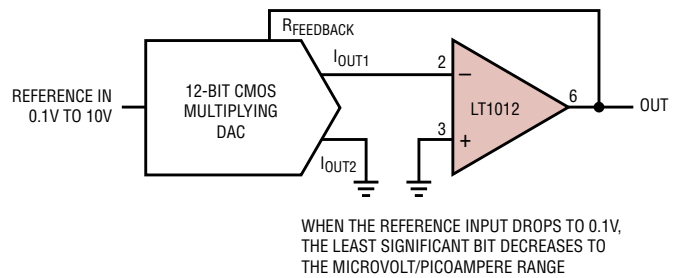
Input Amplifier for 4.5 Digit Voltmeter



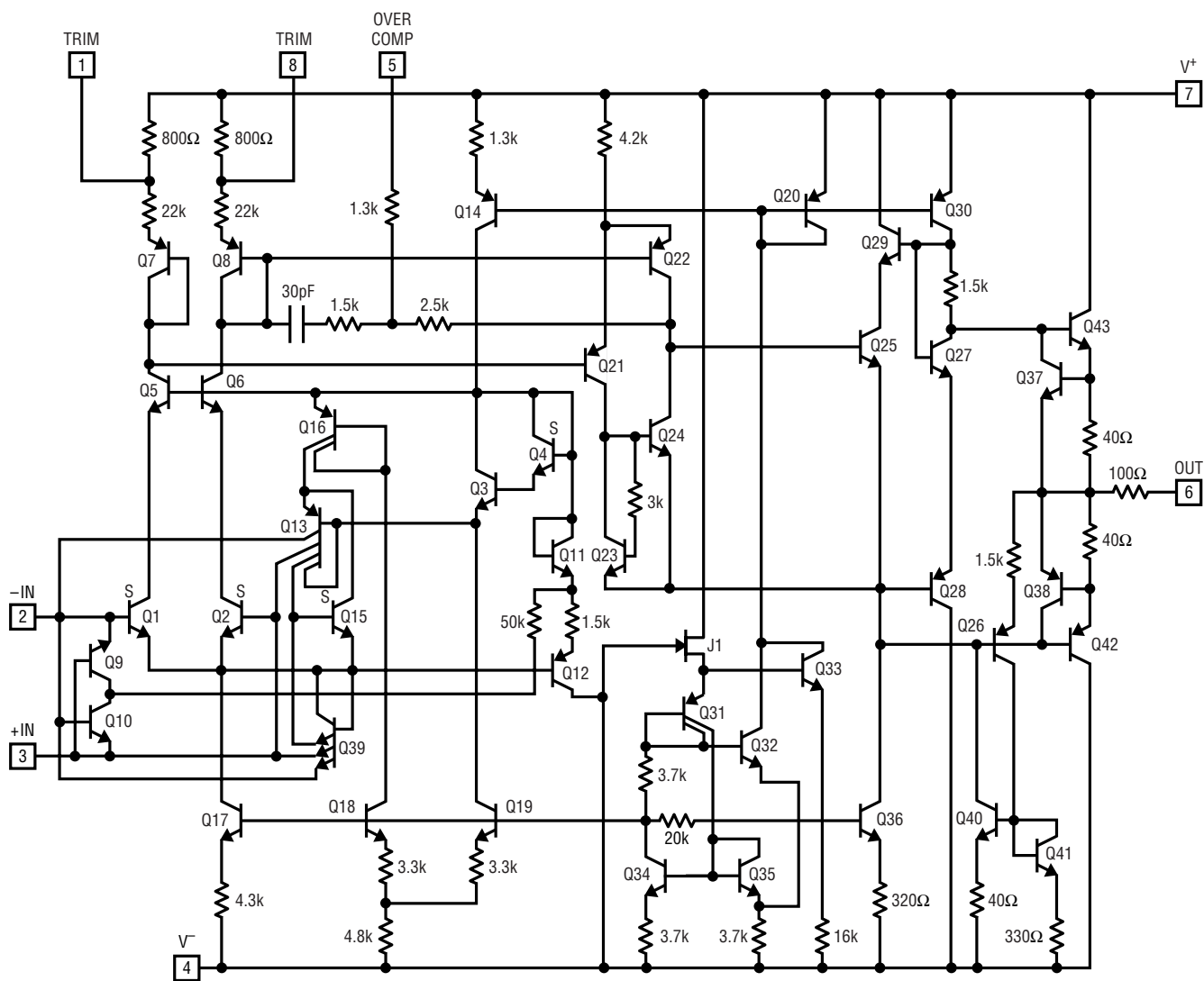
Resistor Multiplier



“No Trims” 12-Bit Multiplying DAC Output Amplifier

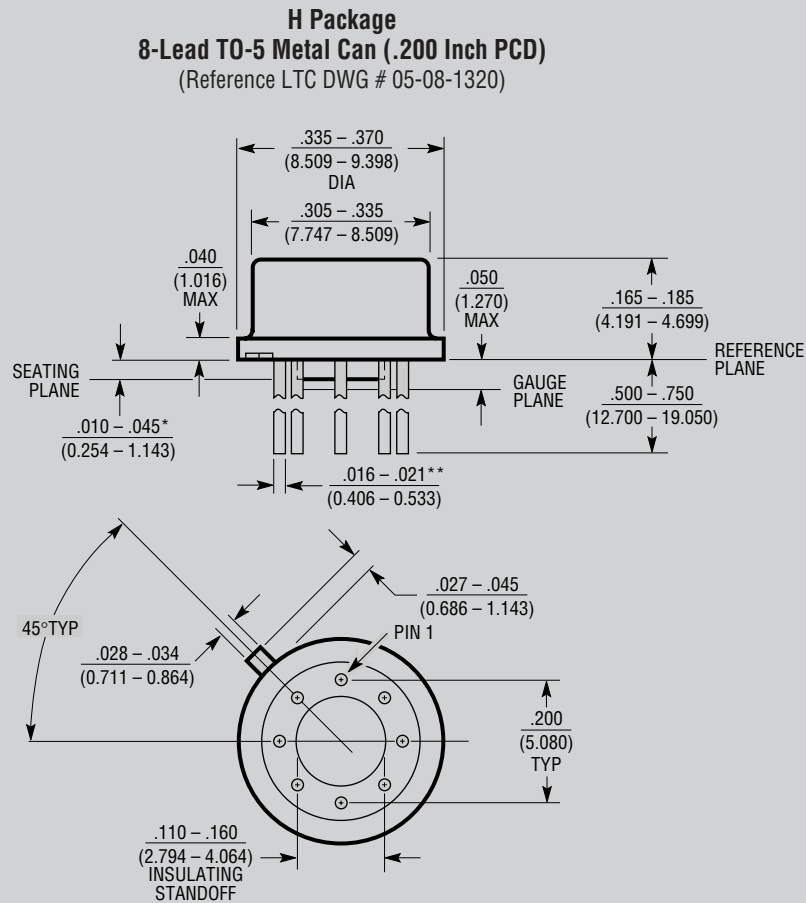


SCHEMATIC DIAGRAM



LT1012A • SD01

PACKAGE DESCRIPTION



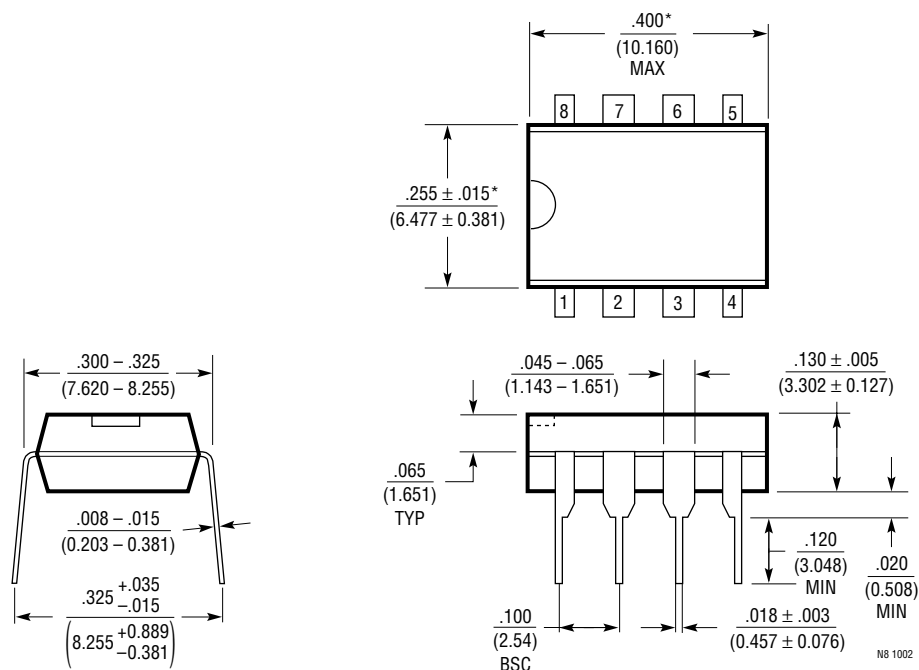
*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{.016 - .024}{(0.406 - 0.610)}$ H8(TO-5) 0.200 PCD 0801

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
 (Reference LTC DWG # 05-08-1510)

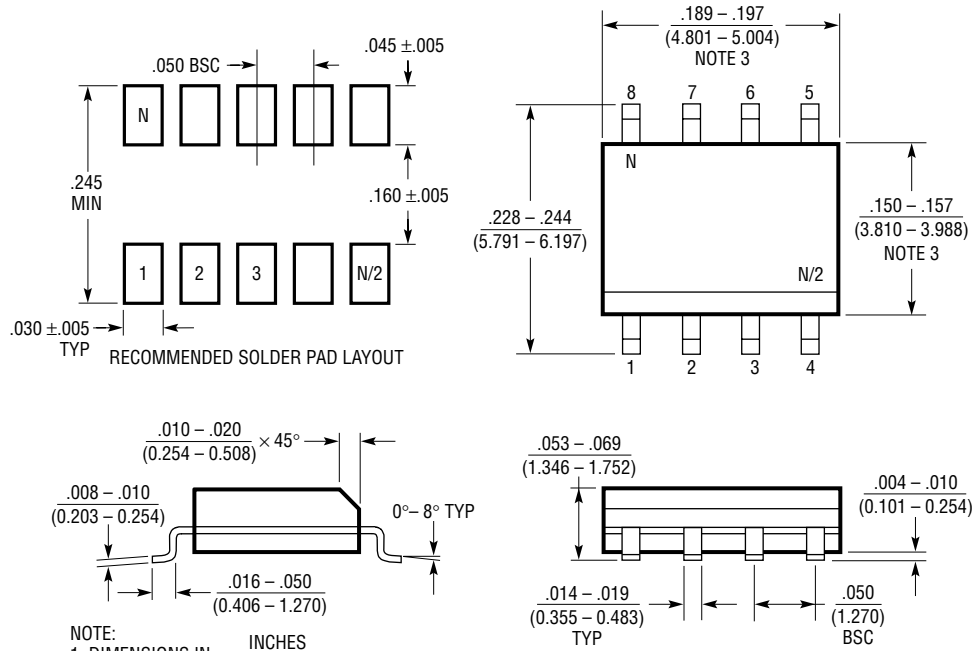


NOTE:
 1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)

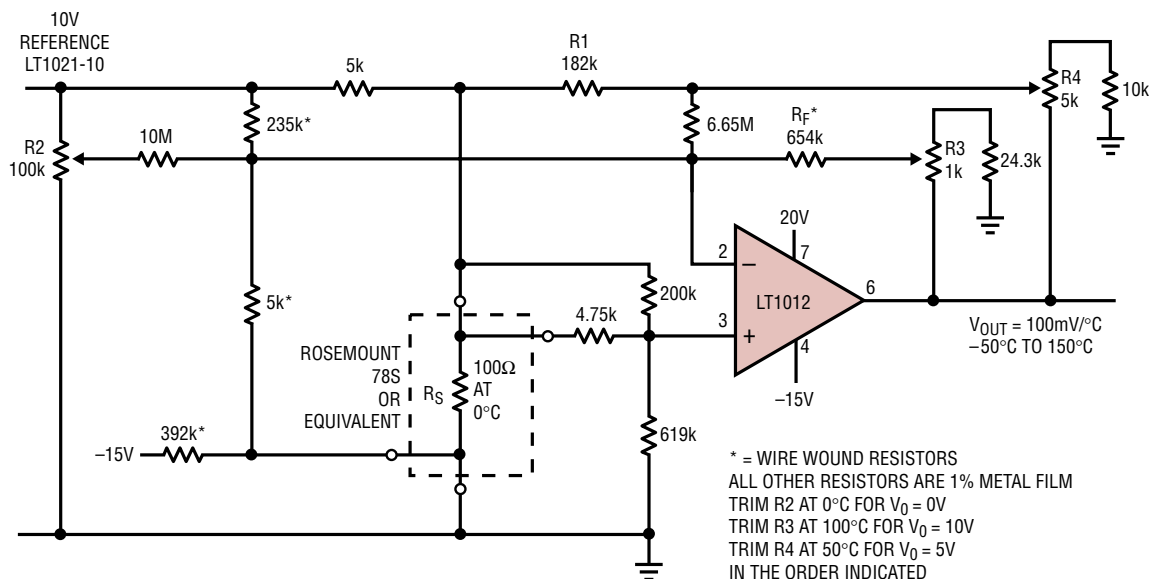


- NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
 2. DRAWING NOT TO SCALE
 3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0502

TYPICAL APPLICATION

Kelvin-Sensed Platinum Temperature Sensor Amplifier



POSITIVE FEEDBACK (R1) LINEARIZES THE
INHERENT PARABOLIC NONLINEARITY OF
THE PLATINUM SENSOR AND REDUCES
ERRORS FROM 1.2°C TO 0.004°C OVER
THE -50°C TO 150°C RANGE

LT1012A • TA04