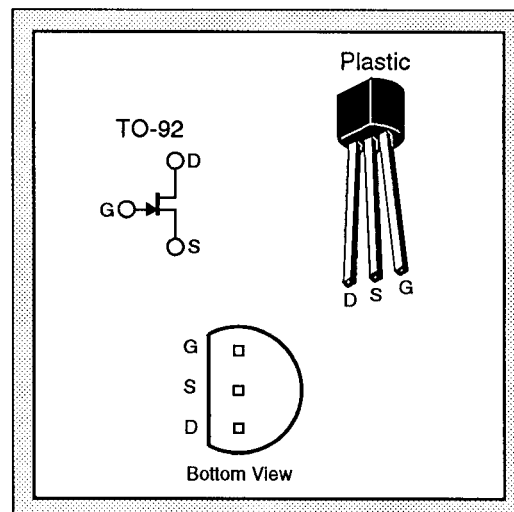


LINEAR SYSTEMS

Linear Integrated Systems

J108, J109, J110, J110A LOW NOISE N-CHANNEL JFET SWITCH

FEATURES	
LOW $r_{DS(on)}$	$< 8\Omega$ (J108)
LOW NOISE e_n	$= 6nV/\sqrt{Hz}$ @ 10Hz TYPICAL
HIGH SPEED $t_{d(on)} + T_r$	$= 5nS$ TYPICAL
ABSOLUTE MAXIMUM RATINGS	
@ 25°C (unless otherwise noted)	
Reverse Gate to Drain or Source	-25V
Gate Forward Current	50mA
Total Device Dissipation @ 25°C	360mW
Storage Temperature	-65°C to +200°C



ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	J108			J109			J110			UNITS	CONDITIONS			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX					
I _{GSS}	Gate Reverse Current	--	--	-3	--	--	-3	--	--	-3	nA	V _{DS} =0	V _{GS} =-15V	(NOTE 1)	
V _{GS(off)}	Gate-Source Cutoff Voltage	-3	--	-10	-2	--	-6	-0.5	--	-4	V	V _{DS} =5V	I _D =1μA		
BV _{GSS}	Gate-Source Breakdown Voltage	-25	--	--	-25	--	--	-25	--	--		V _{DS} =0V	I _G =-1μA		
I _{DSS}	Drain Saturation Current	80	--	--	40	--	--	10	--	--	mA	V _{DS} =15V	V _{GS} =0V	(NOTE 2)	
I _{D(off)}	Drain Cutoff Current	--	--	3	--	--	3	--	--	3	nA	V _{DS} =5V	V _{GS} =-10V		
r _{DS(on)}	Drain-Source ON Resistance	--	--	8	--	--	12	--	--	18	Ω	V _{DS} ≤0.1V	V _{GS} =0V		
	J110A						--	--	25						
C _{dg(off)}	Drain-Gate OFF Capacitance	--	--	15	--	--	15	--	--	15	pF	V _{DS} =0V	V _{GS} =-10V	f=1MHz	
C _{sg(off)}	Source-Gate OFF Capacitance	--	--	15	--	--	15	--	--	15					
C _{dg(on)} + C _{sg(on)}	Drain-Gate Plus Source-Gate ON Capacitance	--	--	85	--	--	85	--	--	85		V _{DS} =V _{GS} =0			
t _{d(on)}	Turn ON Delay Time	--	4	--	--	4	--	--	4	--	ns	Switching Time Test Conditions			
t _r	Rise Time	--	1	--	--	1	--	--	1	--			J108	J109	J110
t _{d(off)}	Turn OFF Delay Time	--	6	--	--	6	--	--	6	--		V _{DD}	1.5V	1.5V	1.5V
t _f	Fall Time	--	30	--	--	30	--	--	30	--		V _{GS(off)}	-12V	-7V	-5V
												R _L	150Ω	150Ω	150Ω

NOTE 1: Approximately doubles for every 10°C increase in T_A .

NOTE 2: Pulse test duration 300 μs ; duty cycle $\leq 3\%$.

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