

LINEAR SYSTEMS

Linear Integrated Systems

3N190, 3N191

MONOLITHIC DUAL
P-CHANNEL ENHANCEMENT MODE
MOSFET

FEATURES	
VERY HIGH INPUT IMPEDANCE	
HIGH GATE BREAKDOWN	
ULTRA LOW LEAKAGE	
LOW CAPACITANCE	
MONOLITHIC DUAL	
ABSOLUTE MAXIMUM RATINGS (NOTE 1)	
(T _A = 25°C unless otherwise noted)	
Drain-Source or Drain-Gate Voltage	-40V (NOTE 2)
Transient G-S Voltages (NOTES 2 and 3)	±125V
Gate-Gate Voltage	±80V
Drain Current (NOTE 2)	50mA
Storage Temperature	-65°C to +200°C
Power Dissipation	375 mW

DIE MAP

TO-99
Bottom View

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise specified)

SYMBOL	CHARACTERISTICS	LIMITS		UNITS	CONDITIONS
		MIN.	MAX.		
I _{GSSF}	Gate Forward Leakage Current	--	10	pA	V _{GS} = 40 V
I _{GSSR}	Gate Reverse Leakage Current	--	-10	pA	V _{GS} = -40 V
I _{DSS}	Drain to Source Leakage Current	--	-200		V _{DS} = -15 V
I _{SDS}	Source-Drain Current	--	-400		V _{SD} = -20V V _{DB} = 0
I _{D(on)}	ON Drain Current	-5	-30	mA	V _{DS} = -15 V V _{GS} = -10 V
r _{DS(on)}	Drain-Source ON Resistance	--	300	ohms	V _{DS} = -20 V I _D = -100μA
V _{DS(on)}	Drain-Source ON Voltage	--	2.0	V	V _{GS} = -10 V I _D = 10 mA
g _{fs}	Forward Transconductance	1500	4000	μs	V _{DS} = -15V I _D = 10mA
g _{os}	Output Admittance	--	300		f=1KHz
C _{iss}	Input Capacitance	--	4.5	pF	f=1MHz
C _{rss}	Reverse Transfer Capacitance	--	1.0		
C _{oss}	Output Capacitance Input Shorted	--	3.0		
MATCHING CHARACTERISTICS 3N190					
Y _{fs1} /Y _{fs2}	Forward Transconductance Ratio	0.85	1.0		V _{DS} = -15V I _D = -500 μA f=1KHz
V _{GS1-2}	Offset Voltage	--	100	mV	V _{DS} = -15V I _D = -500 μA
V _{GS1-2}	Drift vs. Temperature	--	100	μV/°C	V _{DS} = -15V I _D = -500 μA

ΔT

T_A = -55°C to +125°C

NOTES: 1. These ratings are limiting values above which the serviceability of the semiconductor may be impaired.

2. Per Transistor.

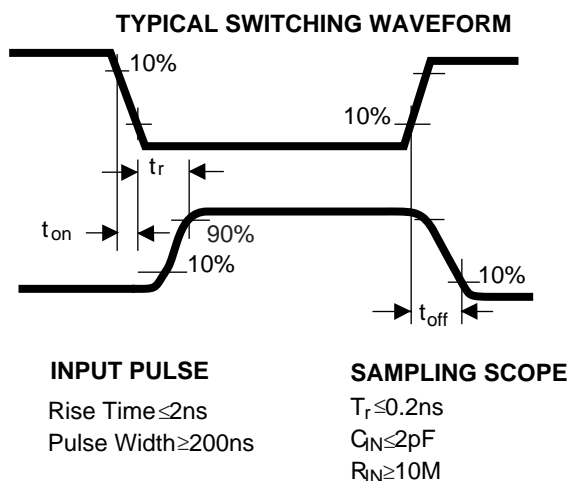
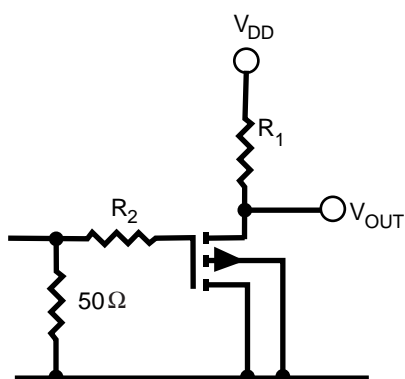
3. Approximately doubles for every 10°C increase in T_A.

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MATCHING CHARACTERISTICS 3N165

SYMBOL	CHARACTERISTICS	LIMITS		UNITS	CONDITIONS
		MIN.	MAX.		
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0		$V_{DS} = -15\text{ V}$ $I_D = -500\text{ }\mu\text{A}$ $f=1\text{ kHz}$
V_{GS1-2}	Gate Source Threshold Voltage Differential	--	100	mV	$V_{DS} = -15\text{ V}$ $I_D = -500\text{ }\mu\text{A}$
$\Delta V_{GS1-2}/\Delta T$	Gate Source Threshold Voltage Differential Change with Temperature	--	100	$\mu\text{V}/^\circ\text{C}$	$V_{DS} = -15\text{ V}$ $I_A = -500\text{ }\mu\text{A}$ $T_A = -55^\circ\text{C to } +25^\circ\text{C}$



Switching Times Test Circuit

NOTES:

1. MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow these procedures:
To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used. Avoid unnecessary handling. Pick up devices by the case instead of the leads. Do not insert or remove devices from circuits with the power on, as transient voltages may cause permanent damage to the devices.
2. Per transistor.
3. Devices must not be tested at $\pm 125\text{ V}$ more than once, nor for longer than 300ms.
4. For design reference only, not 100% tested.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.