

DEVICE
PERFORMANCE
SPECIFICATION

KODAK KAI-1020

Image Sensor

1000 (H) x 1000 (V)
Interline Transfer
Progressive Scan CCD

October 1, 2002
Revision 4

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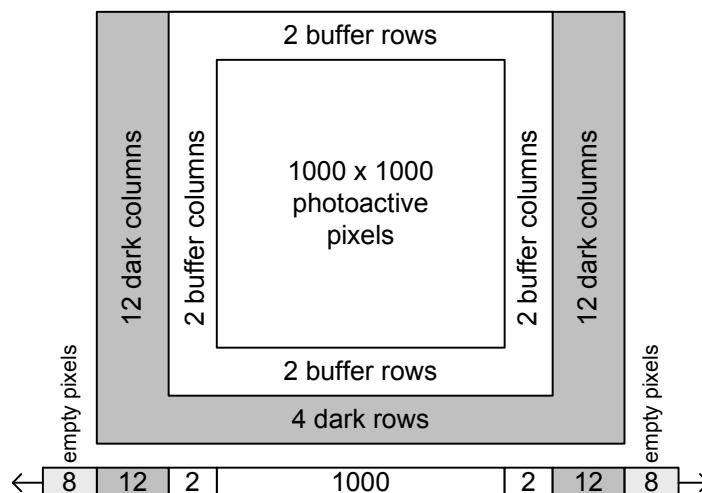
Introduction

Description

The KAI-1020 is a one megapixel interline CCD image sensor with integrated clock drivers and correlated double sampling. The progressive scan architecture and global electronic shutter provides excellent image quality for full motion video and still image capture. The integrated clock drivers allow easy use with CMOS logic timing generators.

Features

- 1 million pixels, 1000 (H) by 1000 (V)
- 10 bits dynamic range at 40 MHz
- Large 7.4 μm square pixels for high sensitivity
- Progressive scan (non-interlaced)
- Integrated vertical clock drivers
- Integrated correlated double sampling (CDS) up to 40 MHz
- Integrated electronic shutter driver
- Reversible HCCD capable of 40MHz operation
- All timing inputs 0 to 5 Volts
- Single or dual video output operation
- Progressive scan or interlaced
- 30 Frames per second progressive scan, one output
- 48 Frames per second progressive scan, two outputs
- 49 Frames per second interlaced, one output
- Fast dump gate for high speed sub-window readout
- Antiblooming protection



KAI-1020 pixel array with dark reference.

Performance Specifications

Optical Specifications

Symbol	Description	Min.	Nom.	Max.	Units	Notes
QE_{max}	Peak Quantum Efficiency	42	45		%	1
λQE	Peak Quantum Efficiency Wavelength		490		nm	1
θQE_h	Microlens Acceptance Angle (horizontal)	± 12	± 13		degrees	2
θQE_v	Microlens Acceptance Angle (vertical)	± 25	± 30		degrees	2
$QE(540)$	Quantum Efficiency at 540nm	38	40		%	1
PNU	Photoresponse nonuniformity		5		%	
NL	Maximum Photoresponse Nonlinearity		2		%	3, 4
ΔG	Maximum Gain Difference Between Outputs		10		%	3, 4
ΔNL	Maximum Signal Error caused by Nonlinearity Differences		1		%	3, 4

CCD Specifications

Symbol	Description	Min.	Nom.	Max.	Units	Notes
Vne	Vertical CCD Charge Capacity	54	60		ke^-	
Hne	Horizontal CCD Charge Capacity	110	120		ke^-	
Pne	Photodiode Charge Capacity	38	42		ke^-	5
I_d	Dark Current		0.2	0.5	nA/cm^2	6
Lag	Image Lag		< 10	50	e^-	7
Xab	Antiblooming factor	100	300			1, 8, 9, 10, 11
Smr	Vertical Smear		-75	-72	dB	1, 8, 9

CDS Output Specifications

Symbol	Description	Nominal	Units	Notes
P_d	Power Dissipation	213	mW	12
F_{-3dB}	Bandwidth	140	MHz	12
C_L	Max Off-chip Load	10	pF	13
A_v	Gain	0.70		12
$\Delta V/\Delta N$	Sensitivity	13	$\mu V/e^-$	12
R	Output Impedance	160	Ω	12
Vsat	Saturation Voltage	500	mV	5, 12

General - Monochrome

Symbol	Description	Nominal	Units	Notes
n_{e-T}	Total Camera Noise	42	e^- rms	6, 14
DR	Dynamic Range	60	dB	15

General - Color

Symbol	Description	Nominal	Units	Notes
n_{e-T}	Total Camera Noise	50	e^- rms	6, 14
DR	Dynamic Range	58	dB	15

Power

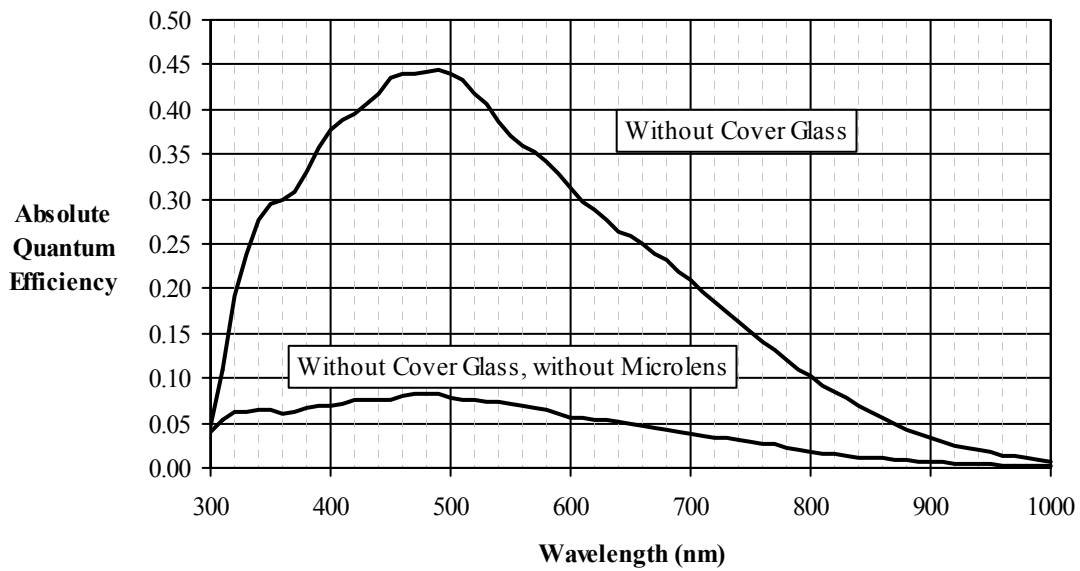
Description	Nominal	Units	Notes
Single Channel CDS	213	mW	12
VCCD clock driver	71	mW	16
Electronic shutter driver	1.1	mW	
HCCD	122	mW	16, 17
Total Power	407	mW	12, 16

Notes

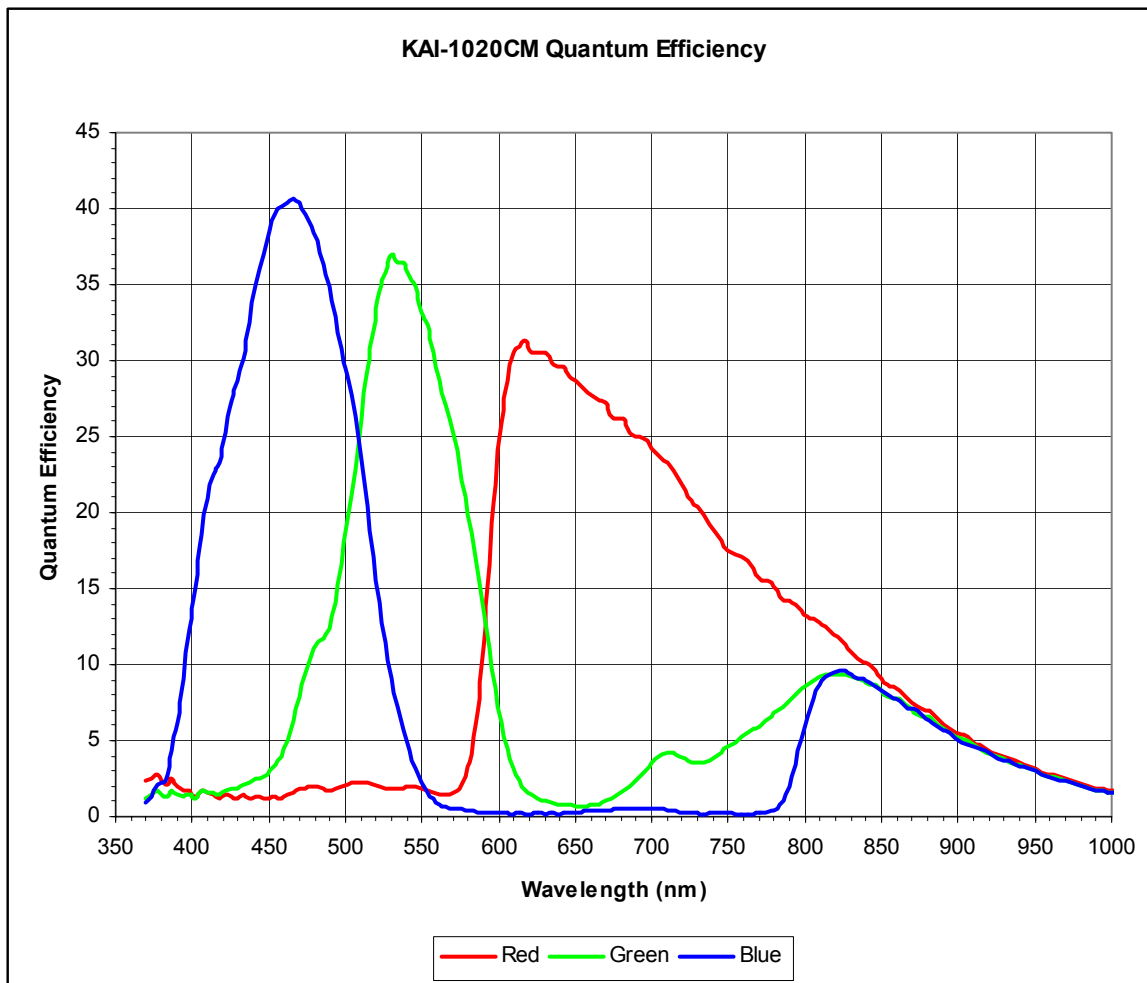
1. Measured with F/4 imaging optics.
2. Value is the angular range of incident light for which the quantum efficiency is at least 50% of QE_{max} at a wavelength of λ_{QE} . Angles are measured with respect to the sensor surface normal in a plane parallel to the horizontal axis (θ_{QEh}) or in a plane parallel to the vertical axis (θ_{QEv}).
3. Value is over the range of 10% to 90% of photodiode saturation.
4. Value is for the sensor operated without binning.
5. This value depends on the substrate voltage setting. Higher photodiode saturation charge capacities will lower the antiblooming specification. Substrate voltage will be specified with each part for 42 ke⁻.
6. Measured at 40°C, 40 MHz HCCD frequency.
7. This is the first field decay lag at 70% saturation. Measured by strobe illumination of the device at 70% of photodiode saturation, and then measuring the subsequent frame's average pixel output in the dark.
8. Measured with a spot size of 100 vertical pixels, no electronic shutter.
9. Measured with green light (500 nm to 580 nm).
10. A blooming condition is defined as when the spot size doubles in size.
11. Antiblooming factor is the light intensity which causes blooming divided by the light intensity which first saturates the photodiodes.
12. Single output power, 3mA load
13. With total output load capacitance of $C_L = 10$ pF between the outputs and AC ground.
14. Includes system electronics noise, dark pattern noise and dark current shot noise at 40 MHz. Total noise measured on the KAI-1020 evaluation board.
15. Uses $20\text{LOG}(P_{Ne}/n_{e,T})$
16. At 30 frames/sec, single output
17. This includes the power of the external HCCD clock driver.

Quantum Efficiency Data

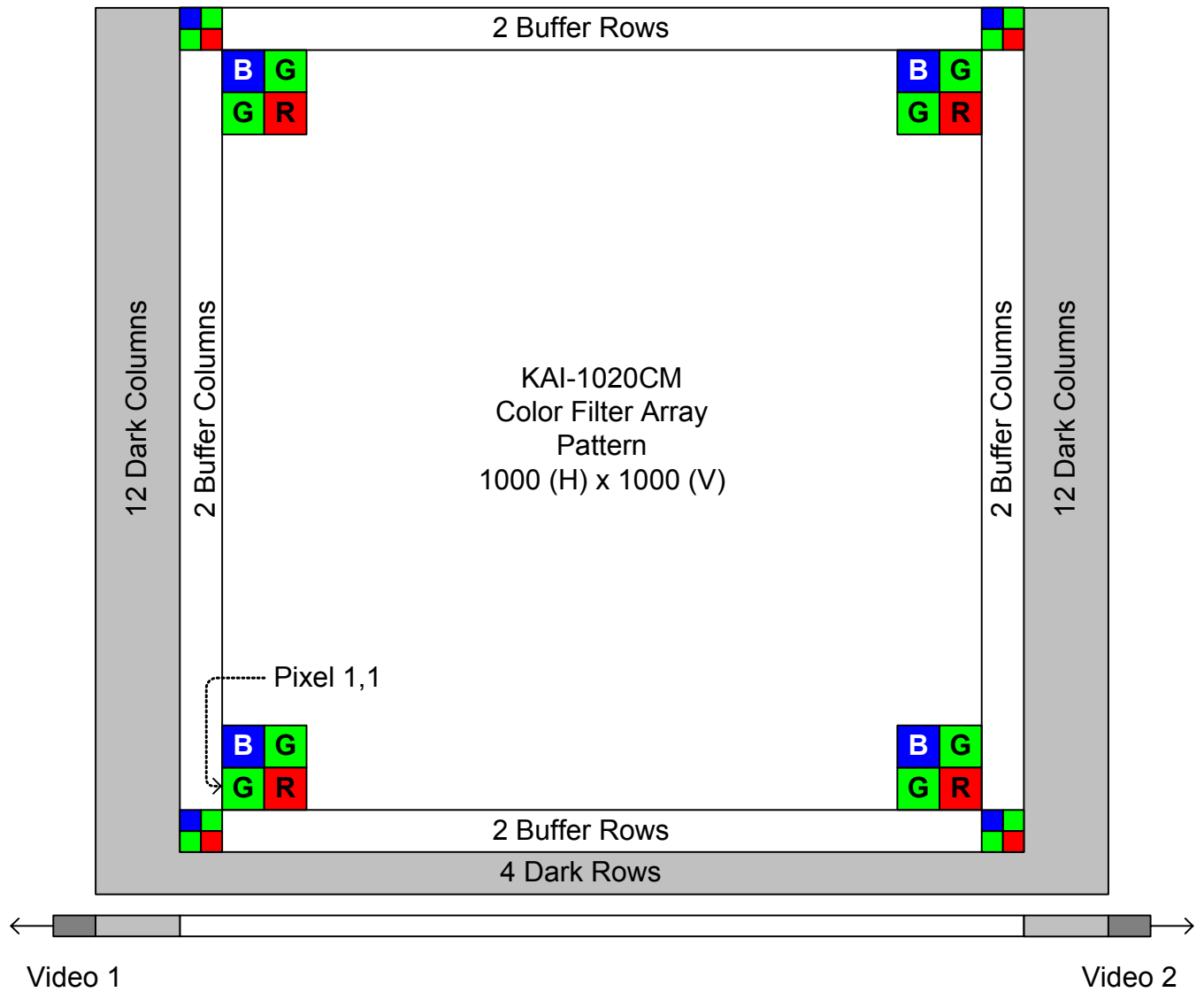
Monochrome Quantum Efficiency



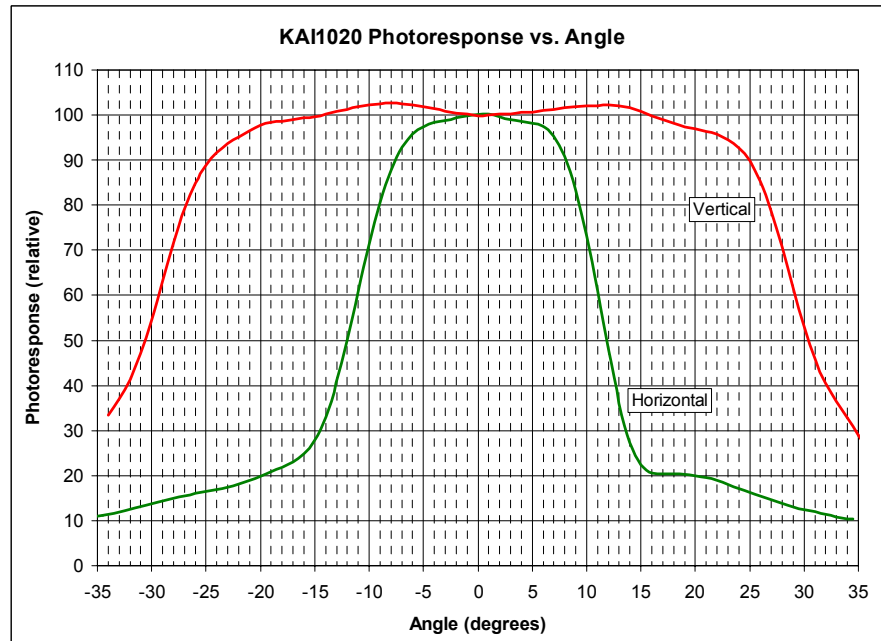
Color Quantum Efficiency



Color Filter Array Pattern

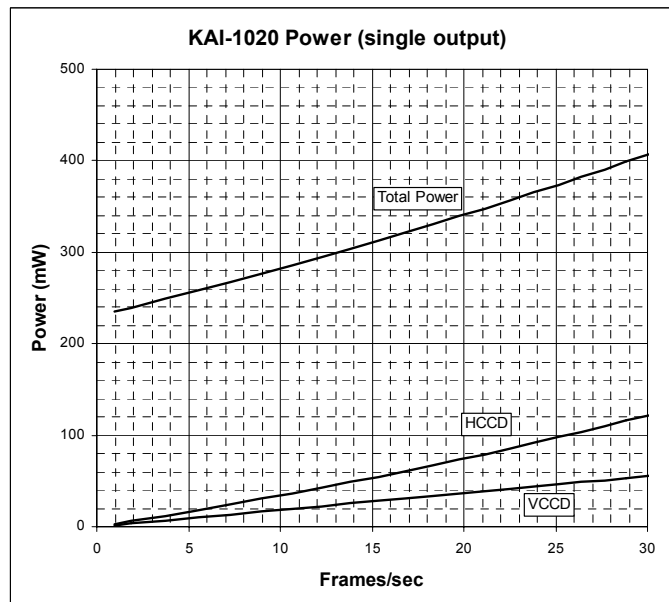


Photoresponse vs. Angle

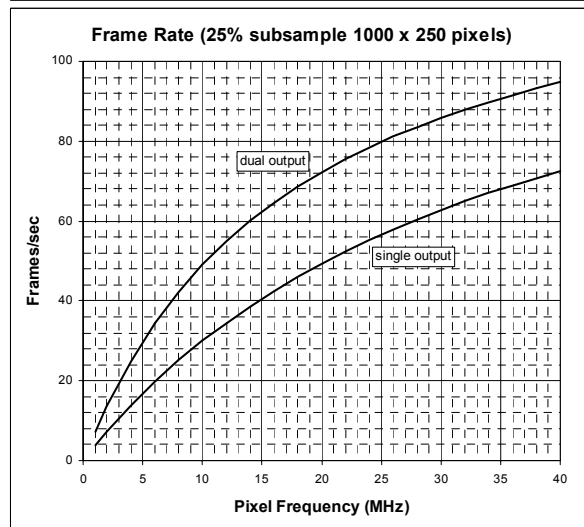
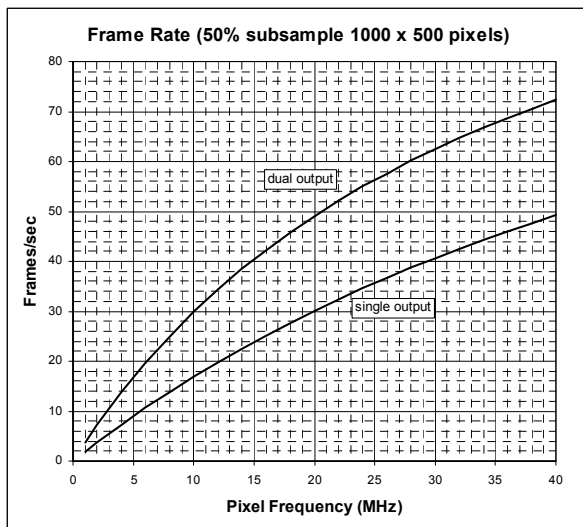
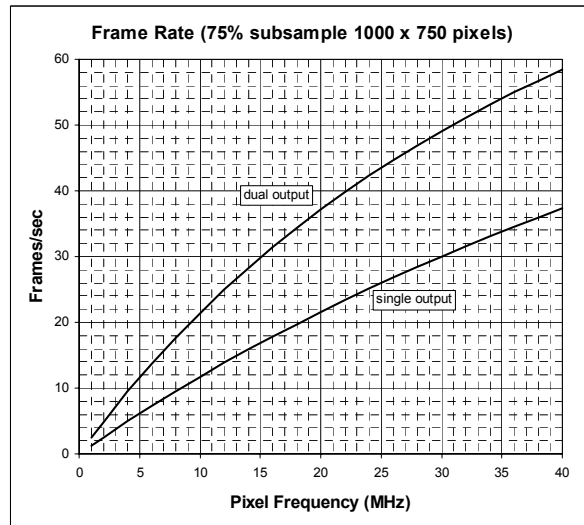
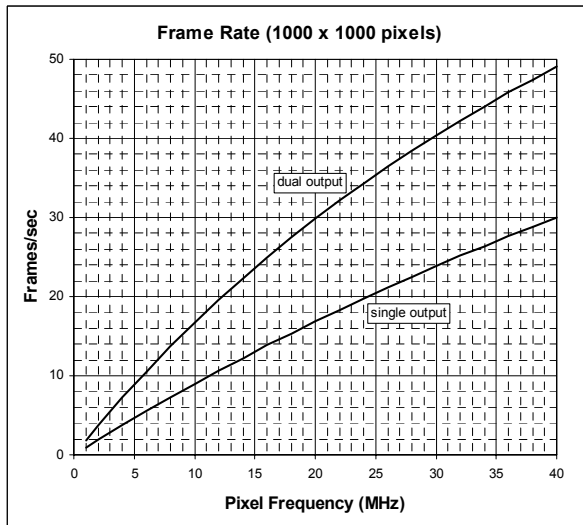


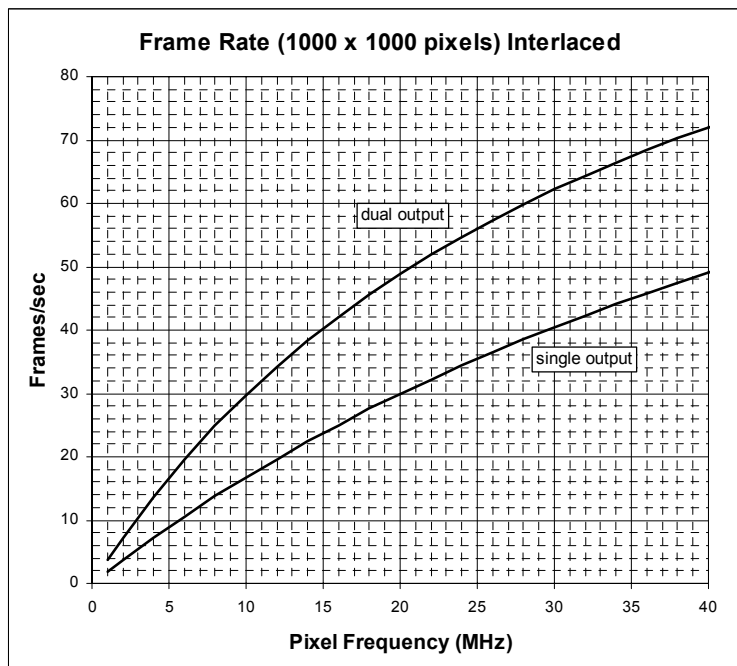
The horizontal curve is where the incident light angle is varied in a plane parallel to the HCCD.
 The vertical curve is where the incident light angle is varied in a plane perpendicular to the HCCD.

Sensor power



Frame Rate





Absolute Maximum Ratings

		Min.	Max.	Units	Notes
Temperature	Operation without damage	-50	70	C	
	Storage	-55	70	C	
Voltage between pins	VSUB to GND	8	20	V	1
	VDD to GND	0	17	V	
	$\phi V1$ to $\phi V2$, ϕFD to $\phi V1$, $\phi V2$	-10	10	V	
	$\phi H1$ to $\phi H2$	-8	8	V	
	ϕR , ϕT , ϕSA , ϕSB to GND	-9	12	V	
	$\phi H1$, $\phi H2$ to $\phi V1$, $\phi V2$	-9	10	V	
Current	Video Output Bias Current	0	7	mA	2

Notes:

1. For electronic shuttering VSUB may be pulsed to 35 V for up to 10 μs .
2. Note that the current bias effects the amplifier bandwidth.

Caution: This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for Class 0 devices (JESD22 Human Body Model) or Class A (Machine Model). Refer to Application Note MTD/PS-0224, “Electrostatic Discharge Control for Image Sensors”

Caution: Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-0237, “Cover Glass Cleaning for Image Sensors”

Quality Assurance and Reliability

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note MTD/PS-0237, Cover Glass Cleaning, for further information.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Ordering Information

Available Part Configurations

Type	Description	Package Configuration	Glass Configuration
KAI-1020	Monochrome without microlens	Pin Grid Array	Taped Clear Glass
KAI-1020M	Monochrome with microlens	Pin Grid Array	Sealed MAR Glass
KAI-1020M	Monochrome with microlens	Leadless Chip Carrier	Sealed MAR Glass
KAI-1020CM	Color with microlens	Pin Grid Array	Sealed MAR Glass
KAI-1020CM	Color with microlens	Leadless Chip Carrier	Sealed MAR Glass

Please contact Image Sensor Solutions for available part numbers.

MAR Glass: Anti-reflective coated, both sides of the glass.

Address all inquiries and purchase orders to:

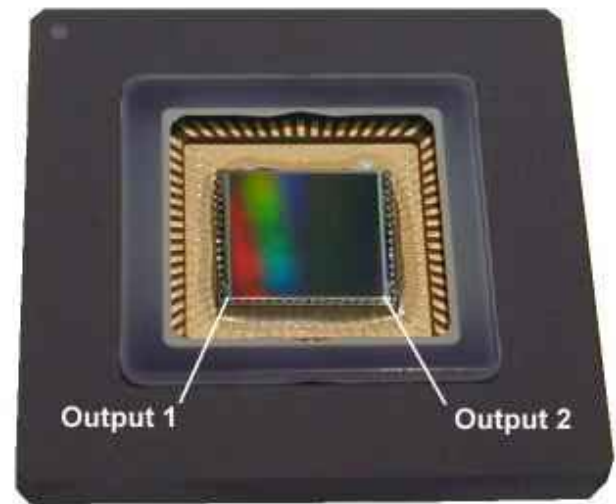
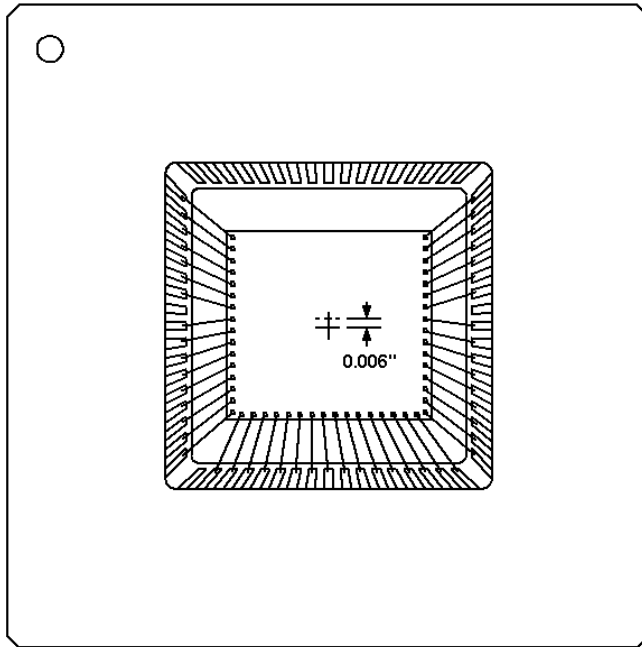
Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

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WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

When viewed from the top with the pin 1 index to the upper left, the center of the photoactive pixel array is offset 0.006" above the physical center of the package. The pin 1 index is located in the corner



of the package above pins L2 and K1. When operated in single output mode the first pixel out of the sensor will be in the corner closest to VOUT1B (pin L9). The HCCD is parallel to the row of pins A10 to L10. In the above pictures, the VCCD transfers charge down.

Pin Grid Array Pin Description

Label	Pin	Function	Label	Pin	Function
V2IN	K2	VCCD gate phase 2 input	ϕ H1S	F11	HCCD storage phase 1 clock input
VSUB	L2	substrate voltage input	GND	E10	Ground (0V)
V2LOW	K3	VCCD phase 2 clock driver low	ϕ H1BR	E11	HCCD right phase 1 barrier clock input
V2OUT	L3	VCCD phase 2 clock driver output	ϕ H2BR	D10	HCCD right phase 2 barrier clock input
V2MID	K4	VCCD phase 2 clock driver mid	ϕ S2B	D11	Video 2 CDS sample B clock input
V2HIGH	L4	VCCD phase 2 clock driver high	ϕ S2A	C10	Video 2 CDS sample A clock input
ϕ V2A	K5	VCCD phase 2 clock driver input A	ϕ R2	C11	Video 2 CDS reset clock input
VSUB	L5	substrate voltage input	ϕ T2	B11	Video 2 CDS transfer clock input
V2S9	K6	VCCD phase 2 clock driver +9V	VDD2	B10	Video 2 CDS +15V
V2S5	L6	VCCD phase 2 clock driver +5V fast dump clock driver +5V	VOUT2B	A10	Video 2 CDS output B
ϕ V2B	K7	VCCD phase 2 clock driver input B	GND	B9	Ground (0V)
ϕ FD	L7	fast dump clock driver input	VOUT2A	A9	Video 2 CDS output A
VDD1	K8	Video 1 CDS +15V	VDD2	B8	Video 2 CDS +15V
VOUT1A	L8	Video 1 CDS output A	ϕ V1	A8	VCCD phase 1 clock driver input
GND	K9	Ground (0V)	V1S5	B7	VCCD phase 1 clock driver +5V
VOUT1B	L9	Video 1 CDS output B	V1MID	A7	VCCD phase 1 clock driver mid
VDD1	L10	Video 1 CDS +15V supply	V1OUT	B6	VCCD phase 1 clock driver output
ϕ T1	K11	Video 1 CDS transfer clock input	V1LOW	B5	VCCD phase 1 clock driver low
ϕ R1	J10	Video 1 CDS reset clock input	SHD1C1	A5	shutter driver connection
ϕ S1A	J11	Video 1 CDS sample A clock input	SHC2	B4	shutter driver connection
ϕ S1B	H10	Video 1 CDS sample B clock input	SHC1	A4	shutter driver connection
ϕ H2BL	H11	HCCD left phase 2 barrier clock input	ϕ SH	B3	shutter driver clock input
ϕ H1BL	G10	HCCD left phase 1 barrier clock input	VSH15	A3	shutter driver +15V
GND	G11	Ground (0V)	V1IN	A2	VCCD gate phase 1 input
ϕ H2S	F10	HCCD storage phase 2 clock input			

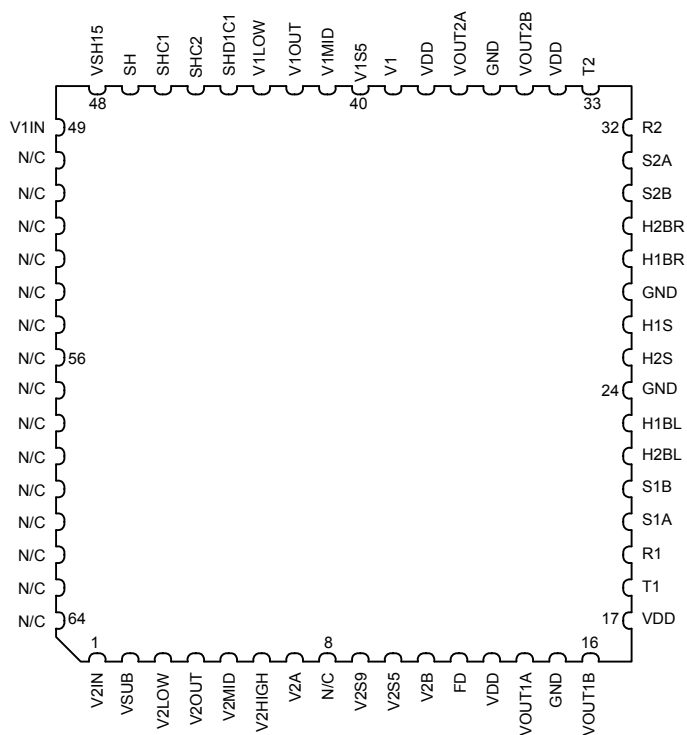
All pins not listed must be unconnected.

Leadless Chip Carrier Pin Description – Table

Pin	Description
1	V2IN
2	VSUB
3	V2LOW
4	V2OUT
5	V2MID
6	V2HIGH
7	V2A
8	No Connect
9	V2S9
10	V2S5
11	V2B
12	FD
13	VDD
14	VOUT1A
15	GND
16	VOUT1B
17	VDD
18	T1
19	R1
20	S1A
21	S1B
22	H2BL
23	H1BL
24	GND
50-64	No Connect

Pin	Description
25	H2S
26	H1S
27	GND
28	H1BR
29	H2BR
30	S2B
31	S2A
32	R2
33	T2
34	VDD
35	VOUT2B
36	GND
37	VOUT2A
38	VDD
39	V1
40	V1S5
41	V1MID
42	V1OUT
43	V1LOW
44	SHD1C1
45	SHC2
46	SHC1
47	SH
48	VSH15
49	V1IN

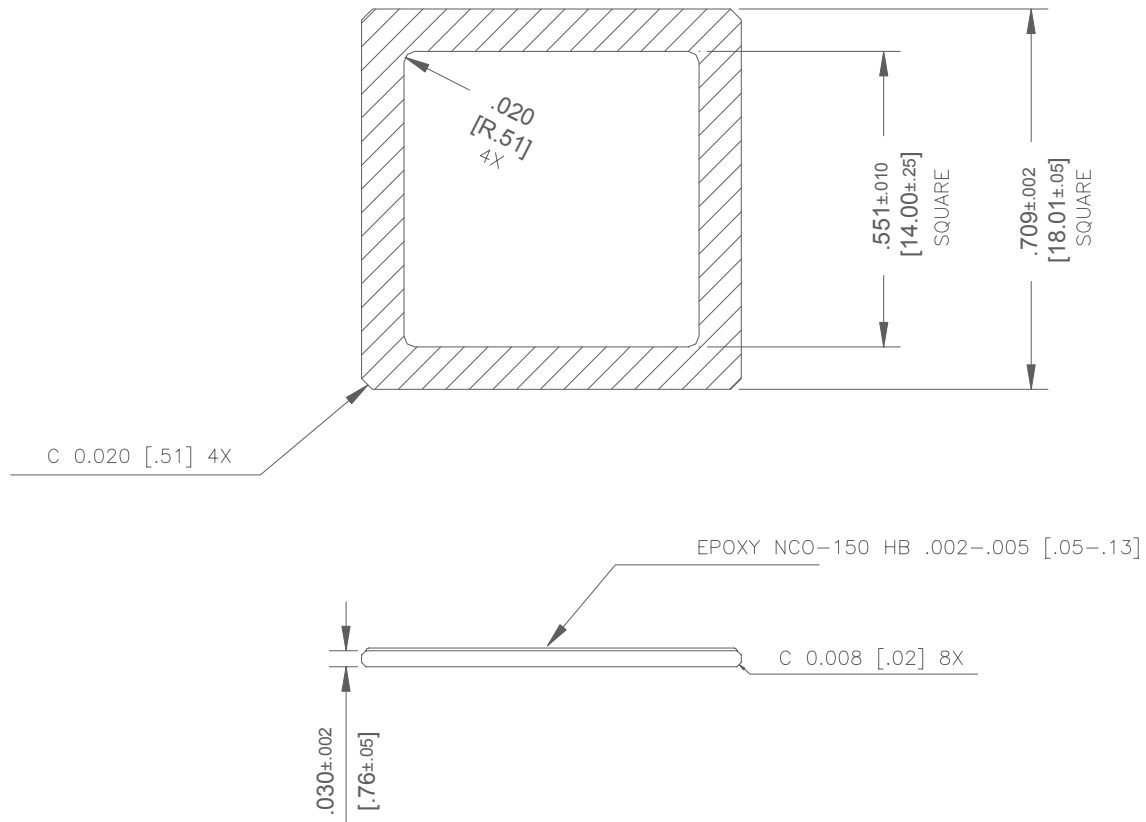
Leadless Chip Carrier Pin Description – Drawing



Top View

Glass

Pin Grid Array Package Cover Glass

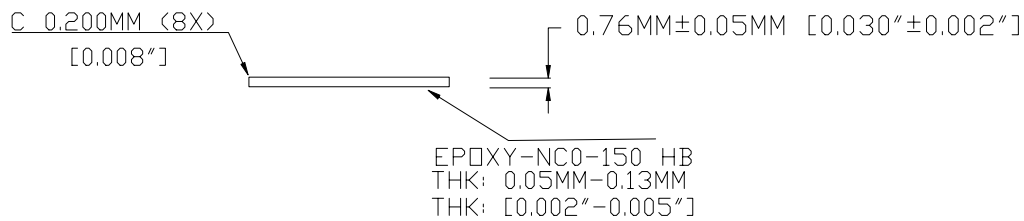
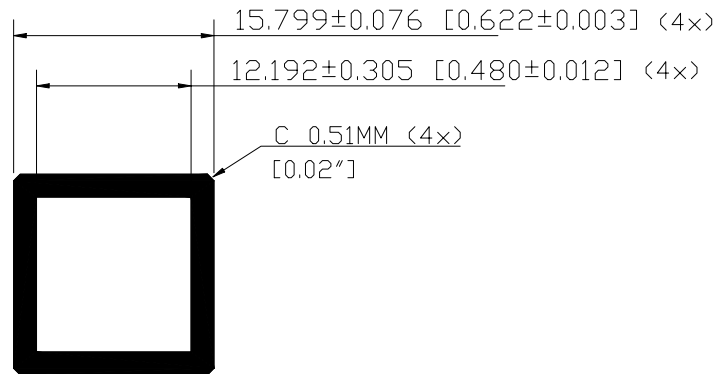


NOTE:

1. DUST/SCRATCH 10 MICRON MAX.
2. SUBSTRATE: SCHOTT D-263 OR EQUIV.
3. EPOXY: NCO-150 HB
4. DOUBLE-SIDED AR COATING REFLECTANCE

420nm-435nm	< 2.0%
435nm-630nm	< 0.8%
630nm-680nm	< 2.0%

Leadless Chip Carrier Cover Glass



DOUBLE-SIDE AR COATING REFLECTANCE

420nm-435nm <2.0%

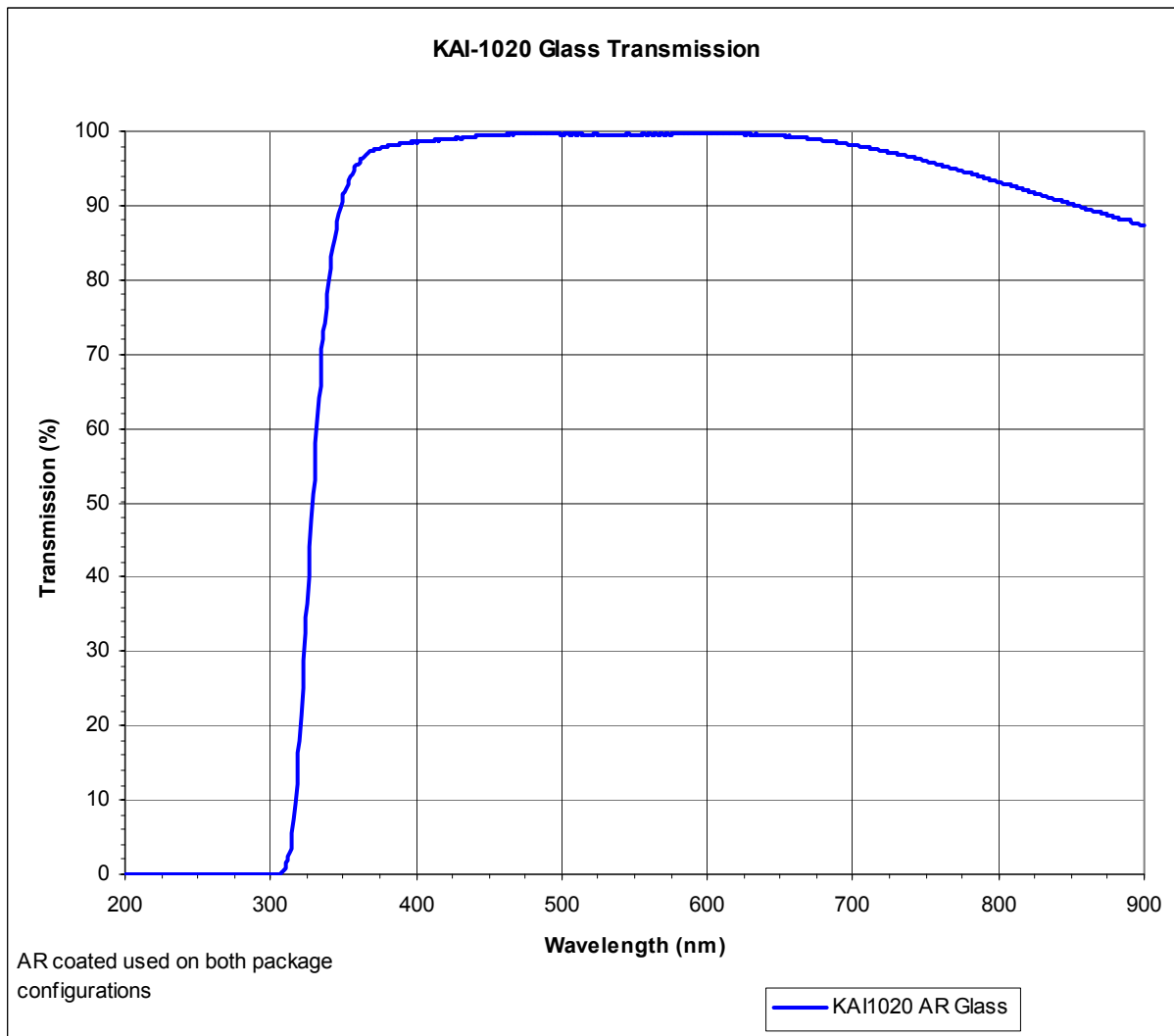
435nm-630nm <0.8%

630nm-680nm <2.0%

SUBSTRATE SCHOTT D-263 OR EQUIVALENT

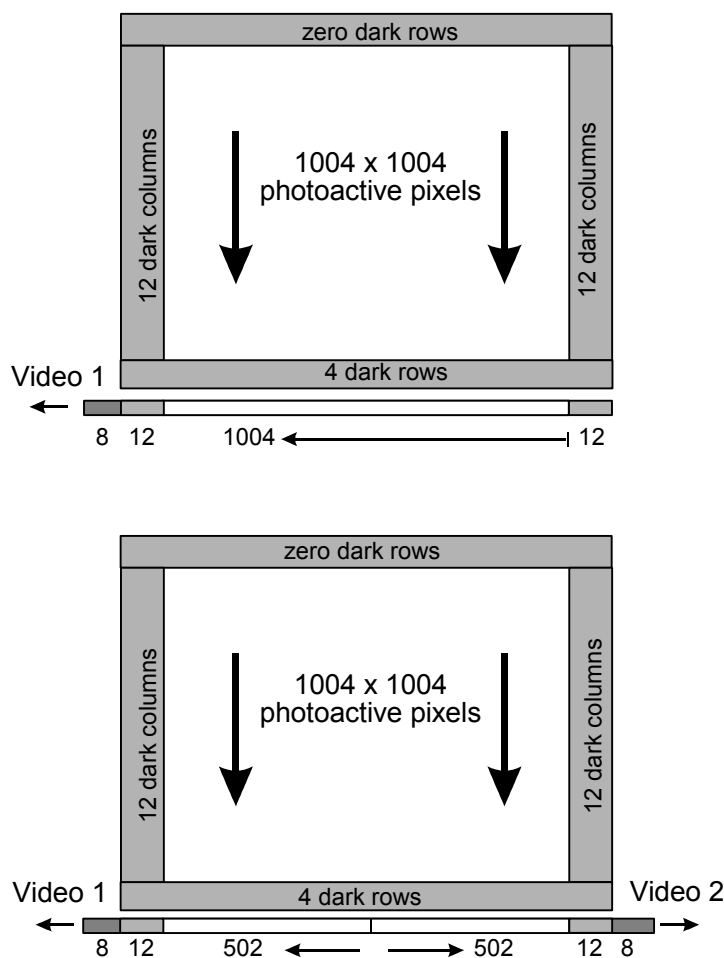
Dust, Scratch specification
 10 micron max

Glass Transmission



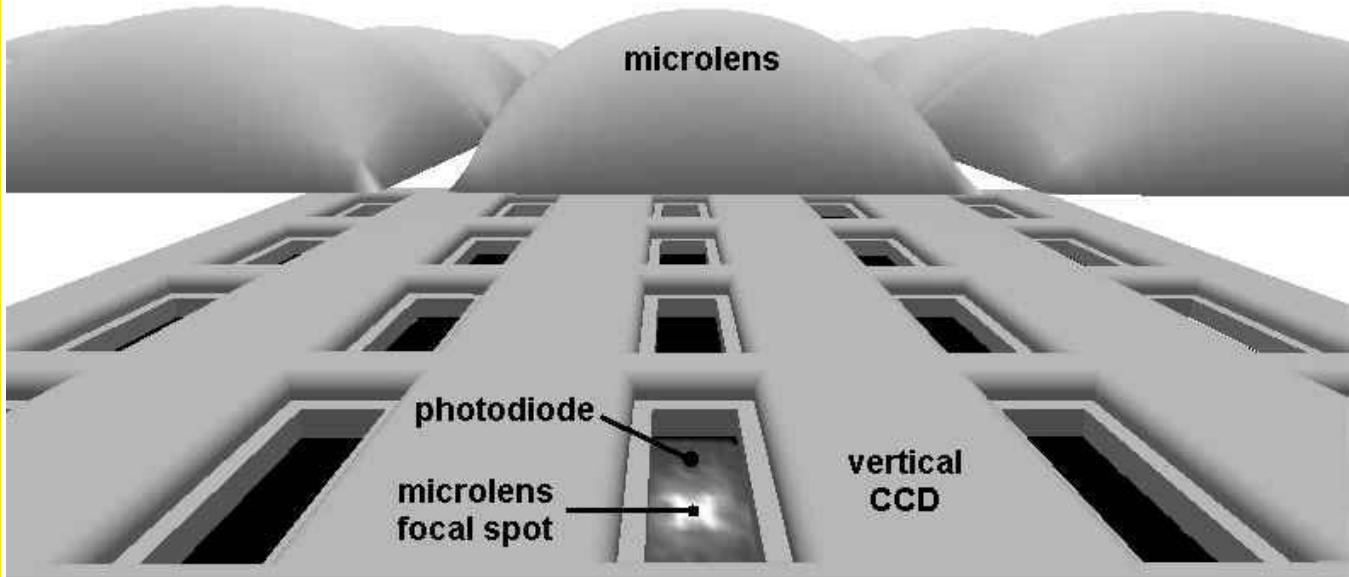
Sensor Operation

Single or dual output



The KAI-1020 is designed to read the image out of one output at 30 frames/second or two outputs at 48 frames/second. In the dual output mode the right half of the horizontal shift register reverses its direction of charge transfer. The left half of the image is read out of video 1 and the right half of the image is read out of video 2.

There are no dark reference rows at the top and 4 dark rows at the bottom of the image sensor. The 4 dark rows should not be used for a dark reference level. The dark rows will contain smear signal from bright light sources. Use the 12 dark columns on the left or right side of the image sensor as a dark reference.

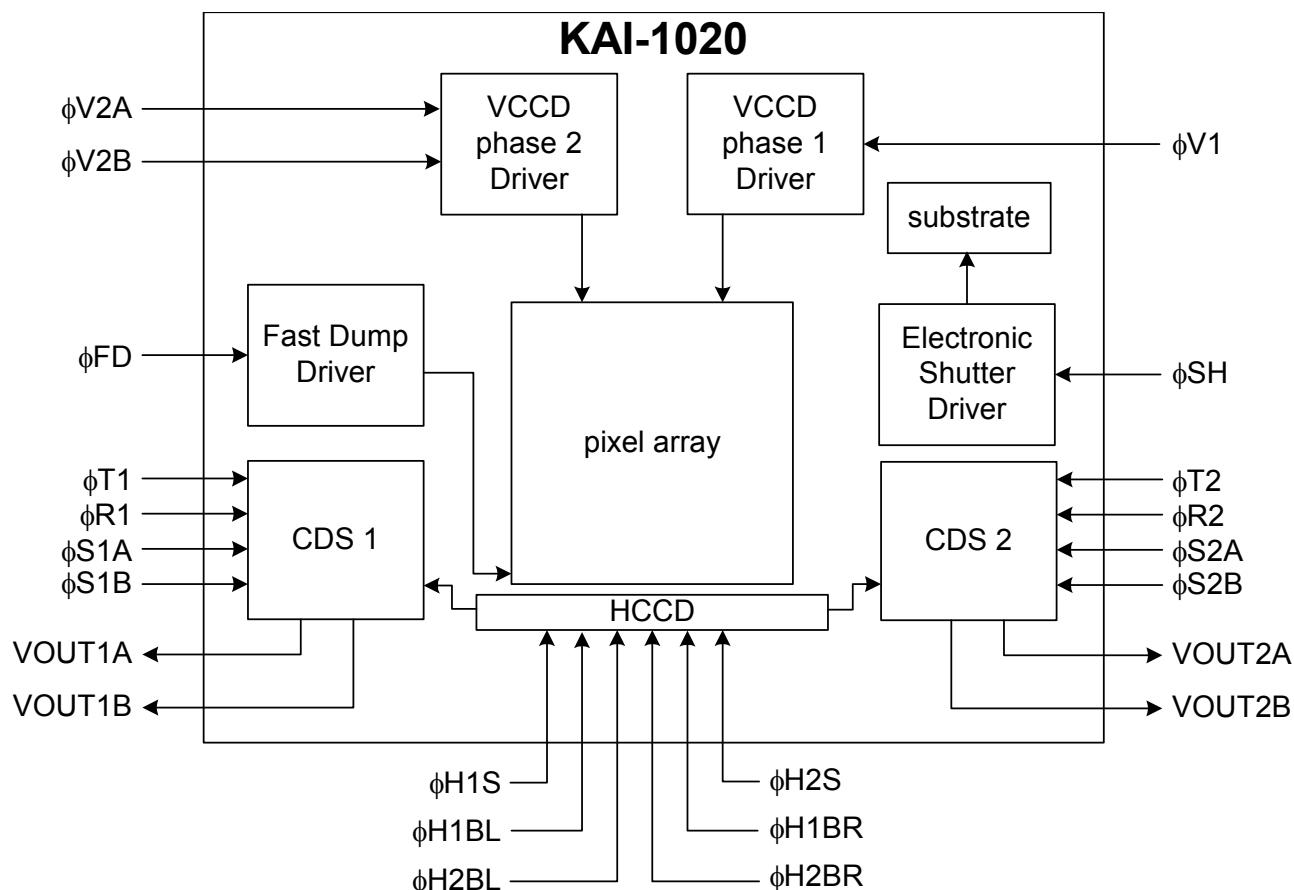


The KAI-1020 Pixel

The pixel is $7.4\ \mu\text{m}$ square. It consists of a light sensitive photodiode and an optically shielded vertical shift register. The vertical shift register is a charge-coupled device (VCCD). Each pixel is covered by a microlens to increase the light gathering efficiency of the photodiode.

Under normal operation, the image capture process begins with a $4\ \mu\text{s}$ long pulse on the electronic shutter trigger input ϕSH . The electronic shutter empties all charge from every photodiode in the pixel array. The photodiodes start collecting light on the falling edge of the ϕSH pulse. For each photon that is incident upon the $7.4\ \mu\text{m}$ square area of the pixel, the probability of an electron being generated in the photodiode is given by the quantum efficiency (QE). At the end of the desired integration time, a $10\ \mu\text{s}$ pulse on ϕV2B transfers the charge (electrons) collected in the photodiode into the VCCD. The integration time ends on the falling edge of ϕV2B .

High level block diagram



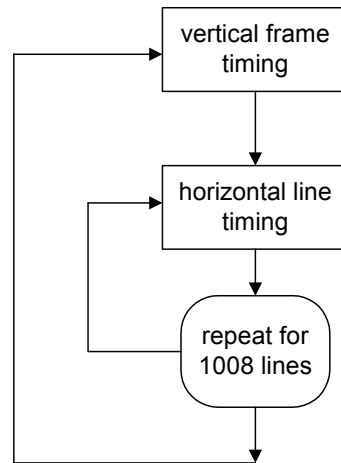
All timing inputs are driven by 5V logic. The image sensor has integrated clock drivers to generate the proper voltages for the internal CCD gates. There are two VCCD clock drivers. Both the phase 1 and phase 2 VCCD drivers control the shifting of charge through the VCCD. The phase 2 driver also controls the transfer of charge from the photodiodes to the VCCD.

There is an integrated fast dump driver, which allows an entire row of pixels to be quickly discarded without clocking the row through the HCCD.

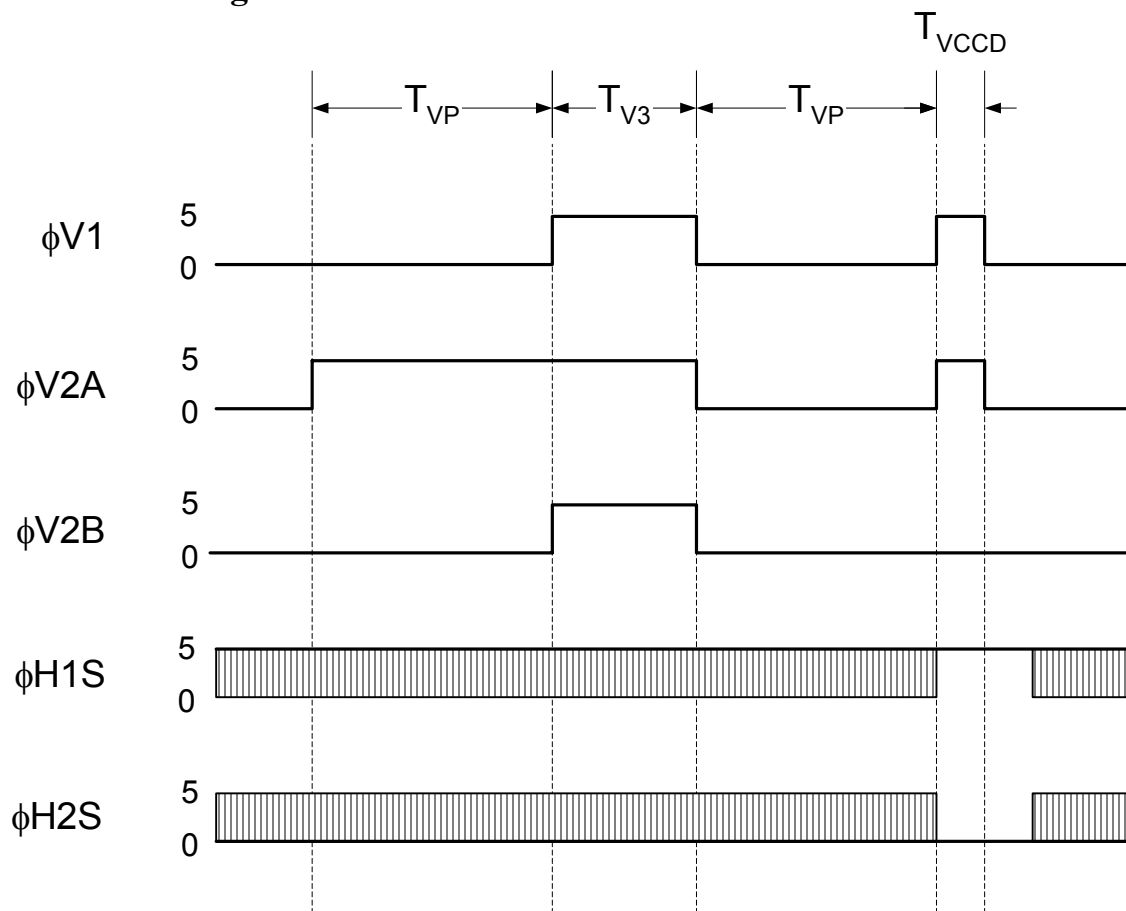
An integrated electronic shutter driver generates a >30 volt pulse on the substrate to simultaneously empty every photodiode on the image sensor.

Each of the two outputs has a correlated double sampling circuit to simplify the analog signal processing in the camera. The horizontal clock timing selects which outputs are active.

Main Timing



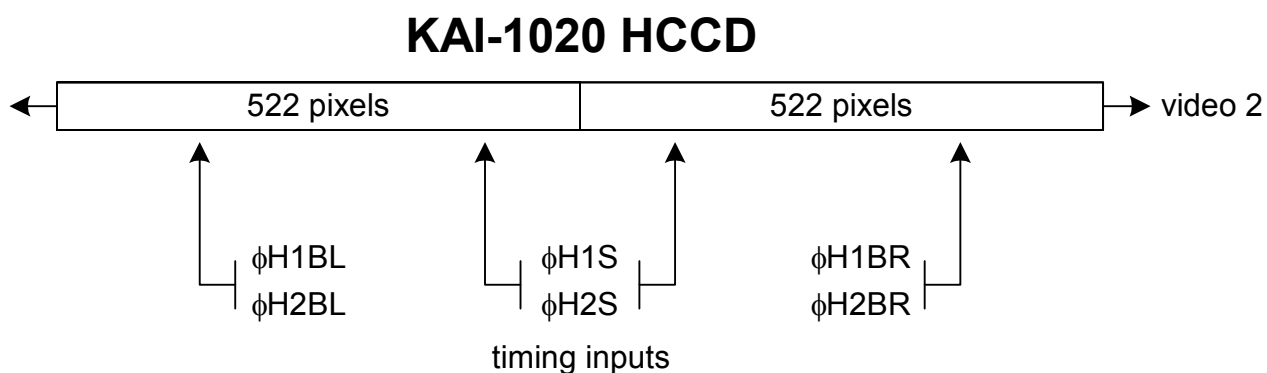
Vertical Frame Timing

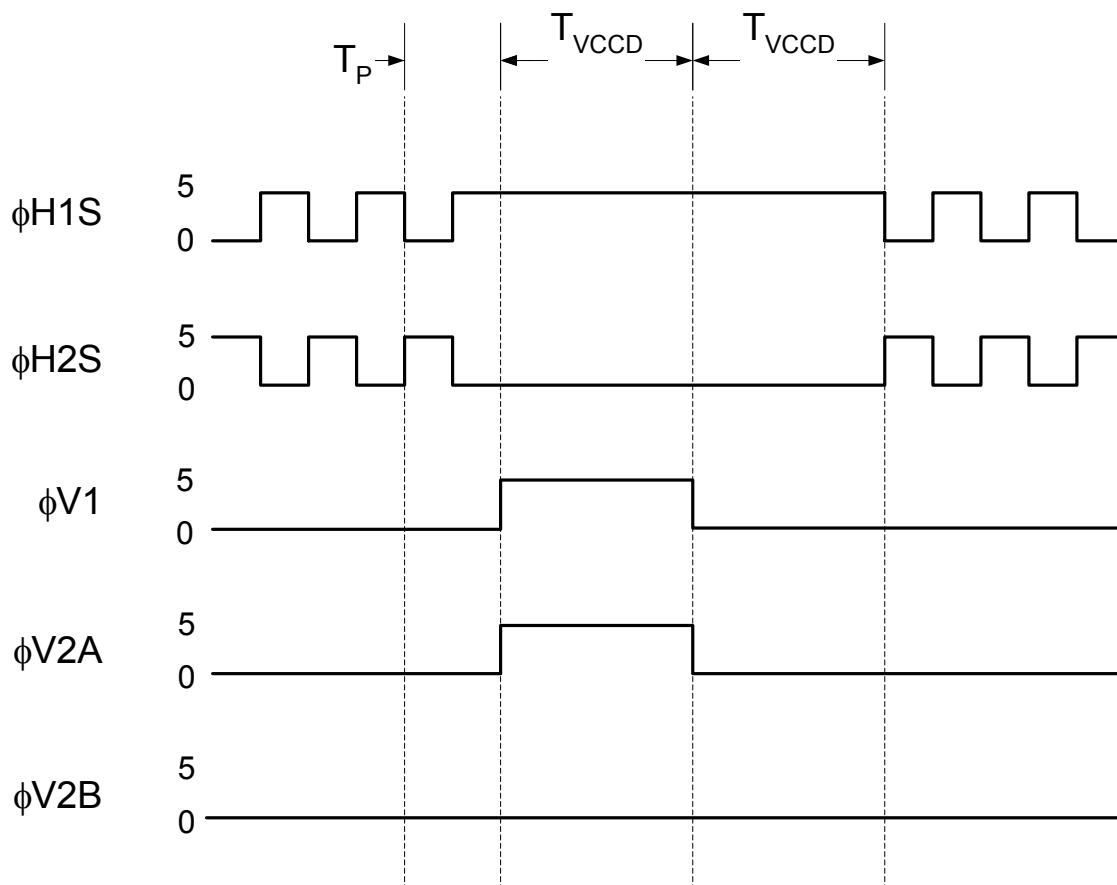


The vertical frame timing may begin once the last pixel of the image sensor has been read out of the HCCD. The beginning of the vertical frame timing is at the rising edge of $\phi V2A$. After the rising edge of $\phi V2A$ there must be a delay of T_{VP} μs before a pulse of T_{V3} μs on $\phi V2B$ and $\phi V1$. The charge is transferred from the photodiodes to the VCCD during the time T_{V3} . The falling edge of $\phi V2B$ marks the end of the photodiode integration time. After the pulse on $\phi V2B$ the $\phi V1$ and $\phi V2A$ should remain idle for T_{VP} μs before the horizontal line timing period begins. This allows the clock and well voltages time to settle for efficient charge transfer in the VCCD.

All HCCD and CDS timing inputs should run continuously through the vertical frame timing period. For an extremely short integration time, it is allowed to place an electronic shutter pulse on ϕSH at any time during the vertical frame timing. The ϕSH and $\phi V2B$ pulses may be overlapped. The integration time will be from the falling edge of ϕSH to the falling edge of $\phi V2B$.

Horizontal Line Timing





When the $\phi V2A$ and $\phi V1$ timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row next to the HCCD is shifted into the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped. $\phi H1S$ must be stopped in the high state and $\phi H2S$ must be stopped in the low state. The HCCD clocking may begin T_{VCCD} μs after the falling edge of the $\phi V2A$ and $\phi V1$ pulse. The timing inputs to the CDS should run continuously through the horizontal line timing.

The HCCD has a total of 1036 pixels. The 1028 vertical shift registers (columns) are shifted into the center 1028 pixels of the HCCD. There are 8 pixels at both ends of the HCCD which receive no charge from a vertical shift register. The first 8 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 12 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 1004 clock cycles will contain photo-electrons (image data). Finally, the last 12 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. Of the 12 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 10 columns of the 12 column dark reference.

When the HCCD is shifting valid image data, the timing inputs to the electronic shutter driver (ϕSH), VCCD driver ($\phi V2A$, $\phi V2B$, $\phi V1$), and fast dump drivers (ϕFD) should be held at the low level. This prevents unwanted noise from being introduced into the CDS circuit.

The HCCD is a type of charge coupled device known as a pseudo-two phase CCD. This type of CCD has the ability to shift charge in two directions. This allows the entire image to be shifted out to the video 1 output CDS, or to the video 2 output CDS (left/right image reversal). The HCCD is split into two equal halves of 522 pixels each. When operating the sensor in single output mode the two halves of the HCCD are shifted in the same direction. When operating the sensor in dual output mode the two halves of the HCCD are shifted in opposite directions. The direction of charge transfer in each half is controlled by the $\phi H1BL$, $\phi H2BL$, $\phi H1BR$, and $\phi H2BR$ timing inputs.

Single output

To direct all pixels to the video 1 output make the following HCCD connections:

$\phi H1S = \phi H1BL, \phi H2BR$

$\phi H2S = \phi H2BL, \phi H1BR$

To direct all pixels to the video 2 output make the following HCCD connections:

$\phi H1S = \phi H2BL, \phi H1BR$

$\phi H2S = \phi H1BL, \phi H2BR$

In each case the first 8 pixels will contain no electrons, followed by 12 dark reference pixels containing only electrons generated by dark current, followed by 1004 photo-active pixels, followed by 12 dark reference pixels. The HCCD must be clocked for at least 1028 cycles. The VCCD may be clocked immediately after the 1028th HCCD clock cycle.

If the sensor is to be permanently operated in single output mode through video 1, then VDD2 (pins B8, and B10) may be connected to GND. This disables the video 2 CDS and lowers the power consumption.

If the sensor is to be permanently operated in single output mode through video 2, then VDD1 and VDD2 supplies must be +15 V. The VDD1 supplies must always be at +15 V for the sensor to operate properly.

Dual output

To use both outputs for faster image readout, make the following HCCD connections:

$\phi H1S = \phi H1BL, \phi H1BR$

$\phi H2S = \phi H2BL, \phi H2BR$

For both outputs the first 8 HCCD clock cycles contain no electrons, followed by 12 dark reference pixels containing only dark current electrons, followed by 502 photo-active pixels. This adds up to 522 pixels, but the HCCD should be clocked for at least 523 cycles before the next VCCD line shift takes place. The extra HCCD clock cycle ensures that the signal from the last pixel exits the CDS circuit before the VCCD drivers switch the gate voltages. This extra cycle is not needed for the single output modes because in that case, the last pixel is from a column of the dark reference which is not used. See the section on correlated double sampling for a description of the one pixel delay in the CDS circuit.

Electronic Shutter

Substrate Voltage

The voltage on the substrate, pins L1 and L5, determines the charge capacity of the photodiodes. When VSUB is 8 volts the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 volts decreases the charge capacity of the photodiodes until 30 volts when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on VSUB, with a peak amplitude greater than 30 volts, empties all photodiodes and provides the electronic shuttering action.

Substrate Voltage and Antiblooming

It may appear the optimal substrate voltage setting is 8 volts to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 volts will provide the maximum dynamic range, it will also provide the minimum antiblooming protection.

The KAI-1020 VCCD has a charge capacity of 60,000 electrons (60 ke). If the VSUB voltage is set such that the photodiode holds more than 60 ke, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size.

The blooming can be eliminated by increasing the voltage on VSUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate.

If that maximum rate is exceeded, (say, for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming.

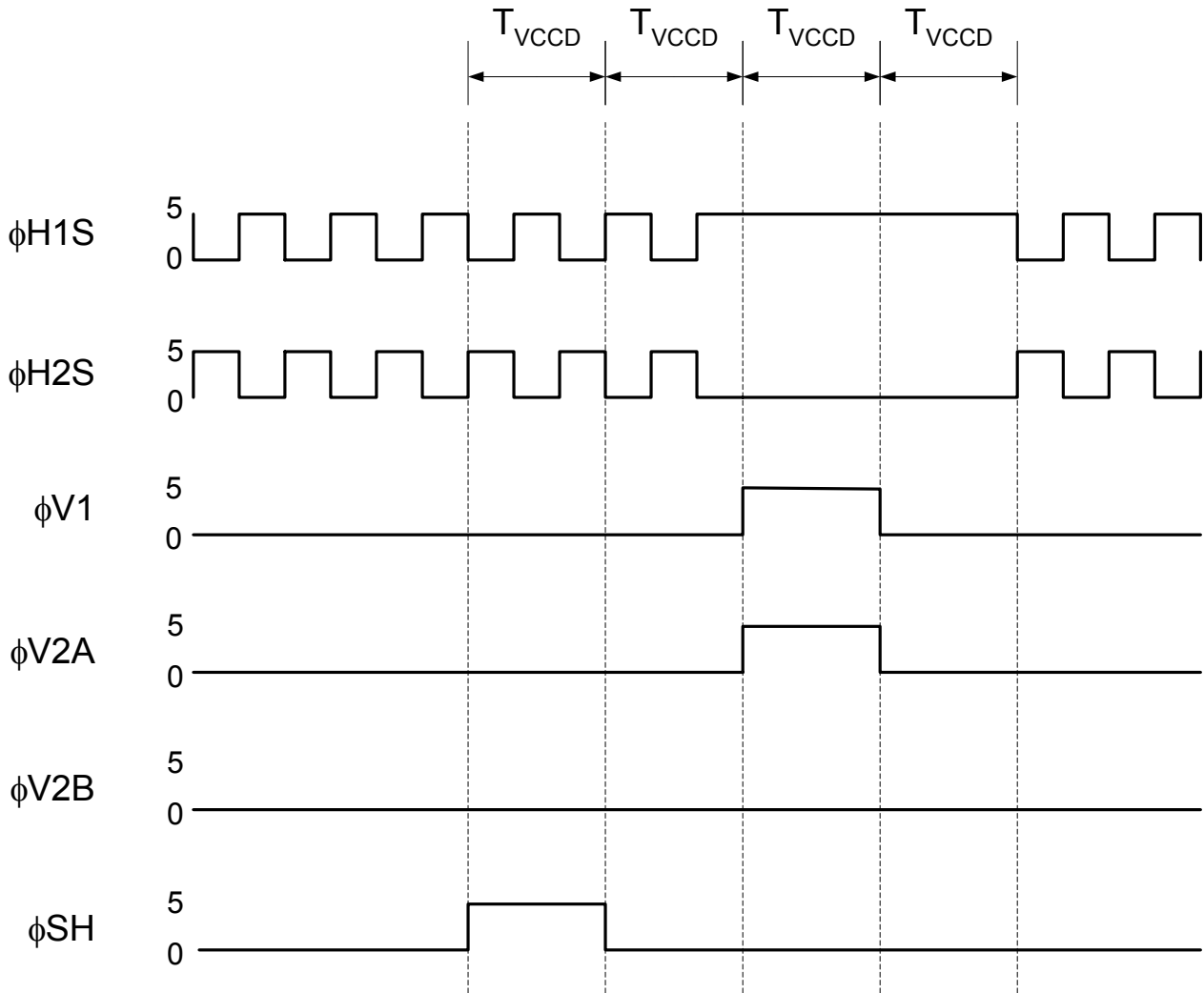
The amount of antiblooming protection also decreases when the integration time is decreased.

There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of antiblooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) antiblooming protection. A high VSUB voltage provides lower dynamic range and maximum antiblooming protection. The optimal setting of VSUB is written on the container in which each KAI-1020 is shipped. The given VSUB voltage for each sensor is selected to provide antiblooming protection for bright spots at least 100 times saturation, while maintaining at least 500 mV of dynamic range.

A detailed discussion of antiblooming and smear may be found in IEEE Transactions on Electron Devices vol. 39 no. 11, pg. 2508.

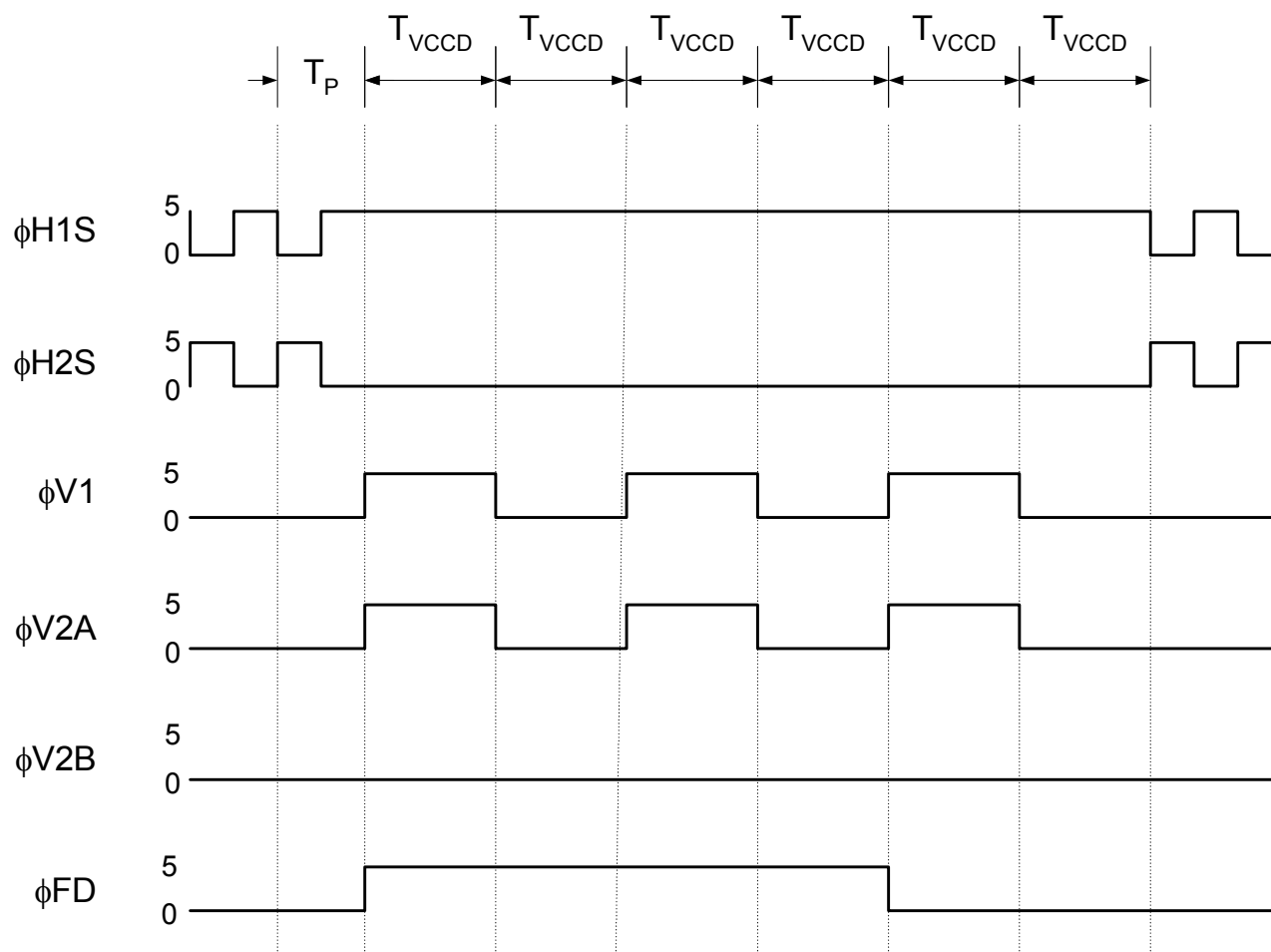
Electronic Shutter Timing

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of T_{INT} is desired, then the substrate voltage of the sensor is pulsed to at least 30 volts T_{INT} seconds before the photodiode to VCCD transfer pulse on $\phi V2B$. The large substrate voltage pulse is generated by the KAI-1020. The electronic shutter is triggered by a 5 volt pulse on ϕSH . Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD. The electronic shutter pulse may be added to the end of the horizontal line timing and just after the last pixel has been read out of the HCCD. $\phi H1S$ and $\phi H2S$ must be clocked during the electronic shutter pulse.



Fast Dump

The KAI-1020 has the ability to rapidly discard (fast dump, FD) entire lines of the image. The fast dump is a drain attached to the last row of the VCCD just before the HCCD. When the fast dump is activated by taking ϕFD high, charge from the VCCD goes into the drain instead of into the HCCD.



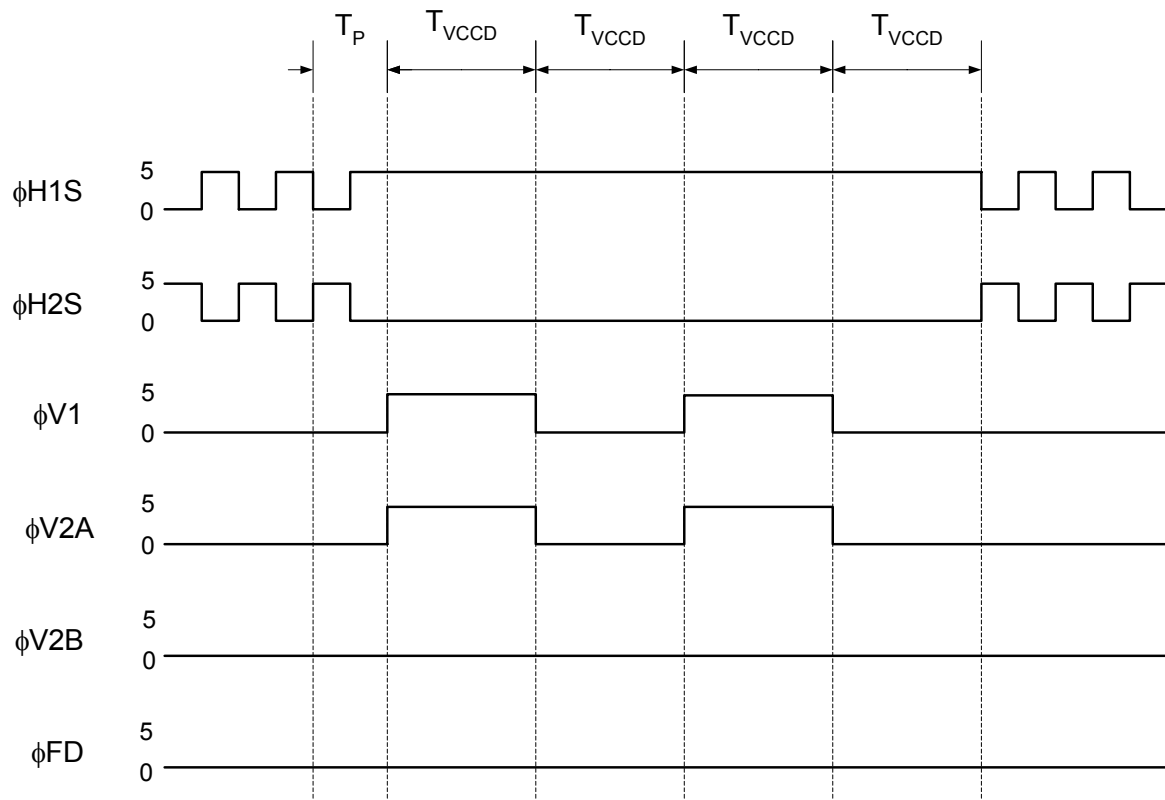
This timing diagram shows how two lines are dumped and the third is read out. ϕFD should go high once the last pixel of the preceding line has been read out. Cycle the VCCD for the number of rows to be dumped. The above timing diagrams shows two rows being dumped. When the proper number of rows have been dumped bring ϕFD low. Then clock the VCCD through one more cycle to shift a row into the HCCD.

The fast dump can be used to sub-sample the image for increased frame rates. For example, by dumping the even numbered lines, the image will be sub-sampled by a factor of 2 and the frame rate will almost increase by a factor of 2. Horizontal sub-sampling is not possible. The HCCD must always be cycled for the entire number of pixels in one line.

Another way to increase the frame rate is through sub-windowing. For example, suppose only the center 512 lines of the image are needed. Turn on the fast dump and clock the VCCD for 256 lines. Then turn off the fast dump and clock the VCCD (and HCCD) for 512 lines. Finally, turn the fast dump on again and clock the VCCD for 240 lines.

Binning and Interlaced modes

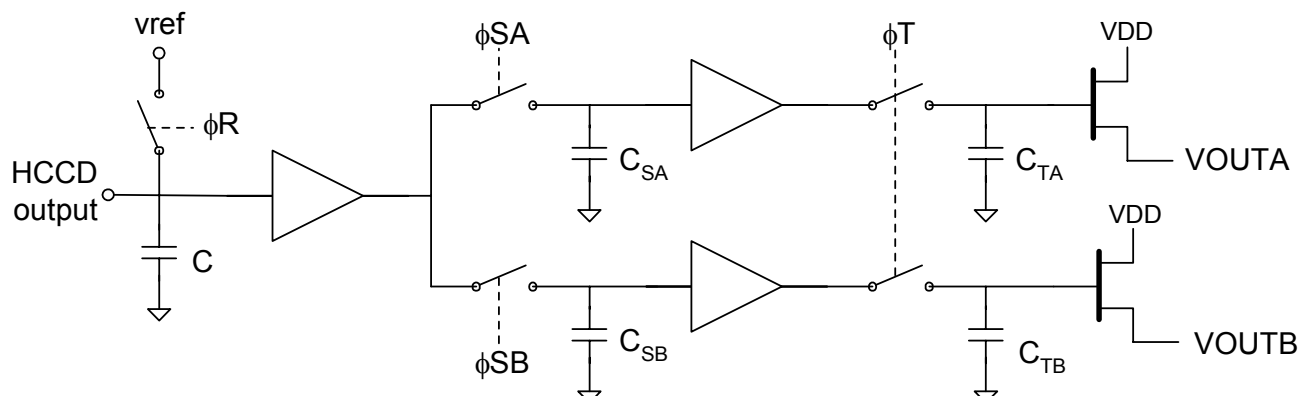
Binning is a readout mode of progressive scan CCD image sensors where more than one row at a time is clocked into the HCCD before reading out the HCCD. This timing mode sums two or more rows together. It increases the frame rate because there are fewer total rows to read out of the HCCD. The following timing diagram shows how two rows are summed together:



When binning two rows together only 504 rows need to be read out of the HCCD instead of the normal 1008 rows. The HCCD will hold up to two VCCD rows of full signal without blooming. Binning more than two rows may cause horizontal blooming for saturated signal levels.

Interlaced readout is a form of binning. To read out the even field use binning to sum together rows 0+1, rows 2+3, ... rows 1006+1007. To read out the odd field use binning to read out rows 0+1+2, rows 3+4, rows 5+6, rows 1005+1006, rows 1007+1008. The odd field may also be read out as row 0, rows 1+2, rows 3+4, rows 1005+1006. See section 3.12 for an example of interlaced timing.

Correlated Double Sampling (CDS)

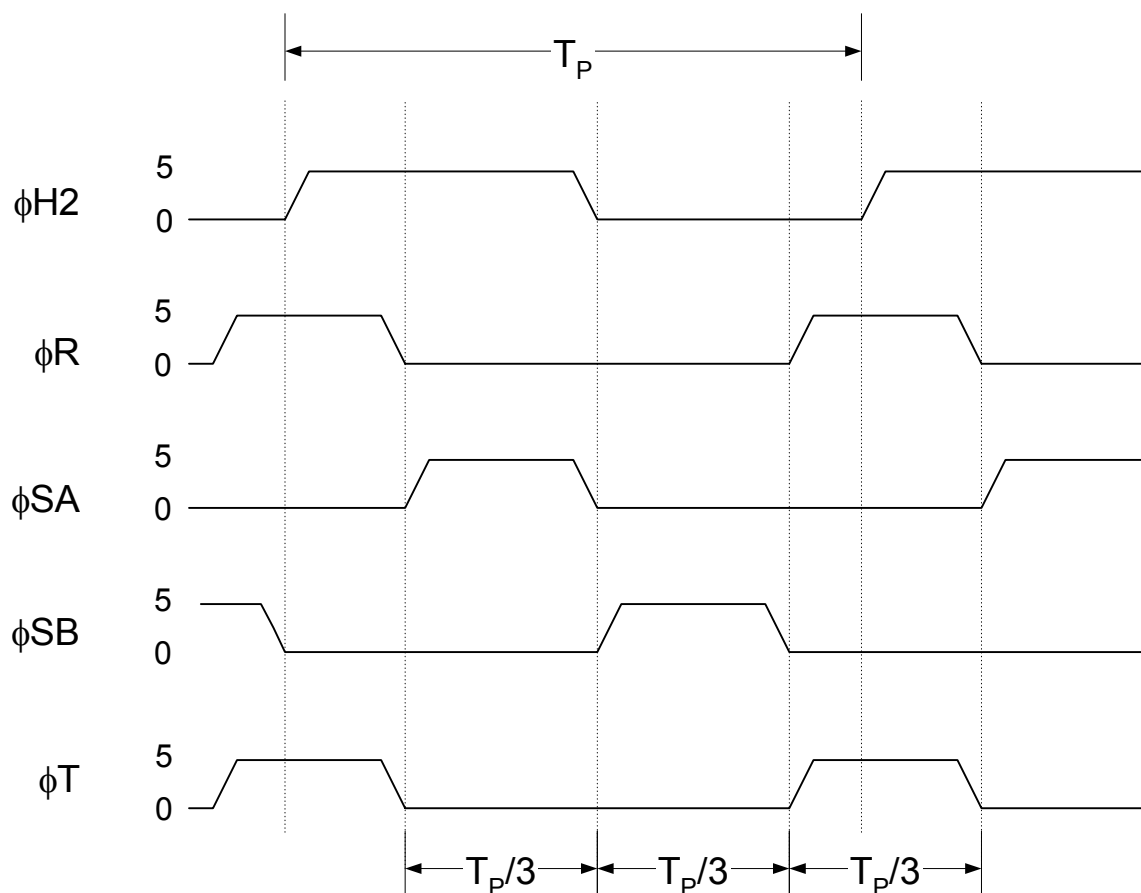


Correlated double sampling is a method of measuring the amount of charge in each pixel. The electrons in the last pixel of the HCCD are transferred onto a very small sensing capacitor, C , on the falling edge of ϕ_{H2S} . The voltage on C will change by about $20 \mu\text{V}$ for each electron that was in the HCCD. The process of measuring the amount of charge begins by resetting the value of C to an internally generated reference voltage, v_{ref} . A short pulse on ϕ_R at the rising edge of ϕ_{H2S} will reset C . After C has been reset, its voltage is sampled and stored on C_{SA} by a short pulse on switch ϕ_{SA} . Then on the falling edge of ϕ_{H2S} , electrons are transferred onto the capacitor, C . The new voltage on C is sampled and stored on C_{SB} by a short pulse on switch ϕ_{SB} . These two sampled voltages are then transferred to capacitors C_{TA} and C_{TB} by a short pulse on ϕ_T . ϕ_T and ϕ_R generally occur at the same time. An external operational amplifier is used to subtract the two voltages on $VOUTA$ and $VOUTB$. The output of the op-amp will be proportional to the number of electrons contained in one pixel. Note that it takes one entire pixel clock cycle for the value of the pixel to appear on $VOUTA$ and $VOUTB$. The A and B outputs of the CDS circuit will be in the range of 7 to 9 volts.

CDS Timing Edge Alignment

The edge alignments of the CDS timing pulses ϕ_{SA} , ϕ_{SB} , ϕ_T , and ϕ_R are critical to proper operation of the CDS circuit.

1. the falling edge of ϕ_R must not overlap the rising edge of ϕ_{SA}
2. the falling edge of ϕ_{SA} must come at the same time or before the falling edge of ϕ_{H2}
3. the rising edge of ϕ_{SB} must come after the falling edge of ϕ_{H2}
4. the falling edge of ϕ_{SB} must come before the rising edge of ϕ_R
5. the rising edge of ϕ_R may come before the rising edge of ϕ_{H2}
6. ϕ_T should always be driven by the same timing signal as ϕ_R
7. the pulse widths should be set such that ϕ_R , ϕ_{SA} , and ϕ_{SB} are $1/3$ of T_P



Disabling the CDS

There may be instances when the camera designer may want to use an external CDS. Such cases may occur at pixel clock frequencies 20MHz or slower where integrated CDS, analog to digital converter (A/D), and auto offset/gain circuits are available. These external CDS circuits require the raw unprocessed video waveform. The raw video can be obtained by permanently turning on the ϕSA , ϕSB , and ϕT switches by connecting them to a voltage in the range of 8 to 10V (the V2HIGH supply voltage, for example). Then place a load of 4mA to 5mA on VOUTA and a load of 0.1mA on VOUTB. VOUTA will be the raw video output suitable for external CDS circuits. The 5mA load may be a 2.0k Ω resistor and the 0.1mA load may be an 80k Ω resistor to GND. An external CDS is not recommended for pixel frequencies above 20MHz.

Timing and Voltage Specifications

Timing

Time	Min.	Nominal	Max.	Units
T _P	25	25	500	ns
T _{VCCD}	3.6	3.6	10	μs
T _{VP}	20	25	40	μs
T _{V3}	8	10	15	μs

Bias Voltages

Bias	Min (Volts)	Nominal (Volts)	Max (Volts)	Peak Current (mA)	Peak Current Frequency	Avg. Current (mA)
V1S5	4	5	6	2	2L	0.13
V1MID	-1.5	-1.2	-1.0	110	L	3
V1LOW	-9.5	-9	-8.5	110	L	3
V2S5	4	5	6	2	2L	0.5
V2S9	8	9	10	2	F	0.3
V2HIGH	8	9	10	110	L	0.01
V2MID	-1.5	-1.2	-1.0	110	L	3
V2LOW	-9.5	-9	-8.5	110 220	L F	3.8
VDD1	14.5	15	15.5			14
VDD2	14.5	15	15.5			14
VSH15	14	15	16	1	F	0.08
VSUB	8	*	14			0.03

Average currents are for 30 frames/second

Peak switching currents are for less than 1 μs duration

L = once per line time, 2L = twice per line time, F = once per frame time

* substrate bias voltage for a 500mV output range is written on the shipping container for each part

Power Up Sequence

1. Power up VSUB, V1LOW, V2LOW first
2. Then power up VDD, VSH15, V2S5, V1S5, V1MID, V2MID and V2HIGH
3. Then after the coupling capacitors on all of the timing inputs have charged, begin clocking the timing inputs.

Any positive voltage should never be allowed to go negative. Any negative voltage should never be allowed to go positive.

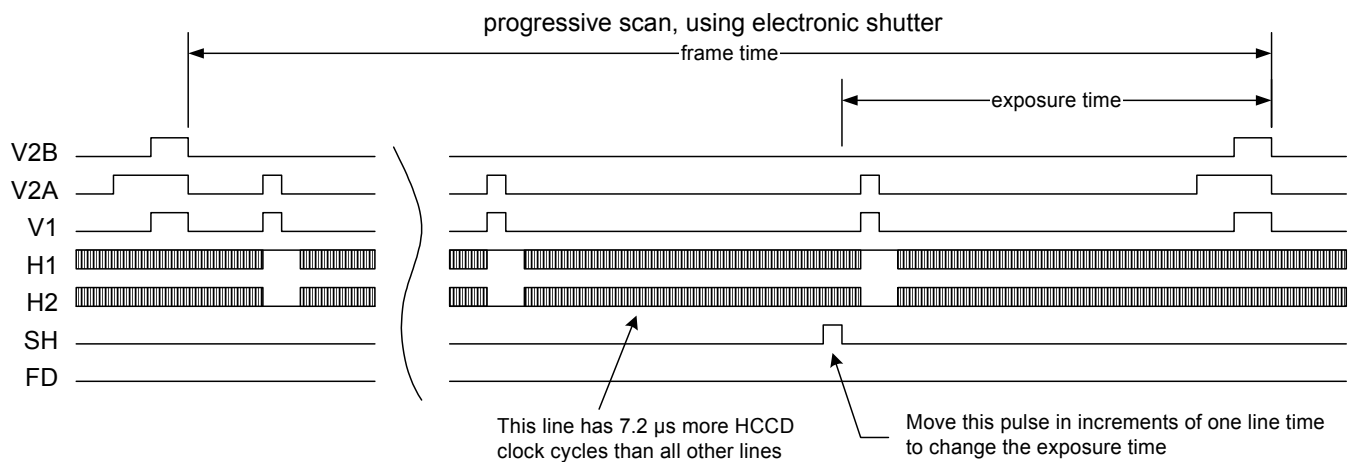
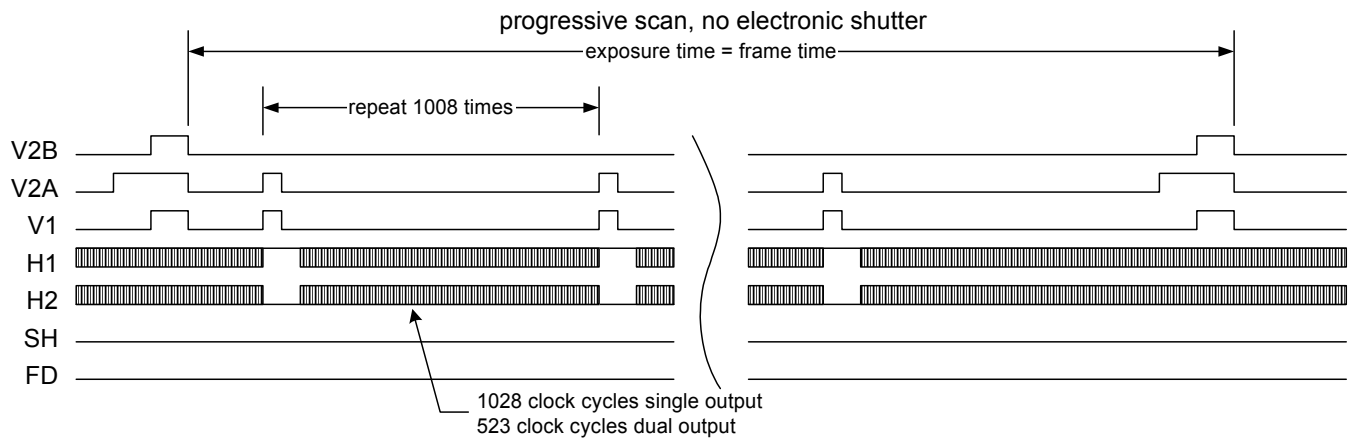
Note that the shutter driver clock input does not use a coupling capacitor. It must be driven directly from a 5V logic buffer as shown in the evaluation board schematic.

Pulse Amplitudes

Clock	Min. Amplitude (volts)	Coupling	Min. Coupling Capacitor Value (μF)	Max. Coupling Capacitor Value (μF)
ϕ SH	3.5	DC	--	--
ϕ H1	4.7	AC	0.1	0.47
ϕ H2	4.7	AC	0.1	0.47
ϕ SA	4.7	AC	0.01	0.47
ϕ SB	4.7	AC	0.01	0.47
ϕ R	4.7	AC	0.01	0.47
ϕ T	4.7	AC	0.01	0.47
ϕ V1	4.0	AC	0.01	0.47
ϕ V2A	4.0	AC	0.01	0.47
ϕ V2B	4.0	AC	0.01	0.47
ϕ FD	4.0	AC	0.1	0.47

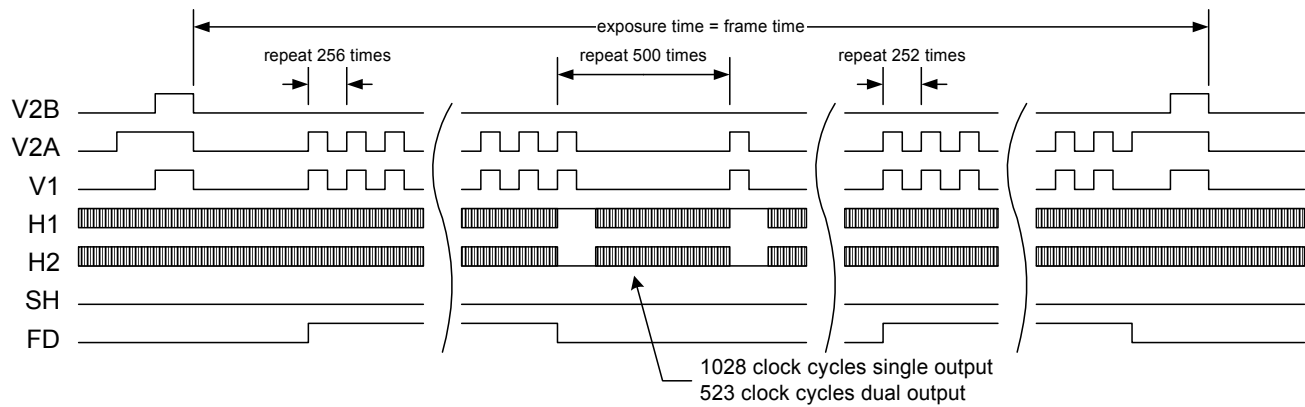
Timing Examples

Progressive Scan

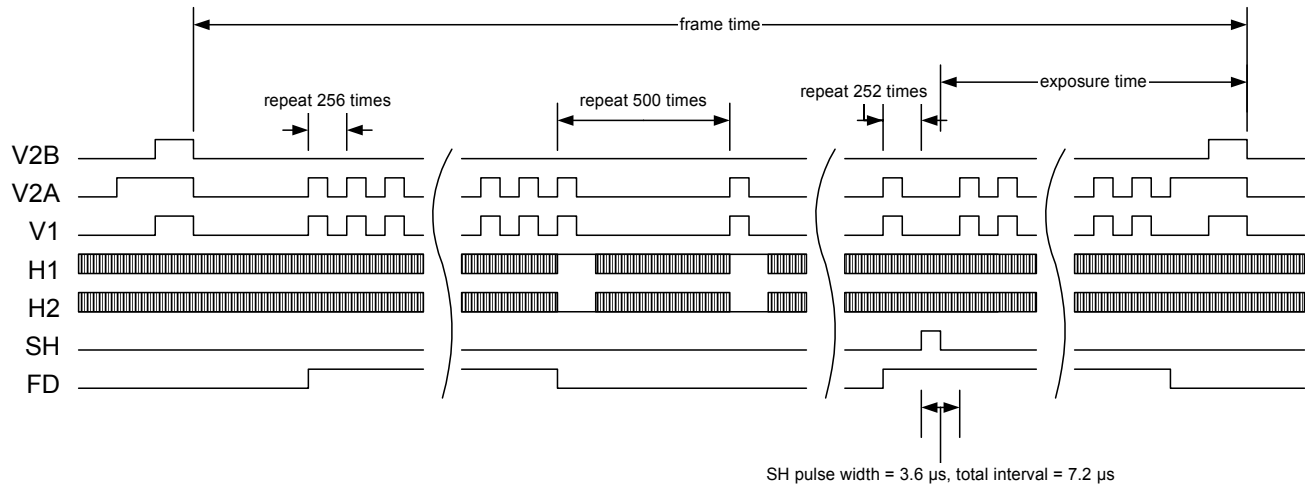


Fast Line Dump

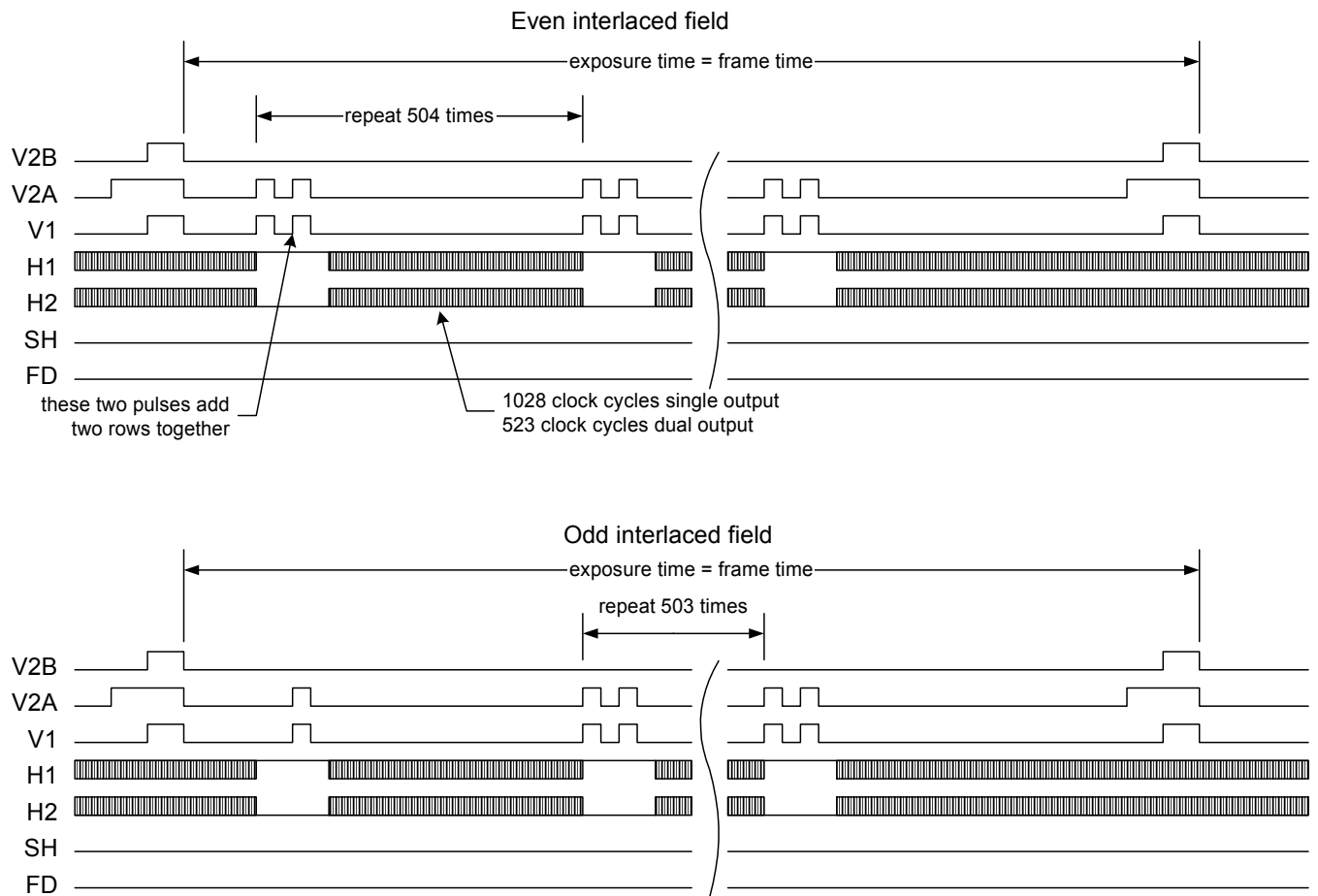
fast dump timing, reads out the center 500 rows



fast dump timing with electronic shutter, reads out the center 500 rows

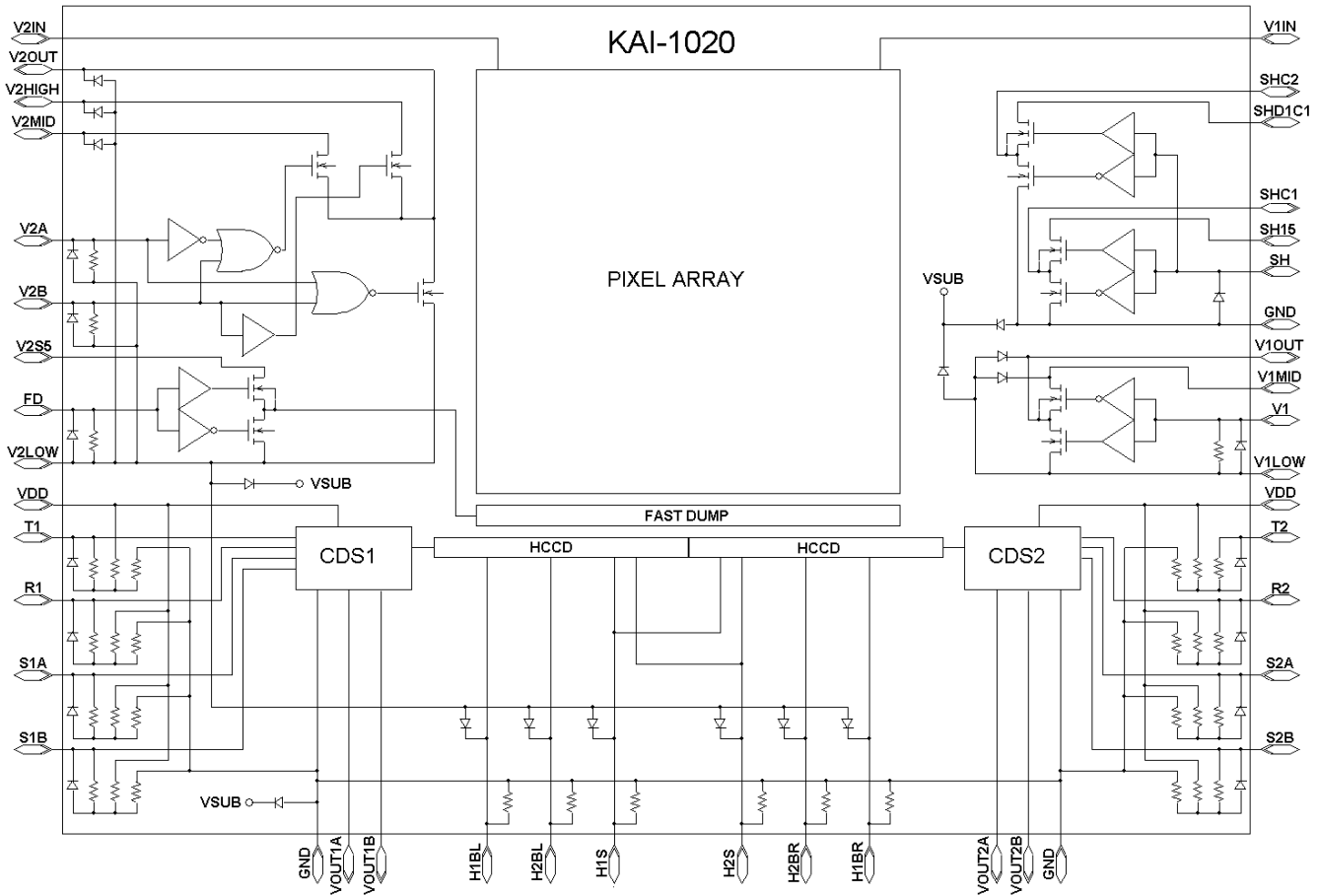


Interlaced – Field Integration



Camera Design

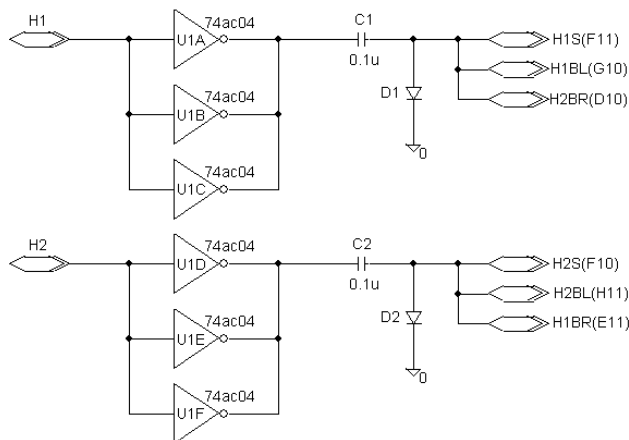
Low level block diagram



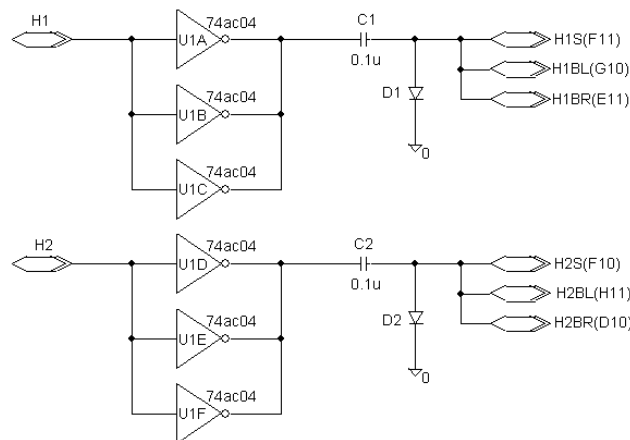
Horizontal CCD Drive Circuit

The HCCD clock inputs should be driven by buffers capable of driving a capacitance of 60pF and having a full voltage swing of at least 4.7 V. A 74AC04 or equivalent is recommended to drive the HCCD. The HCCD requires a 0 to -5V clock. A negative clock level is easily obtained by capacitive coupling and a diode to clamp the high level to GND. Every HCCD clock input has a 300kΩ on chip resistor to GND.

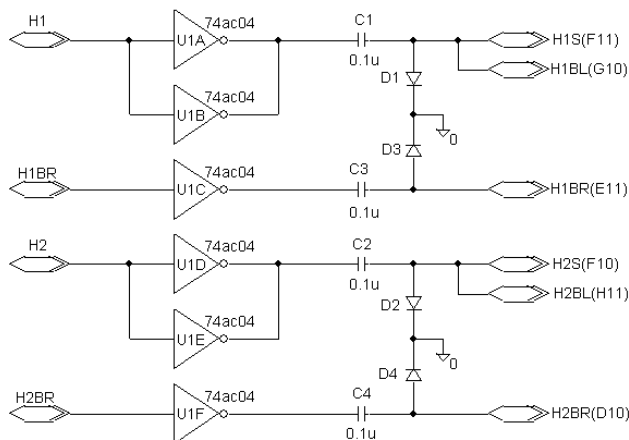
single output only



dual output only



selectable single or dual output



The inputs to the above circuits, H1 and H2, are 5V logic from the timing generator (a programmable gate array for example). If the camera is to have selectable single or dual output modes of operation, then the timing logic needs to generate two extra signals for the H1BR and H2BR timing. For single output mode program the timing such that H1BR=H2 and H2BR=H1. For dual output mode program the timing such that H1BR=H1 and H2BR=H2.

Vertical CCD

The VCCD clock inputs, $\phi V2A$, $\phi V2B$, $\phi V1$, and ϕFD have a capacitive load of approximately 10pF. Each input is connected to V2LOW and V1LOW by a 60k Ω internal resistor. There is also an internal diode connected to V2LOW and V1LOW. The 5V logic drivers must be connected to the sensor inputs through capacitors. These inputs require a clock of at least 4 V amplitude. Most PGA's can drive these inputs directly. The external capacitor and internal diode level shift the 0V to 5V input to V2LOW to V2LOW + 5.

The on chip VCCD clock drivers switch their outputs, V1OUT and V2OUT, between the supply voltages V1LOW, V1MID, V2LOW, V2MID, and V2HIGH. The truth table correlating the voltage on V1OUT and V2OUT to the timing inputs is:

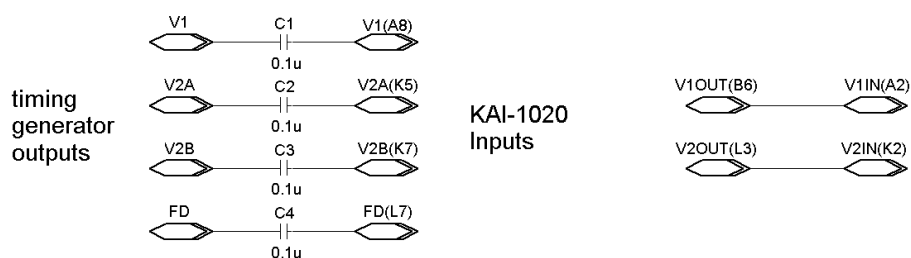
$\phi V1$	V1OUT
L	V1MID
H	V1LOW

$\phi V2A$	$\phi V2B$	V2OUT
L	L	V2LOW
H	L	V2MID
L	H	V2HIGH
H	H	V2HIGH

L = logic low level

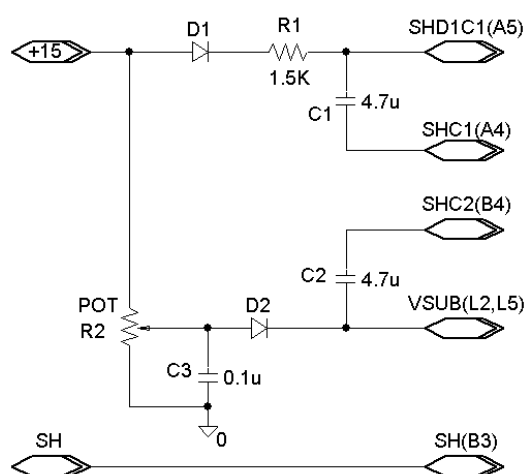
H = logic high level

The output of the VCCD driver is connected to the VCCD gates by wiring V1OUT to V1IN and V2OUT to V2IN. The fast dump driver has no external output. It is wired internally to the VCCD fast dump gate.



Electronic Shutter

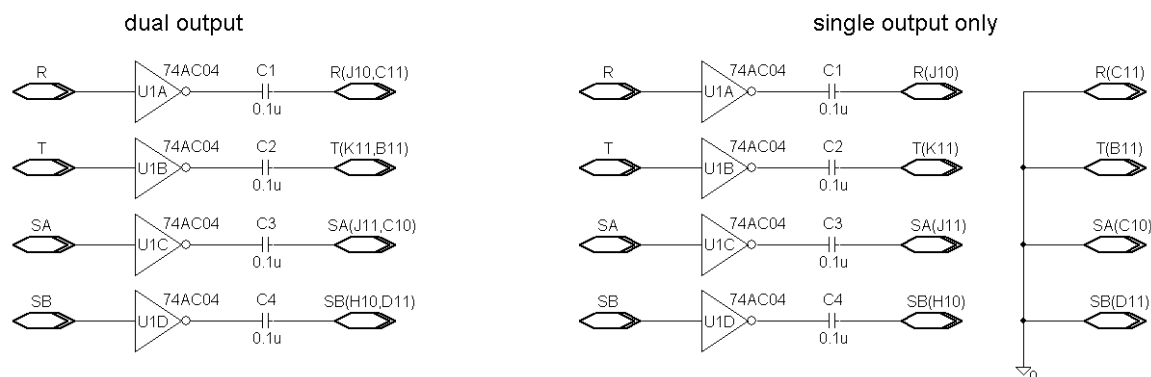
The electronic shutter input, ϕ SH, is the only input driven directly by CMOS logic. No capacitive coupling is required. ϕ SH (pin B3) has approximately a 10pF load. The logic low level must be less than 0.5 V and the logic high level must be greater than 3.5 V. Most programmable gate arrays can drive ϕ SH directly. The on chip electronic shutter driver is a charge pumping circuit. It uses C1, C2, D1, and D2 to generate a >25V pulse that is added onto the substrate DC bias voltage. The substrate bias voltage is set by a trim-pot R2 or by some programmable voltage source. The substrate bias voltage absolutely **MUST** be adjustable. The camera designer **CAN NOT** rely on every KAI-1020 image sensor requiring the same substrate bias. An adjustment range of 8 to 13V must be allowed. Each image sensor has the optimal substrate bias voltage (as measured on the VSUB pin) printed on the shipping container.



The minimum allowed voltage on VSUB is 8 V. Lower voltages may destroy the CDS and clock driver circuits.

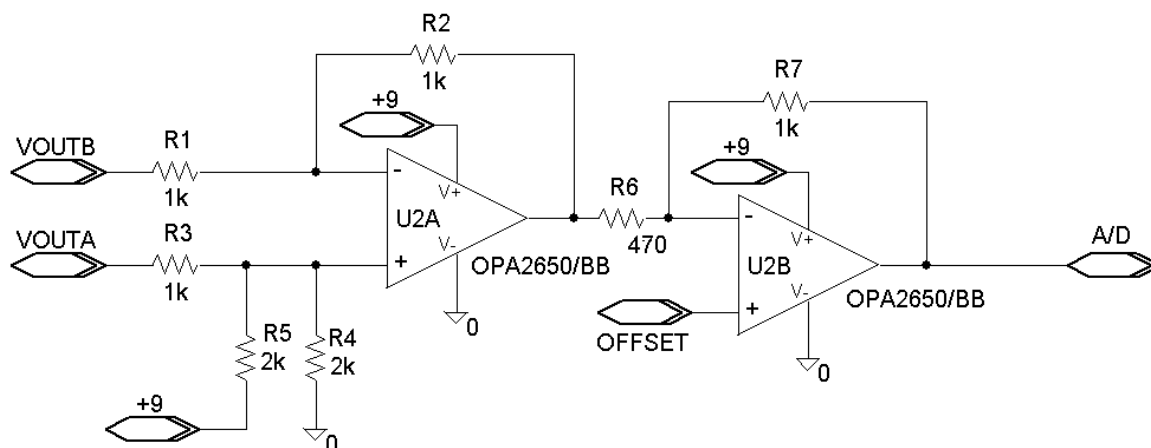
CDS timing inputs

The CDS timing inputs ϕ_R , ϕ_T , ϕ_{SA} , and ϕ_{SB} should be driven by CMOS logic with fast rise and fall times and an amplitude of at least 4.7 V. The capacitance of each pin on the sensor is approximately 10pF. The pulses are level shifted positive by 1 V or 2 V on the sensor. If driving this input directly from a programmable gate array, be aware that some PGA's do not have outputs with amplitudes of 4.7V. It is recommended that the CDS timing inputs be driven by a 74AC04 to insure a 5V pulse amplitude with fast edges.



If the camera will only operate in single output mode then the ϕ_{R2} , ϕ_{T2} , ϕ_{S2A} , and ϕ_{S2B} inputs should be connected to GND. All CDS timing inputs must be coupled with a capacitor.

CDS output circuit



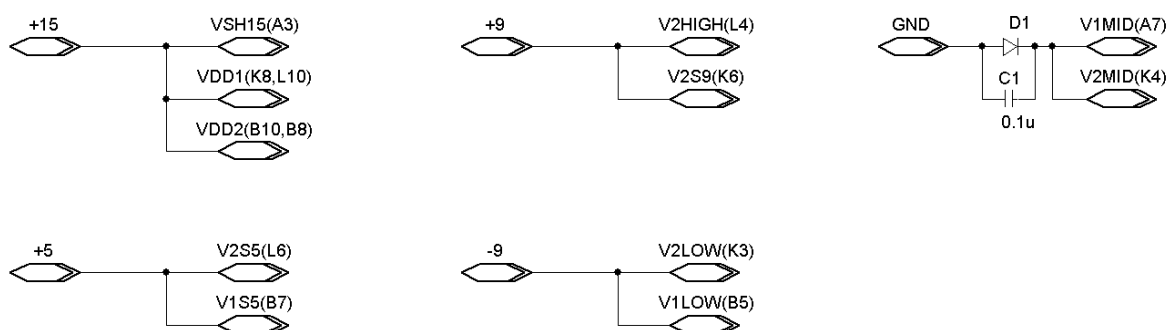
In the above schematic the differential video outputs VOUTB and VOUTA are subtracted by op-amp U2A. The video outputs will have a DC level of 7 to 11V. U2B then inverts the signal and applies a gain of 2.1 relative to the offset voltage. The output of U2B will match the 500mV output range of the KAI-1020 to the 1V input range of the analog to digital converter (A/D).

VOUTB will swing in the negative direction with increasing light level. The output of U2A will swing in the positive direction with increasing light level. The output of U2B (input to the A/D) will swing in the negative direction. This means the A/D output will be 0 counts when the image sensor is saturated. The digital data will have to be inverted before being transmitted to a digital image capture device. See the KAI-1020 evaluation board schematic for a simple method of inverting the data with no additional components.

The offset will have to be dynamically adjusted to match the zero light level of the image sensor. A circuit should examine the digital data in the dark reference columns and adjust the offset voltage of U2B to maintain a constant zero reference level in the A/D converter. The dynamic adjustment of the offset voltage will remove most temperature dependent drifts. Small temperature-dependant gain changes will still be present. See the KAI-1020 evaluation board schematic for an example of a circuit to generate the offset voltage.

This output circuit provides 10 bits of dynamic range on the KAI-1020 evaluation board. It is not the optimum circuit. For optimum differential common mode noise rejection and linearity, the CDS output circuit should take into account the 160 Ω impedance of the CDS output drive transistor.

Power Supplies



The V1MID and V2MID connections must be set to -0.6 to -1.5 V. Since V1MID and V2MID only sink current, a diode can be used to set this voltage.

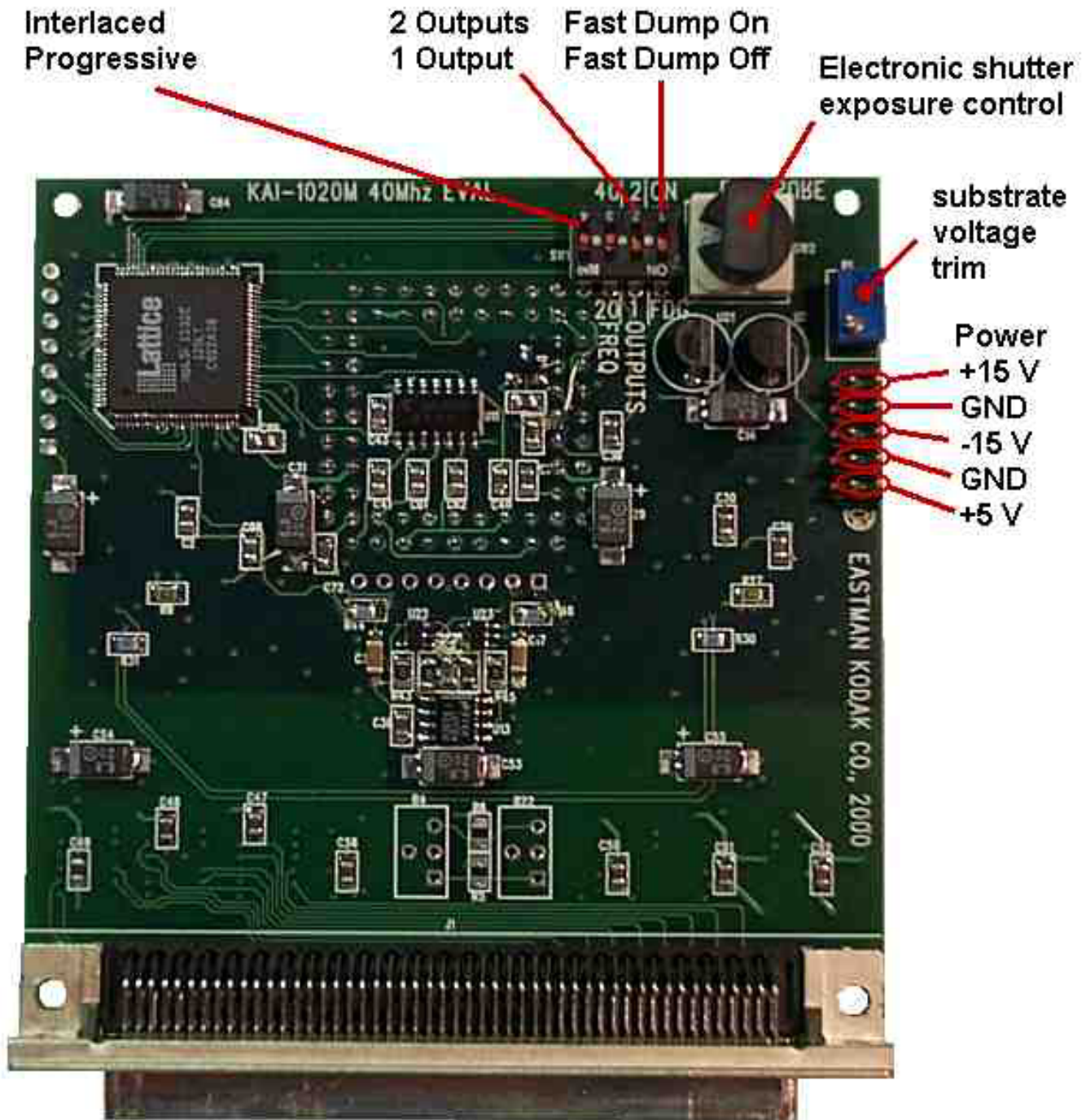
If the sensor is to use only the single output mode, then VDD2(B10, B8) can be connected to GND. VOUT2A(A9) and VOUT2B(A10) also should be connected to GND in the single output only mode.

KAI-1020 Evaluation Board

Front side

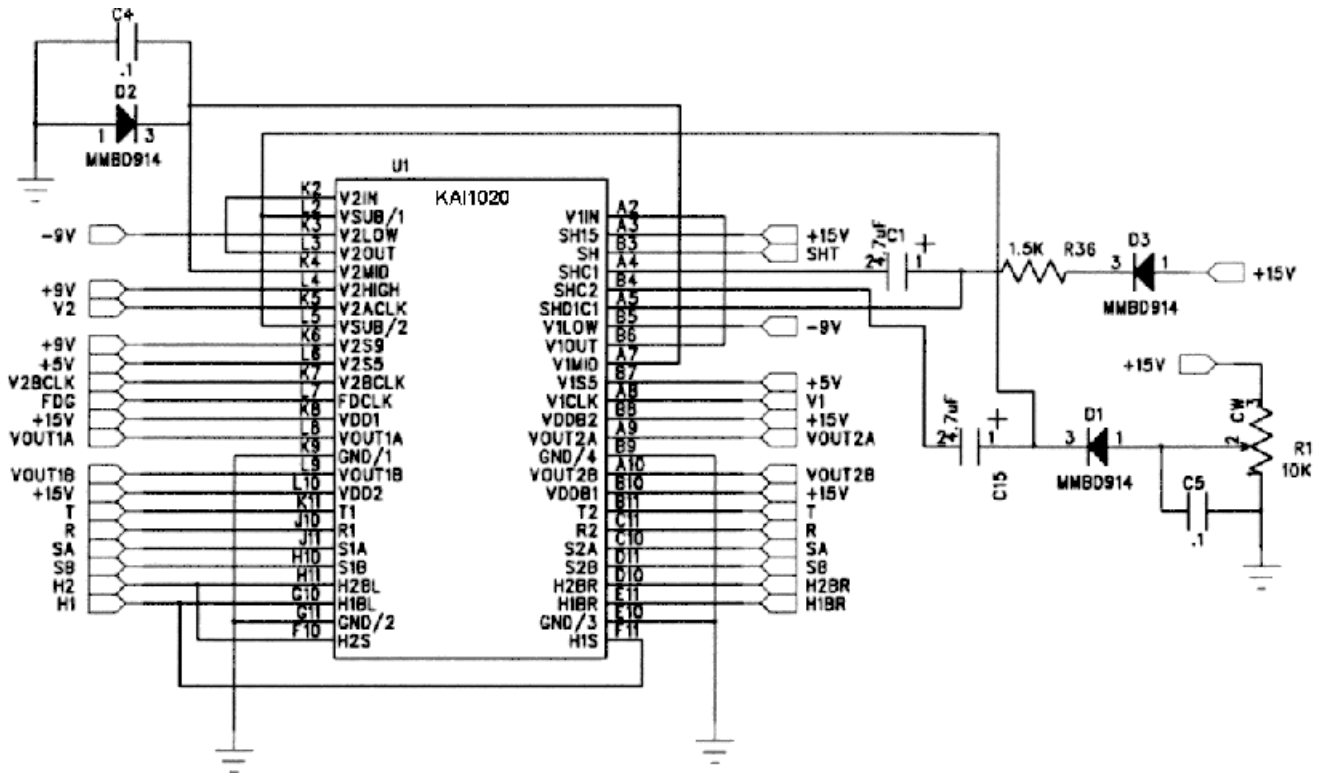


Back Side

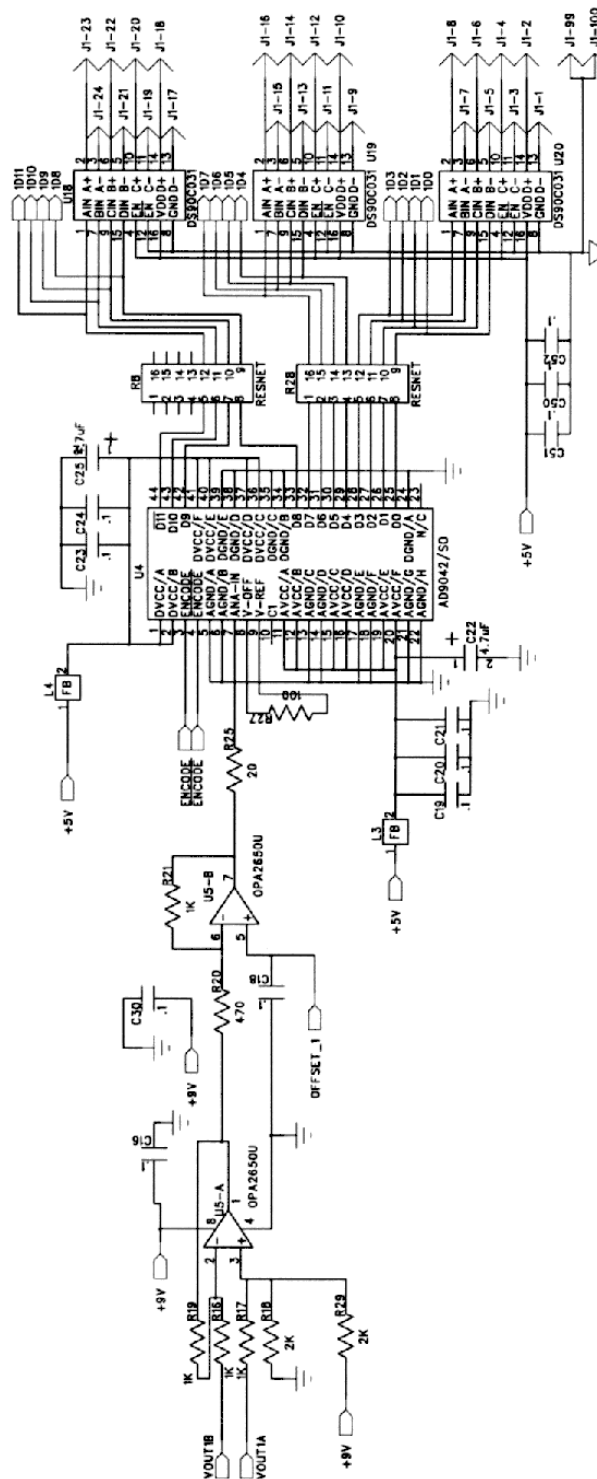


Schematics

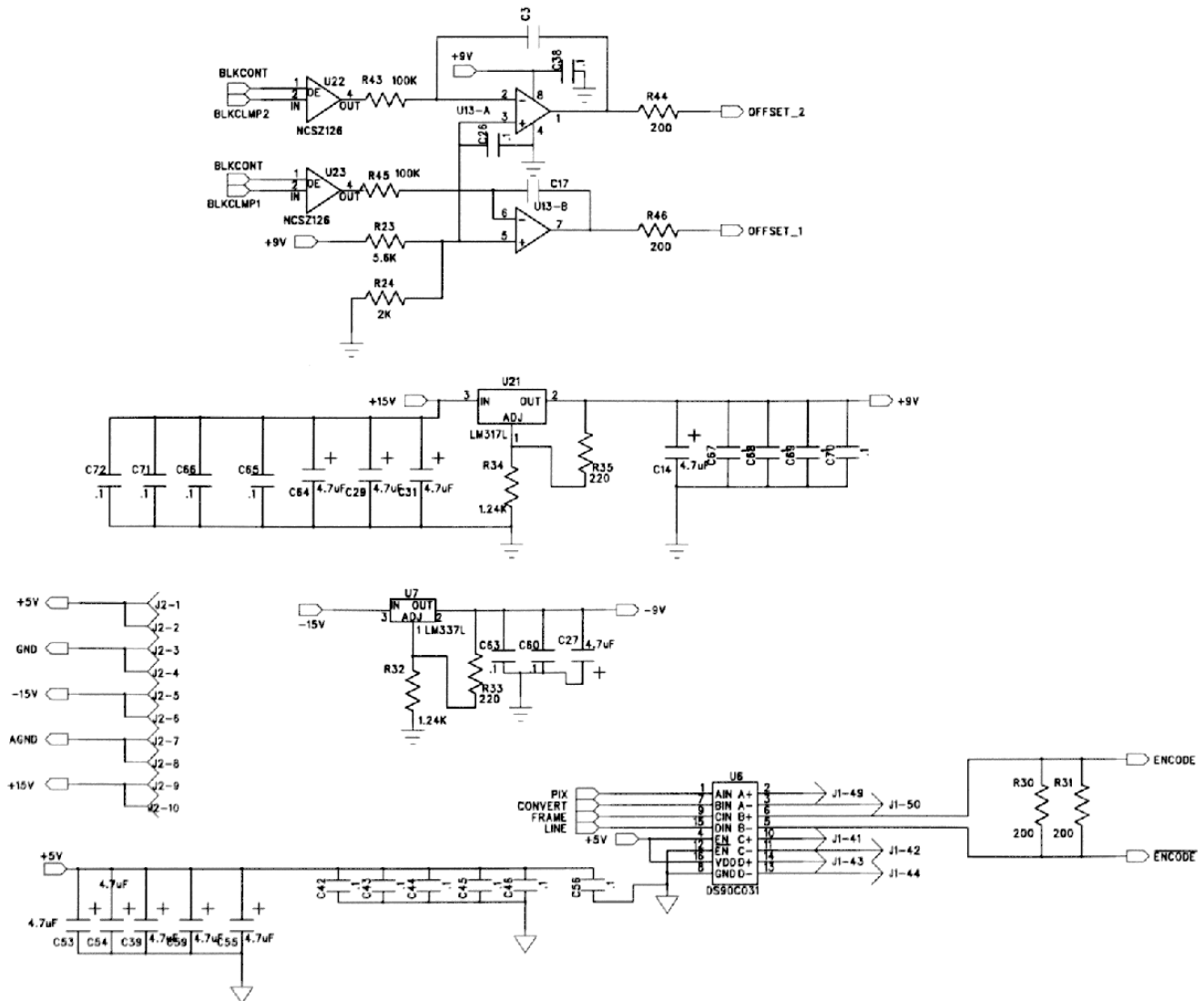
KAI-1020



Output 1



Automatic offset and power supply



Parts list

C1	PCAP, 4.7μF
C2	CAP, 0.1μF
C3	CAP, 1μF
C4-9	CAP, 0.1μF
C10	CAP, 4.7μF
C11, C12	CAP, 0.1μF
C13-15	CAP, 4.7μF
C16	CAP, 0.1μF
C17	CAP, 1μF
C18-21	CAP, 0.1μF
C22	CAP, 4.7μF
C23, C24	CAP, 0.1μF
C25	CAP, 4.7μF
C26	CAP, 0.1μF
C27	CAP, 4.7μF
C28	CAP, 0.1μF
C29	CAP, 4.7μF
C30	CAP, 0.1μF
C31	CAP, 4.7μF
C32-38	CAP, 0.1μF
C39	CAP, 4.7μF
C40-52	CAP, 0.1μF
C53-55	CAP, 4.7μF
C56-58	CAP, 0.1μF
C59	CAP, 4.7μF
C60-63	CAP, 0.1μF
C64	CAP, 4.7μF
C65-72	CAP, 0.1μF
D1-3	MMBD914
D4, D5	MMBD2837

R1	VRES,10K
R2	RES,470
R3	RES,1K
R7	RES,20
R8	RESNET
R9	RES,100
R10, R11	RES,1K
R12	RES,2K
R13	RES,1K
R14	RESNET
R15	RESNET
R16, R17	RES,1K
R18	RES,2K
R19	RES,1K
R20	RES,470
R21	RES,1K
R23	RES,5.6K
R24	RES,2K
R25	RES,20
R26	RES,2K
R27	RES,100
R28	RESNET
R29	RES,2K
R30	RES,200
R31	RES,200
R32	RES,1.24K
R33	RES,220
R34	RES,1.24K
R35	RES,220
R36	RES,1.5K
R43	RES,100K
R44	RES,200
R45	RES,100K
R46	RES,200

SW1	DIP8	4 POS DIP SW
SW2	DIAL	16 POS ROTARY
U1	KAI1020	IMAGE SENSOR
U2	AD9042/SO	A/D ANALOG DEV
U3	OPAMP DUAL,OPA2650U	BURR BROWN
U4	AD9042/SO	A/D ANALOG DEV
U5	OPAMP DUAL,OPA2650U	BURR BROWN
U6	DS90C031	NATIONAL
U7	LM337L	
U8	LAT1032E TQFP100	LATTICE SEMI
U9	74AC04	
U10	DELAY10	DATA DELAY DEV 711 2.5 ns
U11	74AC04	
U12	LAT1016	LATTICE SEMI
U13	OPAMP-DUAL, LMC6492BEM	NATIONAL
U14	OSC\SO	80 MHZ
U15-20	DS90C031	NATIONAL
U21	LM317L	
U22, U23	NC7SZ126	FAIRCHILD
L1-4	FB	FERRITE BEAD
J1	SCSI-100	
J2	HEADER10	POWER CONN
J3	SIP\8P	PROGRAM CONN
J4	LATCON	PROGRAM CONN

Digital output connector

The output connector is a 100 pin female SCSI type connector, pin compatible with the National Instruments PCI-1424 digital frame grabber, part number 777662-02. The interface cable is available from National Instruments, part number 185012-02.

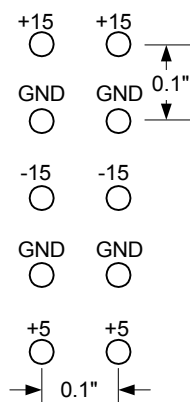
Output 1	Pin
data 0+	1
data 0-	2
data 1+	3
data 1-	4
data 2+	5
data 2-	6
data 3+	7
data 3-	8
data 4+	9
data 4-	10
data 5+	11
data 5-	12
data 6+	13
data 6-	14
data 7+	15
data 7-	16
data 8+	17
data 8-	18
data 9+	19
data 9-	20
data 10+	21
data 10-	22
data 11+	23
data 11-	24

Output 2	Pin
data 0+	51
data 0-	52
data 1+	53
data 1-	54
data 2+	55
data 2-	56
data 3+	57
data 3-	58
data 4+	59
data 4-	60
data 5+	61
data 5-	62
data 6+	63
data 6-	64
data 7+	65
data 7-	66
data 8+	67
data 8-	68
data 9+	69
data 9-	70
data 10+	71
data 10-	72
data 11+	73
data 11-	74

Sync	Pin
pixel +	49
pixel -	50
line +	43
line -	44
frame +	41
frame -	42
field index	45
GND	99
GND	100

All other pins have no connection. All outputs are driven by low voltage differential line drivers (LVDS) except for the field index which is TTL.

Power Connector



The evaluation board requires +15 V, -15 V, and +5 V. The current draw for each supply is:

Supply	Current (mA)
+15	62
-15	18
+5	780

Mode Switch

Switch	On	Off
1	Fast Dump off	Fast Dump on
2	1 output	2 outputs
3	---	----
4	Progressive scan	Interlaced

When the fast dump is activated the timing dumps the first 256 lines, then reads out 512 lines of image data, and finally it dumps the last 240 lines. The resulting image is 1000 columns by 512 rows. The interlaced mode timing is not programmed to support fast dumping.

Exposure Switch

All exposure times are in μ s. Electronic shuttering is not programmed into the timing generator for interlaced mode.

Exposure Setting	FD off		FD on	
	1 output	2 outputs	1 output	2 outputs
0	33300	20600	20600	14160
1	16400	10160	6000	4400
2	7960	4960	3000	2540
3	3740	2320	1860	1840
4	1616	1016	1700	1700
5	564	362	824	824
6	298	198	460	460
7	68	55	93	93

Substrate Voltage Trim

This variable resistor allows the substrate voltage to be varied from 0V to 15V. Adjusting this voltage will change the charge capacity and anti-blooming of the pixel photodiodes. Do not adjust the voltage below 8 V.

Evaluation Board Notes

Timing

The main timing is generated by a programmable gate array U8. The HCCD drive is setup for selectable single or dual output by inverting the H2BR and H2BL timing signals depending on the setting of the mode switch SW1.

The short pulses for ϕ_R , ϕ_T , ϕ_{SA} , and ϕ_{SB} are generated by combining (logical and/or) the outputs of the delay line U10. Each tap on U10 delays the system clock by 2.5ns.

The amount of noise in the KAI1020 will have a strong dependence on the stability of the timing inputs. The most sensitive inputs are the HCCD and the CDS timing inputs. The evaluation board uses one PGA (U8) to hold all of the counters and to generate the CDS timing. This is not the optimum arrangement. Though gray code counters were used, some fixed pattern column noise can be seen in the image from the counters inside U8. The counters inside U8 cause small disturbances of the HCCD and CDS timing. One solution to eliminate this noise source is to separate the counters and CDS pulse generation into two separate PGA's. One PGA would contain all of the counters for the rows and columns, and send a HCCD gating signal to a second PGA. The second PGA would output the HCCD clock as well as form the CDS timing pulses from the multi-tap delay line U10. This second PGA would contain no counters.

Output channel

The output circuit is identical to section 0. The two op-amps U5A and U5B present an inverted signal to the ADC U4. The offset circuit will maintain the digital output of U4 at 4080 when the image sensor is in the dark. The output of U4 will be zero when the image sensor is saturated with light. The digital data is inverted by swapping the high and low outputs of the differential line drivers on the output connector.

Automatic offset

U12 is used to control the automatic offset circuit. U8 sends a signal to U12 on the line BLKLEV when the output of the analog to digital converter corresponds to the center 10 columns of the KAI1020 dark reference. When U12 receives the signal from U8, U12 compares the outputs of the A/D converters to the number 4080. If the output is above or below 4080, U12 enables the buffers U22 and U23 and sets their inputs to cause the integrators U13A and U13B to raise or lower the offset voltages.

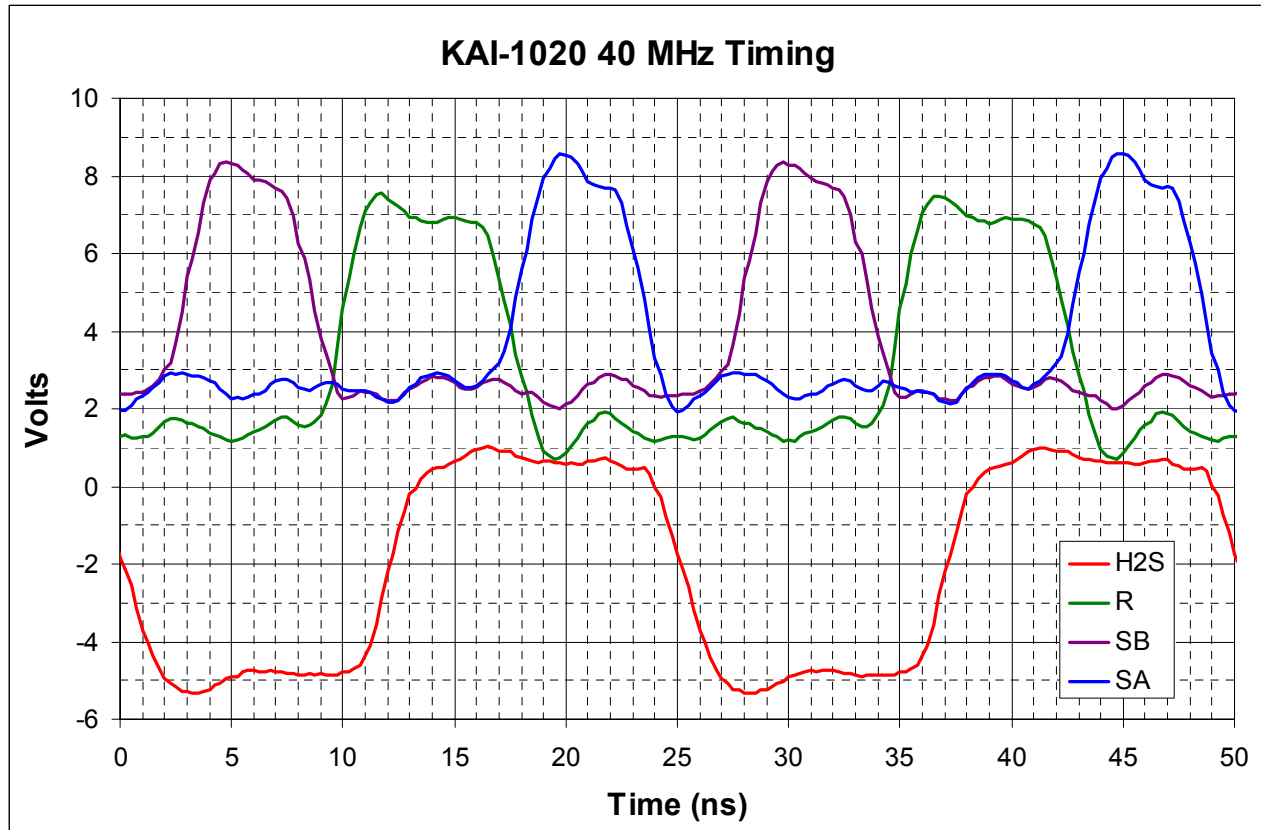
A separate PGA (U12) is used to monitor the output of the A/D converters. This function should not be combined with U8 into one PGA. If only one PGA is used then the digital data will cause noise in the timing outputs to the image sensor. This is especially true when the A/D outputs are near a major bit boundary, such as 2048 or 1024. At these bit boundaries there are a large number of bits changing value that would disturb the stability of the HCCD and CDS clocking.

The automatic offset updates the offset every line. This does cause some noise in the image because the offset changes slightly each line time. An improved offset circuit would measure the offset error along the entire column and then correct the offset voltage once per frame.

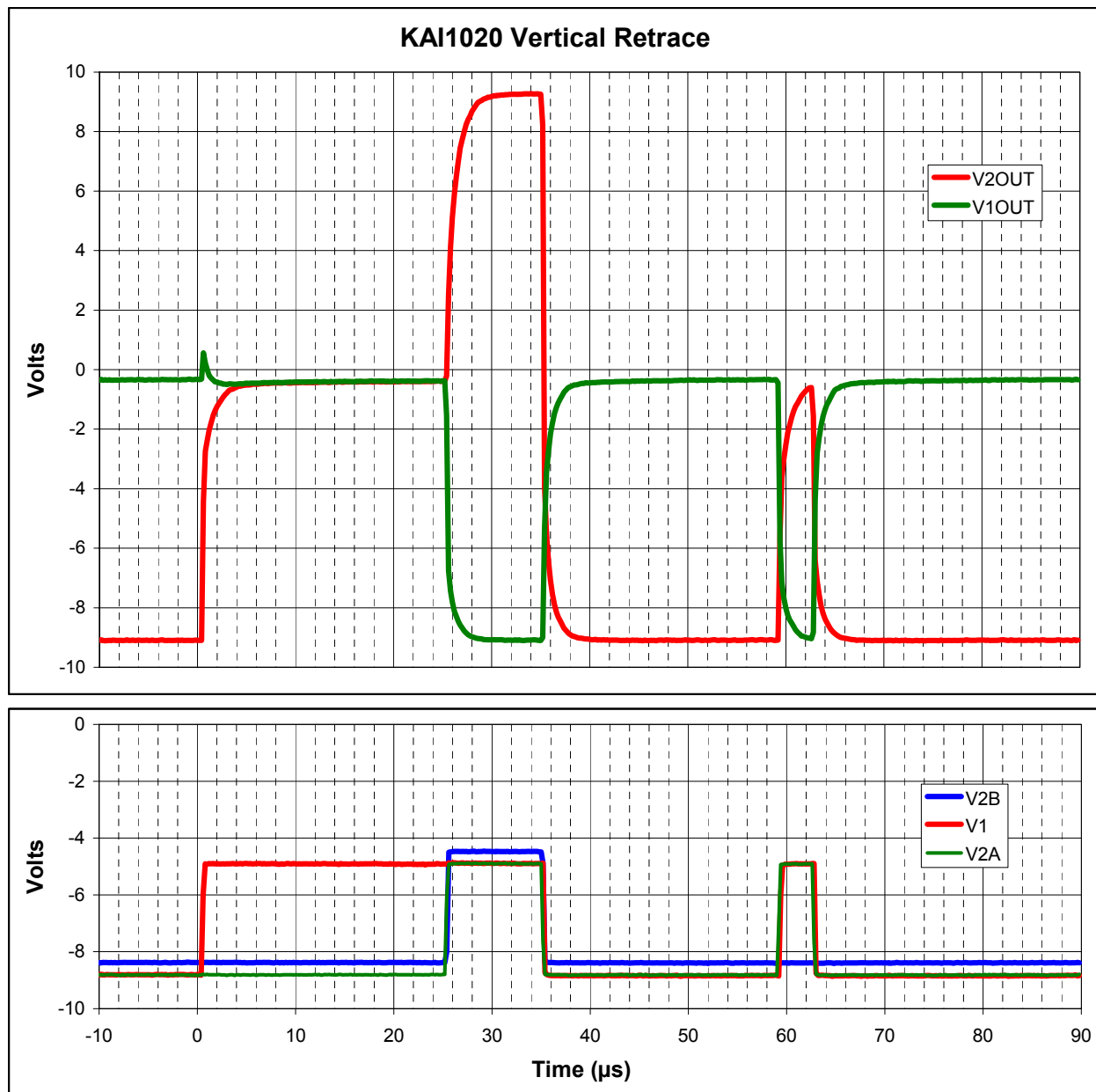
Oscilloscope Traces

This sections contains oscilloscope traces of signals measured on the KAI1020 pins. Some of the timing signals are not 0 to 5V because the KAI1020 has level shifted the signals. All signals were measured on the KAI1020 evaluation board.

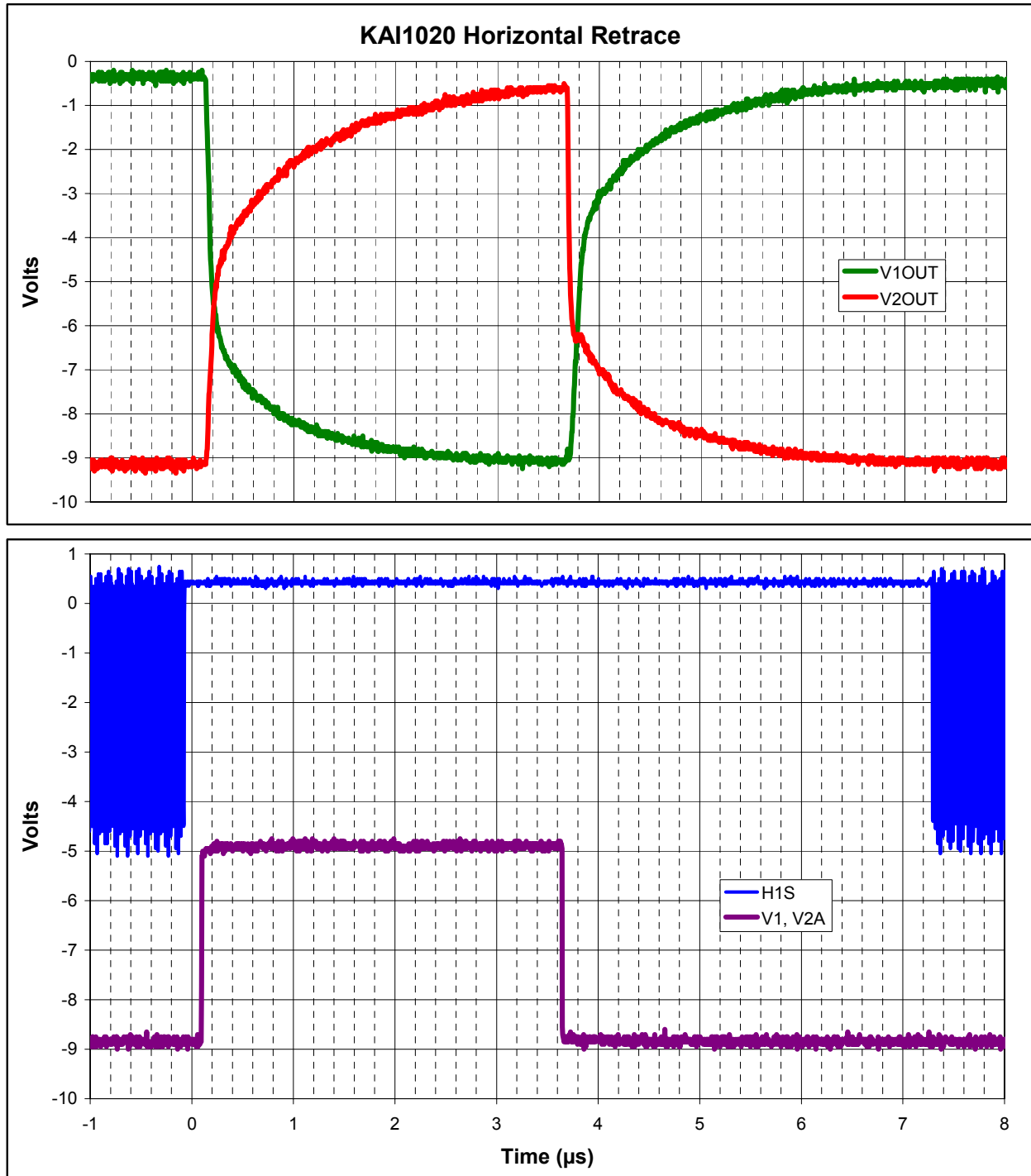
CDS Timing



Vertical Retrace



Horizontal Retrace



Revision Changes

Revision Number	Description of Changes
0	Original formal version.
1	Correct VS29 connection to 9 volt supply, not 15 volt supply in schematic on page 42. Added Revision Changes
2	Added section 1.3.5 General – Color Added section 1.4.2 Color Quantum Efficiency Added section 1.4.3 Color Filter Array Pattern Updated section 2.2.1 Pin Grid Array Package Drawing Added section 2.2 Leadless Chip Carrier Package Added section 3 Glass Section 5.6 Changed “DC level of 7 to 9C” to “DC level of 7 to 11V” Section 6.5 Parts List U13: Corrected from OPAMP-DUAL LM 649BEM to LMC6942BEM U22, U23: Corrected from NCSZ126 to NC7SZ126
3	Updated page layout. Section numbers removed. Updated drawing in section 1.2 to show buffer columns and rows. Updated section 1.4.1 Monochrome Quantum Efficiency. Updated section 1.4.3 CFA pattern to show buffer columns and rows. Updated section 1.9 Quality Assurance and Reliability. Added section 1.10.1 Available Part Configurations. Updated section 3.1 Pin Grid Array Package Cover Glass. Glass changed from clear to MAR. Updated section 3.3 Glass Transmission. Section 4.11.2 Bias Voltages, changed V1MID and V2 MID from min –1.5, nom –1.0, max –0.5 to min –1.5, num –1.2, max –1.0 Section 4.11.2 Added power up sequence note.
4	Corrected figure on page 4. Buffers rows and columns were incorrect. Changed from 4 rows/columns to 2 rows/columns. Corrected figure on page 8. Buffers rows and columns were incorrect. Changed from 4 rows/columns to 2 rows/columns.