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A.HE84772 Introduction

HE84772 is a 8-bit CMOS micro-controller. This IC has 32 COM (4096-dot LCD driver + 24 Bit I/O Port) ….. (3328-dot LCD driver + 48 Bit I/O Port) LCD driver, or 48 COM (5376-dot LCD driver + 24 Bit I/O Port) …. (4224-dot LCD driver + 48 Bit I/O Port) or 64 COM (6144-dot LCD driver + 24 Bit I/O Port) …. (4608-dot LCD driver + 48 Bit I/O Port), or 80 COM (6400-dot LCD driver + 24 Bit I/O Port) …. (4480-dot LCD driver + 48 Bit I/O Port) LCD driver has various combination (depends on Mask Option).It has built in voltage regulator which makes the LCD maintain a stable display. It has built-in one internal Op-Amp, can be used in light, speech, temperature and humidity sensor application. It built-in an internal Voltage detector circuitry which can be used for low battery detection. One 7-bit D/A converter and one PWM output module to provide a speech output interface. Use the built-in 512K Byte ROM which can store around large volume of data including voice, graphics and data.
The HE84772 provides a very simple and effective instruction set, each instruction byte occupies only 1.5 clock cycle time, therefore, it is suitable to apply in the high performance systems.

B.HE84772 Features

- Operating Voltage: 2.4V – 3.6V
- Operation frequency Range: DC ~ 8MHz @ 3.6V
  DC ~ 4MHz @ 2.4V
- ROM size: 512K Bytes (256K Program ROM + 256K Data ROM)
- RAM size: 16K Bytes
- Dual Clock: Normal(Fast) clock: 32.768K ~ 8MHz (No Internal Clock)
  Slow clock: 32.768KHz
- Operating Mode: DUAL，FAST，SLOW，IDLE，SLEEP
- Built-in WATCH DOG TIMER
- 24-48 bi-directional I/O pins, PUSH-PULL or OPEN DRAIN output selected by mask option
- Special designed hardware auto scanning keyboard (4*20), it can both lower the cost of hardware (share with LCD SEG PIN) and lower the burden of software
- Built-in an internal Op-Amp
- Built-in voltage detector, it consists of two testing points: Vth=2.2v/2.4v
- Either of the following combination can be selected: 32COM*128SEG LDC DRIVER or 48COM*112 SEG LDC DRIVER or 64COM*96 SDG LDC DRIVER or 80COM*80SDG LDC DRIVER. All of these are selected B TYPE. Built-in one voltage regulator. Please refer to application circuit, the maximum LCD voltage, the LVP, must be less than 8.5Volt.
- Built-in a PWM output circuit (No rate selection, connect with VDD & PWMP)
- Provides three internal and two external interrupt
- Provides two 16-bit timer, one time-base timer
- Instruction Set : 32 Instructions, 4 types of Addressing Mode, 2 individual Pointer for ROM Used to access and store data into the 21-bit TABLE POINTER and also read/write the 11 bits DATA POINTER from RAM

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D. Pin Assignment

Pin	Pin Name	I/O	Function	Description
106 105	**FXI,** **FXO**	B, O	External Fast Clock pin. To connect the Crystal or R,C oscillation to generate 32.768KHz ~ 8MHz system clock.	Mask Option settings : MO_FCK/SCKN=00：Slow Clock only 01：Illegal 10：Dual Clock 11：Fast Clock only MO_FOSCE=0：Internal fast oscillation 1：External fast oscillation MO_FXTAL=0：R,C oscillation for Fast Clock 1：Crystal oscillation for Fast Clock MO_SXTAL=0：R,C oscillation for 32.768K Clock 1：X'tal oscillation for 32.768K Clock
109 108	**SXI,** **SXO**	I, O	External Slow Clock pin . To connect the 32.768KHz oscillator to generate the stable frequency for Slow Mode, provide LCD for HE84772 and Timer 1 clock source.。	Program the value of OP1and OP2 to change the operating modes (Normal, Slow, Idle and Sleep). In Dual Clock mode，the system runs in Fast Clock, only LCD & Timer 1 use the 32.768K clock source.
104	**RSTP_N**	I	System reset signal	Pull this pin to low level to reset the system. Besides, Select the Mask Option (MO_PORE=1) to enable the HE84772 internal Power-on Reset function. In addition, the MO_WDTE is used for Watch Dog Timer setting： MO_WDTE =0：Disable Watch Dog Timer =1：Enable Watch Dog Timer
107	**TSTP_P**	I	Test Pin. Pull the pin to high level to enter into testing mode.	Connect TSTP_P TO to a TEST POINT, and to make it floating. Test can be done on PCB
129. .136	**PRTC[7:4]/** **SCNI [3:0]** **PRTC[3:0]**	B	Port C bi-directional I/O pin (8 pins) or **PRTC[7:4]** can be used for key scan Dedicated input pin	Mask Option MO_CPP[7:0] to preset the output type: MO_CPP=1 : Push-pull output； = 0 : Open-drain output. When assigned the port to input pin, send a '1' and read the result to get the input value.
119 126	**PRTD[7:0]**	B	Port D bi-directional I/O pin, (8 pins). PRTD[7:2] is also a Wake-up pin and PRTD[7:6] is used for interrupt input pin.	Mask Option MO_DPP[7:0] to preset the output type: MO_DPP=1 : Push-pull output； 0 : Open-drain output. When assigned the port to input pin, send a '1' and read the result to get the input value.
111.. 118	**PRT10[7:0]**	B	Port D bi-directional I/O pin, (8 pins).	Mask Option MO_10PP[7:0] set output type： MO_10PP ='1'，then Push-pull output； ='0'，then Open-drain output。 When assigned the port to input pin, send a '1' and read the result to get the input value.

Pin	Pin Name	I/O	Function	Description
26..33	**PRT14[7:0]/ SEG [23:16]**	B/O	Port 14 bi-directional I/O pin, (8 pin) or LCD Segment [23:16]	Mask Option MO LIO14 [7:0] set these 8 pins to be I/O or LCD Segment： MO_LIO14[7:0] =0; I/O Pin=1, LCD Pin。 When pin assigned to be I/O pin, use Mask Option MO_14PP[7:0] to preset the output MO_14PP[7:0]=1 : Push-pull output； 0 : Open-drain output.
34..41	**PRT15[7:0]/ SEG [15:8]**	B/O	Port 15 bi-directional I/O pin, (8 pin) or LCD Segment [15:8]	Mask Option MO LIO15 [7:0] set these 8 pins to be I/O or LCD Segment： MO_LIO15[7:0] =0; I/O Pin=1, LCD Pin。 When pin assigned to be I/O pin, use Mask Option MO_15PP[7:0] to preset the output MO_15PP[7:0]=1 : Push-pull output； 0 : Open-drain output.
42..49	**PRT17[7:0]/ SEG [7:0]**	B/O	Port 17 bi-directional I/O pin, (8 pin) or LCD Segment [7:0]	Mask Option MO LIO17 [7:0] set these 8 pins to be I/O or LCD Segment： MO_LIO17[7:0] =0; I/O Pin=1, LCD Pin。 When pin assigned to be I/O pin, use Mask Option MO_17PP[7:0] to preset the output MO_17PP[7:0]=1 : Push-pull output； 0 : Open-drain output.
6..25	**SGKY[43:24] /SCNO [19:0]**	O	LCD Segments / key scan out; exist simultaneously	MO_LCDKEY =0: LCD SGKY[43:24] as SEG/KEY SCAN =1: LCD SGKY[43:24] as SEG pin only
50..81	**COM[31:0]**	O	LCD COMmon Output	Refer LCD and RAM map.
185..138	**CMSG[79:32]**		COM[79:32]/ SEG[80:127]	
186..216 1..5	**SEG[79:44]**	O	LCD SEGment Output	
82	**L LV1**	P	LCD Bias Volt 1	LVP>LV5>LV4>LV3>LV2>LV1.
83	**L LV2**	P	LCD Bias Volt 2	LVP-0.5 >= LV5 (be sure to keep 0.5 volt between LVP and LV5 at lease.)
84	**L LV3**	P	LCD Bias Volt 3	
85	**L LV4**	P	LCD Bias Volt 4	Adjust Resistor (R2) between LGS2 and LV5 to set LV5 for LCD glass. The formula is LV5 = (1 + R2/80K)*0.9V
86	**L LV5**	P	LCD Bias Volt 5	
96	**LGS1**	I	Regulator Voltage setting	Could adjust LVREG voltage
87	**LGS2**	I	LCD Drive Voltage setting	For LV5 voltage setting
88	**LVP**	P	Charge Pump Output	LVP=3(,4,5)*LVREG which setting by external Capacitor set LVP must be small than 8.5V
89	**LCAP4A**	O	Charge pump capacitor pin	Different capacitor Configuration make LVP = 3*(,4,5)* LVREG The LCD driving circuit here makes regulation first, then charge pump to LVP. It generates bias voltage based on LVP
90	**LCAP2B**	O	Charge pump capacitor pin	
91	**LCAP2A**	O	Charge pump capacitor pin	
92	**LCAP1A**	O	Charge pump capacitor pin	
93	**LCAP1B**	O	Charge pump capacitor pin	
94	**LCAP3A**	O	Charge pump capacitor pin	
95	**L VREG**	O	Voltage regulator output (To charge Pump Input	Adjust to ~2.0 Volt by Resistor between LGS1 and LVREG

Pin	Pin Name	I/O	Function	Description
97	**L VAG**	O	Reference Voltage output	Fixed 0.9 Volt DC
128	**PWM**	O	PWM Output, can be used to drive Speaker or Buzzer. As Voice output	Preset VOC register Bit2: PWM = 1; Turn on PWM
99	**VO**	O	D/A voice output	Preset the Bit-1 of VOC register: DA=1；turn on VO.
100	**DAO**	O	D/A Output, for OP-Amp use	Preset the Bit-0 of VOC register: OP=1；turn on DAO.
101	**OPIN**	I	OPAMP Inverting I/P pin	Preset the Bit-0 of VOC register: OP=1；turn on OP.
102	**OPIP**	I	OPAMP Non-inverting I/P pin.	Individual built-in OP-Amp
103	**OPO**	O	OPAMP O/P pin	
110	**VDD**	P	Positive Power Input	2 Pair of Power Pin: This two set power pin is separated inside. Adding two 0.1μF capacitor as by-pass capacitor on each set is necessary
98	**GND**	P	Power Ground Input	
137	**VDD_RAM**	P	Dedicated Power for RAM	
127	**GND_PWM**	P	Dedicated GND for PWM	

E. LCD RAM MAP

This IC consists of 32COM, 48COM, 64COM and 80COM four different types of LCD driving method, the RAM map is as follow:

32COM:

Page 7	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]
COM0	7E0H	7C0H	7A0H	780H	760H	740H	720H	700H
COM1	7E1H	7C1H	7A1H	781H	761H	741H	721H	701H
:	:	:	:	:	:	:	:	:
COM15	7EFH	7CFH	7AFH	78FH	76FH	74FH	72FH	70FH
COM16	7F0H	7D0H	7B0H	790H	770H	750H	730H	710H
:	:	:	:	:	:	:	:	:
COM30	7FEH	7DEH	7BEH	79EH	77EH	75EH	73EH	71EH
COM31	7FFH	7DFH	7BFH	79FH	77FH	75FH	73FH	71FH
Page 6	SEG [71:64]	SEG [79:72]	SEG [87:80]	SEG [95:88]	SEG [103:96]	SEG [111:104]	SEG [119:112]	SEG [127:120]
COM0	6E0H	6C0H	6A0H	680H	660H	640H	620H	600H
COM1	6E1H	6C1H	6A1H	681H	661H	641H	621H	601H
:	:	:	:	:	:	:	:	:
COM15	6EFH	6CFH	6AFH	68FH	66FH	64FH	62FH	60FH
COM16	6F0H	6D0H	6B0H	690H	670H	650H	630H	610H
:	:	:	:	:	:	:	:	:
COM30	6FEH	6DEH	6BEH	69EH	67EH	65EH	63EH	61EH

COM31	6FFH	6DFH	6BFH	69FH	67FH	65FH	63FH	61FH

48COM:

Page 7, 6	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]
COM0	7C0H	780H	740H	700H	6C0H	680H	640H
COM1	7C1H	781H	741H	701H	6C1H	681H	641H
:	:	:	:	:	:	:	:
COM15	7CFH	78FH	74FH	70FH	6CFH	68FH	64FH
COM16	7D0H	790H	750H	710H	6D0H	690H	650H
:	:	:	:	:	:	:	:
COM31	7DFH	79FH	75FH	71FH	6DFH	69FH	65FH
COM32	7E0H	7A0H	760H	720H	6E0H	6A0H	660H
:	:	:	:	:	:	:	:
COM46	7EEH	7AEH	76EH	72EH	6EEH	6AEH	66EH
COM47	7EFH	7AFH	76FH	72FH	6EFH	6AFH	66FH

Page 6, 5, 4	SEG [63:56]	SEG [71:64]	SEG [79:72]	SEG [87:80]	SEG [95:88]	SEG [103:96]	SEG [111:104]
COM0	600H	5C0H	580H	540H	500H	4C0H	480H
COM1	601H	5C1H	581H	541H	501H	4C1H	481H
:	:	:	:	:	:	:	:
COM15	60FH	5CFH	58FH	54FH	50FH	4CFH	48FH
COM16	610H	5D0H	590H	550H	510H	4D0H	490H
:	:	:	:	:	:	:	:
COM31	61FH	5DFH	59FH	55FH	51FH	4DFH	49FH
COM32	620H	5E0H	5A0H	560H	520H	4E0H	4A0H
:	:	:	:	:	:	:	:
COM46	62EH	5EEH	5AEH	56EH	52EH	4EEH	4AEH
COM47	62FH	5EFH	5AFH	56FH	52FH	4EFH	4AFH

64COM:

Page 7,6	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]
COM0	7C0H	780H	740H	700H	6C0H	680H
COM1	7C1H	781H	741H	701H	6C1H	681H
:	:	:	:	:	:	:
COM15	7CFH	78FH	74FH	70FH	6CFH	68FH
COM16	7D0H	790H	750H	710H	6D0H	690H
:	:	:	:	:	:	:
COM31	7DFH	79FH	75FH	71FH	6DFH	69FH
COM32	7E0H	7A0H	760H	720H	6E0H	690H
:	:		:	:	:	:
COM47	7EFH	7AFH	76FH	72FH	6EFH	6AFH
COM48	7F0H	7B0H	770H	730H	6F0H	6B0H

:	:	:	:	:	:	:
COM62	7FEH	7BEH	77EH	73EH	6FEH	6BEH
COM63	7FFH	7BFH	77FH	73FH	6FFH	6BFH
Page 6,5	SEG [55:48]	SEG [63:56]	SEG [71:64]	SEG [79:72]	SEG [87:80]	SEG [95:88]
COM0	640H	600H	5C0H	580H	540H	500H
COM1	641H	601H	5C1H	581H	541H	501H
:	:	:	:	:	:	:
COM15	64FH	60FH	5CFH	58FH	54FH	50FH
COM16	650H	610H	5D0H	590H	550H	510H
:	:	:	:	:	:	:
COM31	65FH	61FH	5DFH	59FH	55FH	51FH
COM32	660H	620H	5E0H	5A0H	560H	520H
:	:	:	:	:	:	:
COM47	66FH	62FH	5EFH	5AFH	56FH	52FH
COM48	670H	630H	5F0H	5B0H	570H	530H
:	:	:	:	:	:	:
COM62	67EH	63EH	5FEH	5BEH	57EH	53EH
COM63	67FH	63FH	5FFH	5BFH	57FH	53FH

80COM:

Page 7,3	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]	SEG [71:64]	SEG [79:72]
COM0	780H	700H	680H	600H	580H	500H	480H	400H	380H	300H
COM1	781H	701H	681H	601H	581H	501H	481H	401H	381H	301H
:	:	:	:	:	:	:	:	:	:	:
COM15	78FH	70FH	68FH	60FH	58FH	50FH	48FH	40FH	38FH	30FH
COM16	790H	710H	690H	610H	590H	510H	490H	410H	390H	310H
:	:	:	:	:	:	:	:	:	:	:
COM31	79FH	71FH	69FH	61FH	59FH	51FH	49FH	41FH	39FH	31FH
COM32	7A0H	720H	6A0H	620H	5A0H	520H	4A0H	420H	3A0H	320H
:	:		:	:	:	:	:	:	:	:
COM47	7AFH	72FH	6AFH	62FH	5AFH	52FH	4AFH	42FH	3AFH	32FH
COM48	7B0H	730H	6B0H	630H	5B0H	530H	4B0H	430H	3B0H	330H
:	:	:	:	:	:	:	:	:	:	:
COM62	7BFH	73FH	6BFH	63FH	5BFH	53FH	4BFH	43FH	3BFH	33FH
COM63	7C0H	740H	6C0H	640H	5C0H	540H	4C0H	440H	3C0H	340H
:	:	:	:	:	:	:	:	:	:	:
COM78	7CEH	74EH	6CEH	64EH	5CEH	54EH	4CEH	44EH	3CEH	34EH
COM79	7CFH	74FH	6CFH	64FH	5CFH	54FH	4CFH	44FH	3CFH	34FH

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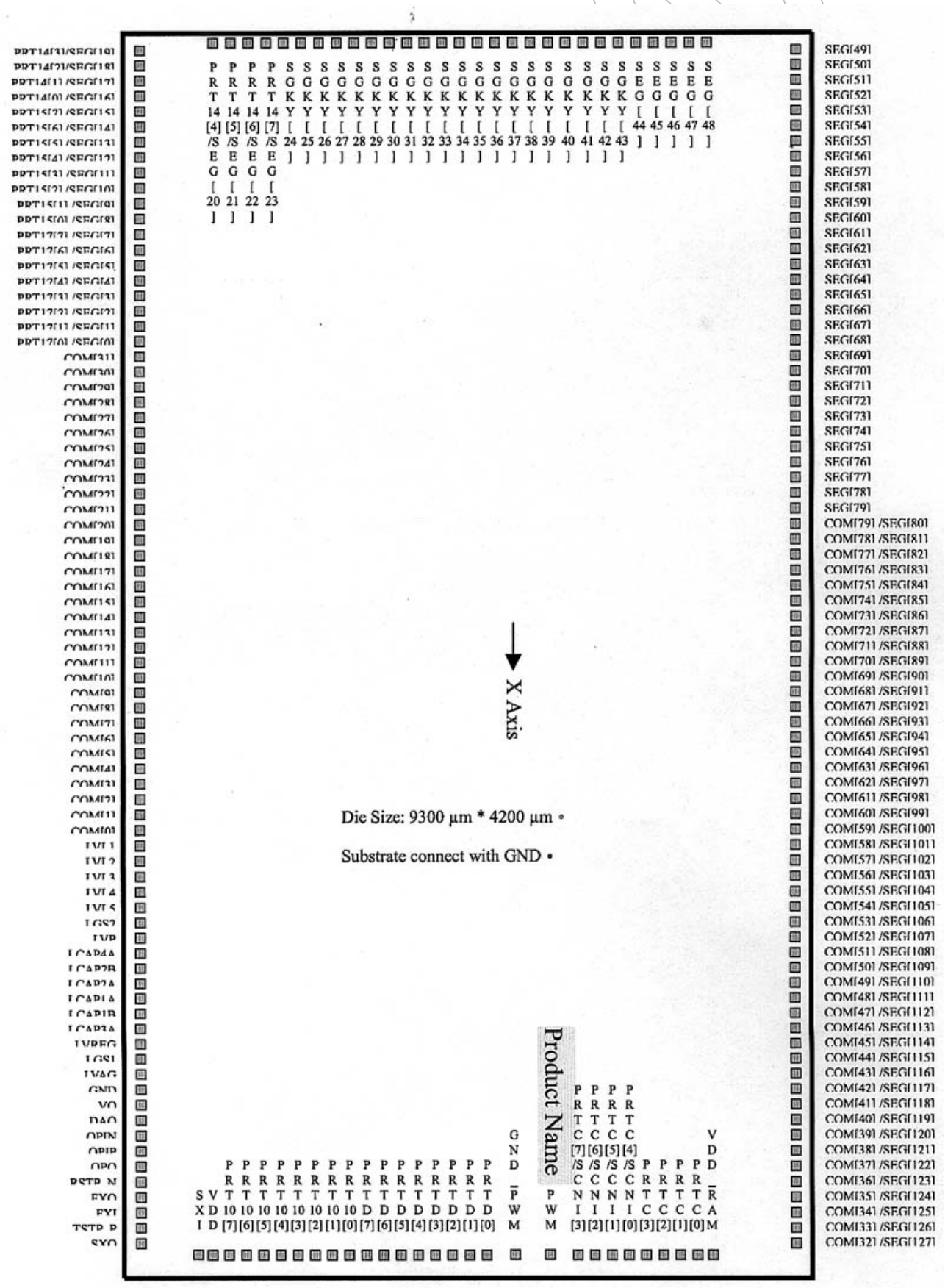
F. Pin Diagram



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G. Bonding Pad Location

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	SEG[48]	X= -4597.00	Y= 1616.90	109	SXI	X= 4601.00	Y= -1682.45
2	SEG[47]	X= -4597.00	Y= 1501.90	110	VDD	X= 4601.00	Y= -1567.45
3	SEG[46]	X= -4597.00	Y= 1386.90	111	PRT10[7]	X= 4601.00	Y= -1452.45
4	SEG[45]	X= -4597.00	Y= 1271.90	112	PRT10[6]	X= 4601.00	Y= -1337.45
5	SEG[44]	X= -4597.00	Y= 1156.90	113	PRT10[5]	X= 4601.00	Y= -1222.45
6	SGKY[43]	X= -4597.00	Y= 1041.90	114	PRT10[4]	X= 4601.00	Y= -1107.45
7	SGKY[42]	X= -4597.00	Y= 926.90	115	PRT10[3]	X= 4601.00	Y= -992.45
8	SGKY[41]	X= -4597.00	Y= 811.90	116	PRT10[2]	X= 4601.00	Y= -877.45
9	SGKY[40]	X= -4597.00	Y= 696.90	117	PRT10[1]	X= 4601.00	Y= -762.45
10	SGKY[39]	X= -4597.00	Y= 581.90	118	PRT10[0]	X= 4601.00	Y= -647.45
11	SGKY[38]	X= -4597.00	Y= 466.90	119	PRTD[7]	X= 4601.00	Y= -532.45
12	SGKY[37]	X= -4597.00	Y= 351.90	120	PRTD[6]	X= 4601.00	Y= -417.45
13	SGKY[36]	X= -4597.00	Y= 236.90	121	PRTD[5]	X= 4601.00	Y= -302.45
14	SGKY[35]	X= -4597.00	Y= 121.90	122	PRTD[4]	X= 4601.00	Y= -187.45
15	SGKY[34]	X= -4597.00	Y= 6.90	123	PRTD[3]	X= 4601.00	Y= -72.45
16	SGKY[33]	X= -4597.00	Y= -108.10	124	PRTD[2]	X= 4601.00	Y= 42.55
17	SGKY[32]	X= -4597.00	Y= -223.10	125	PRTD[1]	X= 4601.00	Y= 157.55
18	SGKY[31]	X= -4597.00	Y= -338.10	126	PRTD[0]	X= 4601.00	Y= 272.55
19	SGKY[30]	X= -4597.00	Y= -453.10	127	GND_PWM	X= 4601.00	Y= 387.55
20	SGKY[29]	X= -4597.00	Y= -568.10	128	PWM	X= 4601.00	Y= 512.50
21	SGKY[28]	X= -4597.00	Y= -683.10	129	PRTC[7]	X= 4601.00	Y= 635.55
22	SGKY[27]	X= -4597.00	Y= -798.10	130	PRTC[6]	X= 4601.00	Y= 750.55
23	SGKY[26]	X= -4597.00	Y= -913.10	131	PRTC[5]	X= 4601.00	Y= 865.55
24	SGKY[25]	X= -4597.00	Y= -1028.10	132	PRTC[4]	X= 4601.00	Y= 980.55
25	SGKY[24]	X= -4597.00	Y= -1143.10	133	PRTC[3]	X= 4601.00	Y= 1095.55
26	PRT14[7]	X= -4597.00	Y= -1258.10	134	PRTC[2]	X= 4601.00	Y= 1210.55
27	PRT14[6]	X= -4597.00	Y= -1373.10	135	PRTC[1]	X= 4601.00	Y= 1325.55
28	PRT14[5]	X= -4597.00	Y= -1488.10	136	PRTC[0]	X= 4601.00	Y= 1440.55
29	PRT14[4]	X= -4597.00	Y= -1603.10	137	VDD_RAM	X= 4601.00	Y= 1555.55
30	PRT14[3]	X= -4450.65	Y= -1996.95	138	CMSG[32]	X= 4552.90	Y= 1997.90
31	PRT14[2]	X= -4335.65	Y= -1996.95	139	CMSG[33]	X= 4437.90	Y= 1997.90
32	PRT14[1]	X= -4208.90	Y= -1996.95	140	CMSG[34]	X= 4322.90	Y= 1997.90
33	PRT14[0]	X= -4093.90	Y= -1996.95	141	CMSG[35]	X= 4207.90	Y= 1997.90
34	PRT15[7]	X= -3978.90	Y= -1996.95	142	CMSG[36]	X= 4092.90	Y= 1997.90
35	PRT15[6]	X= -3863.90	Y= -1996.95	143	CMSG[37]	X= 3977.90	Y= 1997.90
36	PRT15[5]	X= -3748.90	Y= -1996.95	144	CMSG[38]	X= 3862.90	Y= 1997.90

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37	PRT15[4]	X= -3633.90	Y= -1996.95	145	CMSG[39]	X= 3747.90	Y= 1997.90
38	PRT15[3]	X= -3518.90	Y= -1996.95	146	CMSG[40]	X= 3632.90	Y= 1997.90
39	PRT15[2]	X= -3403.90	Y= -1996.95	147	CMSG[41]	X= 3517.90	Y= 1997.90
40	PRT15[1]	X= -3288.90	Y= -1996.95	148	CMSG[42]	X= 3402.90	Y= 1997.90
41	PRT15[0]	X= -3173.90	Y= -1996.95	149	CMSG[43]	X= 3287.90	Y= 1997.90
42	PRT17[7]	X= -3058.90	Y= -1996.95	150	CMSG[44]	X= 3172.90	Y= 1997.90
43	PRT17[6]	X= -2943.90	Y= -1996.95	151	CMSG[45]	X= 3057.90	Y= 1997.90
44	PRT17[5]	X= -2828.90	Y= -1996.95	152	CMSG[46]	X= 2942.90	Y= 1997.90
45	PRT17[4]	X= -2713.90	Y= -1996.95	153	CMSG[47]	X= 2827.90	Y= 1997.90
46	PRT17[3]	X= -2598.90	Y= -1996.95	154	CMSG[48]	X= 2712.90	Y= 1997.90
47	PRT17[2]	X= -2483.90	Y= -1996.95	155	CMSG[49]	X= 2597.90	Y= 1997.90
48	PRT17[1]	X= -2368.90	Y= -1996.95	156	CMSG[50]	X= 2482.90	Y= 1997.90
49	PRT17[0]	X= -2253.90	Y= -1996.95	157	CMSG[51]	X= 2367.90	Y= 1997.90
50	COM[31]	X= -2138.90	Y= -1996.95	158	CMSG[52]	X= 2252.90	Y= 1997.90
51	COM[30]	X= -2023.90	Y= -1996.95	159	CMSG[53]	X= 2137.90	Y= 1997.90
52	COM[29]	X= -1908.90	Y= -1996.95	160	CMSG[54]	X= 2022.90	Y= 1997.90
53	COM[28]	X= -1793.90	Y= -1996.95	161	CMSG[55]	X= 1907.90	Y= 1997.90
54	COM[27]	X= -1678.90	Y= -1996.95	162	CMSG[56]	X= 1792.90	Y= 1997.90
55	COM[26]	X= -1563.90	Y= -1996.95	163	CMSG[57]	X= 1677.90	Y= 1997.90
56	COM[25]	X= -1448.90	Y= -1996.95	164	CMSG[58]	X= 1562.90	Y= 1997.90
57	COM[24]	X= -1333.90	Y= -1996.95	165	CMSG[59]	X= 1447.90	Y= 1997.90
58	COM[23]	X= -1218.90	Y= -1996.95	166	CMSG[60]	X= 1332.90	Y= 1997.90
59	COM[22]	X= -1103.90	Y= -1996.95	167	CMSG[61]	X= 1217.90	Y= 1997.90
60	COM[21]	X= -988.90	Y= -1996.95	168	CMSG[62]	X= 1102.90	Y= 1997.90
61	COM[20]	X= -873.90	Y= -1996.95	169	CMSG[63]	X= 987.90	Y= 1997.90
62	COM[19]	X= -758.90	Y= -1996.95	170	CMSG[64]	X= 872.90	Y= 1997.90
63	COM[18]	X= -643.90	Y= -1996.95	171	CMSG[65]	X= 757.90	Y= 1997.90
64	COM[17]	X= -528.90	Y= -1996.95	172	CMSG[66]	X= 642.90	Y= 1997.90
65	COM[16]	X= -393.90	Y= -1996.95	173	CMSG[67]	X= 527.90	Y= 1997.90
66	COM[15]	X= -278.90	Y= -1996.95	174	CMSG[68]	X= 412.90	Y= 1997.90
67	COM[14]	X= -163.90	Y= -1996.95	175	CMSG[69]	X= 297.90	Y= 1997.90
68	COM[13]	X= -48.90	Y= -1996.95	176	CMSG[70]	X= 182.90	Y= 1997.90
69	COM[12]	X= 66.10	Y= -1996.95	177	CMSG[71]	X= 67.90	Y= 1997.90
70	COM[11]	X= 181.10	Y= -1996.95	178	CMSG[72]	X= -47.10	Y= 1997.90
71	COM[10]	X= 296.10	Y= -1996.95	179	CMSG[73]	X= -162.10	Y= 1997.90
72	COM[9]	X= 411.10	Y= -1996.95	180	CMSG[74]	X= -277.10	Y= 1997.90
73	COM[8]	X= 526.10	Y= -1996.95	181	CMSG[75]	X= -392.10	Y= 1997.90
74	COM[7]	X= 641.10	Y= -1996.95	182	CMSG[76]	X= -527.10	Y= 1997.90
75	COM[6]	X= 756.10	Y= -1996.95	183	CMSG[77]	X= -642.10	Y= 1997.90
76	COM[5]	X= 871.10	Y= -1996.95	184	CMSG[78]	X= -757.10	Y= 1997.90
77	COM[4]	X= 986.10	Y= -1996.95	185	CMSG[79]	X= -872.10	Y= 1997.90

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78	COM[3]	X= 1101.10	Y= -1996.95	186	SEG[79]	X= -987.10	Y= 1997.90
79	COM[2]	X= 1216.10	Y= -1996.95	187	SEG[78]	X= -1102.10	Y= 1997.90
80	COM[1]	X= 1331.10	Y= -1996.95	188	SEG[77]	X= -1217.10	Y= 1997.90
81	COM[0]	X= 1446.10	Y= -1996.95	189	SEG[76]	X= -1332.10	Y= 1997.90
82	LVL1	X= 1561.10	Y= -1996.95	190	SEG[75]	X= -1447.10	Y= 1997.90
83	LVL2	X= 1676.10	Y= -1996.95	191	SEG[74]	X= -1562.10	Y= 1997.90
84	LVL3	X= 1791.10	Y= -1996.95	192	SEG[73]	X= -1677.10	Y= 1997.90
85	LVL4	X= 1906.10	Y= -1996.95	193	SEG[72]	X= -1792.10	Y= 1997.90
86	LVL5	X= 2021.10	Y= -1996.95	194	SEG[71]	X= -1907.10	Y= 1997.90
87	LGS2	X= 2136.10	Y= -1996.95	195	SEG[70]	X= -2022.10	Y= 1997.90
88	LVP	X= 2251.10	Y= -1996.95	196	SEG[69]	X= -2137.10	Y= 1997.90
89	LCAP4A	X= 2366.10	Y= -1996.95	197	SEG[68]	X= -2252.10	Y= 1997.90
90	LCAP2B	X= 2481.10	Y= -1996.95	198	SEG[67]	X= -2367.10	Y= 1997.90
91	LCAP2A	X= 2596.10	Y= -1996.95	199	SEG[66]	X= -2482.10	Y= 1997.90
92	LCAP1A	X= 2711.10	Y= -1996.95	200	SEG[65]	X= -2597.10	Y= 1997.90
93	LCAP1B	X= 2826.10	Y= -1996.95	201	SEG[64]	X= -2712.10	Y= 1997.90
94	LCAP3A	X= 2941.10	Y= -1996.95	202	SEG[63]	X= -2827.10	Y= 1997.90
95	LVREG	X= 3056.10	Y= -1996.95	203	SEG[62]	X= -2942.10	Y= 1997.90
96	LGS1	X= 3171.10	Y= -1996.95	204	SEG[61]	X= -3057.10	Y= 1997.90
97	LVAG	X= 3286.10	Y= -1996.95	205	SEG[60]	X= -3172.10	Y= 1997.90
98	GND	X= 3401.10	Y= -1996.95	206	SEG[59]	X= -3287.10	Y= 1997.90
99	VO	X= 3516.10	Y= -1996.95	207	SEG[58]	X= -3402.10	Y= 1997.90
100	DAO	X= 3631.10	Y= -1996.95	208	SEG[57]	X= -3517.10	Y= 1997.90
101	OPIN	X= 3746.10	Y= -1996.95	209	SEG[56]	X= -3632.10	Y= 1997.90
102	OPIP	X= 3861.10	Y= -1996.95	210	SEG[55]	X= -3747.10	Y= 1997.90
103	OPO	X= 3976.10	Y= -1996.95	211	SEG[54]	X= -3862.10	Y= 1997.90
104	RSTP_N	X= 4091.10	Y= -1996.95	212	SEG[53]	X= -3977.10	Y= 1997.90
105	FXO	X= 4206.10	Y= -1996.95	213	SEG[52]	X= -4092.10	Y= 1997.90
106	FXI	X= 4321.10	Y= -1996.95	214	SEG[51]	X= -4207.10	Y= 1997.90
107	TSTP_P	X= 4436.10	Y= -1996.95	215	SEG[50]	X= -4322.10	Y= 1997.90
108	SXO	X= 4551.10	Y= -1996.95	216	SEG[49]	X= -4437.10	Y= 1997.90

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H. Electrical Characteristics

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 4V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~3.6V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =5.0V
		4MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

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Test condition:TEMP=25℃, VDD=3V+/-10%, GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		1	1.5	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		15	30	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		10	25	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable, LCD option=300Kohm LVD=6 Volt		65	72	μA
			LCD Enable, LCD option=30Kohm, LVD=6 Volt		350	385	
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{PWM}	PWM Output Drive Current	PWMP, PWMN*2	With 32Ω Loading	10	14		mA
			With 64Ω Loading	6	8		mA
			With 100Ω Loading	4	5		mA
I_{ovo}	DAC Output Current	VO	V_{DD}=3V; VO=0~2v, Data=7F	2.5	3		mA
V_{ih}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{oL}=2.0V	50			μA
I_{oL_1}	Output Sink Current	I/O pull-low*1	V_{oL}=0.4V	1.0			mA
I_{iL_1}	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
I_{iL_2}	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Spec. for Push-Pull I/O port only
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.
*2: This Spec. base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current
to get the total amount of current.(IPWM* N; N=0,1,2,3,4,5)

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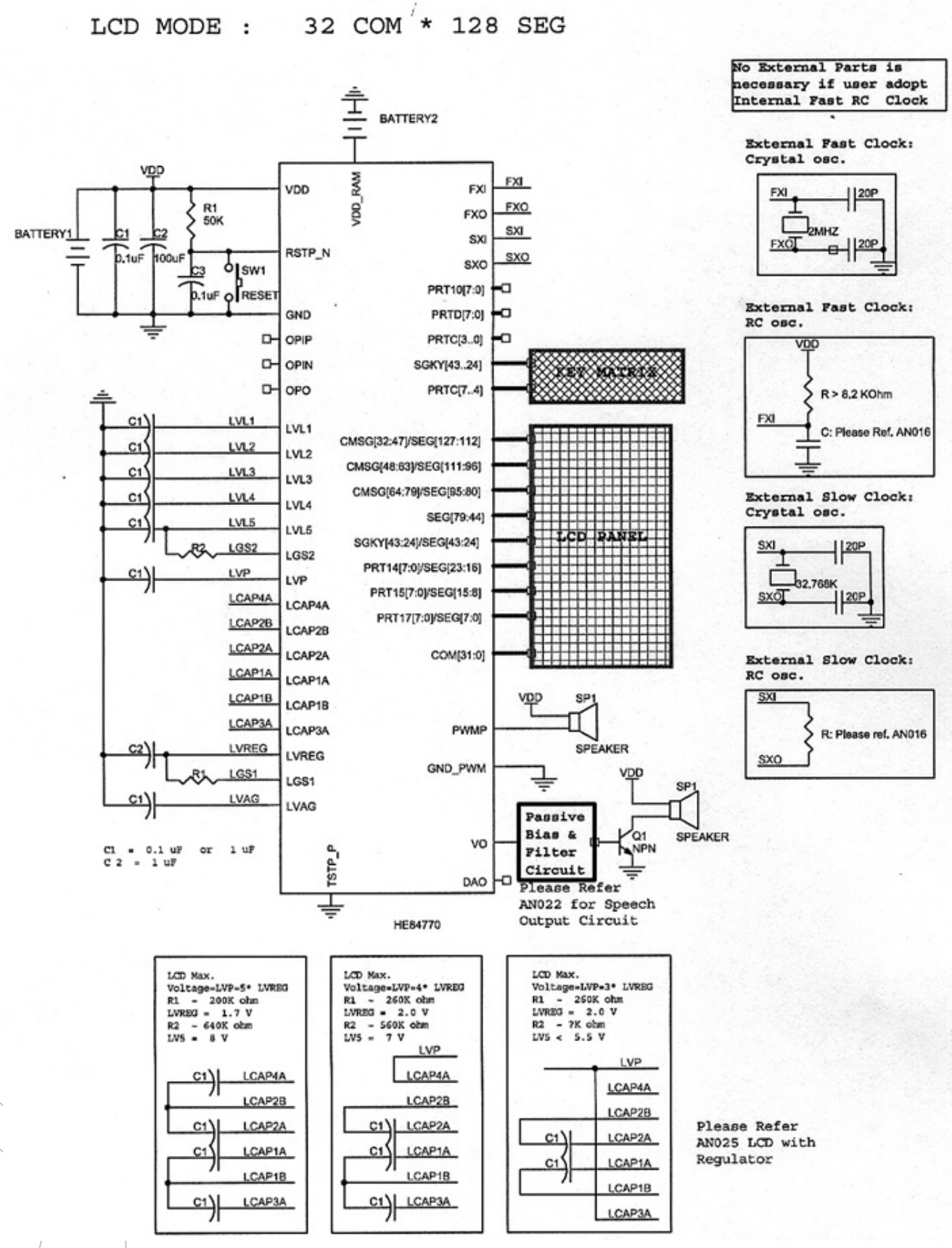
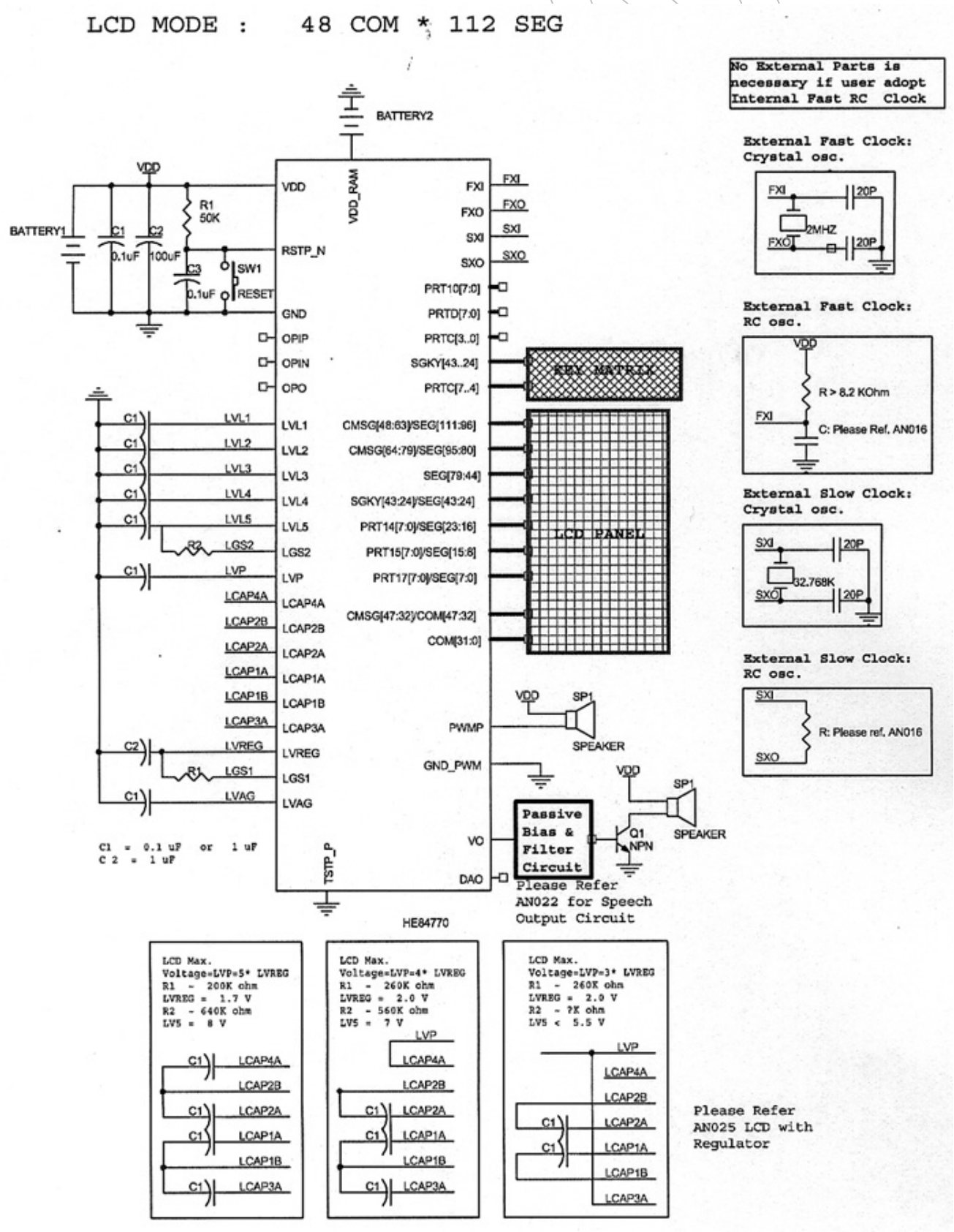
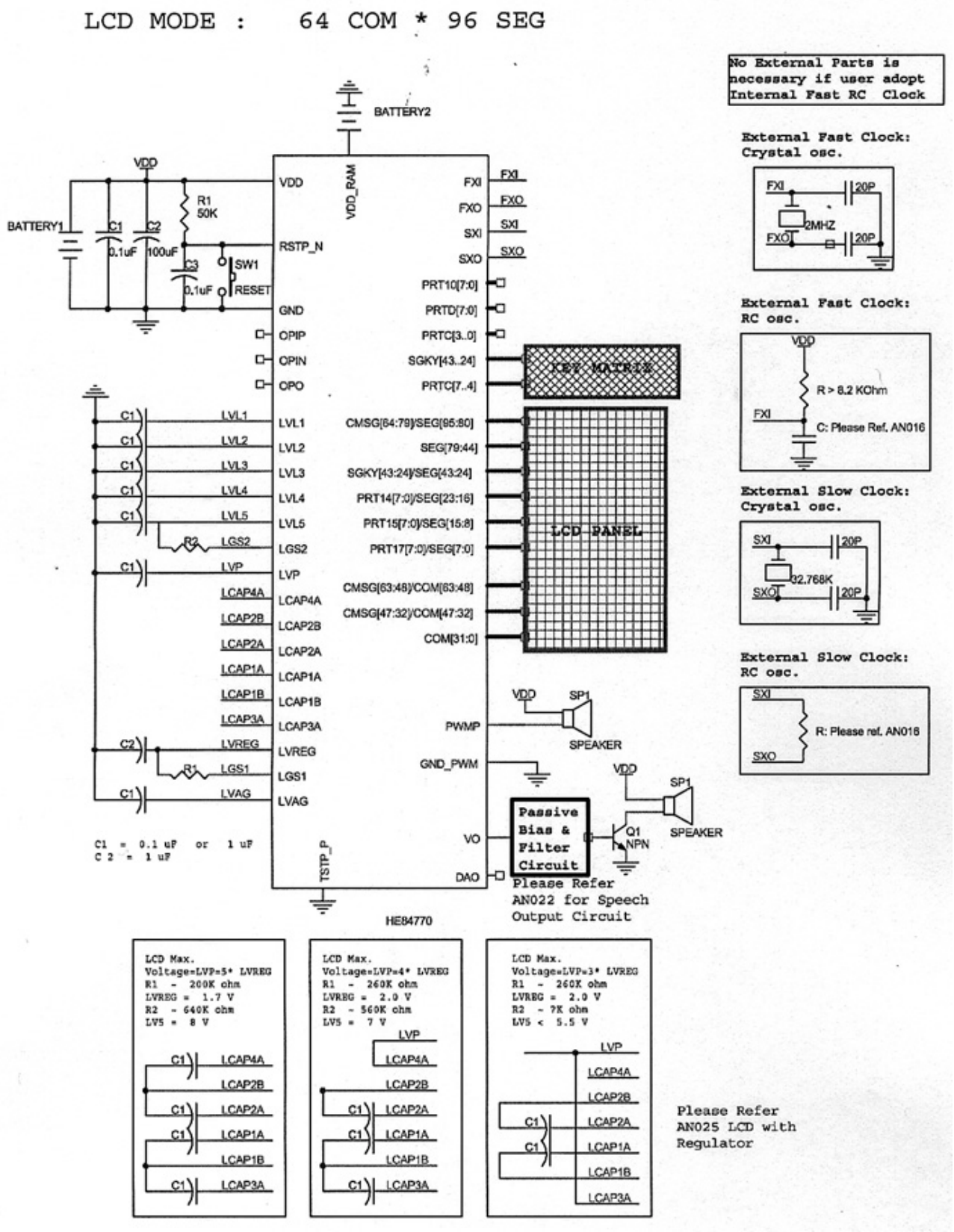
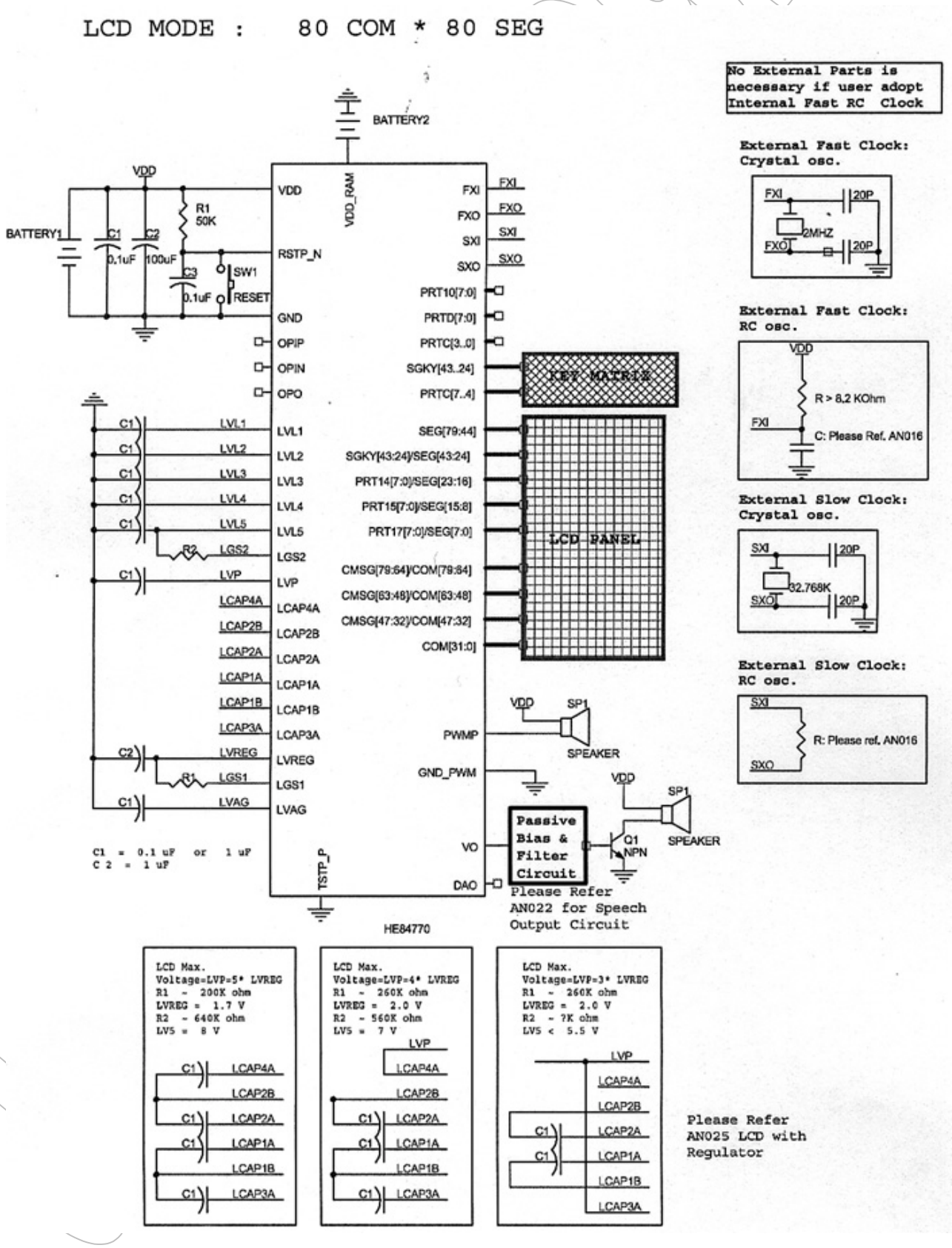
I. Application Circuit




LCD MODE : 48 COM * 112 SEG
No External Parts is necessary if user adopt Internal Fast RC Clock
BATTERY2
VDD
BATTERY1
C1
C2
0.1uF
100uF
R1
50K
C3
0.1uF
SW1
RESET
RSTP_N
GND
OPIP
OPIN
OPO
VDD_RAM
FXI
FXO
SXI
SXO
PRT10[7:0]
PRTD[7:0]
PRTC[3..0]
SGKY[43..24]
PRTC[7..4]
KEY MATRIX
LCD PANEL
LVL1
LVL2
LVL3
LVL4
LVL5
LGS2
LVP
LCAP4A
LCAP2B
LCAP2A
LCAP1A
LCAP1B
LCAP3A
LVREG
LGS1
LVAG
CMSG[48:63]/SEG[111:96]
CMSG[64:79]/SEG[95:80]
SEG[79:44]
SGKY[43:24]/SEG[43:24]
PRT14[7:0]/SEG[23:16]
PRT15[7:0]/SEG[15:8]
PRT17[7:0]/SEG[7:0]
CMSG[47:32]/COM[47:32]
COM[31:0]
PWMP
GND_PWM
VO
DAO
TSTP_P
SP1
SPEAKER
Q1
NPN
Passive Bias & Filter Circuit
Please Refer AN022 for Speech Output Circuit
C1 = 0.1 uF or 1 uF
C 2 = 1 uF
HE84770
External Fast Clock: Crystal osc.
FXI
FXO
20P
2MHZ
External Fast Clock: RC osc.
R > 8.2 KOhm
C: Please Ref. AN016
External Slow Clock: Crystal osc.
SXI
SXO
32.768K
External Slow Clock: RC osc.
R: Please ref. AN016
LCD Max. Voltage=LVP=5* LVREG
R1 - 200K ohm
LVREG = 1.7 V
R2 - 640K ohm
LVS = 8 V
LCD Max. Voltage=LVP=4* LVREG
R1 - 260K ohm
LVREG = 2.0 V
R2 - 560K ohm
LVS = 7 V
LCD Max. Voltage=LVP=3* LVREG
R1 - 260K ohm
LVREG = 2.0 V
R2 - ?K ohm
LVS < 5.5 V
Please Refer AN025 LCD with Regulator


LCD MODE : 64 COM * 96 SEG
No External Parts is necessary if user adopt Internal Fast RC Clock
External Fast Clock: Crystal osc.
External Fast Clock: RC osc.
R > 8.2 KOhm
C: Please Ref. AN016
External Slow Clock: Crystal osc.
External Slow Clock: RC osc.
R: Please ref. AN016
BATTERY2
VDD
VDD_RAM
RSTP_N
GND
OPIP
OPIN
OPO
FXI
FXO
SXI
SXO
PRT10[7:0]
PRTD[7:0]
PRTC[3..0]
SGKY[43..24]
PRTC[7..4]
KEY MATRIX
LCD PANEL
CMSG[64:79]/SEG[95:80]
SEG[79:44]
SGKY[43:24]/SEG[43:24]
PRT14[7:0]/SEG[23:16]
PRT15[7:0]/SEG[15:8]
PRT17[7:0]/SEG[7:0]
CMSG[63:48]/COM[63:48]
CMSG[47:32]/COM[47:32]
COM[31:0]
LVL1
LVL2
LVL3
LVL4
LVL5
LGS2
LVP
LCAP4A
LCAP2B
LCAP2A
LCAP1A
LCAP1B
LCAP3A
LVREG
LGS1
LVAG
PWMP
GND_PWM
VO
DAO
TSTP_P
SP1
SPEAKER
Q1 NPN
Passive Bias & Filter Circuit
Please Refer AN022 for Speech Output Circuit
C1 = 0.1 uF or 1 uF
C 2 = 1 uF
HE84770
LCD Max. Voltage=LVP=5* LVREG
R1 - 200K ohm
LVREG = 1.7 V
R2 - 640K ohm
LV5 = 8 V
LCD Max. Voltage=LVP=4* LVREG
R1 - 260K ohm
LVREG = 2.0 V
R2 - 560K ohm
LV5 = 7 V
LCD Max. Voltage=LVP=3* LVREG
R1 - 260K ohm
LVREG = 2.0 V
R2 - 7K ohm
LV5 < 5.5 V
Please Refer AN025 LCD with Regulator


LCD MODE : 80 COM * 80 SEG
No External Parts is necessary if user adopt Internal Fast RC Clock
External Fast Clock: Crystal osc.
External Fast Clock: RC osc.
R > 8.2 KOhm
C: Please Ref. AN016
External Slow Clock: Crystal osc.
External Slow Clock: RC osc.
R: Please ref. AN016
BATTERY2
BATTERY1
VDD
R1 50K
C1 0.1uF
C2 100uF
C3 0.1uF
SW1
RESET
RSTP_N
GND
OPIP
OPIN
OPO
VDD_RAM
FXI
FXO
SXI
SXO
PRT10[7:0]
PRTD[7:0]
PRTC[3..0]
SGKY[43..24]
PRTC[7..4]
KEY MATRIX
SEG[79:44]
SGKY[43:24]/SEG[43:24]
PRT14[7:0]/SEG[23:16]
PRT15[7:0]/SEG[15:8]
PRT17[7:0]/SEG[7:0]
LCD PANEL
CMSG[79:64]/COM[79:64]
CMSG[63:48]/COM[63:48]
CMSG[47:32]/COM[47:32]
COM[31:0]
LVL1
LVL2
LVL3
LVL4
LVL5
LGS2
LVP
LCAP4A
LCAP2B
LCAP2A
LCAP1A
LCAP1B
LCAP3A
LVREG
LGS1
LVAG
C1 = 0.1 uF or 1 uF
C 2 = 1 uF
PWMP
GND_PWM
VO
DAO
TSTP_P
SP1
SPEAKER
Passive Bias & Filter Circuit
Q1 NPN
Please Refer AN022 for Speech Output Circuit
HE84770
LCD Max. Voltage=LVP=5* LVREG
R1 = 200K ohm
LVREG = 1.7 V
R2 = 640K ohm
LV5 = 8 V
LCD Max. Voltage=LVP=4* LVREG
R1 = 260K ohm
LVREG = 2.0 V
R2 = 560K ohm
LV5 = 7 V
LCD Max. Voltage=LVP=3* LVREG
R1 = 260K ohm
LVREG = 2.0 V
R2 = 7K ohm
LV5 < 5.5 V
Please Refer AN025 LCD with Regulator

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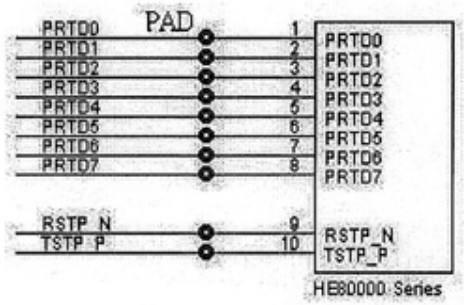
J. Important Note

1. For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.
(針對超過 64KB 的母體時，必須要將 TP 的設定順序維持在 Update r_tpp, r_tph, r_tpl 的先後順序。如此才能確保 Data ROM 的 pre-charge 會開始執行。並且要在 pre-charge 開始到讀取資料之間，等待 5us.以確保資料的正確性。需要如此做的原因是因為在 ICE 上無法模擬到較低速的 Data ROM 所致。)
2. LCD driving circuit must be turn off before IC goes into sleep mode.
3. Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB (can be soldered and probed) as you can, then KB can do some IC testing job on PCB. Neither VDD nor GND connection is necessary for TSTP_P. The following figure is an example (Testing point with through hole).



4. LVP must small than 8.5 Volt. Otherwise IC may breakdown.
5. Users must call the library " swap_page" in the file swappage.asm of AN029. The real IC register is different from ICE4.x or ICE5.x. This subroutine make sure that users can run on both real IC and ICE for page swapping. The program of swappage.asm as following:

```
.area       swapping_variable(data)
_mapreg1::      .ds     1   ;store page register(R1Bh)
_mapreg2::      .ds     1   ;store page register(R1Ch)

.area       swapping_page(code,pag0)
;=============================================================
;swap page function
;=============================================================
```

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```
swap_page::
    lda  #10h
    sta  _mapreg1
    lda  #00h          ; P1E_O[2] <--0    to enable Port R1Fh
    sta  r_iceco       ; R_ICECO is write only
    lda  _mapreg2
    sta  r_iced
    lda  _mapreg2
    anda #0fh
    ora  #20h      ;Mapping _mapreg2 low nibble to Logical segment2
;   sta  r1Ch
    sta  r_ps1
    lda  _mapreg2
    rorc
    rorc
    rorc
    rorc
    anda #0fh      ;Mapping _mapreg2 high nibble to Logical segment3
    ora  #30h
;   sta  r_ps1
    sta  r1Ch
    ret
```