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A.HE83130 Introduction

HE83130 is a member of Jess Tech HE8000 series 8-bit CMOS micro-controller. This IC provides 640 dots of LCD driver and 12-bit I/O pin. Besides, it built-in one internal Op-Amp, one 7-bit D/A converter and one PWM output module to provide a speech output interface. Use the built-in 64K ROM can store around 20 seconds of speech data. It is suitable for the application in digital meter, stopwatch, thermometer and so on.

The HE83130 provides a very simple and effective instruction set, each instruction byte occupies only 1.5 clock cycle time, therefore, it is suitable to apply in the high performance systems.

B.HE83130 Features

- Operating Voltage: 2.4V – 5.2V
- Operation frequency Range: DC ~ 8MHz @ 5.0V
  DC ~ 4MHz @ 2.4V
- ROM size: 64K Bytes
- RAM size: 256 Bytes
- Dual Clock: Normal(Fast) clock: 32.768K ~ 8MHz
  Slow clock: 32.768KHz
- Operating Mode: DUAL、FAST、SLOW、IDLE、SLEEP
- Built-in WATCH DOG TIMER
- 12-bit bi-directional I/O pins, PUSH-PULL or OPEN DRAIN output selected by mask option
- Built-in an internal Op-Amp
- 640 dots of LCD driver (A、B TYPE)
- Built-in one 7-bit D/A Converter
- Built-in a PWM output circuit
- Provides two internal and two external interrupt
- Provides two 16-bit timer (no time base)
- Instruction Set : 32 Instructions, 4 types of Addressing Mode, 2 individual Pointer for ROM (16-bit) and RAM (8-bit) table access.

C.HE83130 Application

- For LCD games, education toys and the mid-end device.
- Interface to Light, Sound, Temperature and Humidity sensor for controlling application.
- Interface to external SRAM or Flash RAM for recording function.

D. Pin Assignment

Pin	Pin Name	I/O	Function	Description
78 77	**FXI,** **FXO**	B, O	External Fast Clock pin. To connect the Crystal or R,C oscillation to generate 32.768KHz ~ 8MHz system clock.	Mask Option settings : MO_FCK/SCKN=00：Slow Clock only 01：Illegal 10：Dual Clock 11：Fast Clock only MO_FOSCE=0：Internal fast oscillation 1：External fast oscillation MO_FXTAL=0：R,C oscillation for Fast Clock 1：Crystal oscillation for Fast Clock MO_SXTAL=0：R,C oscillation for 32.768K Clock 1：X'tal oscillation for 32.768K Clock Program the value of OP1and OP2 to change the operating modes (Normal, Slow, Idle and Sleep). In Dual Clock mode，the system runs in Fast Clock, only the Timer 1 use the 32.768K clock source.
81 80	**SXI,** **SXO**	I, O	External Slow Clock pin . To connect the 32.768KHz oscillator to generate the stable frequency for Slow Mode, and provide IC LCD display, Timer clock source.	
76	**RSTP_N**	I	System reset signal	Pull this pin to low level to reset the system. Besides, Select the Mask Option (MO_PORE=1) to enable the IC internal Power-on Reset function. In addition, the MO_WDTE is used for Watch Dog Timer setting： MO_WDTE =0：Disable Watch Dog Timer =1：Enable Watch Dog Timer
79	**TSTP_P**	I	Test Pin.	Please bond this pin and add a test point on PCB for debugging. Leave this pin floating is OK.
91.. 92, 93, 1	**PRTC[3:0]**	B	Port C bi-directional I/O pin (4 pins).	Mask Option MO_CPP[3:0] to preset the output type: MO_CPP=1 : Push-pull output； = 0 : Open-drain output. When assigned the port to input pin, send a '1' and read the result to get the input value.
83.. 90	**PRTD[7:0]**	B	Port D bi-directional I/O pin, (8 pins). PRTD[7:2] is also a Wake-up pin and PRTD[7:6] is used for interrupt input pin.	Mask Option MO_DPP[7:0] to preset the output type: MO_DPP=1 : Push-pull output； 0 : Open-drain output. When assigned the port to input pin, send a '1' and read the result to get the input value.
11..4. 52.. 59	**COM[15:0]**	O	LCD COMmon Output	Fill the data from 80H, refer LCD and RAM map.
12.. 51	**SEG[39:0]**	O	LCD SEGment Output	
61	**LC2**	B	Charge Pump Switch 1	Refer to application circuit.
60	**LC1**	B	Charge Pump Switch 2	
63	**LV3**	B	Charge Pump V3	Refer to application circuit.
62	**LV1**	B	Charge Pump V1	
64.. 68	**LR[4..0]**	B	LCD Resister level 4 ~ 0	Refer to application circuit.
69	**LVG**	I	LCD Virtual Ground	Refer to application circuit.
2	**PWMP**	O	PWM +ve O/P pin, can directly drive Speaker or	Preset the Bit2 of VOC register: PWM =1；turn on

			Buzzer for voice output.	PWM.

3	**PWMN**	O	PWM -ve O/P pin, can directly drive Speaker or Buzzer for voice output.	Preset the Bit2 of VOC register: PWM =1；turn on PWM.
71	**VO**	O	D/A voice output	Preset the Bit-1 of VOC register: DA=1；turn on VO.
72	**DAO**	O	D/A output used by OP	Preset the Bit-0 of VOC register: OP=1；turn on DAO.
73	**OPIN**	I	OPAMP Inverting I/P pin	Individual built-in OP-Amp
74	**OPIP**	I	OPAMP Non-inverting I/P pin.	
75	**OPO**	O	OPAMP O/P pin	
82	**VDD**	P	Positive Power Input	Adding 0.1mF capacitor as by-pass capacitor is between VDD and GND is necessary
70	**GND**	P	Power Ground Input	

E.LCD RAM Map

Page 0	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]
COM0	80H	90H	A0H	B0H	C0H
COM1	81H	91H	A1H	B1H	C1H
COM2	82H	92H	A2H	B2H	C2H
:	:	:	:	:	:
:	:	:	:	:	:
COM13	8DH	9DH	ADH	BDH	CDH
COM14	8EH	9EH	AEH	BEH	CEH
COM15	8FH	9FH	AFH	BFH	CFH

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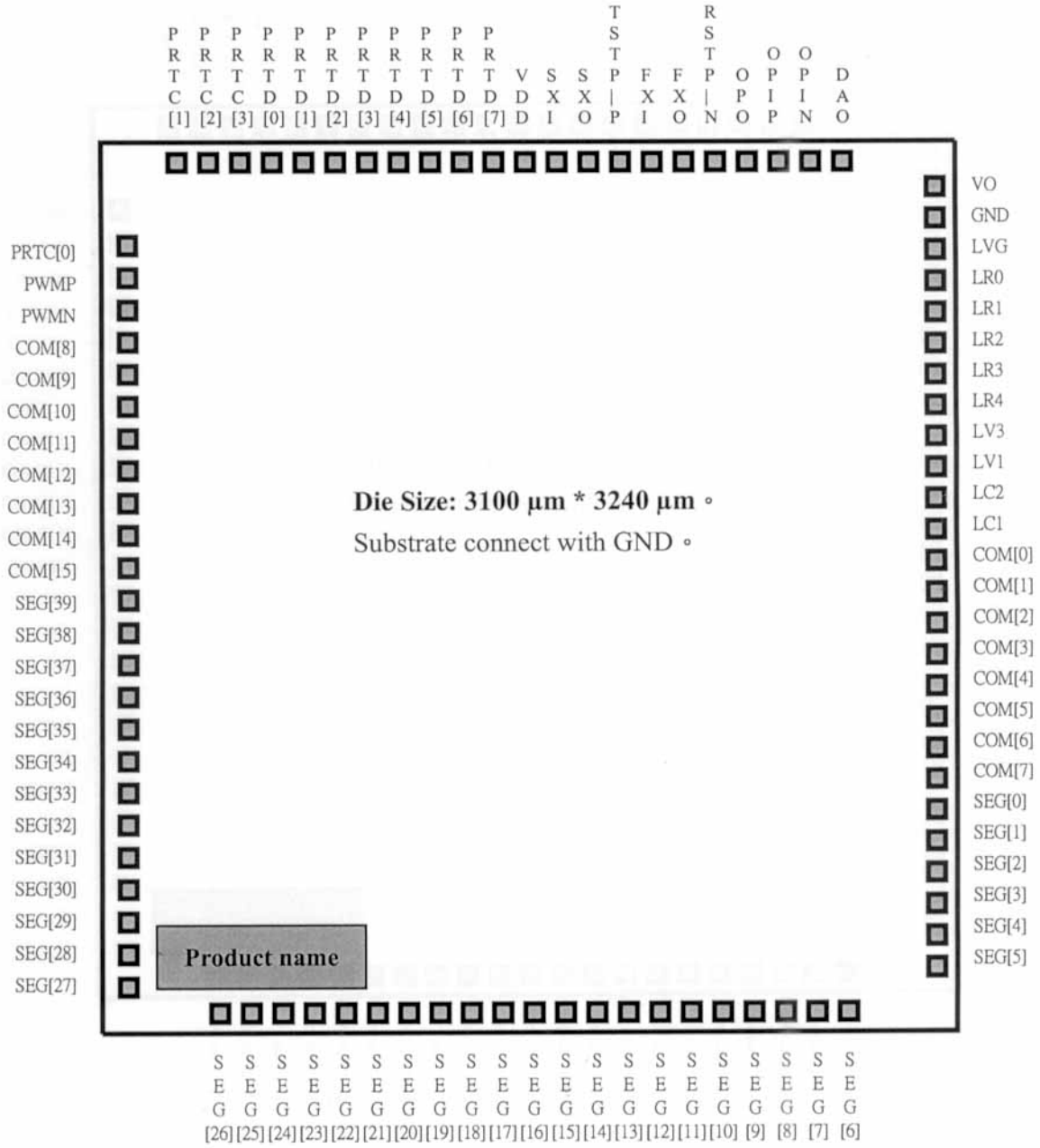
F. Pin Diagram



G. Bonding Pad Location

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	PRTC[0]	-1475.80	1246.95	48	SEG[3]	1474.30	-1236.15
2	PWMP	-1475.80	1107.20	49	SEG[2]	1474.30	-1120.65
3	PWMN	-1475.80	943.85	50	SEG[1]	1474.30	-1005.15
4	COM[8]	-1475.80	804.75	51	SEG[0]	1474.30	-889.65
5	COM[9]	-1475.80	689.25	52	COM[7]	1474.30	-774.15
6	COM[10]	-1475.80	573.75	53	COM[6]	1474.30	-658.65
7	COM[11]	-1475.80	458.25	54	COM[5]	1474.30	-543.15
8	COM[12]	-1475.80	342.75	55	COM[4]	1474.30	-427.65
9	COM[13]	-1475.80	227.25	56	COM[3]	1474.30	-312.15
10	COM[14]	-1475.80	111.75	57	COM[2]	1474.30	-196.65
11	COM[15]	-1475.80	-3.75	58	COM[1]	1474.30	-81.15
12	SEG[39]	-1475.80	-119.25	59	COM[0]	1474.30	34.35
13	SEG[38]	-1475.80	-234.75	60	LC1	1474.30	149.85
14	SEG[37]	-1475.80	-350.25	61	LC2	1474.30	265.35
15	SEG[36]	-1475.80	-465.75	62	LV1	1474.30	380.85
16	SEG[35]	-1475.80	-581.25	63	LV3	1474.30	496.35
17	SEG[34]	-1475.80	-696.75	64	LR4	1474.30	611.85
18	SEG[33]	-1475.80	-812.25	65	LR3	1474.30	727.35
19	SEG[32]	-1475.80	-927.75	66	LR2	1474.30	842.85
20	SEG[31]	-1475.80	-1043.25	67	LR1	1474.30	958.35
21	SEG[30]	-1475.80	-1158.75	68	LR0	1474.30	1073.85
22	SEG[29]	-1475.80	-1274.25	69	LVG	1474.30	1189.35
23	SEG[28]	-1475.80	-1389.75	70	GND	1474.30	1304.85
24	SEG[27]	-1475.80	-1505.25	71	VO	1474.30	1438.50
25	SEG[26]	-1155.05	-1541.50	72	DAO	1124.45	1539.10
26	SEG[25]	-1093.55	-1541.50	73	OPIN	990.80	1539.10
27	SEG[24]	-924.05	-1541.50	74	OPIP	875.30	1539.10
28	SEG[23]	-808.55	-1541.50	75	OPO	759.80	1539.10
29	SEG[22]	-693.05	-1541.50	76	RSTP_N	644.30	1539.10
30	SEG[21]	-577.55	-1541.50	77	FXO	528.80	1539.10
31	SEG[20]	-462.05	-1541.50	78	FXI	413.30	1539.10
32	SEG[19]	-346.55	-1541.50	79	TSTP_P	297.80	1539.10
33	SEG[18]	-231.05	-1541.50	80	SXO	182.30	1539.10
34	SEG[17]	-115.55	-1541.50	81	SXI	66.80	1539.10
35	SEG[16]	-0.05	-1541.50	82	VDD	-48.70	1539.10
36	SEG[15]	115.45	-1541.50	83	PRTD[7]	-164.20	1539.10
37	SEG[14]	230.95	-1541.50	84	PRTD[6]	-279.70	1539.10
38	SEG[13]	346.45	-1541.50	85	PRTD[5]	-395.20	1539.10
39	SEG[12]	461.95	-1541.50	86	PRTD[4]	-510.70	1539.10
40	SEG[11]	577.45	-1541.50	87	PRTD[3]	-626.20	1539.10
41	SEG[10]	692.95	-1541.50	88	PRTD[2]	-741.70	1539.10
42	SEG[9]	808.45	-1541.50	89	PRTD[1]	-857.20	1539.10
43	SEG[8]	923.95	-1541.50	90	PRTD[0]	-972.70	1539.10
44	SEG[7]	1039.45	-1541.50	91	PRTC[3]	-1088.20	1539.10

45	SEG[6]	1154.95	-1541.50	92	PRTC[2]	-1203.70	1539.10
46	SEG[5]	1474.30	-1467.15	93	PRTC[1]	-1319.20	1539.10
47	SEG[4]	1474.30	-1351.65				

H. Electrical Characteristics

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.2V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =5.0V
		4MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

Test condition:TEMP=25℃, VDD=3V+/-10%, GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		10	20	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		6	10	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable, LCD option=300Kohm Voltage-doubler OFF		12	20	μA
			LCD Enable, LCD option=30Kohm, Voltage-doubler ON		100	120	
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{oHPWM}	PWM Output Drive Current	PWMP, PWMN*2	V_{DD}=3V; V_{oh}=2V	12	15		mA
I_{oLPWM}	PWM Output Sink Current	PWMP, PWMN*2	V_{DD}=3V; V_{oL}=1V	33	40		mA
I_{oVO}	DAC Output Current	VO	V_{DD}=3V;VO=0~2V,Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{oL}=2.0V	50			μA
I_{oL_1}	Output Sink Current	I/O pull-low*1	V_{oL}=0.4V	1.0			mA
I_{iL_1}	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
I_{iL_2}	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Spec. for Push-Pull I/O port only
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.
*2: This Spec. base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current to get the total amount of current.(I_{oHPWM} 、I_{oLPWM} * N; N=0,1,2,3,4,5)

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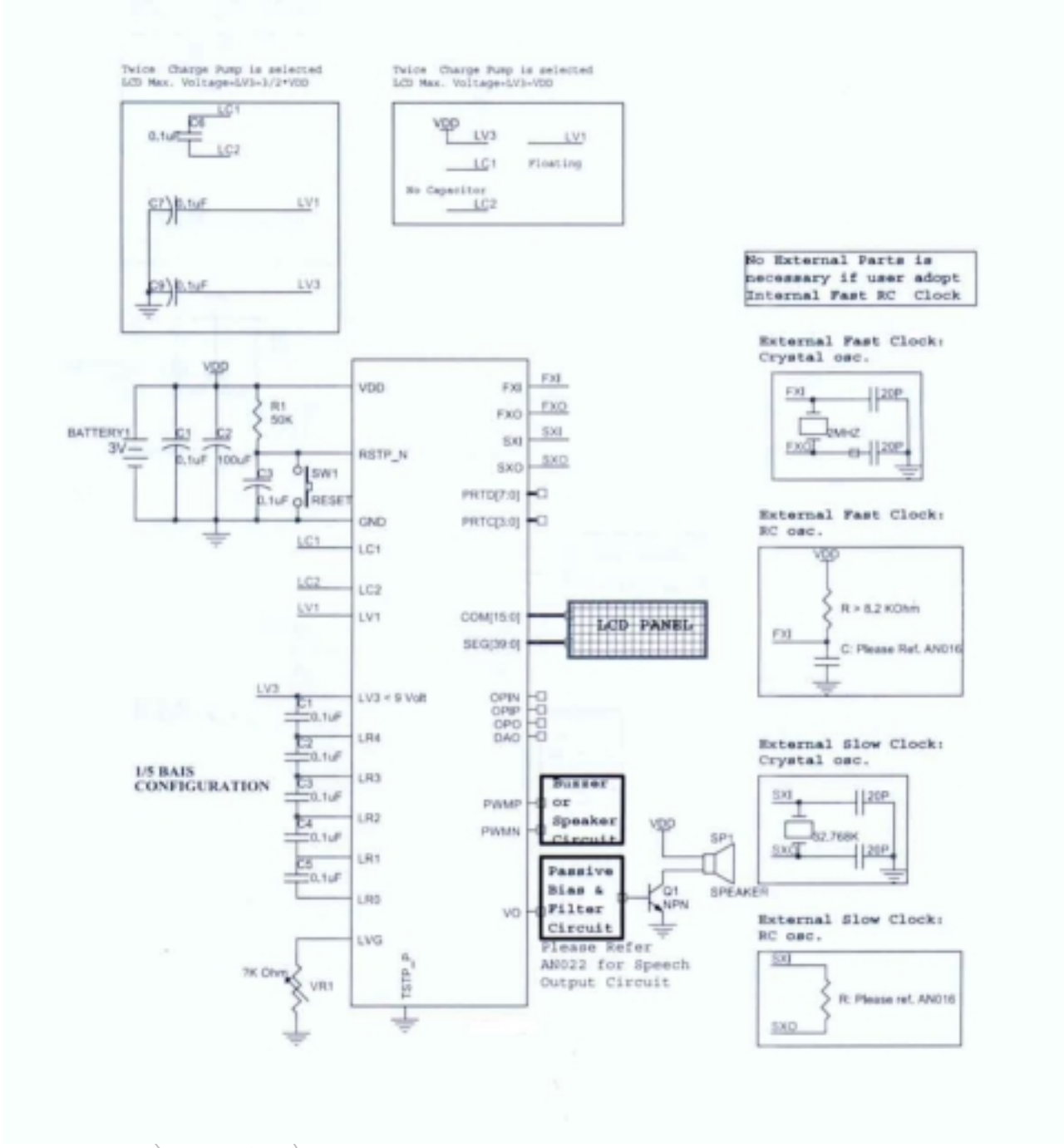
I. Application Circuit



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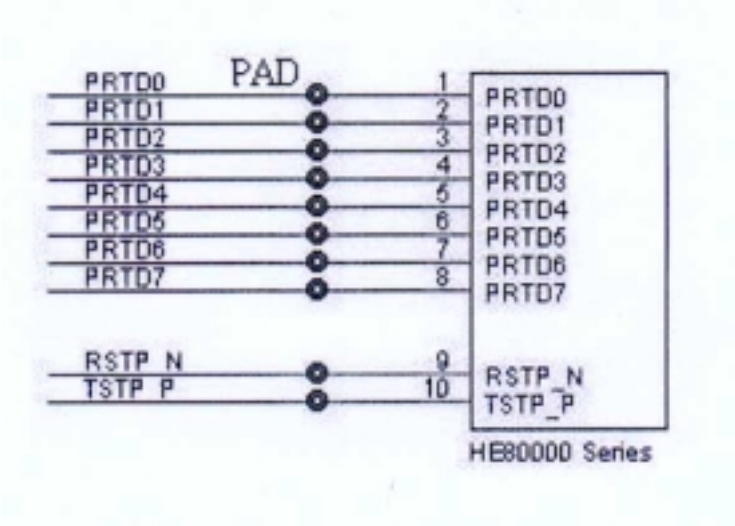
J. Important Note

For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.

LCD driving circuit must be turn off before IC goes into sleep mode

Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB (can be soldered and probed) as you can, then JESS can do some IC testing job on PCB. Neither VDD nor GND connection is necessary for TSTP_P. The following figure is an example (Testing point with through hole.)



LV3 must small than 9.0 Volt. Otherwise IC may breakdown.

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SUPPLEMENTARY SPECIFICATION : HE82/83/89 PWM application

Description:

For HE83/89 PWM application, the following points must be bare in mind.

1. **The PWM output can direct drive buzzer.**
2. **For direct drive speaker, it must use 32Ω or above speaker.**
3. **For speaker application, it must add capacitors between IC's VDD ground and its PWM output, see below figure.**

Note: the 1 F capacitor must be connected near IC's