

#### Features

- High-speed access times
  - Com'l: 10, 12, 15 and 20 ns
  - Ind: 12, 15 and 20 ns
- Low power operation (typical)
  - PDM41532SA
    - Active: 350 mW
    - Standby: 50 mW
  - PDM41532LA
    - Active: 300 mW
    - Standby: 25mW
- High-density 64K x 16 architecture
- Single +5V ( $\pm 10\%$ ) power supply
- Fully static operation
- TTL-compatible inputs and outputs
- Output buffer controls:  $\overline{OE}$
- Data byte controls:  $\overline{LB}$ ,  $\overline{UB}$
- Packages:
  - Plastic SOJ (400 mil) - SO
  - Plastic TSOP (II) - T

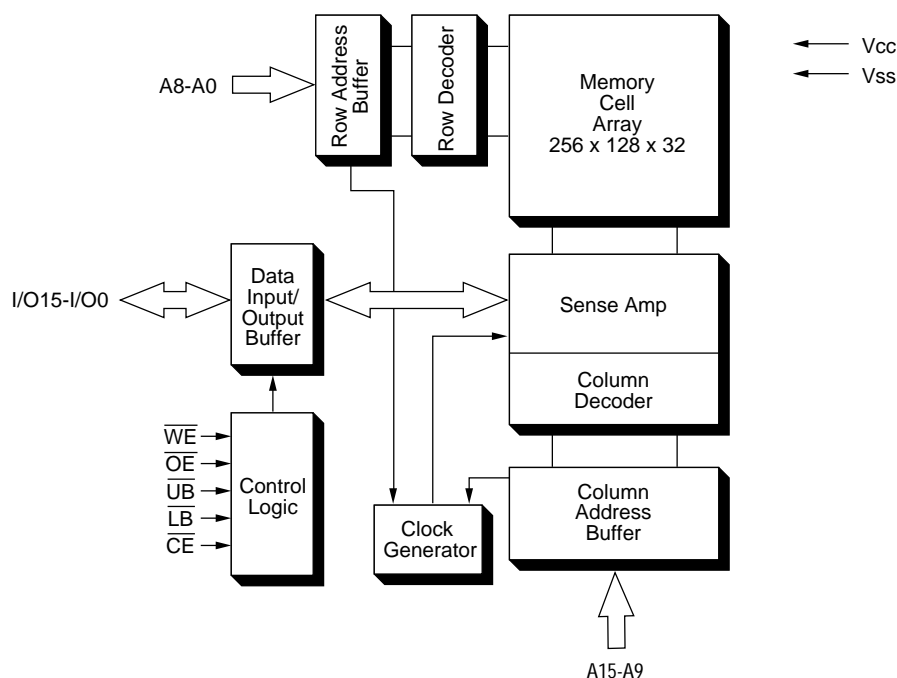
#### Description

The PDM41532 is a high-performance CMOS static RAM organized as 65,536 x 16 bits. The PDM41532 features low power dissipation using chip enable (CE) and has an output enable input (OE) for fast memory access. Byte access is supported by upper and lower byte controls.

The PDM41532 operates from a single 5.0V power supply and all inputs and outputs are fully TTL-compatible. The PDM41532 comes in two versions, the standard power version PDM41532SA and a low power version PDM41532LA. The two versions are functionally the same and only differ in their power consumption.

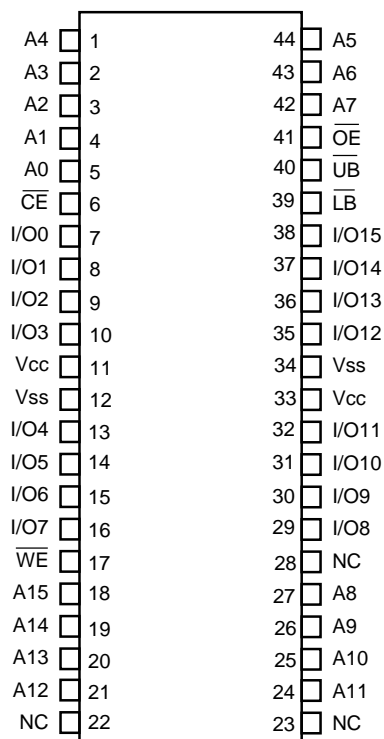
The PDM41532 is available in a 44-pin 400 mil plastic SOJ and a 44-pin plastic TSOP (II) package suitable for high-density surface assembly and is suitable for use in high-speed applications such as cache memory and high-speed storage.

#### Functional Block Diagram

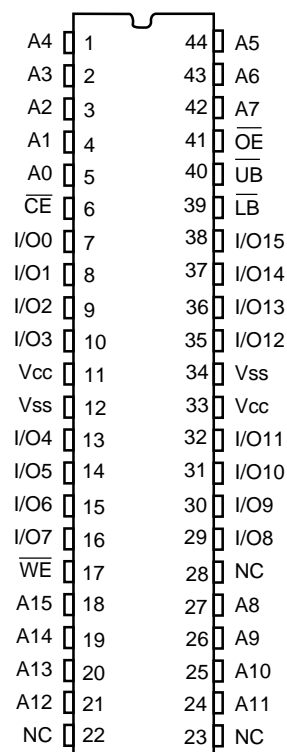


## Pin Configuration

## TSOP (II)



## SOJ



## Pin Description

Name	Description
A15-A0	Address Inputs
I/O15-I/O0	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$ , $\overline{UB}$	Data Byte Control Inputs
NC	No connect
Vss	Ground
Vcc	Power (+5V)

Capacitance ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Symbol	Parameter	Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = V_{SS}$	6	pF
$C_{I/O}$	Output Capacitance	$V_{I/O} = V_{SS}$	8	pF

NOTE: 1. This parameter is determined by device characterization, but is not production tested.

## Operating Mode

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O7-I/O0	I/O15-I/O8	Power
Read	L	L	H	L	L	Output	Output	$I_{CC}$
				H	L	High Impedance	Output	$I_{CC}$
				L	H	Output	High Impedance	$I_{CC}$
Write	L	X	L	L	L	Input	Input	$I_{CC}$
				H	L	High Impedance	Input	$I_{CC}$
				L	H	Input	High Impedance	$I_{CC}$
Output Disable	L	H	H	X	x	High Impedance	High Impedance	$I_{CC}$
	L	X	X	H	H	High Impedance	High Impedance	$I_{CC}$
Standby	H	X	X	X	X	High Impedance	High Impedance	$I_{SB}$

NOTE: 1. H =  $V_{IH}$ , L =  $V_{IL}$ , X = DON'T CARE

## Absolute Maximum Ratings <sup>(1)</sup>

Symbol	Rating	Com'l.	Ind.	Unit
$V_{TERM}$	Terminal Voltage with Respect to $V_{SS}$	-0.5 to +7.0	-0.5 to +7.0	V
$T_{BIAS}$	Temperature Under Bias	-55 to +125	-65 to +135	°C
$T_{STG}$	Storage Temperature	-55 to +125	-65 to +150	°C
$P_T$	Power Dissipation	1.5	1.5	W
$I_{OUT}$	DC Output Current	50	50	mA
$T_j$	Maximum Junction Temperature <sup>(2)</sup>	125	145	°C

- NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form:  $T_j = T_a + P * \theta_{ja}$  where  $T_a$  is the ambient temperature, P is average operating power and  $\theta_{ja}$  the thermal resistance of the package. For this product, use the following  $\theta_{ja}$  values:

SOJ: 59° C/W

TSOP: 87° C/W

## Recommended DC Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

## DC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	PDM41532SA		PDM41532LA		Unit
			Min.	Max.	Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	-5	5	-5	5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., CE = V <sub>IH</sub> , V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>	-5	5	-5	5	μA
V <sub>IL</sub>	Input Low Voltage		-0.5 <sup>(1)</sup>	0.8	-0.5 <sup>(1)</sup>	0.8	V
V <sub>IH</sub>	Input High Voltage		2.2	V <sub>CC</sub> + 0.5	2.2	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8 mA, V <sub>CC</sub> = Min.	—	0.4	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4 mA, V <sub>CC</sub> = Min.	2.4	—	2.4	—	V

NOTE: 1. V<sub>IL</sub>(min) = -3.0V for pulse width less than 20 ns.

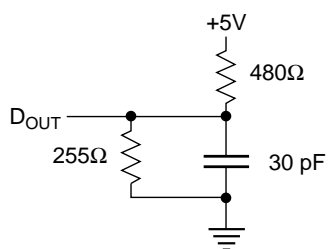
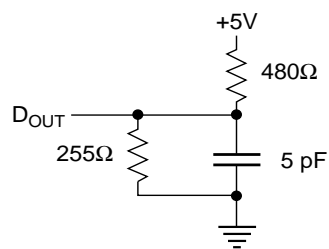
## Power Supply Characteristics

Symbol	Parameter	Power	-10		-12		-15		-20		Unit
			Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I <sub>CC</sub>	Operating Current CE = V <sub>IL</sub>	SA	300	280	290	260	270	240	250		mA
	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = Max. I <sub>OUT</sub> = 0 mA	LA	150	140	150	130	140	120	130		mA
I <sub>SB</sub>	Standby Current CE = V <sub>IH</sub>	SA	40	40	40	35	35	30	30		mA
	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = Max.	LA	30	30	30	25	25	20	20		mA
I <sub>SB1</sub>	Full Standby Current CE ≥ V <sub>CC</sub> - 0.2V	SA	10	10	15	10	15	10	15		mA
	f = 0 V <sub>CC</sub> = Max., V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or ≤ 0.2V	LA	5	5	10	5	10	5	10		mA

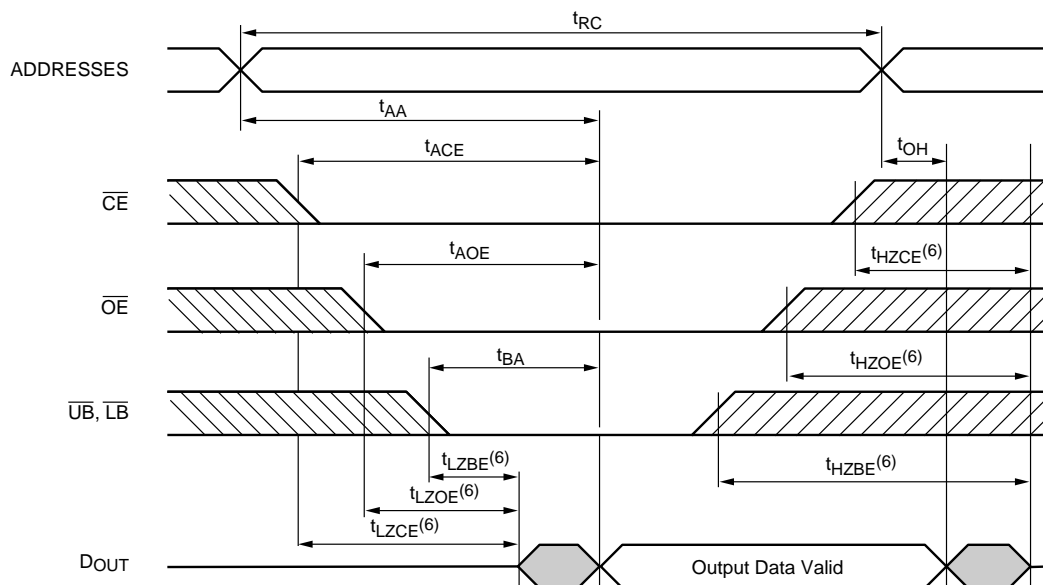
NOTES: All values are maximum guaranteed values.

**AC Test Conditions**

Input pulse levels	$V_{SS}$ to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

**Figure 1. Output Load****Figure 2. Output Load Equivalent**  
(for  $t_{LZCE}$ ,  $t_{HZCE}$ ,  $t_{LZWE}$ ,  $t_{HZWE}$ ,  $t_{LZOE}$ ,  $t_{HZOE}$ ,  
 $t_{LZBE}$ ,  $t_{HZBE}$ )

## Read Cycle Timing Diagram



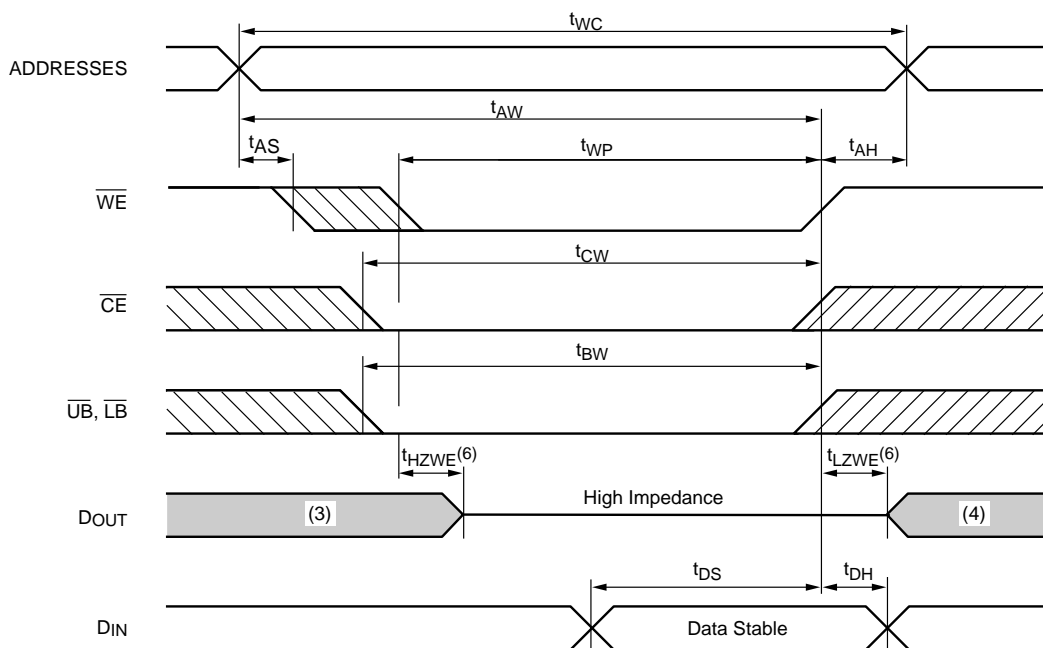
## AC Electrical Characteristics

Description		-10		-12		-15		-20		
READ Cycle	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
READ cycle time	$t_{RC}$	10	—	12	—	15	—	20	—	ns
Address access time	$t_{AA}$	—	10	—	12	—	15	—	20	ns
Chip enable access time	$t_{ACE}$	—	9	—	11	—	14	—	18	ns
Byte access time	$t_{BA}$	—	5	—	6	—	7	—	9	ns
Output hold from address change	$t_{OH}$	2	—	2	—	3	—	3	—	ns
Byte disable to output in low-Z <sup>(1, 6)</sup>	$t_{LZBE}$	0	—	0	—	0	—	0	—	ns
Byte enable to output in high-Z <sup>(1, 6)</sup>	$t_{HZBE}$	—	5	—	6	—	7	—	9	ns
Chip enable to output in low-Z <sup>(1, 6)</sup>	$t_{LZCE}$	3	—	3	—	3	—	3	—	ns
Chip disable to output high-Z <sup>(1, 6)</sup>	$t_{HZCE}$	—	5	—	6	—	7	—	9	ns
Output enable access time	$t_{AOE}$	—	5	—	6	—	7	—	9	ns
Output enable to output in low-Z <sup>(1, 6)</sup>	$t_{LZOE}$	0	—	0	—	0	—	0	—	ns
Output disable to output in high-Z <sup>(1, 6)</sup>	$t_{HZOE}$	—	5	—	6	—	7	—	9	ns

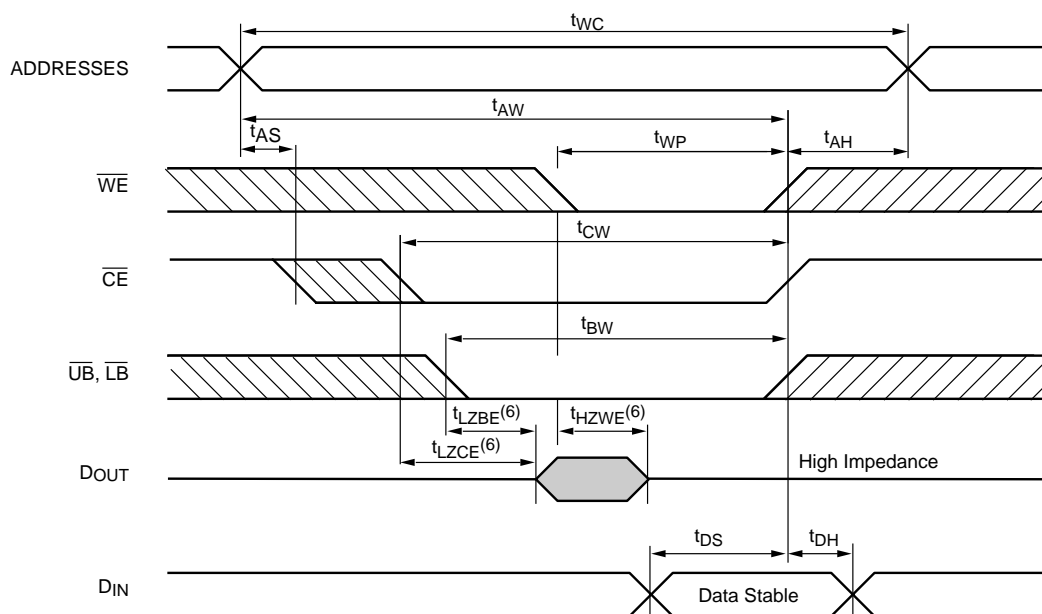
NOTES: 1. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZWE}$  is less than  $t_{LZWE}$ .

2.  $t_{HZCE}$ ,  $t_{HZOE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in Figure 2. Transition is measured  $\pm 200$  mV from steady state voltage.

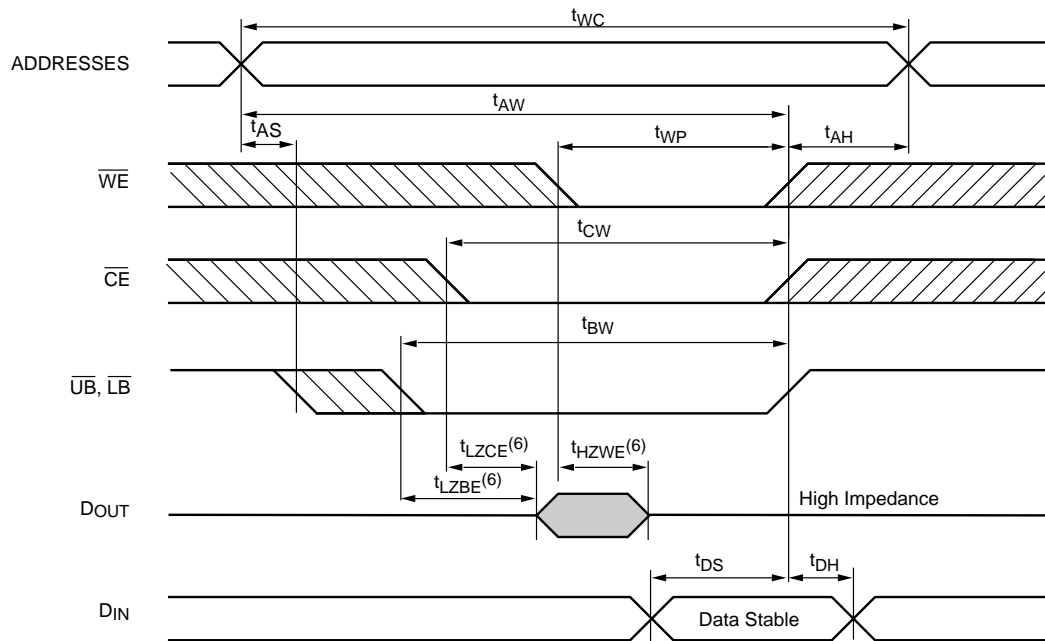
### Write Cycle 1 Timing Diagram<sup>(5)</sup> ( $\overline{\text{WE}}$ Controlled)



### Write Cycle 2 Timing Diagram<sup>(5)</sup> ( $\overline{\text{CE}}$ Controlled)



### Write Cycle 3 Timing Diagram<sup>(5)</sup> ( $\overline{UB}$ , $\overline{LB}$ Controlled)



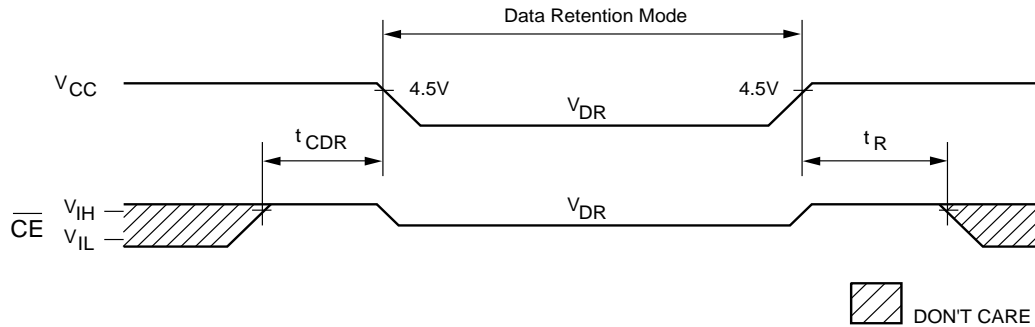
### AC Electrical Characteristics

Description		-10		-12		-15		-20		
WRITE Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE cycle time	$t_{WC}$	10	—	12	—	15	—	20	—	ns
Chip enable to end of write	$t_{CW}$	9	—	10	—	12	—	12	—	ns
Address valid to end of write	$t_{AW}$	9	—	8	—	10	—	12	—	ns
Byte pulse width	$t_{BW}$	9	—	8	—	10	—	12	—	ns
Address setup time	$t_{AS}$	0	—	0	—	0	—	0	—	ns
Address hold from end of write	$t_{AH}$	0	—	0	—	0	—	0	—	ns
Write pulse width	$t_{WP}$	9	—	8	—	9	—	10	—	ns
Data setup time	$t_{DS}$	5	—	6	—	7	—	9	—	ns
Data hold time	$t_{DH}$	0	—	0	—	0	—	0	—	ns
Byte disable to output in low-Z <sup>(1, 5, 6)</sup>	$t_{LZBE}$	0	—	0	—	0	—	0	—	ns
Byte enable to output in high-Z <sup>(1, 5, 6)</sup>	$t_{HZBE}$	—	5	—	6	—	7	—	9	ns
Output disable to output in low-Z <sup>(1, 5, 6)</sup>	$t_{LZOE}$	0	—	0	—	0	—	0	—	ns
Output enable to output in high-Z <sup>(1, 5, 6)</sup>	$t_{HZOE}$	—	5	—	6	—	7	—	9	ns
Write disable to output in low-Z <sup>(1, 5, 6)</sup>	$t_{LZWE}$	0	—	0	—	0	—	0	—	ns
Write enable to output in high-Z <sup>(1, 5, 6)</sup>	$t_{HZWE}$	—	5	—	6	—	7	—	9	ns



- NOTES:**
1. This parameter is determined by device characterization but is not production tested.
  2.  $\overline{WE}$  is HIGH for read cycles.
  3. If the  $\overline{CE}$  LOW transition occurs coincident with or after the  $\overline{WE}$  LOW transition, outputs remain in a high impedance state.
  4. If the  $\overline{CE}$  HIGH transition occurs coincident with or after the  $\overline{WE}$  HIGH transition, outputs remain in a high impedance state.
  5. If  $\overline{OE}$  is HIGH during a write cycle, the outputs are in a high-impedance state during this period.
  6. Measured with  $C_L = 5\text{pF}$  as in Figure 2. Transition is measured  $\pm 200\text{mV}$  from steady state voltage.

### Low $V_{CC}$ Data Retention Waveform



### Data Retention Electrical Characteristics (LA Version Only)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Retention Data		2.5	—	5.5	V
$I_{CCDR}$	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$				
		$V_{CC} = 2V$	—	95	500	$\mu A$
		$V_{CC} = 3V$	—	350	750	$\mu A$
$t_{CDR}$	Chip Deselect to Data Retention Time		0	—	—	ns
$t_R^{(1)}$	Operation Recovery Time		$t_{RC}$	—	—	ns

NOTE: 1. This parameter is sampled.

## Ordering Information

<u>XXXXXX</u>	<u>X</u>	<u>XX</u>	<u>X</u>	<u>X</u>	<u>X</u>	
Device Type	Power	Speed	Package Type	Process Temp. Range	Preferred Shipping Container	
						Blank Tubes
						TR Tape & Reel
						TY Tray
						Blank Commercial (0° to +70°C)
						I Industrial (−40°C to +85°C)
						A Automotive (−40°C to +105°C)
						SO 44-pin 400 mil Plastic SOJ
						T 44-pin Plastic TSOP
						10 Commercial Only
						12
						15
						20
						SA Standard Power
						LA Low Power
						PDM41532 - (64Kx16) Static RAM