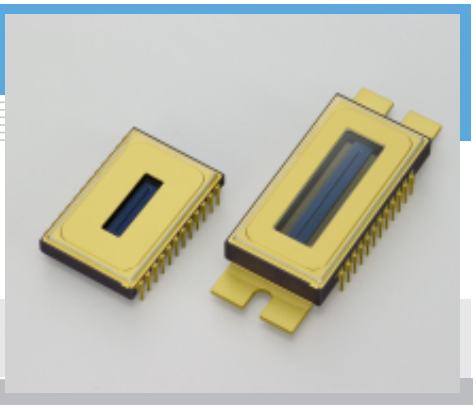
NEW

IMAGE SENSOR



CCD image sensor
S9037/S9038 series

High-speed operation, back-thinned FFT-CCD

S9037/S9038 series FFT-CCD image sensors were developed for high-speed line scan cameras. Since an on-chip amplifier having a wide bandwidth is used to an image sensor, a pixel rate of 10 MHz can be obtained. S9037/S9038 series image sensors also deliver a high line scan rate equivalent to interline CCD sensors when used in line binning operation mode, because they have an active area pixel format where the number of vertical pixels is less than the number of horizontal pixels. This makes S9037/S9038 series ideal for line scan cameras.
S9037/S9038 series image sensors have a pixel size of 24 × 24 µm and are available in pixel formats of 512 × 4 pixels and 1024 × 4 pixels.
S9038 series has a one-stage thermoelectric cooler assembled in the same package allowing stable operation at cooled temperatures. Both S9037/S9038 series image sensors use a quartz glass window equivalent to SUPRASIL glass that provides high transmittance even at 193 nm wavelength. These image sensors also have stable quantum efficiency in the UV region making them ideal for excimer laser monitors.

Features

- High-speed operation: 10 MHz
- Pixel size: 24 × 24 µm
- Line/pixel binning operation
- S9038 series: one-stage thermoelectric cooling
- High quantum efficiency: 90 % or more at peak
- MPP operation

Applications

- Excimer laser monitors
- High-speed line scan cameras

■ Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]
S9037-0902	Non-cooled	520 × 6	512 × 4	12.288 × 0.096
S9037-1002		1044 × 8	1024 × 4	24.576 × 0.096
S9038-0902	One-stage TE-cooled	520 × 6	512 × 4	12.288 × 0.096
S9038-1002		1044 × 8	1024 × 4	24.576 × 0.096

■ Specifications

Parameter	S9037-0902	S9037-1002	S9038-0902	S9038-1002
Line rate	16 kHz	8 kHz	16 kHz	8 kHz
Data rate	10 MHz			
Vertical clock	2 phases			
Horizontal clock	2 phases			
Output circuit	Two-stage MOSFET source follower			
Package	24 pin metal package			
Window material	Quartz window equivalent to SUPRASIL *1			

*1: Windowless type is available as option.

PRELIMINARY DATA
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SOLID STATE DIVISION

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+70	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+25	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGH voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	12	15	-	V
Reset drain voltage		V_{RD}	11.5	12	12.5	V
Output gate voltage		V_{OG}	1	3	5	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (horizontal input gate)		V_{IG1H}, V_{IG2H}	-8	0	-	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	4	6	8	V
	Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	4	6	8	V
	Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	4	6	8	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	4	6	8	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	4	6	8	V
	Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency		fc	-	-	-	10	MHz
Reset clock frequency		frg	-	-	-	10	MHz
Vertical shift register capacitance	-0902	C_{P1V}, C_{P2V}	-	-	300	-	pF
	-1002		-	-	500	-	pF
Horizontal shift register capacitance	-0902	C_{P1H}, C_{P2H}	-	-	200	-	pF
	-1002		-	-	300	-	pF
Summing gate capacitance		C_{SG}	-	-	7	-	pF
Reset gate capacitance		C_{RG}	-	-	7	-	pF
Transfer gate capacitance		C_{TG}	-	-	15	-	pF
Transfer efficiency		CTE	*2	-	0.99995	-	-
DC output level		Vout	-	-	7	-	V
Output impedance		Zo	*3	-	500	-	Ω
Power dissipation		P	*3, *4	-	100	-	mW

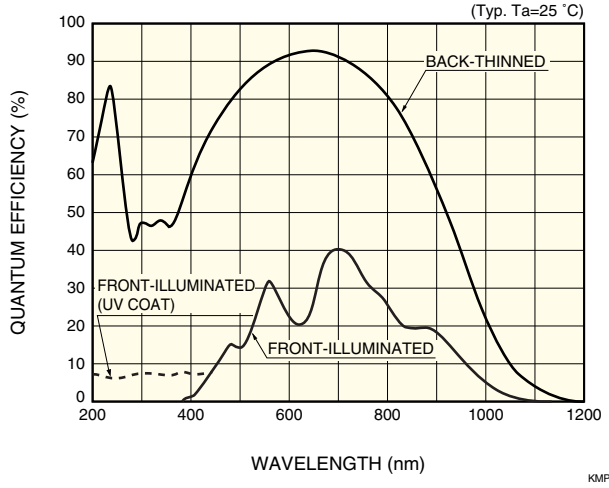
*2: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*3: This depends on the output transistor drain voltage.
*4: Power dissipation of the on-chip amplifier.

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

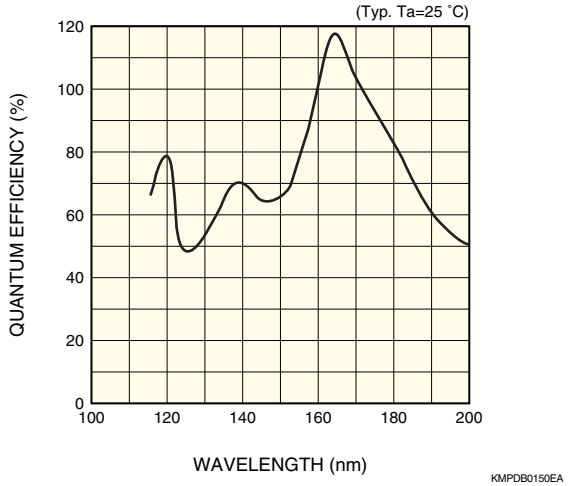
Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat		Fw × Sv		V
Full well capacity	Vertical	Fw	-	300	-	ke⁻
	Horizontal (summing)		-	600	-	
CCD node sensitivity		Sv	-	1.2	-	μV/e⁻
Dark current *5 (MPP mode)	25 °C	DS	-	4,000	-	e⁻/pixel/s
	0 °C		-	200	-	
Readout noise *6		Nr	-	100	-	e⁻rms
Dynamic range (line binning)		DR	-	6000	-	-
Photo response non-uniformity *7		PRNU	-	-	±10	%
Spectral response range (without window)		λ	-	200 to 1100	-	nm

*5: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*6: -40 °C, operating frequency is 80 kHz.
*7: Condition: half of saturation output voltage.

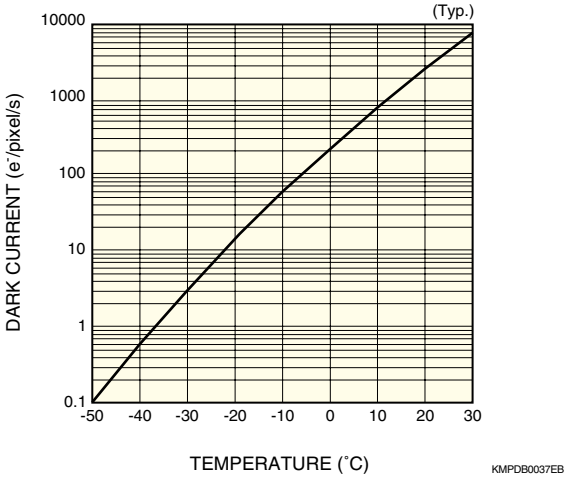
■ Spectral response



■ Spectral response of photosensitive surface (without cap)

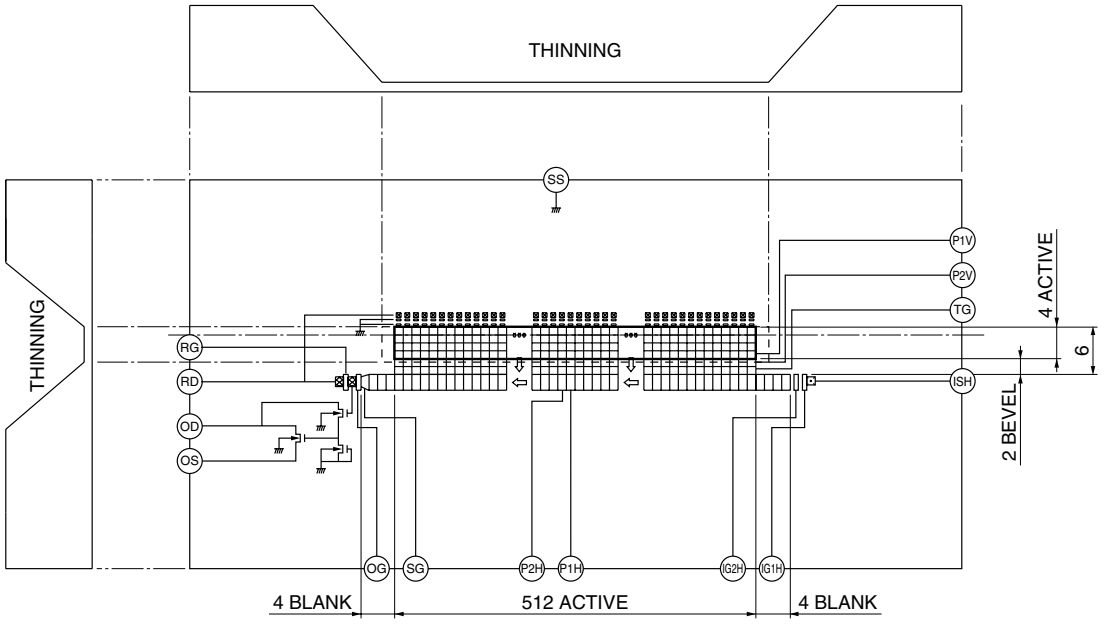


■ Dark current vs. temperature



■ Device structure

S9037/S9038-0902



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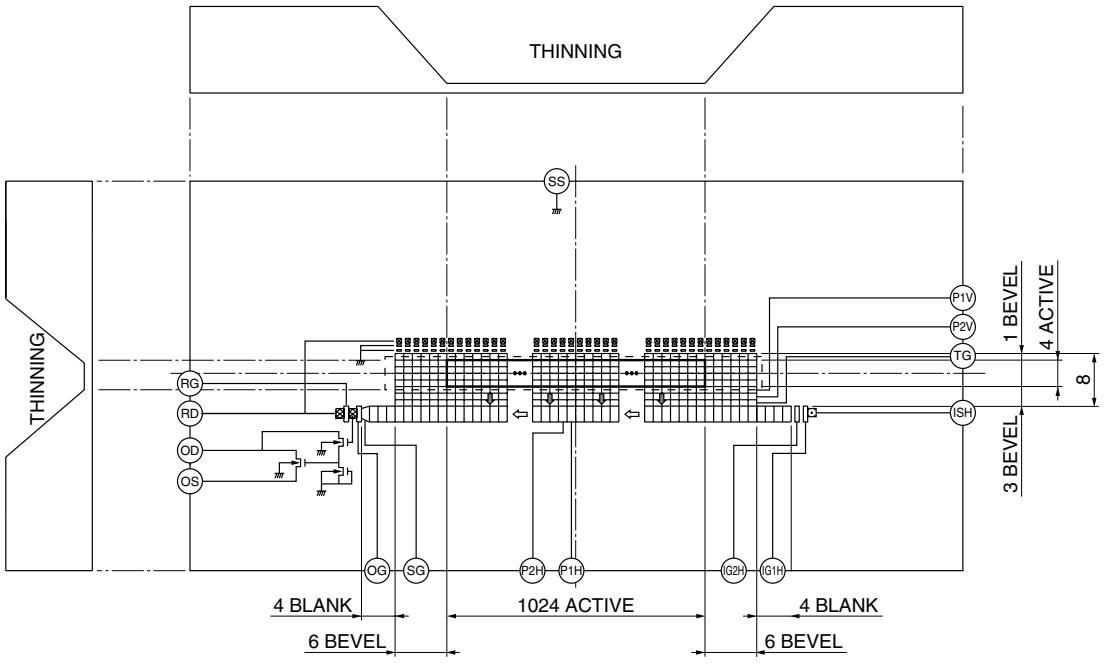
S9037/S9038-1002



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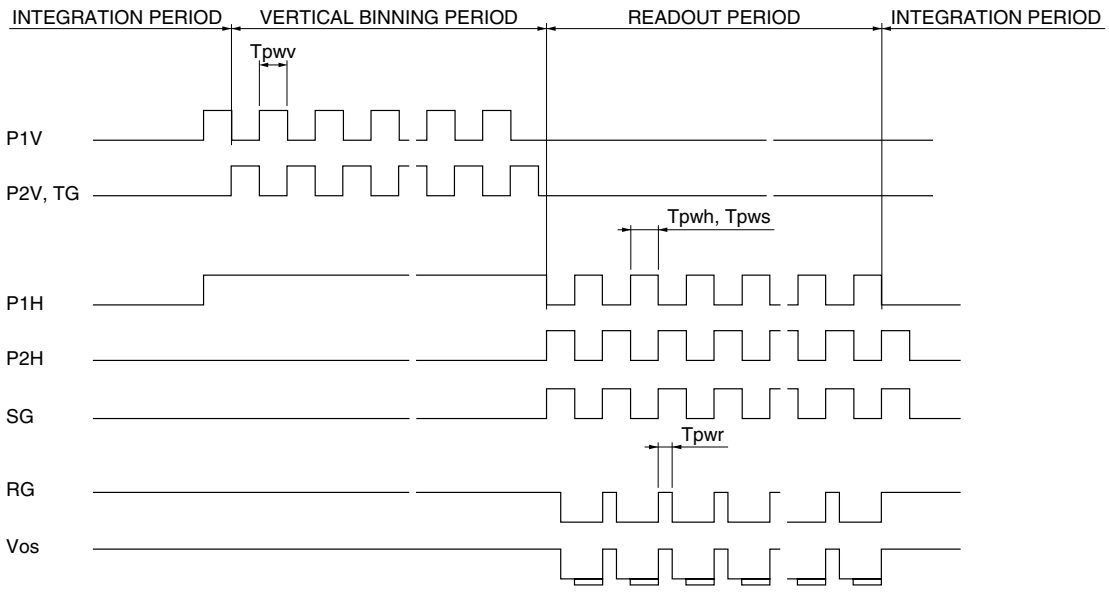
■ Timing chart (line binning)



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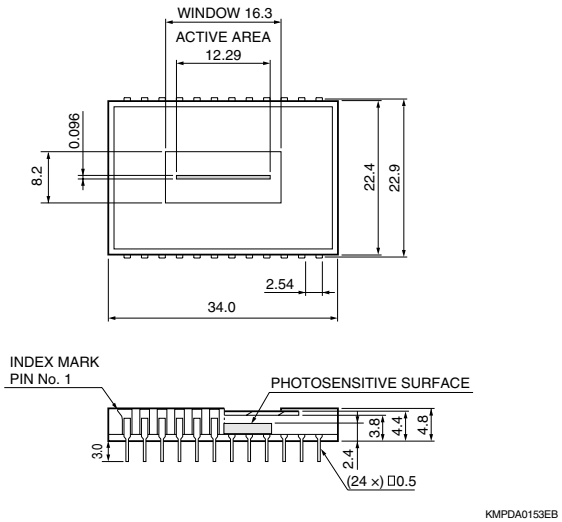
Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	1	-	-	µs
	Rise and fall time	Tprv, Tpfv	-	20	-	ns
P1H, P2H	Pulse width	Tpwh	50	-	-	ns
	Rise and fall time	Tprh, Tpfh	-	10	-	ns
	Duty ratio	-	-	50	-	%
SG	Pulse width	Tpws	50	-	-	ns
	Rise and fall time	Tprs, Tpfs	-	10	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	Tpwr	-	15	-	ns
	Rise and fall time	Tprr, Tpfr	5	-	-	ns
TG (P2V) - P1H	Overlap time	Tovr	3	-	-	µs

■ Dimensional outlines (unit: mm)

S9037-0902



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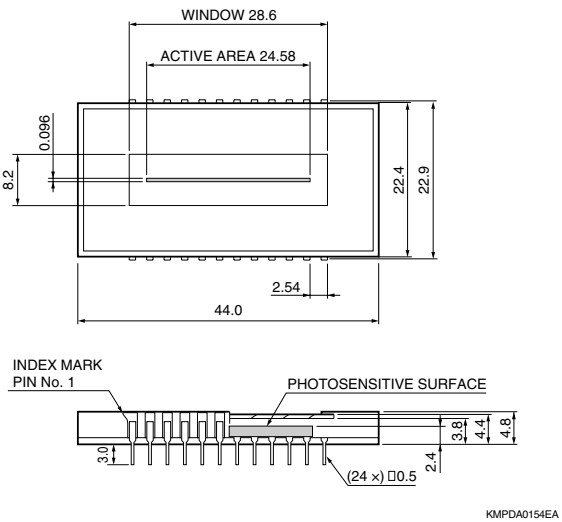

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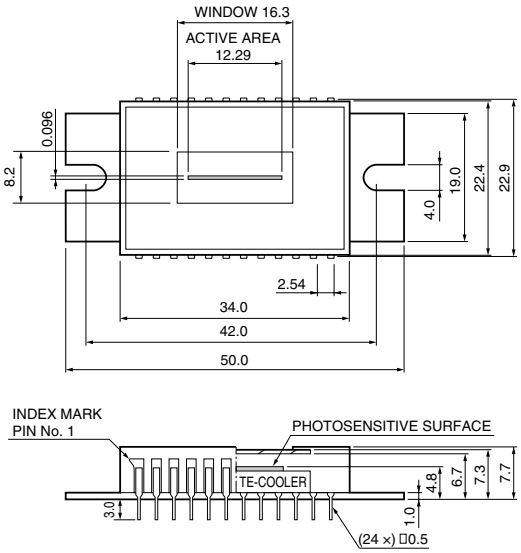

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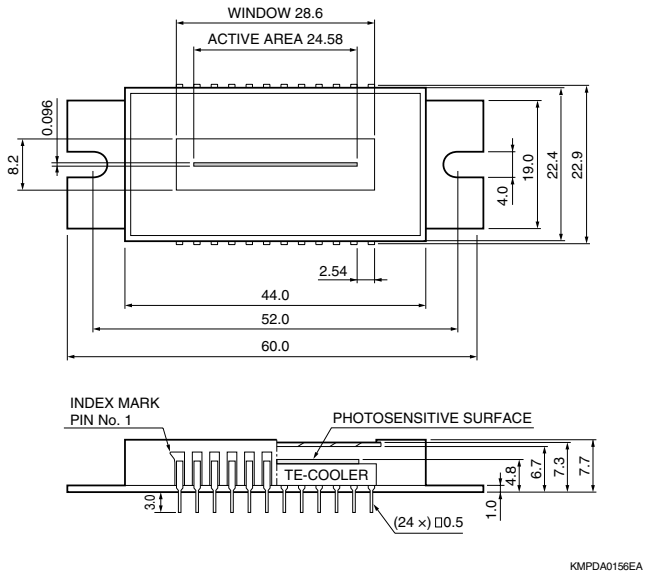

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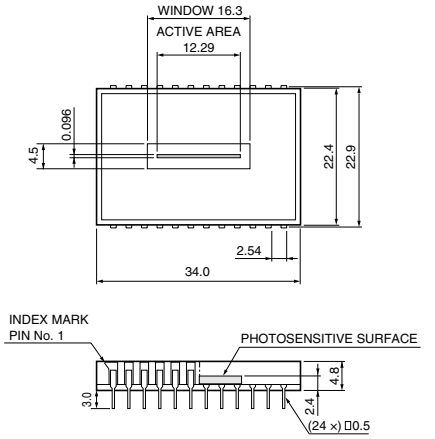
■ Dimensional outlines of windowless types (unit: mm)

S9037-0902N



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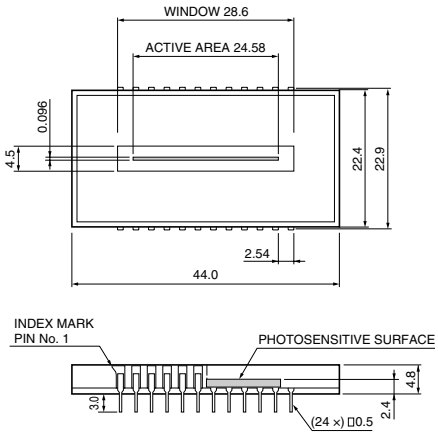

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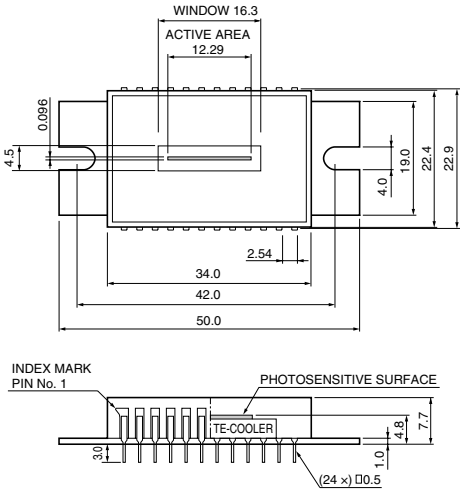

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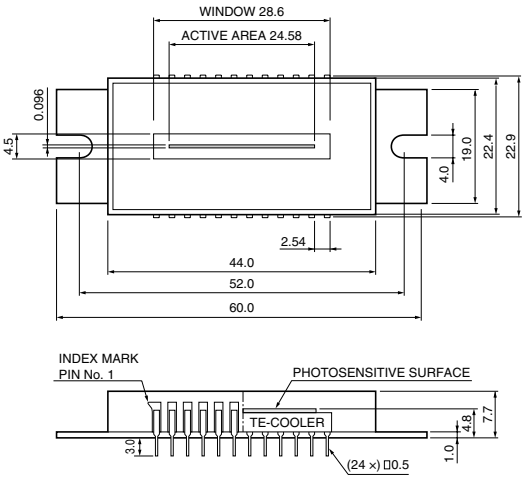

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■ Pin connections

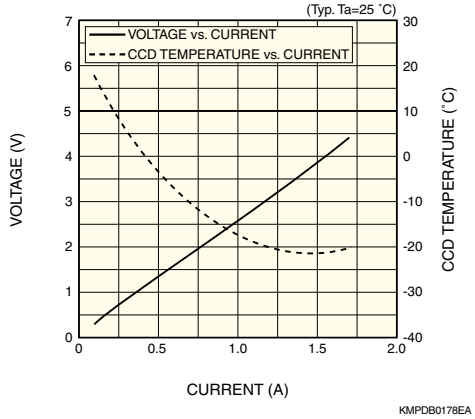
Pin No.	S9037 series		Remark	S9038 series		Remark
	Symbol	Description		Symbol	Description	
1	RD	Reset drain	+12 V	RD	Reset drain	+12 V
2	OS	Output transistor source	External R_2=2.2 kΩ	OS	Output transistor source	External R_L=2.2 kΩ
3	OD	Output transistor drain	+15 V	OD	Output transistor drain	+15 V
4	OG	Output gate	+3 V	OG	Output gate	+3 V
5	SG	Summing gate	Same timing as P2H	SG	Summing gate	Same timing as P2H
6	-			-		
7	-			-		
8	P2H	CCD horizontal register clock-2		P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1		P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	GND	IG2H	Test point (horizontal input gate-2)	GND
11	IG1H	Test point (horizontal input gate-1)	GND	IG1H	Test point (horizontal input gate-1)	GND
12	ISH	Test point (horizontal input source)	Shorted to RD	ISH	Test point (horizontal input source)	Shorted to RD
13	TG	Transfer gate	Same timing as P2V	TG	Transfer gate	Same timing as P2V
14	P2V	CCD vertical register clock-2		P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1		P1V	CCD vertical register clock-1	
16	NC			Th1	Thermistor	
17	NC			Th2	Thermistor	
18	NC			P-	TE-cooler-	
19	NC			P+	TE-cooler+	
20	SS	Substrate (GND)	GND	SS	Substrate (GND)	
21	NC			NC		
22	NC			NC		
23	NC			NC		
24	RG	Reset gate		RG	Reset gate	

■ Specifications of built-in TE-cooler (Typ.)

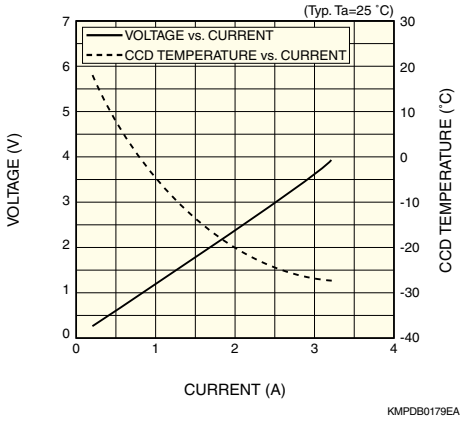
Parameter	Symbol	Condition	S9038-0902	S9038-1002	Unit
Internal resistance	Rint	Ta=25 °C	2.5	1.2	Ω
Maximum current *8	Imax	Tc *9=Th *10=25 °C	1.5	3.0	A
Maximum voltage	Vmax	Tc *9=Th *10=25 °C	3.8	3.6	V
Maximum heat absorption *11	Qmax		3.4	5.1	W
Maximum temperature of heat radiating side	-		70	70	°C

*8: Maximum current Imax:
If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.
*9: Temperature of the cooling side of thermoelectric cooler.
*10: Temperature of the heat radiating side of thermoelectric cooler.
*11: Maximum heat absorption Qmax.
This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.

S9038-0902



S9038-1002

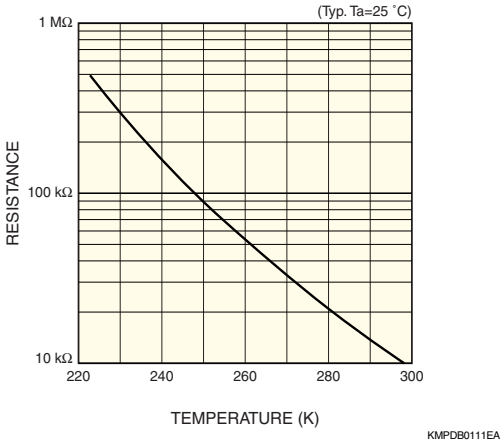


■ Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R1 = R2 \times \exp B\,(1 / T1 - 1 / T2)$
where R1 is the resistance at absolute temperature T1 (K)
R2 is the resistance at absolute temperature T2 (K)
B is so-called the B constant (K)

The characteristics of the thermistor used are as follows.
R (298K) = 10 kΩ
B (298K / 323K) = 3450 K



■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing and use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

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