FAIRCHILD SEMICONDUCTOR™

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# DM74LS164
# 8-Bit Serial In/Parallel Out Shift Register

## General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the LOW-to-HIGH level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

## Features

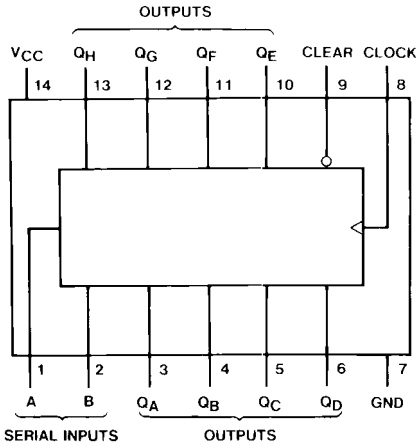
- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74LS164M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| DM74LS164N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram



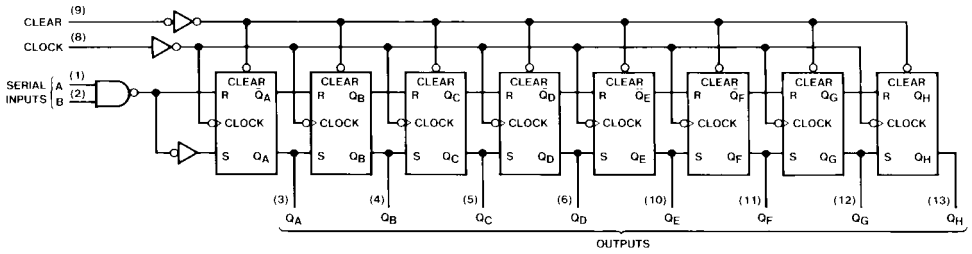

## Function Table

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| **Clear** | **Clock** | **A** | **B** | $Q_A$ | $Q_B$ | ... | $Q_H$ |
| L | X | X | X | L | L | ... | L |
| H | L | X | X | $Q_{A0}$ | $Q_{B0}$ | ... | $Q_{H0}$ |
| H | ↑ | H | H | H | $Q_{An}$ | ... | $Q_{Gn}$ |
| H | ↑ | L | X | L | $Q_{An}$ | ... | $Q_{Gn}$ |
| H | ↑ | X | L | L | $Q_{An}$ | ... | $Q_{Gn}$ |

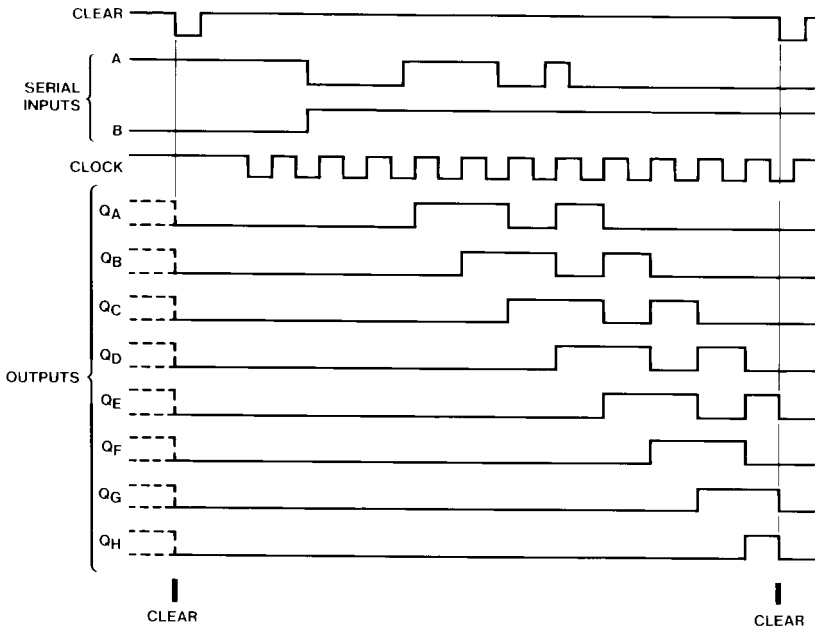
H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from LOW-to-HIGH level
$Q_{A0}$, $Q_{B0}$, $Q_{H0}$ = The level of $Q_A$, $Q_B$, or $Q_H$, respectively, before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Gn}$ = The level of $Q_A$ or $Q_G$ before the most recent ↑ transition of the clock; indicates a one-bit shift.

## Logic Diagram




## Timing Diagram



## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" tables will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Nom | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | HIGH Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | | −0.4 | mA |
| $I_{OL}$ | LOW Level Output Current | | | | 8 | mA |
| $f_{CLK}$ | Clock Frequency (Note 2) | | 0 | | 25 | MHz |
| $t_W$ | Pulse Width | Clock | 20 | | | ns |
| | (Note 2) | Clear | 20 | | | |
| $t_{SU}$ | Data Setup Time (Note 2) | | 17 | | | ns |
| $t_H$ | Data Hold Time (Note 2) | | 5 | | | ns |
| $t_{REL}$ | Clear Release Time (Note 2) | | 30 | | | ns |
| $T_A$ | Free Air Operating Temperature | | 0 | | 70 | °C |

**Note 2:** $T_A = 25°C$ and $V_{CC} = 5V$.

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 3) | Max | Units |
|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | −1.5 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max<br>$V_{IL}$ = Max, $V_{IH}$ = Min | 2.7 | 3.4 | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max<br>$V_{IL}$ = Max, $V_{IH}$ = Min | | 0.35 | 0.5 | V |
| | | $I_{OL}$ = 4 mA, $V_{CC}$ = Min | | 0.25 | 0.4 | |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 7V | | | 0.1 | mA |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7V | | | 20 | µA |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V | | | −0.4 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 4) | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (Note 5) | | 16 | 27 | mA |

**Note 3:** All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

**Note 4:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

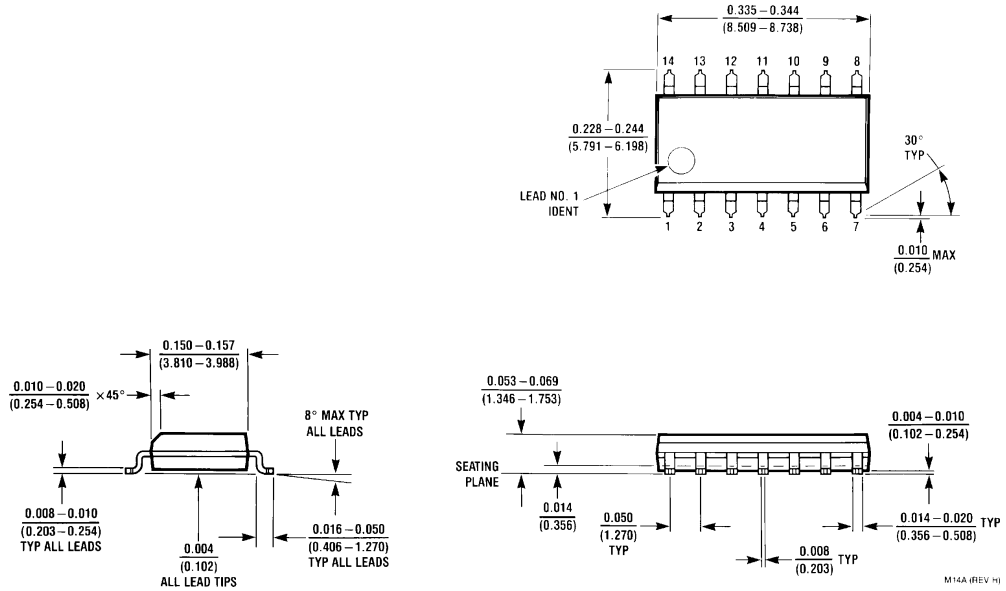
**Note 5:** $I_{CC}$ is measured with all outputs OPEN, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

## Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$

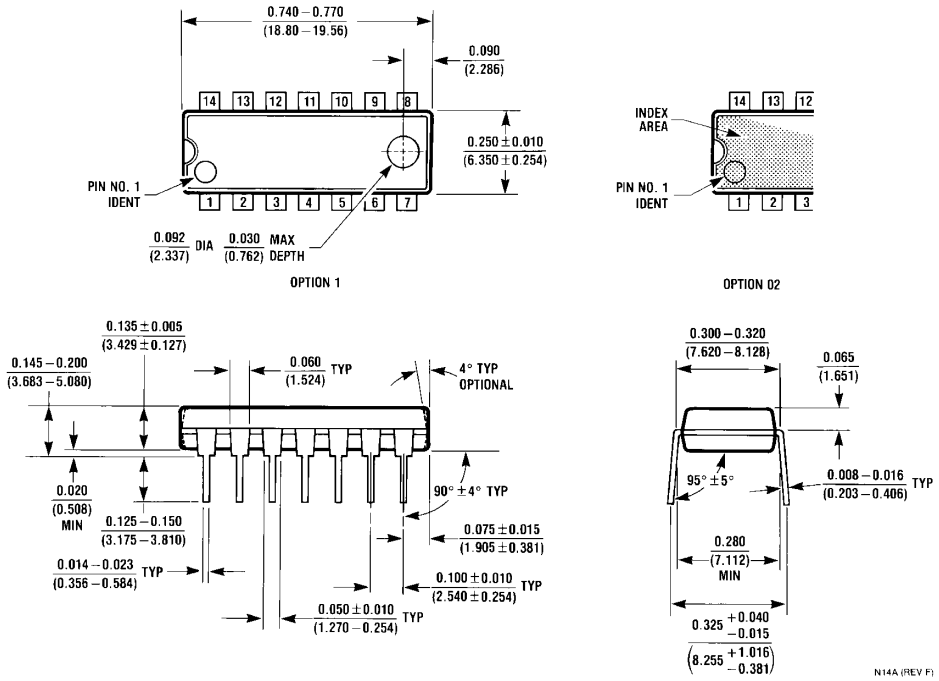
| Symbol | Parameter | From (Input) To (Output) | $R_L$ = 2 kΩ | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 15 pF | | $C_L$ = 50 pF | | |
| | | | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | 25 | | | | MHz |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Clock to Output | | 27 | | 30 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Clock to Output | | 32 | | 40 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Clear to Output | | 36 | | 45 | ns |

## Physical Dimensions inches (millimeters) unless otherwise noted




**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow**
**Package Number M14A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N14A**