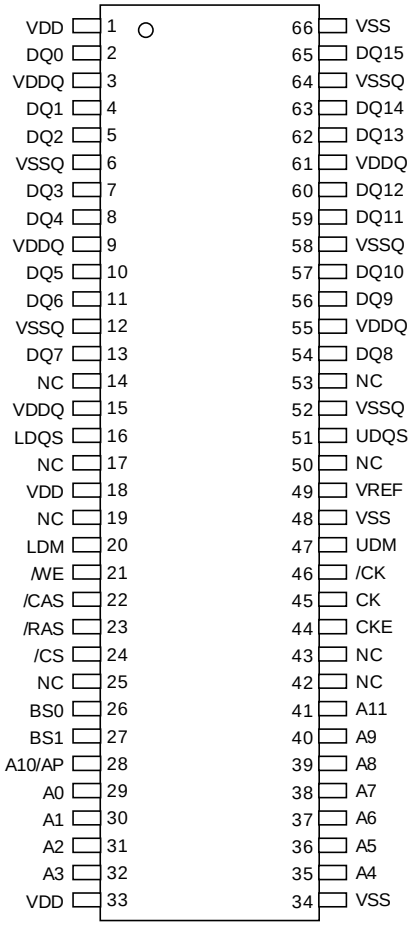
4M x 16 DDR Synchronous DRAM (SDRAM)

Etron Confidential **(Rev. 1.1 Jan./2002)**

Features

- Fast clock rate: 300/285/250/200/166/143/125MHz
- Differential Clock CK & /CK
- Bi-directional DQS
- DLL enable/disable by EMRS
- Fully synchronous operation
- Internal pipeline architecture
- Four internal banks, 1M x 16-bit for each bank
- Programmable Mode and Extended Mode registers
  - /CAS Latency: 2, 2.5, 3
  - Burst length: 2, 4, 8
  - Burst Type: Sequential & Interleaved
- Individual byte write mask control
- DM Write Latency = 0
- Auto Refresh and Self Refresh
- 4096 refresh cycles / 64ms
- Precharge & active power down
- Power supplies: V_{DD} = 3.3V ± 0.3V
  V_{DDQ} = 2.5V ± 0.2V
- Interface: SSTL_2 I/O Interface
- Package: 66 Pin TSOP II, 0.65mm pin pitch

Pin Assignment (Top View)



Ordering Information

Part Number	Frequency	Package
EM658160TS-3.3	300MHz	TSOP II
EM658160TS-3.5	285MHz	TSOP II
EM658160TS-4	250MHz	TSOP II
EM658160TS-5	200MHz	TSOP II
EM658160TS-6	166MHz	TSOP II
EM658160TS-7	143MHz	TSOP II
EM658160TS-8	125MHz	TSOP II

Overview

The EM658160 SDRAM is a high-speed CMOS double data rate synchronous DRAM containing 64 Mbits. It is internally configured as a quad 1M x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK). Data outputs occur at both rising edges of CK and /CK. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The EM658160 provides programmable Read or Write burst lengths of 2, 4, 8, full page.

An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. In addition, EM658160 features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth, result in a device particularly well suited to high performance main memory and graphics applications.

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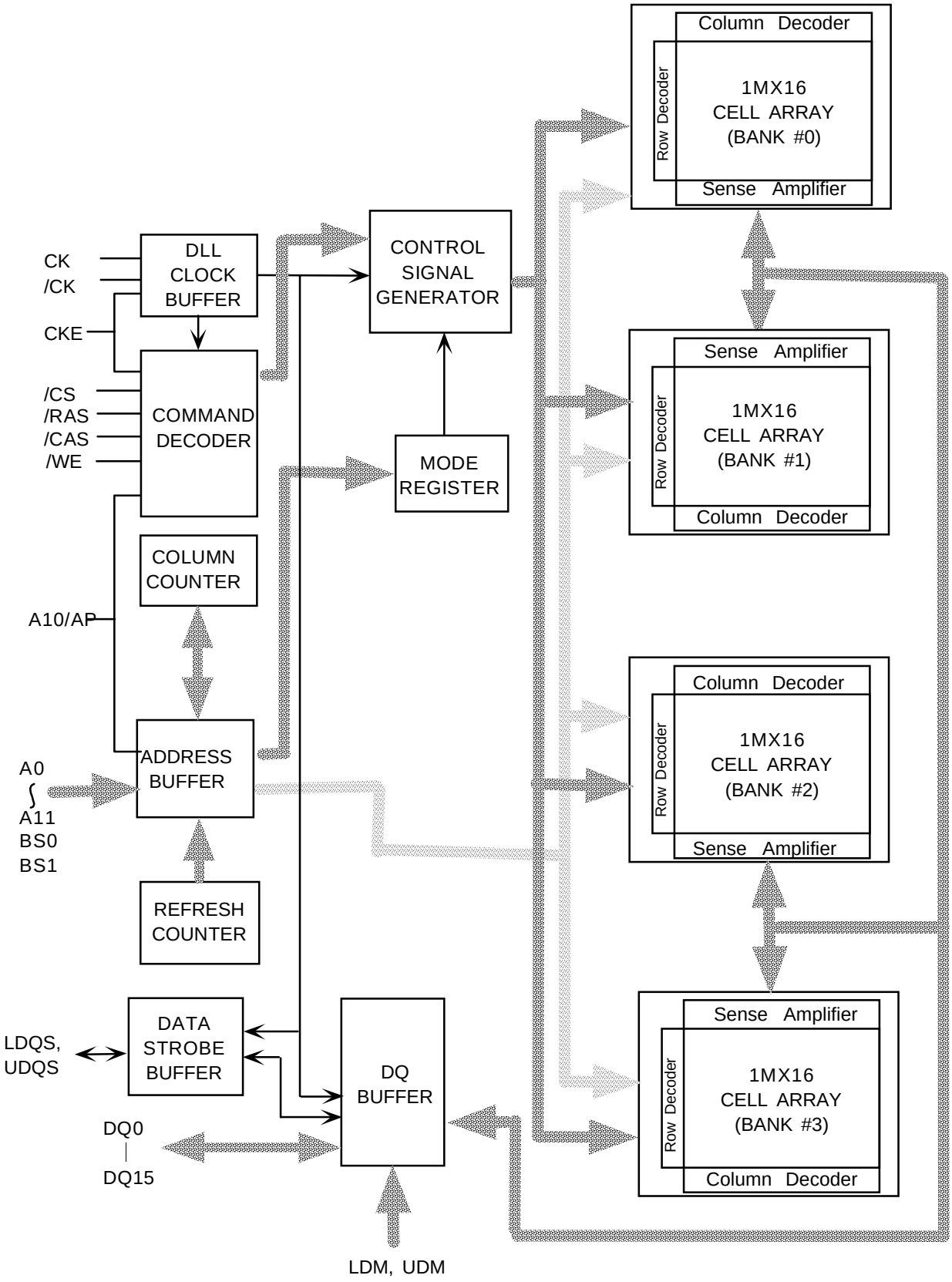
Block Diagram



Pin Descriptions

Table 1. Pin Details of EM658160

Symbol	Type	Description
CK, /CK	Input	**Differential Clock:** CK, /CK are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. Both CK and /CK increment the internal burst counter and controls the output registers.
CKE	Input	**Clock Enable:** CKE activates(HIGH) and deactivates(LOW) the CK signal. If CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BS0, BS1	Input	**Bank Select:** BS0 and BS1 defines to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
A0-A11	Input	**Address Inputs:** A0-A11 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7with A10 defining Auto Precharge).
/CS	Input	**Chip Select:** /CS enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when /CS is sampled HIGH. /CS provides for external bank selection on systems with multiple banks. It is considered part of the command code.
/RAS	Input	**Row Address Strobe:** The /RAS signal defines the operation commands in conjunction with the /CAS and /WE signals and is latched at the positive edges of CK. When /RAS and /CS are asserted "LOW" and /CAS is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the /WE signal. When the /WE is asserted "HIGH," the BankActivate command is selected and the bank designated by BS is turned on to the active state. When the /WE is asserted "LOW," the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.
/CAS	Input	**Column Address Strobe:** The /CAS signal defines the operation commands in conjunction with the /RAS and /WE signals and is latched at the positive edges of CK. When /RAS is held "HIGH" and /CS is asserted "LOW," the column access is started by asserting /CAS "LOW." Then, the Read or Write command is selected by asserting /WE "HIGH " or LOW"."
/WE	Input	**Write Enable:** The /WE signal defines the operation commands in conjunction with the /RAS and /CAS signals and is latched at the positive edges of CK. The /WE input is used to select the BankActivate or Precharge command and Read or Write command.
LDQS, UDQS	Input / Output	**Bidirectional Data Strobe:** Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15.
LDM, UDM	Input	**Data Input Mask:** Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.
DQ0 - DQ15	Input / Output	**Data I/O:** The DQ0-DQ15 input and output data are synchronized with the positive edges of CK and /CK. The I/Os are byte-maskable during Writes.

V_{DD}	Supply	**Power Supply:** +3.3V ±0.3V
V_{SS}	Supply	**Ground**
V_{DDQ}	Supply	**DQ Power:** +2.5V ±0.2V. Provide isolated power to DQs for improved noise immunity.
V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
V_{REF}	Supply	**Reference Voltage for Inputs:** +0.5*V_{DDQ}
NC	-	**No Connect:** These pins should be left unconnected.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CK. Table 2 shows the truth table for the operation commands.

Table 2. Truth Table (Note (1), (2))

Command	State	CKE_{n-1}	CKE_n	DM	BS0,1	A10	A0-9,11	/CS	/RAS	/CAS	/WE
BankActivate	Idle(3)	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	X	V	H		L	H	L	L
Read	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	H
Read and Autoprecharge	Active(3)	H	X	X	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
Extended MRS	Idle	H	X	X	OP code			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Note: 1. V=Valid data, X=Don't Care, L=Low level, H=High level
2. CKE_n signal is input level when commands are provided.
CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BS signal.
4. Device state is 1, 2, 4, 8, and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
When this command is asserted in the burst cycle, device state is clock suspend mode.

Mode Register Set (MRS)

The mode register is divided into various fields depending on functionality.

- Burst Length Field (A2~A0)

  This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2, 4, 8.

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

- Addressing Mode Select Field (A3)

  The Addressing Mode can be one of two modes, both Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 2,4 and 8.

A3	Addressing Mode
0	Sequential
1	Interleave

--- Addressing Sequence of Sequential Mode

An internal column address is performed by increasing the address from the column address which is input to the device. The internal column address is varied by the Burst Length as shown in the following table.

Data n	0	1	2	3	4	5	6	7
Column Address	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7
Burst Length	2 words							
	4 words							
	8 words							
	Full Page (Even starting address)							

--- Addressing Sequence of Interleave Mode

A column access is started in the input column address and is performed by inverting the address bits in the sequence shown in the following table.

Data n	Column Address								Burst Length	
Data 0	A7	A6	A5	A4	A3	A2	A1	A0		
Data 1	A7	A6	A5	A4	A3	A2	A1	A0#	4 words	
Data 2	A7	A6	A5	A4	A3	A2	A1#	A0		
Data 3	A7	A6	A5	A4	A3	A2	A1#	A0#		8 words
Data 4	A7	A6	A5	A4	A3	A2#	A1	A0		
Data 5	A7	A6	A5	A4	A3	A2#	A1	A0#		
Data 6	A7	A6	A5	A4	A3	A2#	A1#	A0		
Data 7	A7	A6	A5	A4	A3	A2#	A1#	A0#		

- CAS Latency Field (A6~A4)

  This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field.

  $t_{CAC}(min) \leq$ CAS Latency X t_{CK}

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	0	1	Reserved
1	1	0	2.5 clocks
1	1	1	Reserved (3.5 clocks)

- Test Mode field (A8~A7)

  These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

A8	A7	Test Mode
0	0	Normal mode
1	0	DLL Reset
X	1	Test mode

- (BS0, BS1)

BS1	BS0	An ~ A0
RFU	0	MRS Cycle
RFU	1	Extended Functions (EMRS)

Extended Mode Register Set (EMRS)

BS1	BS0	A11~ A1	A0	
RFU	1	RFU	0	DLL Enable
RFU	1	RFU	1	DLL Disable

Absolute Maximum Rating

Symbol	Item	Rating	Unit	Note
V_{IN}, V_{OUT}	Input, Output Voltage	- 0.3~ V_{DD} + 0.3	V	1
V_{DD}, V_{DDQ}	Power Supply Voltage	- 0.3~3.6	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	- 55~150	°C	1
T_{SOLDER}	Soldering Temperature (10s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

Recommended D.C. Operating Conditions (Ta = 0 ~ 70 °C)

Parameter	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	3.0	3.6	V	
Power Supply Voltage (for I/O Buffer)	V_{DDQ}	2.3	2.7	V	
Input Reference Voltage	V_{REF}	1.15	1.35	V	
Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	
Input High Voltage (DC)	V_{IH} (DC)	V_{REF} + 0.18	V_{DDQ} + 0.3	V	
Input Low Voltage (DC)	V_{IL} (DC)	-0.3	V_{REF} – 0.18	V	
Input Voltage Level, CLK and CLK# inputs	V_{IN} (DC)	-0.3	V_{DDQ} + 0.3	V	
Input Different Voltage, CLK and CLK# inputs	V_{ID} (DC)	-0.36	V_{DDQ} + 0.6	V	
Input leakage current	I_I	-5	5	μA	
Output leakage current	I_{OZ}	-5	5	μA	
Output High Voltage	V_{OH}	V_{TT} + 0.76	-	V	I_{OH} = -15.2 mA
Output Low Voltage	V_{OL}		V_{TT} – 0.76	V	I_{OL} = +15.2 mA

Capacitance (V_{DD} = 3.3V, f = 1MHz, Ta = 25 °C)

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance (except for CK pin)	2.5	5	pF
	Input Capacitance (CK pin)	2.5	4	pF
$C_{I/O}$	DQ, DQS, DM Capacitance	4	6.5	pF

Note: These parameters are periodically sampled and are not 100% tested.

Recommended D.C. Operating Conditions (V_{DD} = 3.3V ± 0.3, Ta = 0~70 °C)

Parameter	Symbol		Max. - 3.3/3.5/4/5/6/7/8	UNIT
Operation Current (one bank active)	I_{DD0}	t_{RC} = min, t_{CK} = min Active-precharge	250/240/230/220/190/180/160	mA
Operation Current (one bank active)	I_{DD1}	Burst = 2, t_{RC} = min, CL = 3 I_{OUT} = 0mA, Active-Read-Precharge	320/300/260/250/220/210/200	
Precharge Power-down Standby Current	I_{DD2P}	CKE ≤ V_{IL}(max), t_{CK} = min, All banks idle	80/80/80/65/65/60/55	
Idel Standby Current	I_{DD2N}	CKE ≥ V_{IH}(min), CS# ≥ V_{IH}(min), t_{CK} = min	170/160/150/130/110/100/90	
Active Power-down Standby Current	I_{DD3P}	All banks ACT, CKE ≤ V_{IL}(max), t_{CK} = min	80/80/80/65/65/60/55	
Active Standby Current	I_{DD3N}	One bank; Active-Precharge, t_{RC} = t_{RAS}(max), t_{CK} = min	180/170/160/155/145/140/135	
Operation Current (Read)	I_{DD4R}	Burst = 2, CL = 3, t_{CK} = min, I_{OUT} = 0mA	330/310/270/250/220/200/180	
Operation Current (Write)	I_{DD4W}	Burst = 2, CL = 3, t_{CK} = min	330/310/270/250/220/200/180	
Auto Refresh Current	I_{DD5}	t_{RC}(min)	190/180/170/155/145/140/135	
Self Refresh Current	I_{DD6}	CKE ≤ 0.2v	2	

Electrical Characteristics and Recommended A.C. Operating Conditions

(V_{DD} = 3.3 ± 0.3 V, Ta = 0~70 °C)

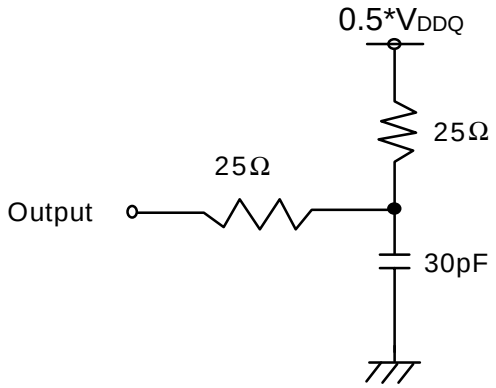
Symbol	Parameter		- 3.3/3.5/4/5/6/7/8		Unit
			Min.	Max.	
t_{RC}	Row cycle time		44/44/44/55/60/70/80		ns
t_{RFC}	Refresh row cycle time		56/56/56/70/84/91/96		ns
t_{RAS}	Row active time		32/32/32/40/42/49/56	120000	ns
t_{RCD}	/RAS to /CAS Delay		12/12/12/15/18/21/24		ns
t_{RP}	Row precharge time		12/12/12/15/18/21/24		ns
t_{RRD}	Row active to Row active delay		6.6/7/8/10/12/14/16		ns
t_{WR}	Write recovery time		2		t_{CK}
t_{CDLR}	Last data in to Read command		$2.5t_{CK}$-t_{DQSS}		t_{CK}
t_{CCD}	Col. Address to Col. Address delay		1		t_{CK}
t_{CK}	Clock cycle time	CL*=3	3.3/3.5/4/5/6/7/8	15	ns
		CL*=2.5	5/5/5.5/6/7.5/8/9	15	
		CL*=2	6/6/7/8/9/10/11	15	
t_{CH}	Clock high level width		0.45	0.55	t_{CK}
t_{CL}	Clock low level width		0.45	0.55	t_{CK}
t_{DQSCK}	DQS-out access time from CK,/CK		-0.6/-0.6/-0.6/-0.7/-0.7/-0.75/-0.8	0.6/0.6/0.6/0.7/0.7/0.75/0.8	ns
t_{AC}	Output access time from CK,/CK		-0.6/-0.6/-0.6/-0.7/-0.7/-0.75/-0.8	0.6/0.6/0.6/0.7/0.7/0.75/0.8	ns
t_{DQSQ}	DQS-DQ Skew		-0.5/-0.5/-0.5/-0.5/-0.5/-0.5/-0.6	0.5/0.5/0.5/0.5/0.5/0.5/0.6	ns
t_{RPRE}	Read preamble		0.9	1.1	t_{CK}
t_{RPST}	Read postamble		0.4	0.6	t_{CK}
t_{DQSS}	CK to valid DQS-in		0.75	1.25	t_{CK}
t_{WPRES}	DQS-in setup time		0.4/0.4/0.4/0.4/0.45/0.5/0.55		ns
t_{WPREH}	DQS-in hold time		0.4/0.4/0.4/0.4/0.45/0.5/0.55		ns
t_{WPST}	DQS write postamble		0.4	0.6	t_{CK}
t_{DQSH}	DQS in high level pulse width		0.4	0.6	t_{CK}
t_{DQSL}	DQS in low level pulse width		0.4	0.6	t_{CK}
t_{IS}	Address and Control input setup time		1.1		ns
t_{IH}	Address and Control input hold time		1.1		ns
t_{MRD}	Mode register set cycle time		1		t_{CK}
t_{DS}	DQ & DM setup time to DQS		0.4/0.4/0.4/0.4/0.45/0.5/0.55		ns
t_{DH}	DQ & DM hold time to DQS		0.4/0.4/0.4/0.4/0.45/0.5/0.55		ns
t_{QH}	Output DQS valid window		0.3		t_{CK}
t_{PDEX}	Power down exit time		t_{IS}+1t_{CK}	t_{IS}+2t_{CK}	ns
t_{XSA}	Self refresh exit to active command delay		12/12/11/11/10/10/10		t_{CK}
t_{XSR}	Self refresh exit to read command delay		200		t_{CK}

Note:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
4. Power-up sequence is described in Note 6.
5. A.C. Test Conditions

SSTL_2 Interface

Reference Level of Output Signals (V_{RFE})	0.5 * V_{DDQ}
Output Load	Reference to the Under Output Load (A)
Input Signal Levels	V_{REF}+0.35 V / V_{REF}-0.35 V
Input Signals Slew Rate	1 V/ns
Reference Level of Input Signals	0.5 * V_{DDQ}



SSTL_2 A.C. Test Load

6. **Power up Sequence**

   Power up must be performed in the following sequence.

   1) Power must be applied to V_{DD} and V_{DDQ}(simultaneously) when all input signals are held "NOP" state and maintain CKE “LOW”. Power applied to V_{DDQ} the same time as V_{TT} and V_{REF}.
   2) After power-up, No-Operation of 200 μ–seconds minimum is required.
   3) Start clock and keep CKE “HIGH” to maintain either No-Operation or Device Deselect at the input.
   4) Issue EMRS – enable DLL.
   5) Issue MRS – reset DLL and set device to idle with bit A8 (An additional 200 cycles min of clock are needed for DLL lock)
   6) Precharge all banks of the device.
   7) Two or more Auto Refresh commands.
   8) Issue MRS – Initialize device operation.

Timing Waveforms

Figure 1. AC Parameters for Read Timing (Burst Length=4, CAS Latency=2.5)

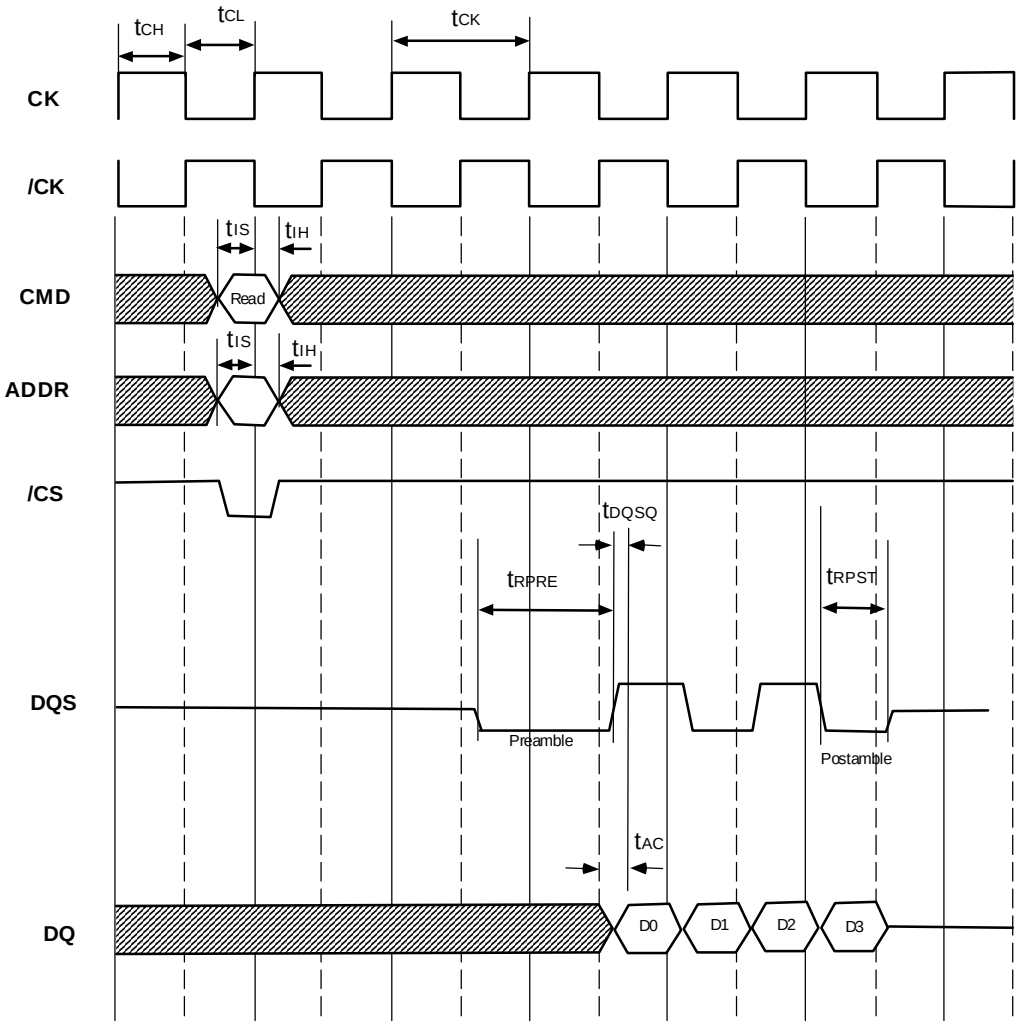


Figure 2. AC Parameters for Write Timing (Burst Length=4)

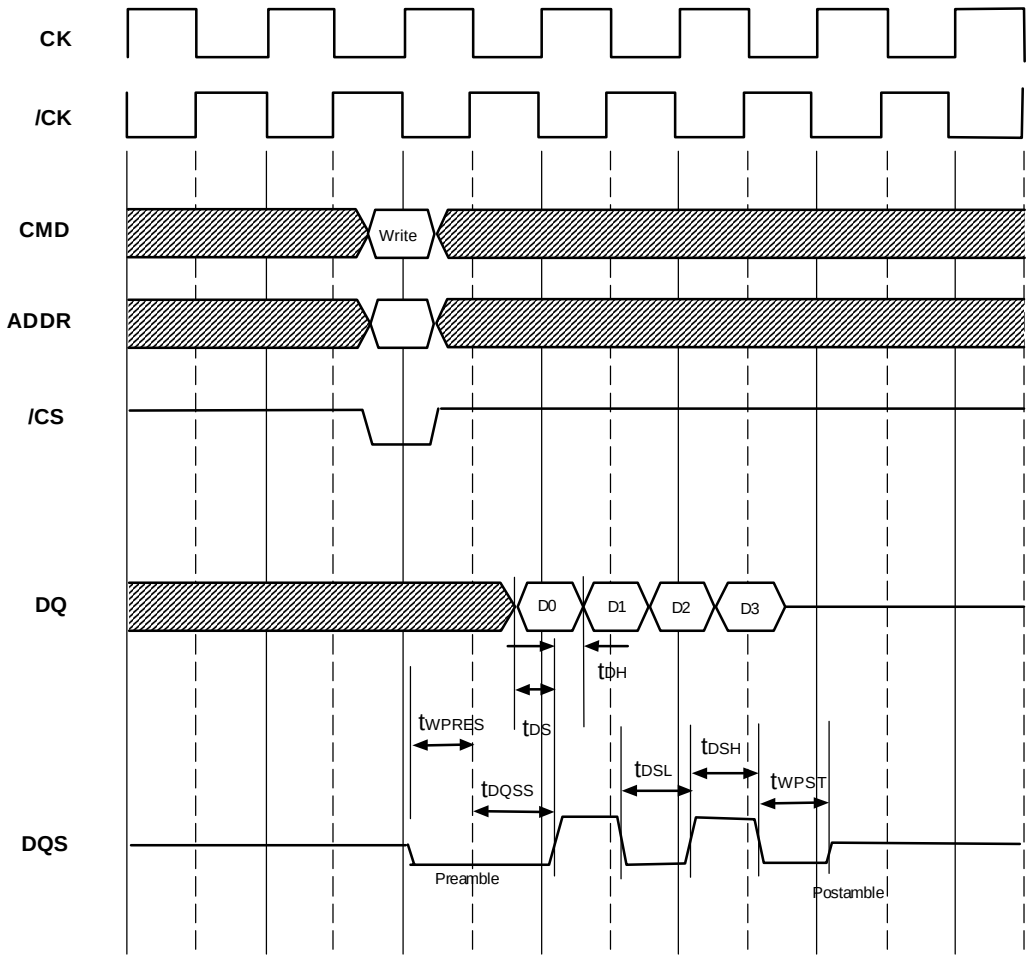


Figure 3. Read Command to Output Data Latency (Burst Length=2)

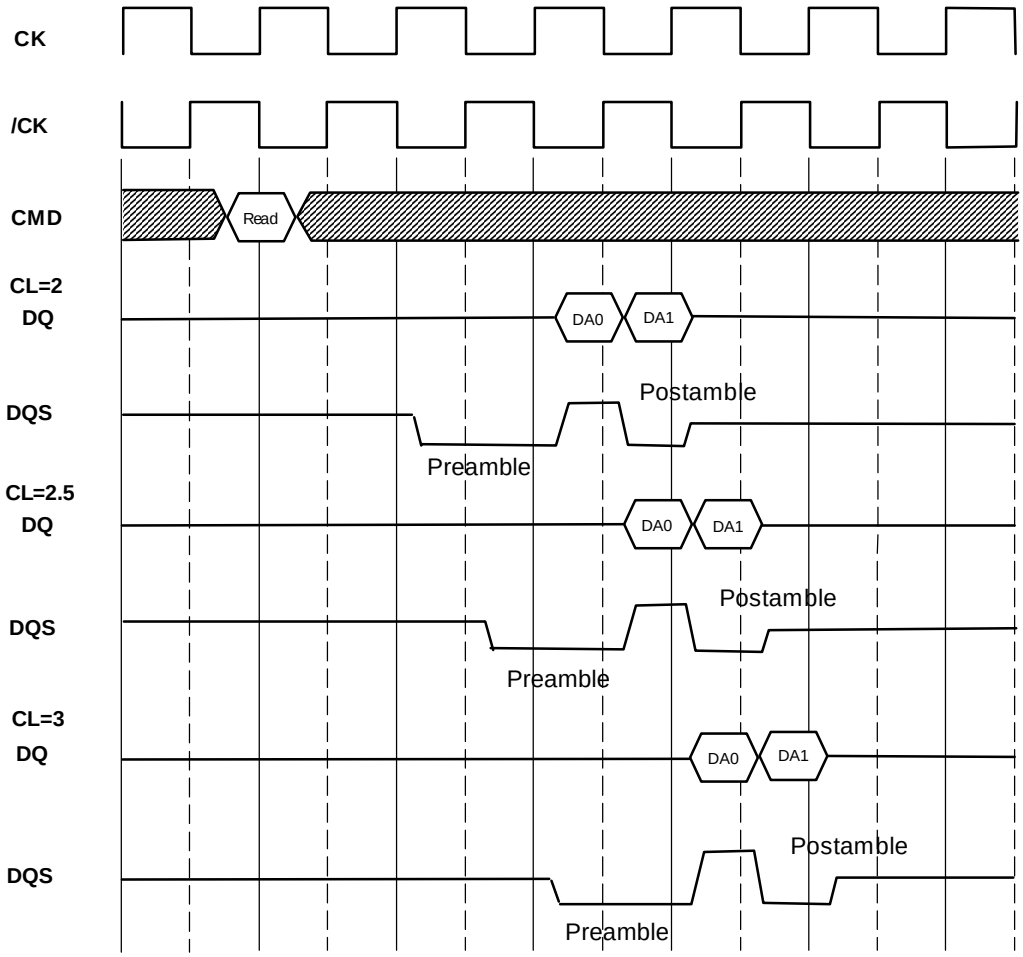


Figure 4. Read Followed by Write (Burst Lenth=4, CAS Latency=3)

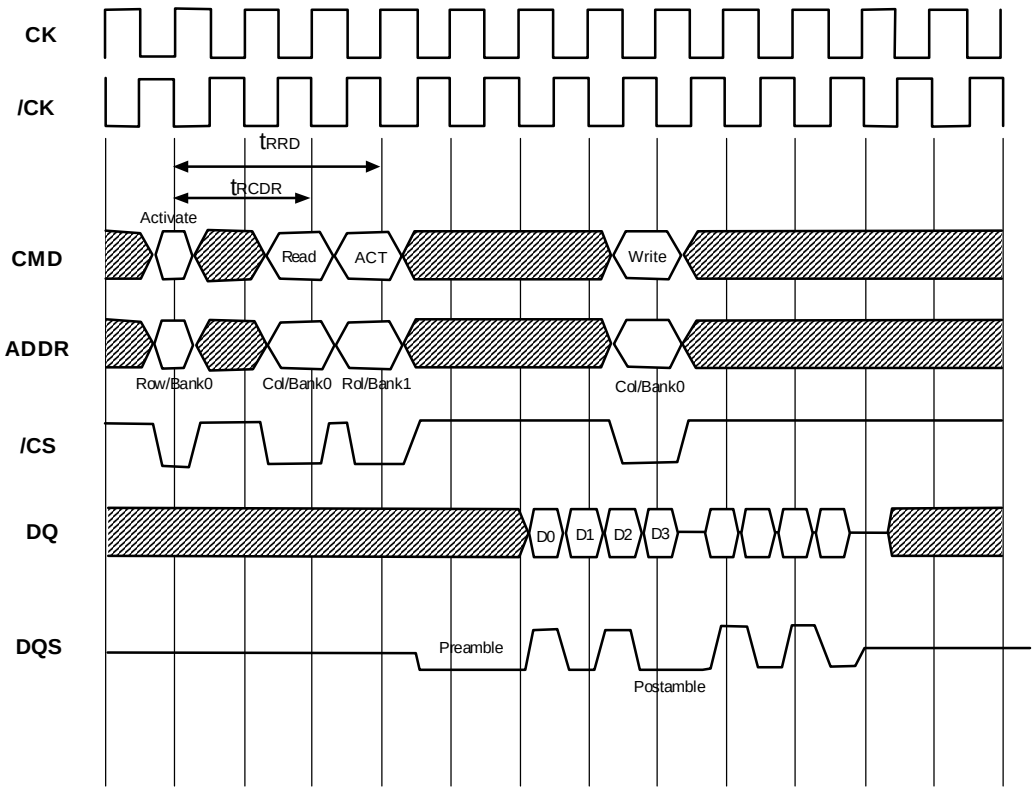


Figure 5. Write followed by Read (Burst Lenth=4, CAS Latency=3)

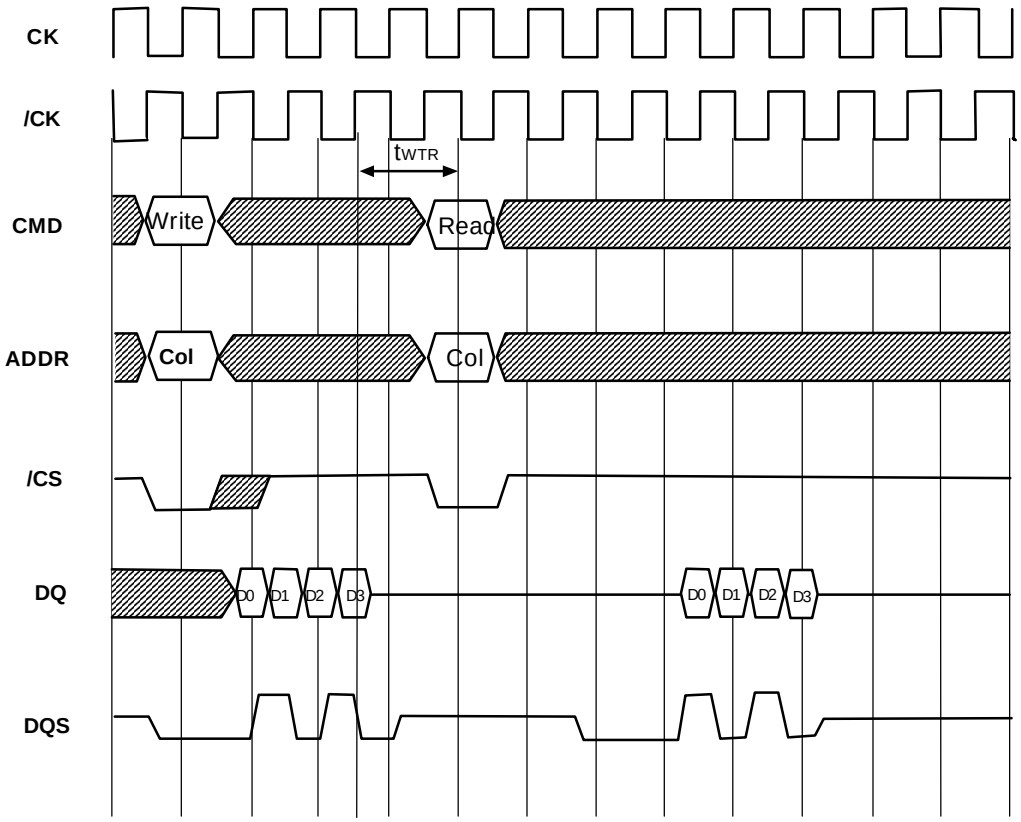


Figure 6. Precharge Termination of a Burst Read (Burst Length=4, CAS Latency=3)

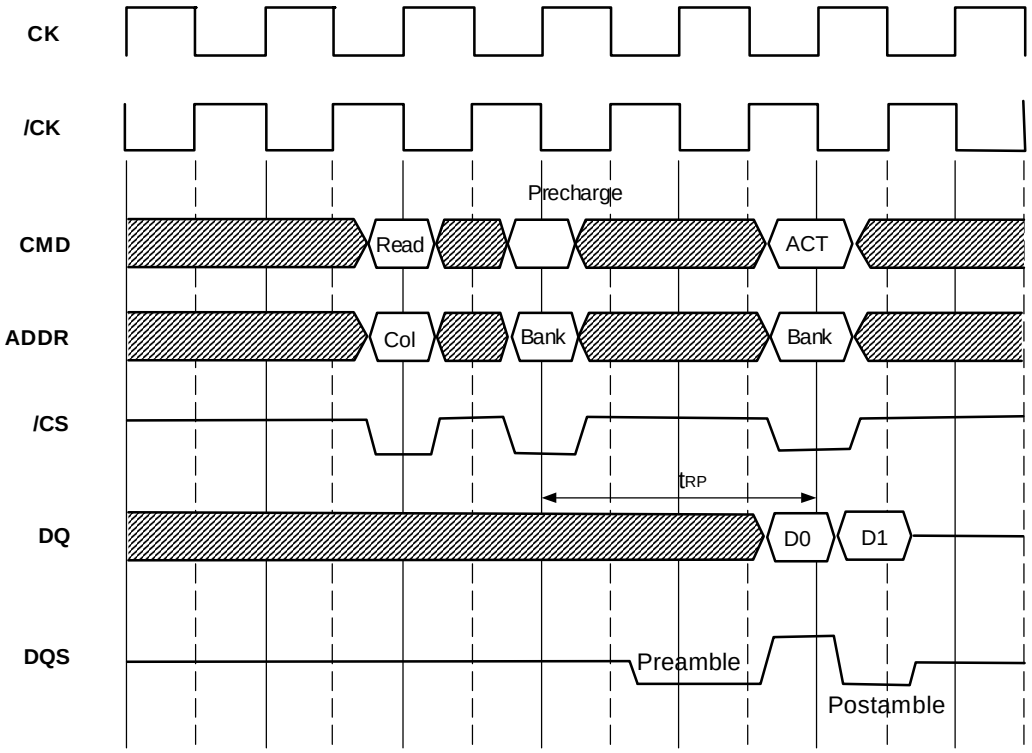


Figure 7. Precharge Termination of a Burst Write (Burst Length=4)

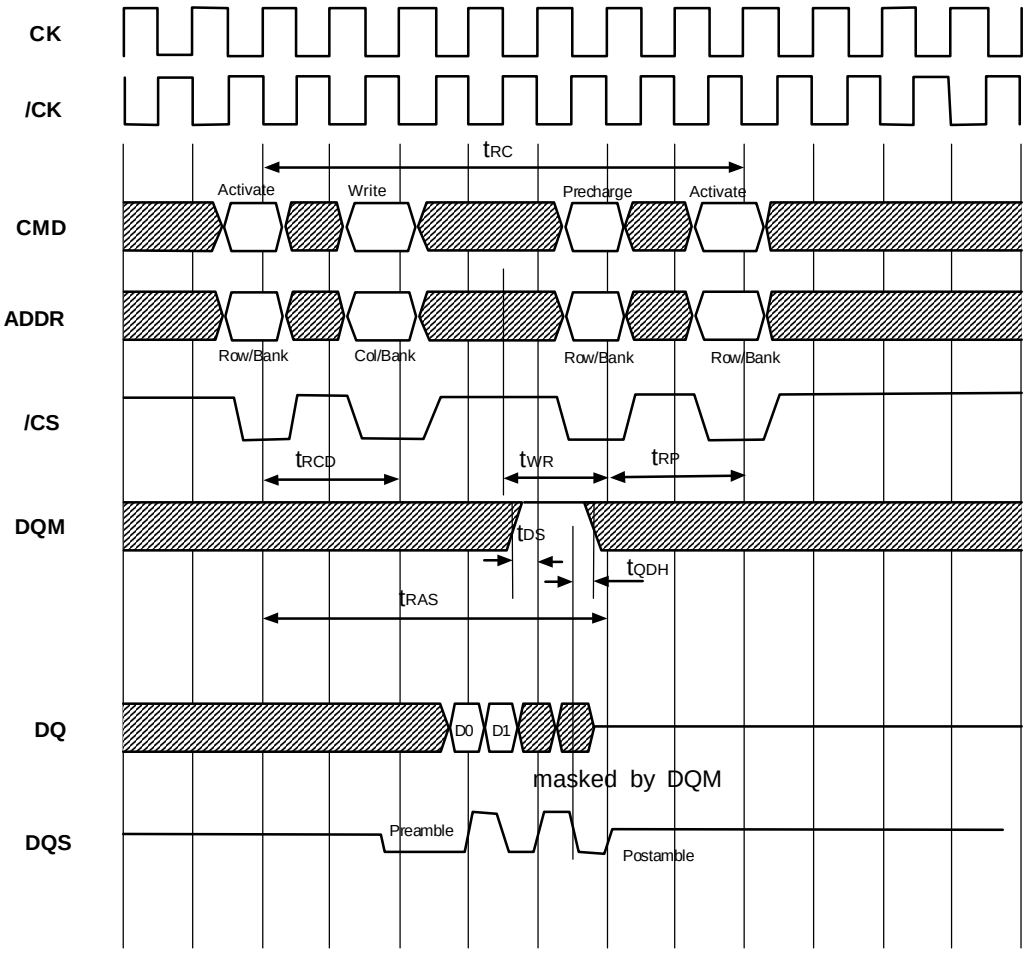


Figure 8. Auto Precharge after Read Burst (CAS Latency=3)

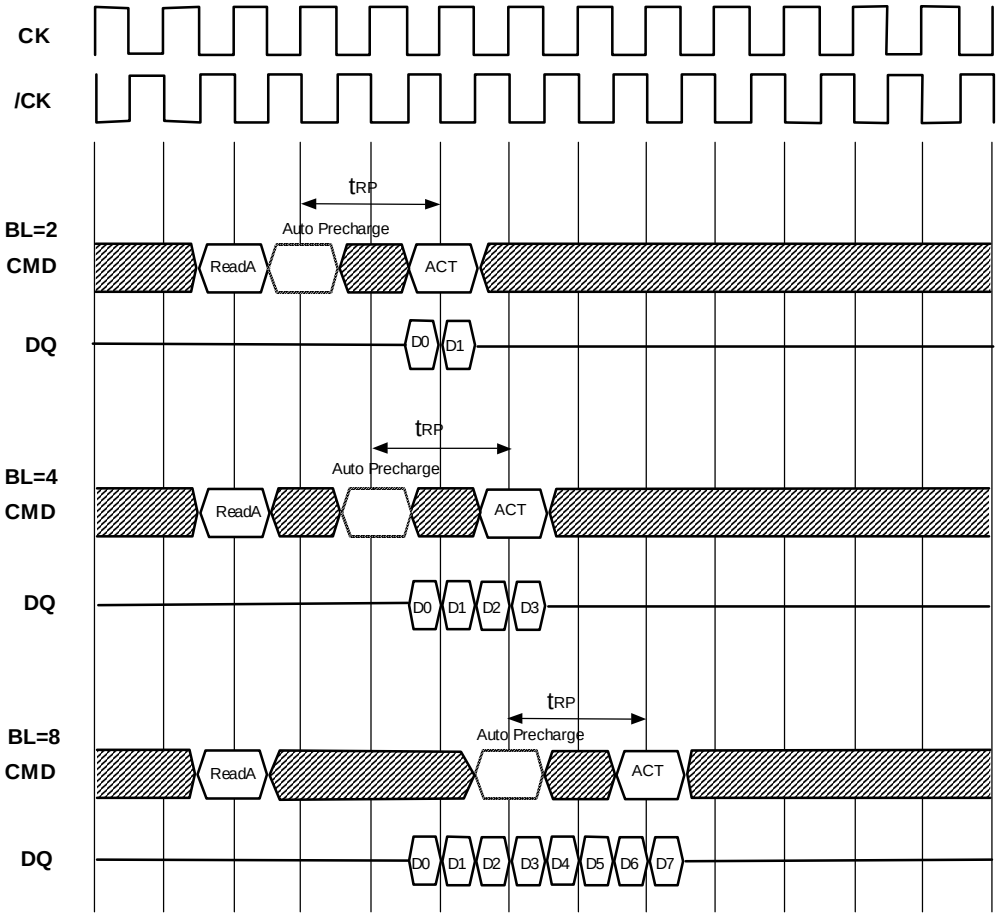


Figure 9. Auto Precharge after Write Burst

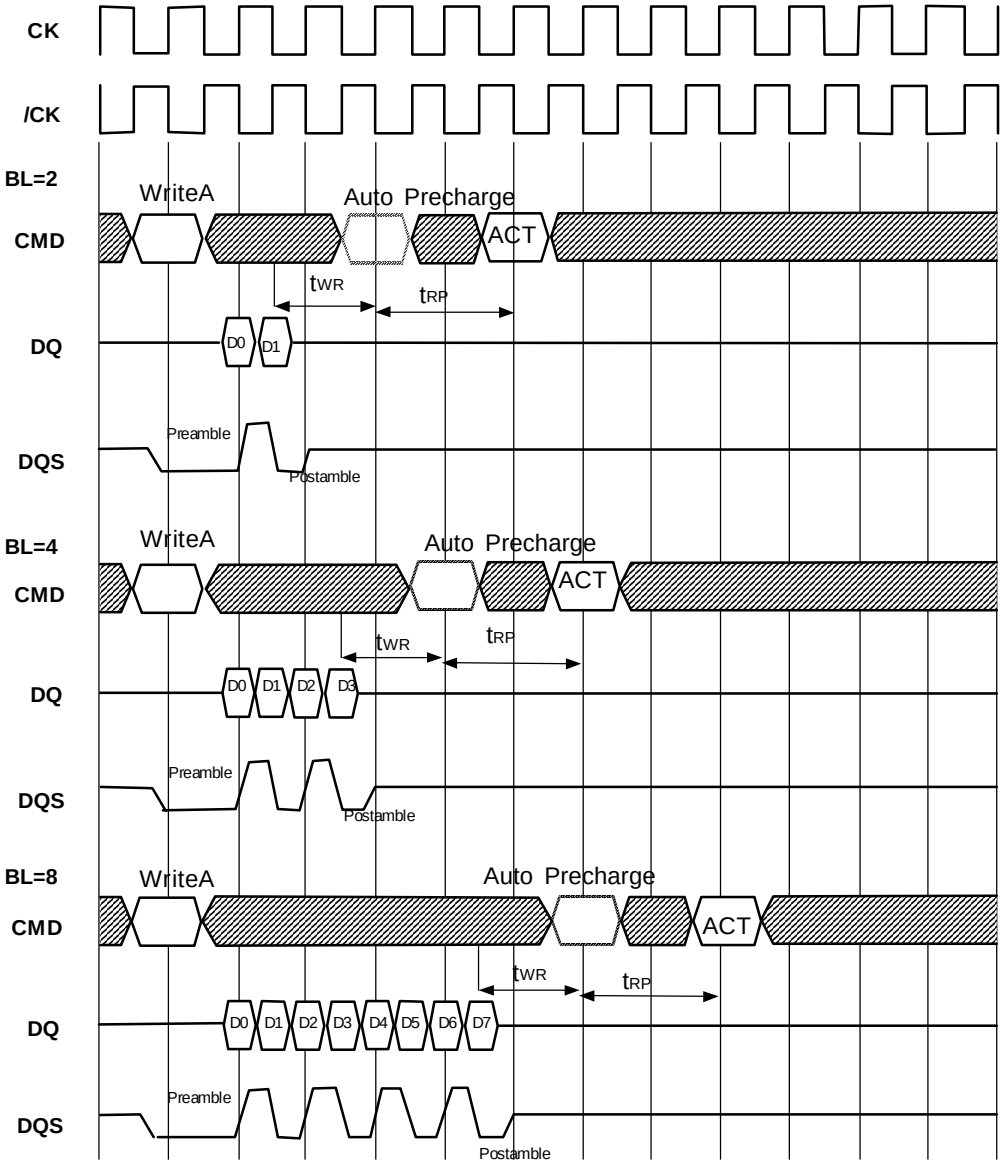


Figure 10. Read Terminated By Burst Stop (Burst Length=8)

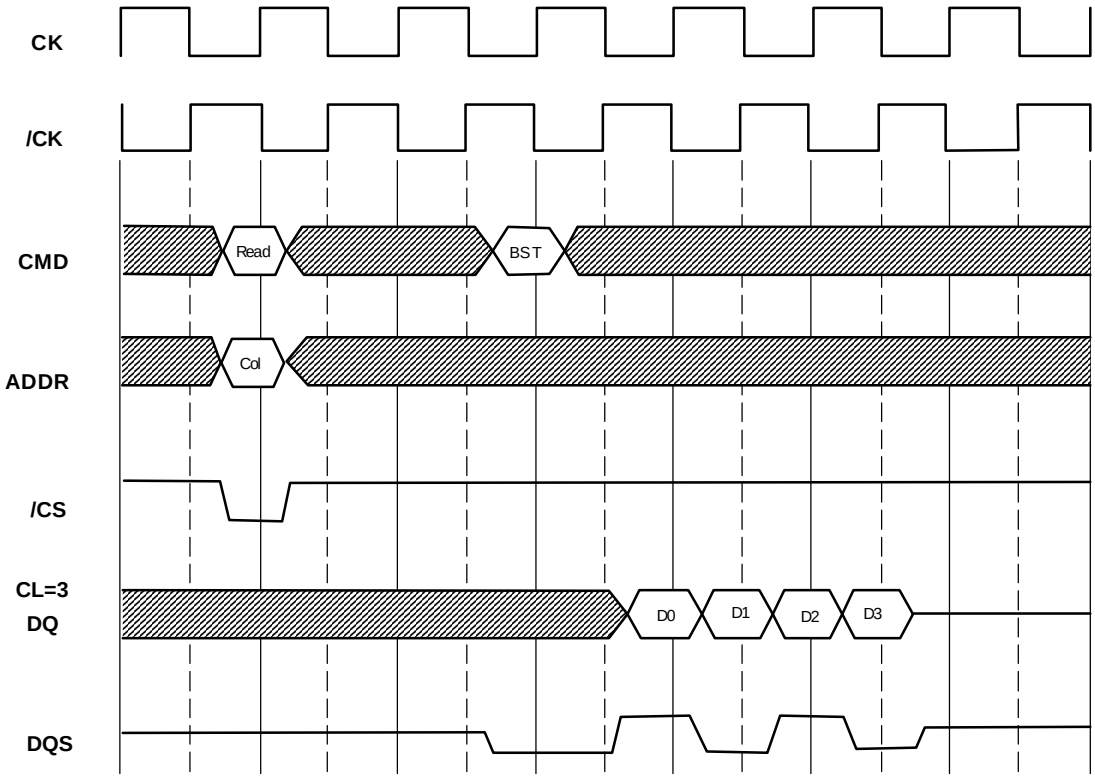


Figure 11. Read Terminated by Read (Burst Length=4, CAS Latency=3)

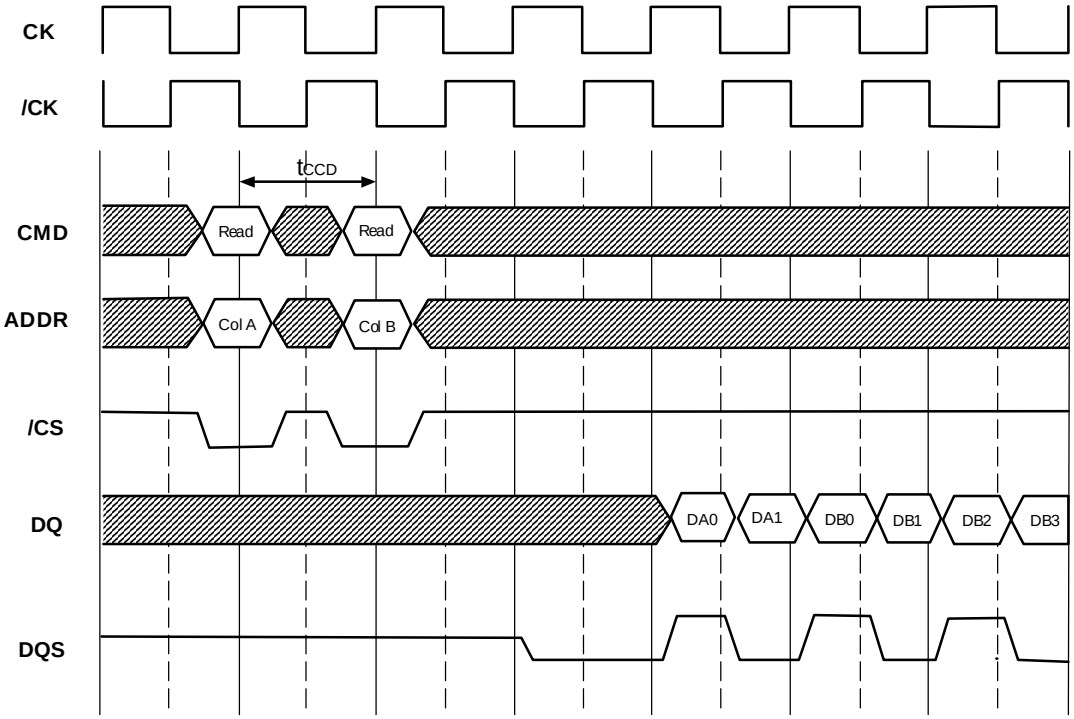


Figure 12. Mode Register Set Command

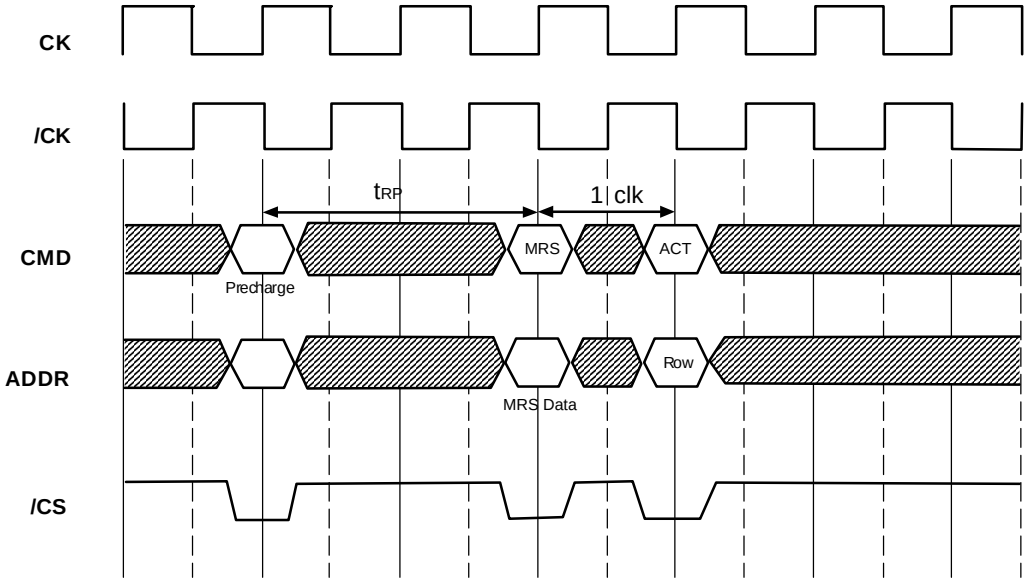
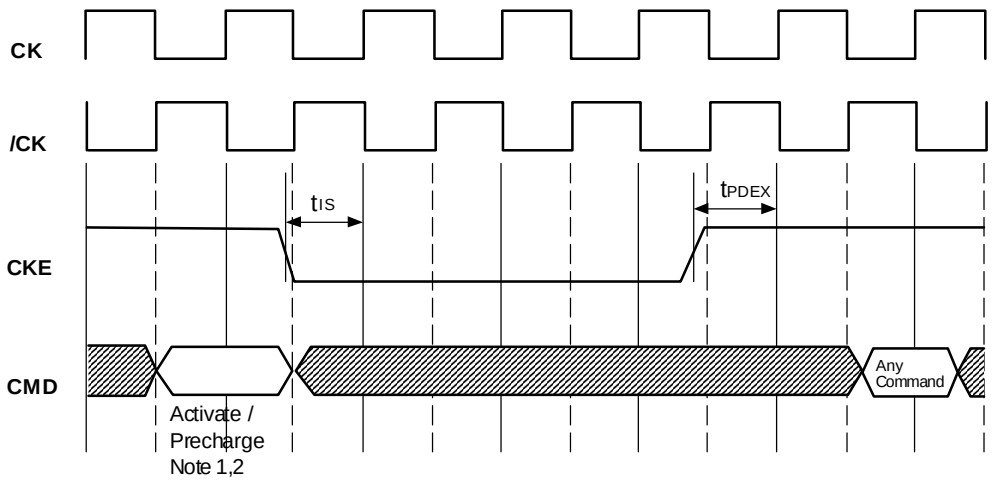


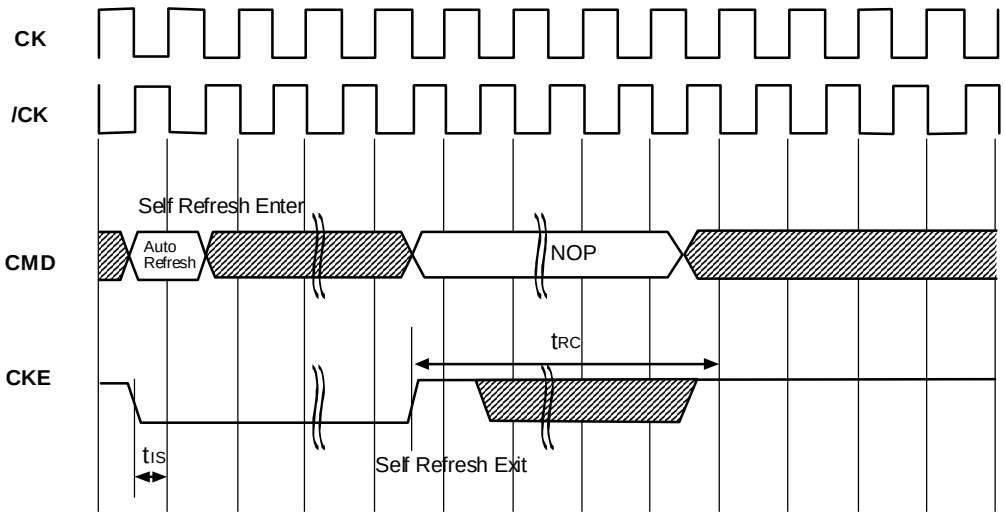
Figure 13. Active / Precharge Power Down Mode



Note: 1. All banks should be in idle state prior to entering precharge power down mode.

2. One of the banks should be in active state prior to entering active power down mode.

Figure 14. Self Refresh Entry and Exit Cycle



t_{RC} is required before any command can be applied, and 200 cycles of clk are required before a READ command can be applied.

66 Pin TSOP II Package Outline Drawing Information
Units: mm