DL5000™ Family

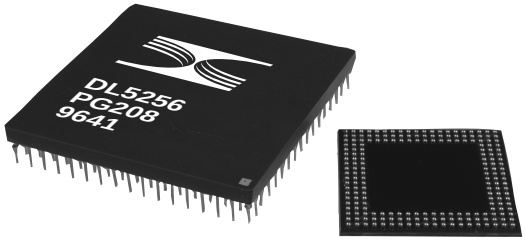
Fast Field Programmable Gate Array

Features

- Fast Field Programmable Gate Arrays™
- Patented Active Repeater™ Architecture
- Data and Clock Rates up to 270 MHz
- Complex operations up to 200 MHz
- Input Block Register Setup Time 800 ps
- Output Block Register Clock-to-out 1.6 ns
- ECL, PECL and GTL Interface Levels
- 100K and 100KH Compatible
- Differential Outputs
- 1,000 to 10,000 Gates
- 6 Low-skew Clock Trees
- Highly Predictable, Fanout Independent Routing Delays
- SRAM-based Programming
- JTAG Boundary Scan
- Fully Automatic Implementation Using DynaTool™

Applications Examples

- **Telecommunications and Datacommunications**
  Sonet and ATM Interfaces
  Satellite Communications
  FDDI
- **Test and Instrumentation**
  VLSI and Memory Testers
  Oscilloscopes and Logic Analyzers
- **High-Speed Graphics**
  Real-Time Video Imaging
  HDTV
- **Servers and Peripherals**
  High-speed Servers
  High-speed Bus Interfaces
  Fast Graphics Interfaces
- **Emulation**



Introduction

The DL5000 is the industry's first Fast Field Programmable Gate Array (FFPGA™) family. Utilizing a breakthrough in field programmable interconnect techniques called *Active Repeaters*, this family provides unprecedented system level performance.

High operating frequencies combined with fast ECL, GTL and PECL input and output structures make these devices ideal for high-speed interfaces, subsystems and core logic.

DL5000 family devices are ideal for applications where other FPGAs can not meet performance requirements. They are also ideal for applications where designers want to integrate many discrete ECL devices.

Benefits to the user include ultra high-speed, fast time-to-market, reduced risk and maximum design flexibility.

The DL5000 features SRAM-based programming allowing the devices to be configured in-circuit and reprogrammed on-the-fly. They can be reconfigured an unlimited number of times providing maximum flexibility for design iterations and field upgrades.

Device	Gates	Logic Blocks	Input Blocks	Output Blocks	Flip Flops	Clock Trees
DL5064	1,250	64	48	49	212	6
DL5256	5,000	256	76	76	664	6
DL5528	10,000	528	104	112	1,272	6

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Performance Examples

The DL5000 family with DynaChip's patented Active Repeater Architecture supports data and clock rates up to 270 MHz and performs complex operations up to 200 MHz. The following table shows the performance of functions implemented in the DL5256 device.

Function	DL5256 - G	Logic Block Count
2-bit Shift Register	251 MHz	2
16-bit Synchronous Serial In Shift Register	251 MHz	16
16-bit Loadable Shift Register		
Shift	251 MHz	16
Load	213 MHz	16
2 to 1 Mux		
Data	251 MHz	1
Select	213 MHz	1
4 to 1 Mux		
Data	232 MHz	1
Select	201 MHz	1
Complex Operations to 200 MHz		
8-bit Fully Synchronous, Loadable Counter	200 MHz	9
32-bit Fully Synchronous, Loadable Counter	140 MHz	42
64-bit Fully Synchronous, Loadable Counter	120 MHz	86
16 to 1 Mux		
Data	116 MHz	5
Select	100 MHz	5
Pipelined Operations		
4 x 4 Pipelined Multiplier	170 MHz	49
24-bit Pipelined Adder Accumulator	182 MHz	24

Table 1: Performance of Various Applications*

*Worst case performance over commercial temperature and voltage range.

High Performance Active Repeater Technology

The enabling technology behind DynaChip's Fast Field Programmable Gate Arrays is the Active Repeater.

As shown in figure 1, conventional FPGA devices use pass gates to create programmable interconnections. These pass gates act like a series of resistors with distributed capacitance to ground. Nets formed out of these pass gates slow down dramatically as the number of programmable connections increases.

This results in long, unpredictable delays, especially for nets that have to travel a long distance or drive a large number of loads.

long distance or drive a large number of loads.

In contrast, DynaChip uses Active Repeaters to create programmable interconnections. These repeaters buffer the signal at every interconnection point and isolate the capacitance of the rest of the net.

The result is fast, predictable performance even for long, high fanout nets.

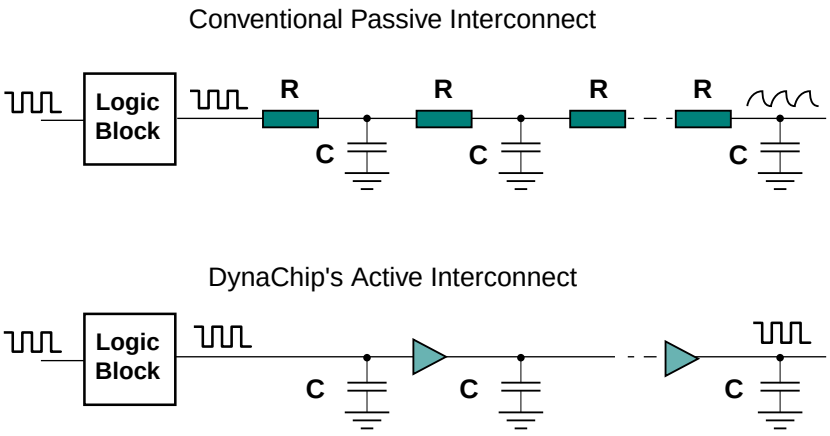


Figure 1: Active vs. Passive Interconnect

In FPGA devices that use pass-gate based interconnect, net delays increase quadratically with the number of programmable interconnect points, as shown in figure 2.

DynaChip devices use Active Repeater interconnect making net delays linear. The result is much higher performance and greater predictability.

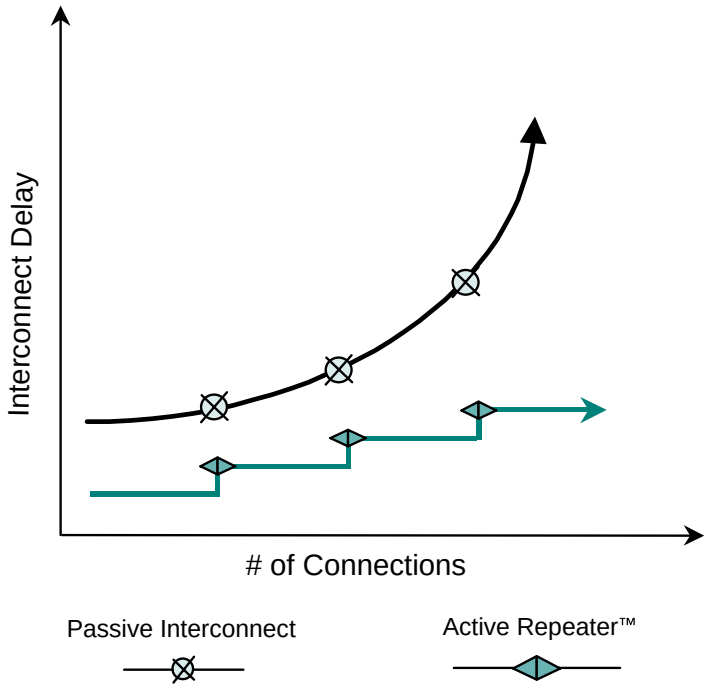


Figure 2: Active Repeater™ vs. Passive Interconnect

Active Repeater Architecture

At the very top level, DynaChip devices look a lot like conventional FPGA devices. As shown in figure 3, input/output blocks surround the edges of the device, an array of logic blocks fill the interior and routing tracks are distributed between the rows and columns of logic blocks.

The difference in DynaChip's architecture lies in the routing resources.

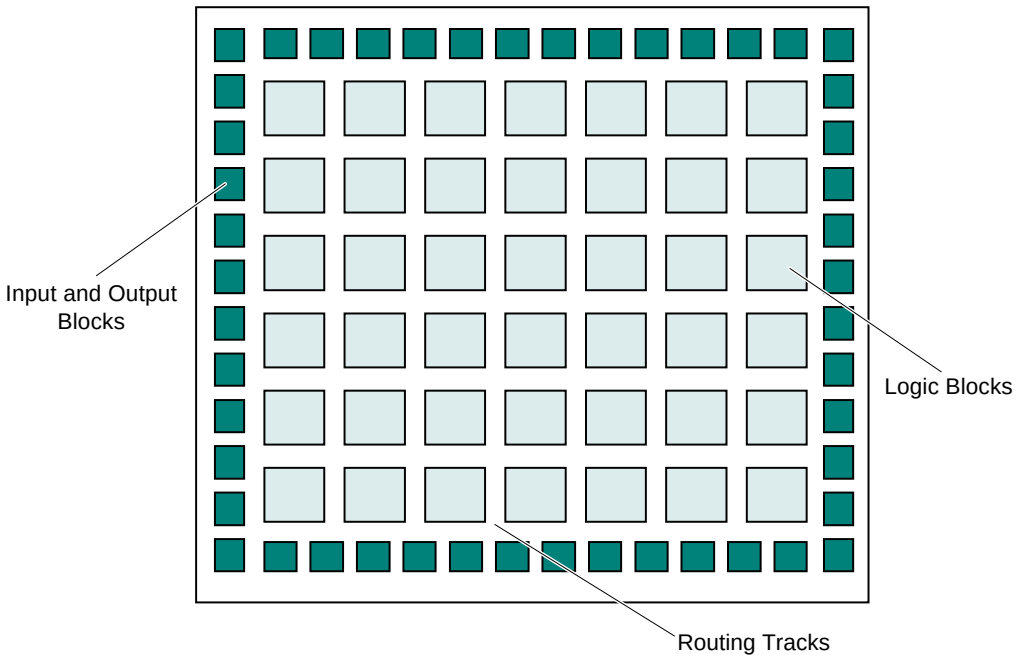


Figure 3: Device Architecture

DynaChip's architecture is optimized for Active Repeater technology.

As shown in figure 4, interconnect resources consist of a series of vertical and horizontal busses that make up a routing region. Buffers that drive these busses can be turned on and off to create the required connections. Since every buffer drives a fixed load, it has been carefully optimized to provide maximum performance. The fixed load nature of the interconnect also results in completely predictable performance since the delay through the buffer does not vary.

DynaChip's logic blocks are arranged in 5 column by 7 row areas called routing regions. Logic blocks within a routing region can be connected without using Active Repeaters. Since all the routing delays within a region are included in the logic block delay (see Table 10, Logic Block Switching Characteristics), performance with in a routing region is completely predictable.

The location of the Active Repeaters are staggered so that each logic block has its own 5 x 7 routing region. A single logic block typically implements about 20 gates of user logic. Therefore, a 5 x 7 routing region consisting of 35 blocks can implement about 700 gates of logic with no routing delays.

For larger functions, high-speed Active Repeaters are used to connect routing regions. With one Active Repeater delay (1 ns worst case delay for –G speed grade), the region can be extended to 100 blocks of logic or about 2,000 gates.

Logic block and Active Repeater delays are not affected by the number of loads on their output. This allows completely predictable, high-speed performance even for circuits with high fanout nets.

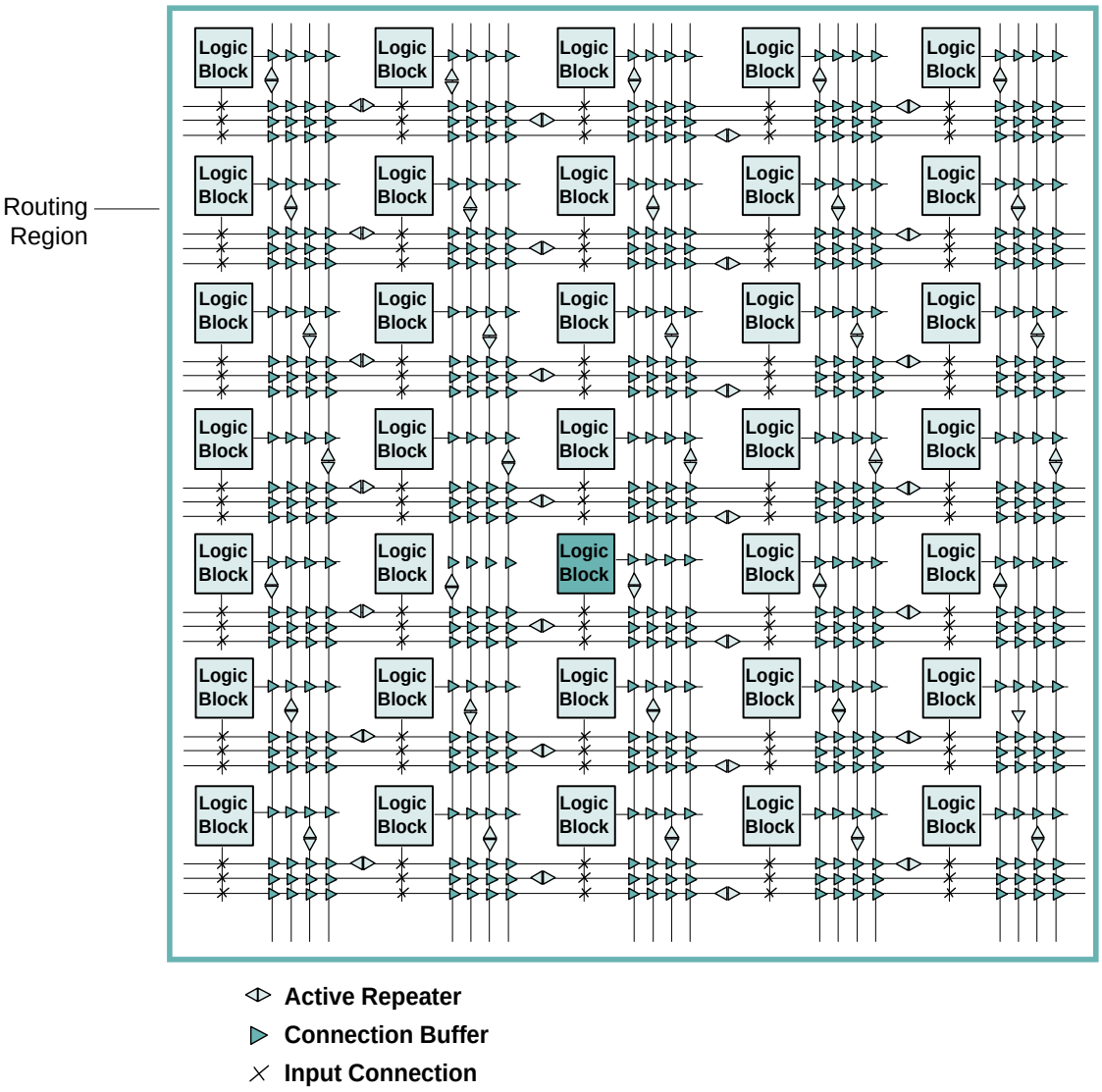


Figure 4: Interconnect Resources in a Routing Region

This architecture results in completely deterministic performance within a routing region. The logic block delays specified in this datasheet include the delay of the connection buffers and the routing (refer to table 10 for logic block delays).

As shown in figure 5, this architecture allows a logic block to drive all 35 blocks in the 5 column x 7 row routing region with no additional routing delays. As a result, even high fanout nets have extremely high performance.

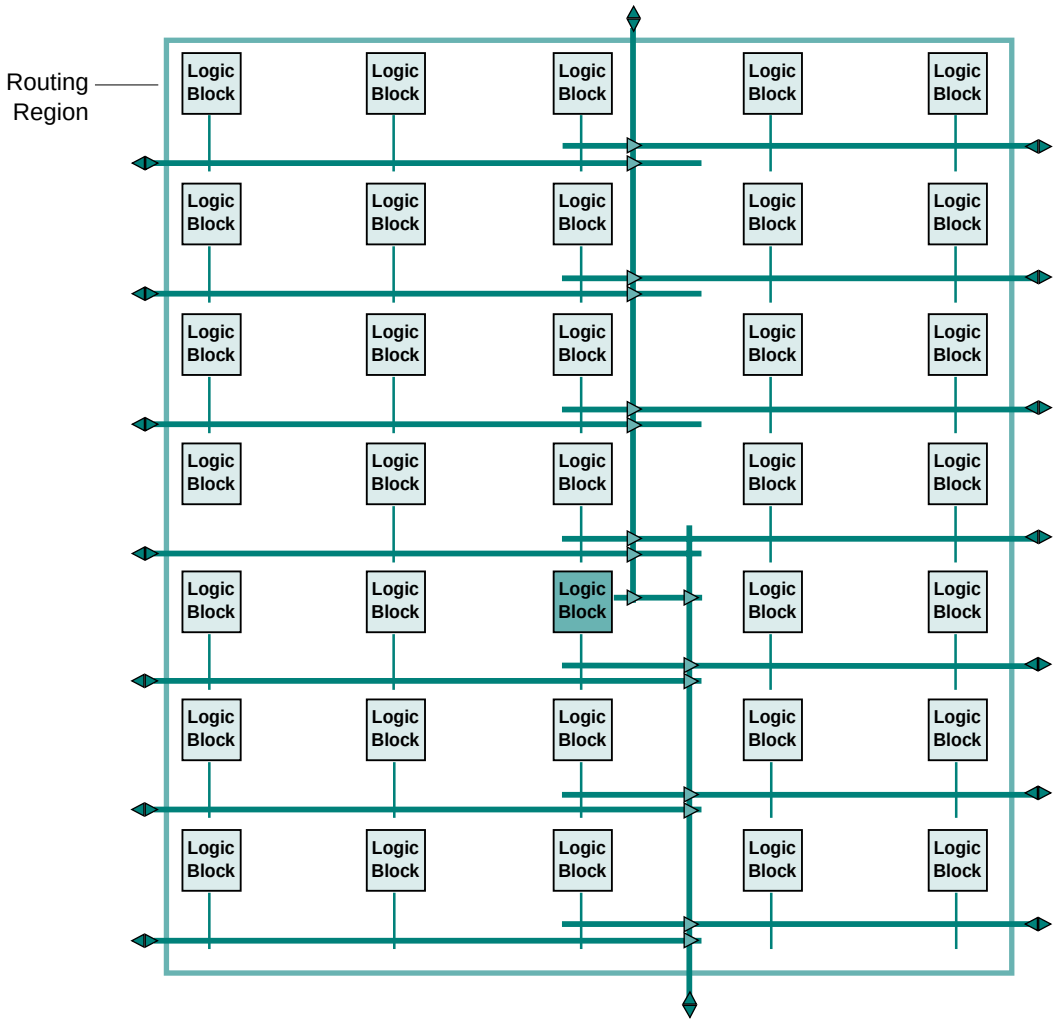


Figure 5: A logic block can drive all 35 blocks in a 5 x 7 routing region with no routing delays

For signals that drive blocks in the next region, the fixed delay through an Active Repeater is added to the logic block delay. These Active Repeater delays are the only routing delays in the device and their performance is completely specified in this datasheet (refer to table 11 for Active Repeater delays).

Input and Output Blocks

To accommodate the fast system clock and data rates associated with high-performance systems, input and output blocks provide ECL, PECL and GTL interface levels. Interface levels are set by applying the proper V_{CC} and V_{EE} as shown in table 5 - *Recommended Operating Conditions*.

Each input or output block can be configured as a direct or registered input or output. If configured as registered, the flip flop has an asynchronous reset and edge triggered clock input. The clock input has polarity control allowing the register to be triggered from either clock edge.

Clock signals for registered input and output blocks are sourced from 4 dedicated I/O clock pins or either of the 2 global clock pins.

Each input and output block contains dedicated JTAG Boundary Scan logic compatible with IEEE specifications.

Logic Block

The logic block in the DL5000 is extremely flexible and can implement a wide variety of functions. Each block has 18 inputs and 3 outputs. One of the inputs is dedicated for clocking and one is for a set or reset signal. The remaining 16 are general purpose inputs to the logic block.

Each logic block contains combinatorial logic and two flip flops. The combinatorial section contains flexible logic structures optimized for high utilization. Structures like multiplexers, AND/OR gates, comparators and arithmetic functions are automatically mapped to these resources by the DynaTool Development System.

The outputs of the combinatorial logic exit the block directly or serve as inputs to the two flip flops in the block.

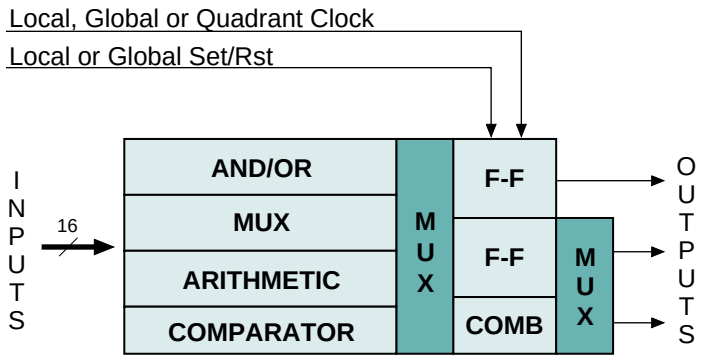


Figure 6: DL5000 Logic Block Overview

Clock Distribution

DL5000 family devices have 6 low-skew clock distribution networks that are driven by dedicated pins on the device. Two of these networks are global clocks that can drive every flip flop in the device. Four of these networks are quadrant clocks. The quadrant clocks can drive all the logic block flip flops in one quarter of the device.*

Flip flops in the input and output blocks can be driven by the two global clocks or by 4 additional I/O clock pins.

* There are no quadrant clocks in the DL5064 device.

Detailed Functional Description

Input and Output Blocks

Devices in the DL5000 family feature high-speed input and output blocks. These blocks are compatible with ECL, PECL and GTL interface levels.

To achieve ECL interface levels, power supply pins on the device are connected to 0 and -4.5 volts. To achieve PECL interface levels, power supply pins are connected to +5 volts and 0. To achieve GTL interface levels, power supply pins are connected to +2 and -3 volts.

Input Block

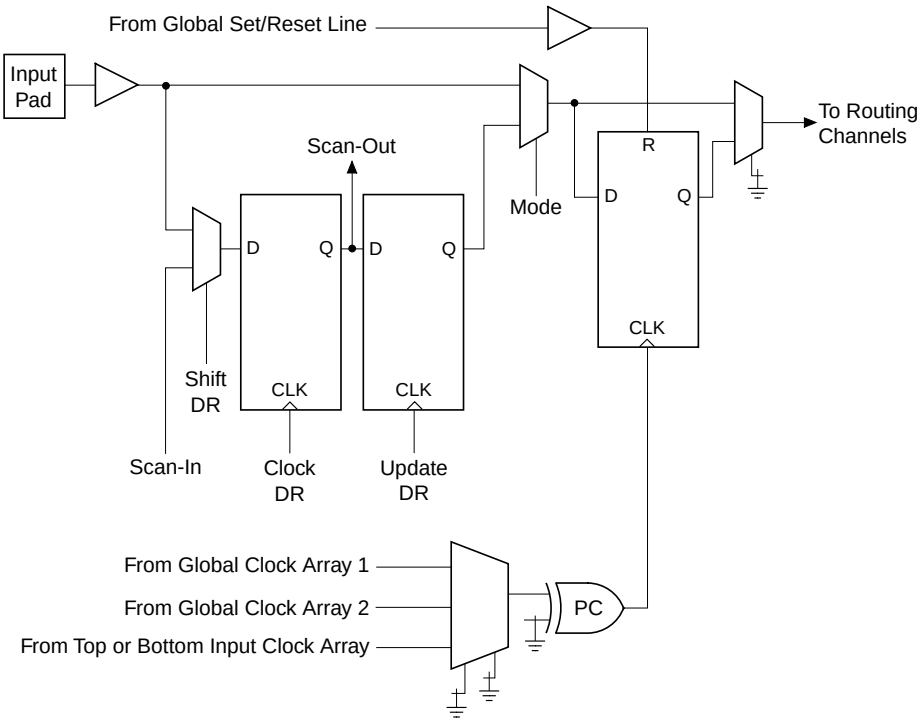


Figure 7: Input Block Diagram

Figure 7 shows the resources in the DL5000 input block. Each input block contains a direct path into the device and a path that includes an edge triggered flip flop. Additional flip flops and muxes support JTAG Boundary Scan.

Output Block

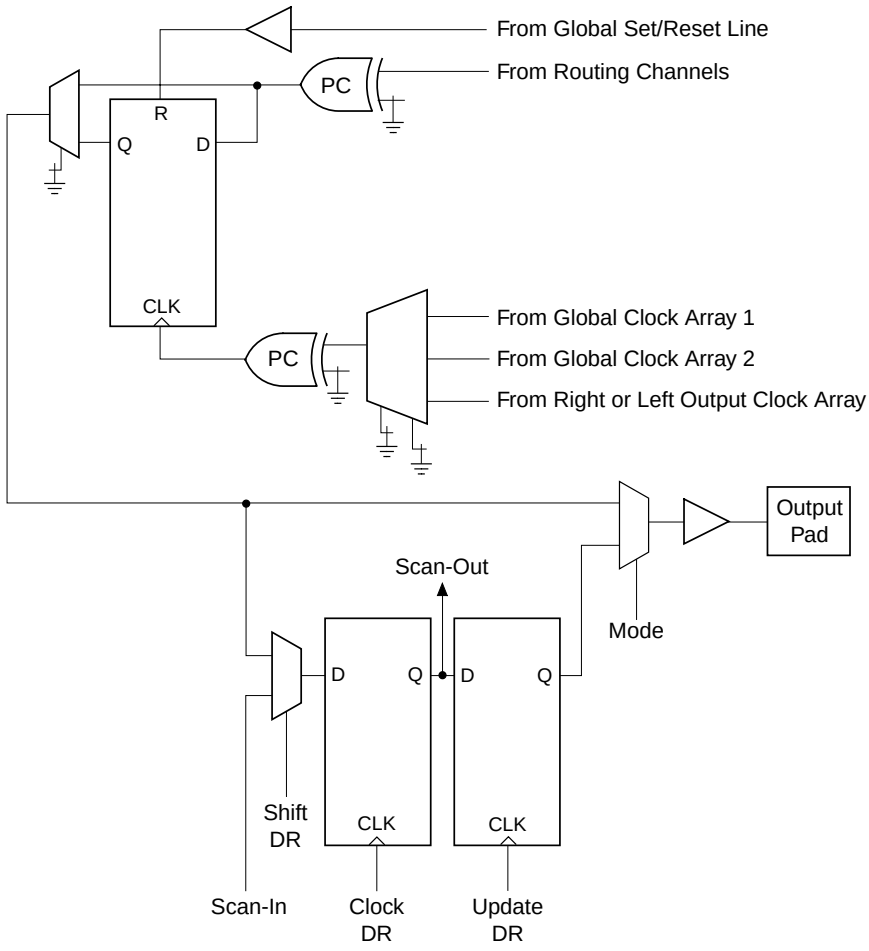


Figure 8: Output Block Diagram

Figure 8 shows the resources in the DL5000 output block. Each output block contains a direct path out of the device and a path that includes an edge triggered flip flop. Additional flip flops and muxes support JTAG Boundary Scan

All outputs must be terminated through a 50Ω resistor to a supply 2V below the top supply. For example, if supply voltages of 0V and -4.5V are used, termination is to -2V.

Differential Outputs

To create differential outputs, connect the output signal to two output pins and invert one of the outputs as shown in figure 9. During implementation, use placement constraints or the DynaTool Design Editor to insure that the pins are placed next to each other.

Differential outputs should only be used when the output signal is registered using the flip flop in the output block. This insures that there is no skew between the differential pairs.

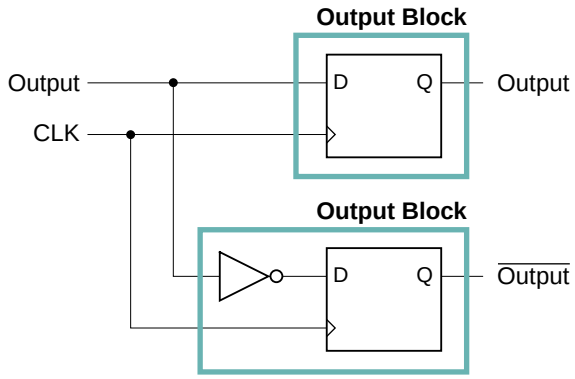


Figure 9: Differential outputs

Logic Blocks

Figure 10 shows a detailed diagram of the logic block in the DL5000. Each block has 18 inputs and 3 outputs. One input is dedicated for clocking and one is for a set/reset signal. The remaining 16 are general purpose inputs to the logic block.

All logic block inputs have polarity control allowing signals to be inverted as they enter the block.

As shown in figure 10, the top section of the combinatorial logic is optimized for AND/OR logic, the middle section is for multiplexers, and the bottom section is for arithmetic logic.

The output of the combinatorial logic functions exit the block directly or serve as inputs to the flip flops. Each logic block has 3 outputs. The output labeled O3 comes from the combinatorial logic. The output labeled O2 can come from the combinatorial logic or from the lower flip flop. The output labeled O1 comes from the upper flip flop.

Each logic block contains two storage elements that can be configured as D-type or toggle flip flops. The flip flops share a common clock that can be driven by the device's global or quadrant clocks or by local interconnect. The clock input to each logic block has polarity control allowing the flip flops to be triggered from either clock edge.

The flip flops also share a common set/reset signal that is driven by the device's global set/reset or by local interconnect. Each flip flop can be configured to have either a set or reset capability. The set/reset input to each logic block has polarity control allowing active high or active low control.

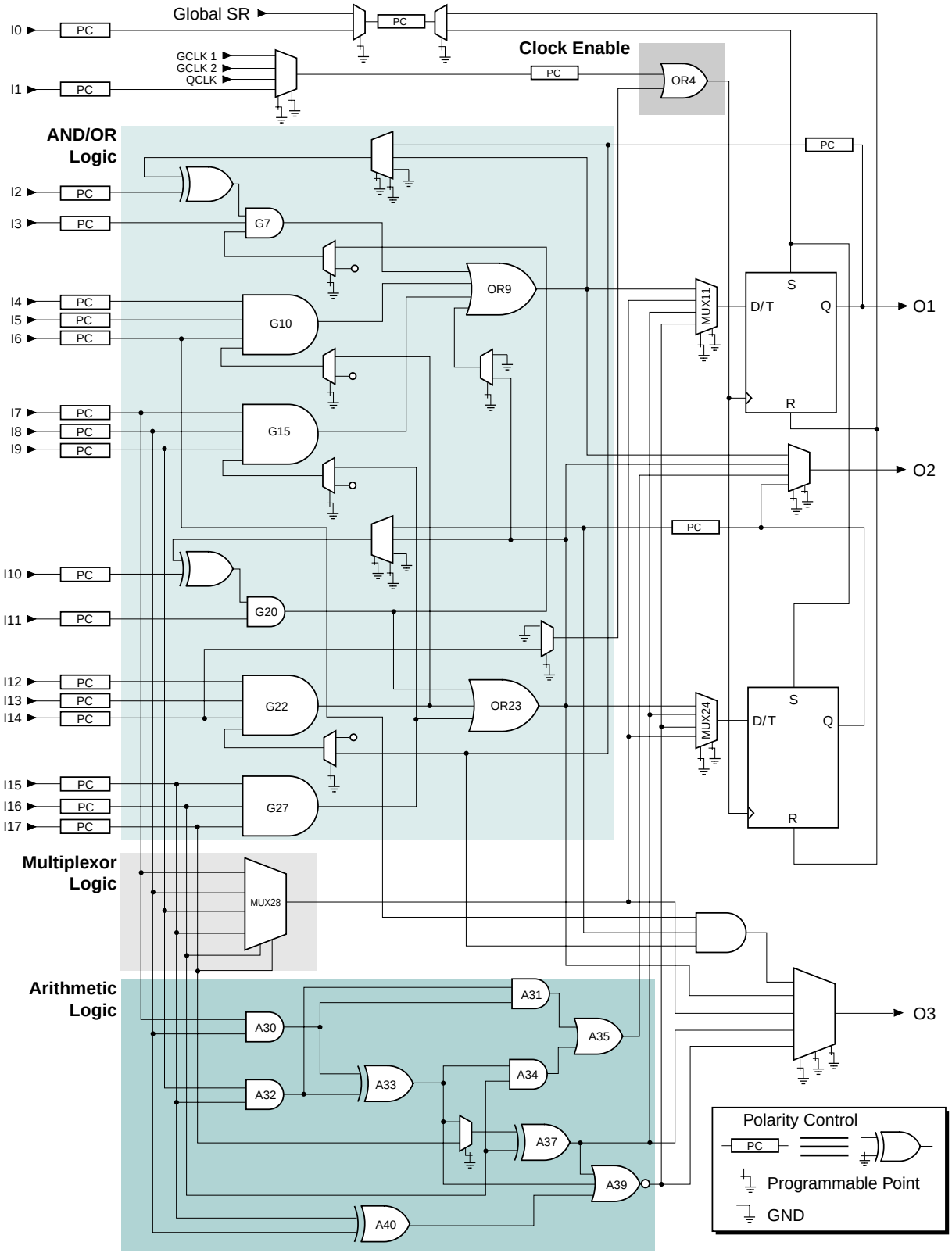


Figure 10: DL5000 Logic Block Diagram

Boundary Scan

All devices in the DL5000 family provide JTAG Boundary Scan. Completely compatible with IEEE specifications, this feature simplifies testing of boards with surface mount packages or closely spaced pins.

Power Consumption

Power consumption for logic blocks in DL5000 family devices averages 50 mW per used block independent of operating frequency. Special circuitry in the DL5000 automatically powers-down resources in the logic blocks that are not used in a design.

Power consumption for output blocks averages 25 mW per output plus the termination power. DynaTool software reports total power consumption for each design after implementation.

Configuration

Memory cells within the DL5000 family devices store configuration bits used to implement the design. These configuration bits are loaded automatically from a PROM at power-up or under user control through a microprocessor or serial communication link.

DL5000 family devices are in-circuit programmable and can be reprogrammed on-the-fly. They can be reconfigured an unlimited number of times providing maximum flexibility for design iterations and field upgrades.

Configuration Modes

Several configuration modes are supported including loading from a serial PROM, serial communication link or microprocessor interface. If the system has multiple DL5000 family devices, a multi-device configuration mode can be used to simplify the connections.

In serial modes, the configuration loading can be controlled from the FPGAs internal clock or from an externally supplied user clock.

Mode Pin Settings

Four special pins on the DL5000 device named M0, M1, M2 and M3 determine the loading mode. To load the device from a microprocessor, set the mode pins as shown in table 2.

To load the device from a serial PROM or serial communication link, first determine if the device is in a single or multi-device configuration.

In a single device configuration, determine if the loading is controlled using an internal or external clock. Then set the mode pins as shown in table 2.

In a multi-device configuration, determine if the device is the last one in the chain. If the device is the last in the chain, determine if the loading is controlled using an internal or external clock. Then set the mode pins as shown in table 2.

MODE	M0	M1	M2	M3	Bpsel	RB	WE
Microprocessor Configuration	0	0	0	0	0	0	See description
Multi-device Serial Configuration Where Device is Not Last	0	1	0	0	0	0	0
Multi-device Serial Configuration Where Device is Last Using Internal Clock	0	0	1	0	0	0	0
Multi-device Serial Configuration Where Device is Last Using External Clock	0	1	1	0	0	0	0
Single Serial Configuration Using Internal Clock	0	0	1	0	0	0	0
Single Serial Configuration Using External Clock	0	1	1	0	0	0	0

Table 2: Mode Pin Settings

Serial PROM Configuration Loading Mode

In the serial PROM configuration loading mode, the device automatically loads itself from a serial PROM when the system is powered up. The PROM provides serial data and responds to a clock signal generated by the DL5000 device.

Systems using this loading mode should be connected as shown in Figure 11.

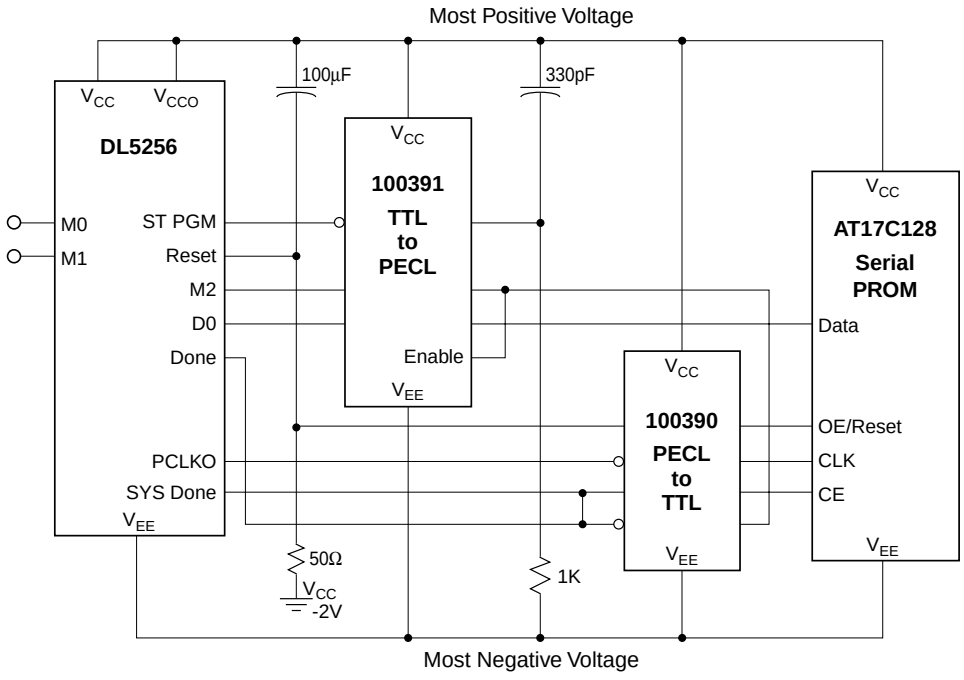


Figure 11: Serial PROM Configuration Schematic

Microprocessor Interface Loading Mode*

In the microprocessor interface loading mode, the device is loaded under user control from a microprocessor interface. Data is loaded into the DL5000 device byte-wide in response to the rising edge of a write enable signal. The DL5000 device generates a ready signal that indicates it is ready for the next byte of data.

Systems using this loading mode should be connected as shown in Figure 12.

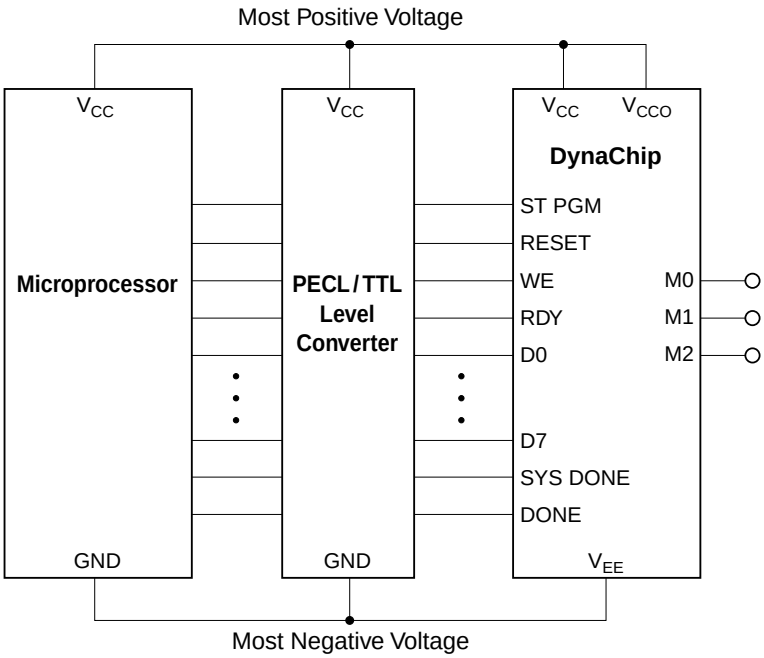


Figure 12: Microprocessor Configuration

*This mode is not available in the DL5064 device.

Serial Link Loading Mode

In the serial link loading mode, the device is loaded under user control through a serial communication link. Data is loaded serially in response to the rising edge of the clock input.

Systems using this loading mode should be connected as shown in Figure 13.

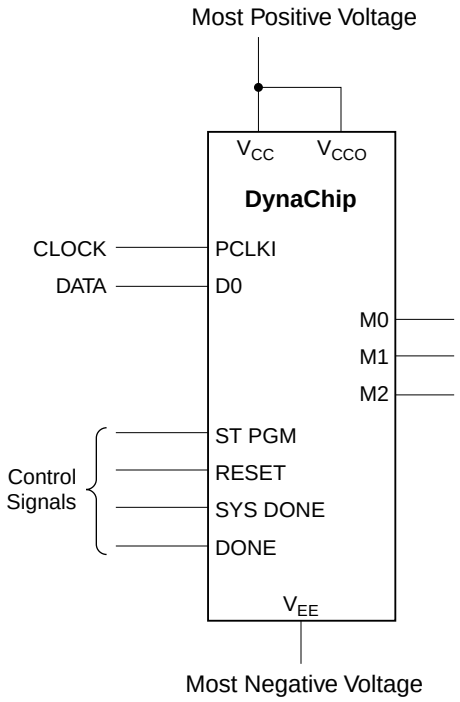


Figure 13: Serial Link Configuration Schematic

Multi-device Configuration Loading Mode

The multi-device configuration loading mode simplifies connections for systems that use more than one DL5000 family device. Using this mode one DL5000, called the last device, connects to the source of the configuration data. The remaining DL5000 devices connect in a chain using their serial configuration pins.

Systems using this loading mode should be connected as shown in Figure 14.

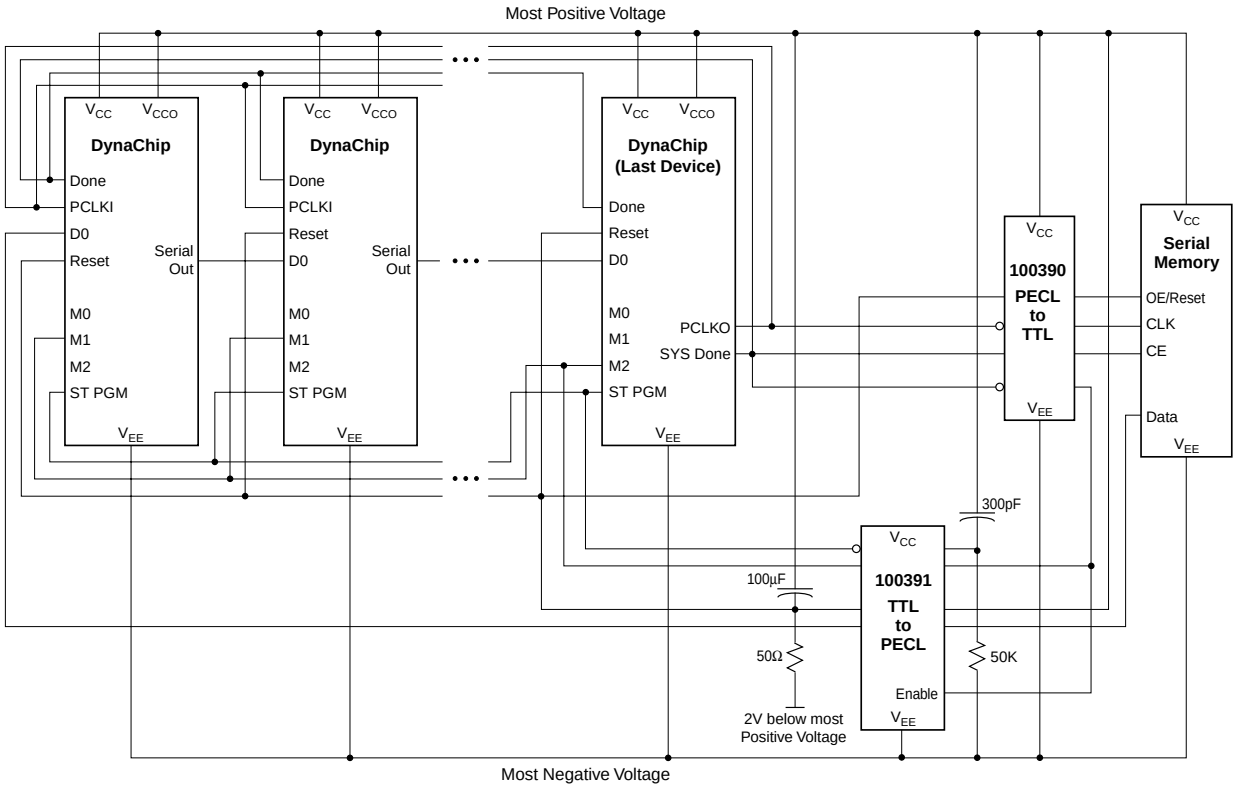


Figure 14: Multi-device Configuration Schematic

Note: PCLKI is not connected to the last chip in the chain.

Bitstream Size

The following table shows the size of the programming bitstreams for DL5000 family devices.

DEVICE	Bitstream Size
DL5064	81,426 bits
DL5256	81,426 bits
DL5528	160,738 bits

Table 3: Programming Bitstreams

Configuration Pins

Two types of pins are used in the configuration process. Permanently dedicated pins are always dedicated to configuration functions. User pins that can have special functions become user input or output pins after device configuration.

Permanently Dedicated Pins

V_{CC}:

The number of V_{CC} pins depend on the device type and package. All V_{CC} pins must be connected to the most positive voltage supply.

V_{CCO}:

These pins supply power to the outputs. The number of V_{CCO} pins depend on the number of outputs. All V_{CCO} pins must be connected to the most positive supply. On the circuit board, V_{CCO} and V_{CC} should be shorted together with the shortest possible connections.

V_{EE}:

The number of V_{EE} pins depend on the device type and package. All V_{EE} pins must be connected to the most negative voltage supply.

PCLKI:

This is an input pin that serves 2 functions. In a multiple device loading mode, the PCKLO pin of the last device can be connected to the PCLKI pin of all the other devices to provide a programming clock.

This pin also serves as a clock input in systems that use an externally generated programming clock.

PCLKO:

This is an output pin that supplies the programming clock in a multiple device configuration mode.

The programming clock is generated by the last device and is connected to the PCLKI pin of all other devices.

RESET:

This is an input pin that is used to trigger reconfiguration of a device that has already been programmed.

See configuration diagrams for normal operation.

ST PGM:

A Low-to-High transition on this input pin is used to start the configuration process. Refer to the programming diagrams for more information on how to use this pin.

SYS DONE:

This is an output pin that signals the configuration has been completed.

User Pins That Can Have Special Functions

DONE:

This is an input pin that shuts down the programming circuitry. It is tied to the SYS DONE pin during configuration. It is an input during normal operation.

M0 - M3:

These pins are used to set the configuration mode for each device. Please refer to table 2 - *Mode Pin Settings* for the proper connections for each configuration mode. These pins are inputs during normal operation.

SEROUT:

This output pin is used to send serial data to the next device in a multiple device configuration mode. It can be used as an output during normal operation.

D0:

This input pin is the data input in a serial loading mode or the LSB data bit in a microprocessor loading mode. It can be used as an input during normal operation.

D1 - D7:

These input pins are the upper 7 data bits in a microprocessor loading mode. They can be used as inputs during normal operation.

WE:

In the microprocessor loading mode, one byte of configuration data is loaded into the device on the rising edge transition of WE. In all other loading modes, WE must be low. This pin can be used as an input during normal operation.

RDY:

This output pin is used in the microprocessor loading mode to indicate that the DL5000 is ready to receive the next byte of data. This pin can be used as an output during normal operation.

TDI, TCK, TMS:

These pins serve as clock and control inputs when boundary scan is selected. TDI is Test Data In, TCK is Test Clock and TMS is Test Mode Select. When boundary scan is not selected, these pins are normal inputs.

TDO:

When boundary scan is selected, this pin is the Test Data Output. When boundary scan is not selected, this pin can be used as a normal output.

GCK1, GCK2:

These pins provide global clock inputs for the device. Clock signals connected to these pins are available to every logic block, input block and output block flip flop in the device.

The use of these clocks is controlled by selections made in the schematic or HDL design description. If either of these pins are not used for global clocks, they can be used as standard inputs.

QCK1, QCK2, QCK3, QCK4:

These pins provide the 4 quadrant clock inputs for the device. Clock signals connected to each of these pins are available to the flip flops in 1/4 of the logic modules.

Use of these clocks is controlled by selections made in the schematic or HDL design description. If these pins are not used for quadrant clocks, they can be used as standard inputs.

OLCK, ORCK:

These input pins provide dedicated clock signals for the flip flops in the output blocks. OLCK is for the output blocks on the left side of the device and ORCK is for the output blocks on the right side of the device.

Use of these clocks is controlled by selections made in the schematic or HDL design description. If either of the pins are not used for clocks, they can be used as standard inputs.

ITCK, IBCK:

These input pins provide dedicated clock signals for the flip flops in the input blocks. ITCK is for the input blocks on the top of the device and IBCK is for the input blocks on the bottom of the device.

Use of these clocks is controlled by selections made in the schematic or HDL design description. If either of the pins are not used for clocks, they can be used as standard inputs.

GSR:

This input pin provides a global set/reset signal for the device. It drives a dedicated net that is connected to every logic block, input block and output block flip flop in the device. When this pin is asserted, all input and output block flip flops are reset. All logic block flip flops are either set or reset depending on their definition in the schematic or HDL design description.

If this pin is not used for a global set/reset it can be used as a standard input.

RB

Must be low during configuration.

Bpsel:

Must be low during configuration.

Product Specifications

Maximum Ratings

Symbol	Description	Value	Unit
V_{EE}	V_{EE} Pin Potential to V_{CC} Pin	+0.5 to -7.0	V
V_{IN}	Input Voltage	V_{CC}+.5 to V_{EE}	V
I_{OUT}	DC Output Current (Output High)	-30	mA
T_J	Junction Temperature	-55 to +125	°C
T_{STORE}	Storage Temperature	+150	°C

Table 4: Absolute Maximum Ratings

Note:

Permanent damage to the device may occur if the Absolute Maximum ratings are exceeded. This is a stress rating only. Functional operation of the device at these or any other conditions other than those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{EE}	ECL Supply Voltage (1, 2)	-5.7	-4.2	V
V_{CC}	PECL Supply Voltage (3)	4.75	5.25	V
V_{CCO}	Output PECL Supply Voltage (3)	4.75	5.25	V
V_{CC}	GTL Supply Voltage (4)	1.9	2.1	V
V_{CCO}	Output GTL Supply Voltage (4)	1.9	2.1	V
T_J	Junction Temperature	0	+85	°C

Table 5: Recommended Operating Conditions

Notes:

(1) For ECL 100K operation, connect V_{EE} to -4.5V, V_{CC} and V_{CCO} to GND.
(2) For ECL 100KH operation, connect V_{EE} to -5.0V, V_{CC} and V_{CCO} to GND.
(3) For PECL operation, connect V_{EE} to GND, V_{CC} and V_{CCO} to +5V.
(4) For GTL operation, connect V_{EE} to -3V, V_{CC} and V_{CCO} to +2V.

DC Characteristics Over Operating Conditions

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}	High level output voltage	-1025	-880	mV	$V_{IN} = V_{IH}$ MAX or V_{IL} MIN
V_{OHT}	High level output threshold voltage	-1035		mV	$V_{IN} = V_{IH}$ MAX or V_{IL} MIN
V_{OL}	Low level output voltage	-1810	-1620	mV	$V_{IN} = V_{IH}$ MAX or V_{IL} MIN
V_{OLT}	Low level output threshold voltage		-1610	mV	$V_{IN} = V_{IH}$ MAX or V_{IL} MIN
V_{IH}	High level input voltage	-1165	-880	mV	Guaranteed input voltage high for all inputs
V_{IL}	Low level input voltage	-1810	-1475	mV	Guaranteed input voltage low for all inputs
I_{IH}	High level input current		220	µA	$V_{IN} = V_{IH}$ MAX
I_{IL}	Low level input current	0.3		mA	$V_{IN} = V_{IL}$ MIN

Table 6: DC Electrical Characteristics

Notes:
(1) All voltage measurements are referenced to the V_{CC} terminal.
(2) All devices have been designed to meet the DC specifications after thermal equilibrium has been established.
(3) All used outputs should be terminated through a 50Ω resistor to a supply that is set to 2V below V_{CC}. All unused outputs should be left electrically disconnected to reduce current consumption.
(4) All unused inputs should be left electrically disconnected. They should not be connected to either V_{EE} or V_{CC}. An internal pull-down resistor will pull unused inputs to a logic "0".

Clock Buffer Switching Characteristics

Description	Symbol	Speed Grade (Max)			Units
		-E	-F	-G	
Global clock buffer delay (1)	T_{GCKD}	3.0	2.7	2.5	ns
Global clock buffer skew	T_{GCKS}	0.25	0.25	0.25	ns
Quadrant clock buffer delay (1)	T_{QCKD}	3.0	2.7	2.5	ns
Quadrant clock buffer skew	T_{QCKS}	0.25	0.25	0.25	ns
Input clock buffer delay (1)	T_{ICKD}	3.0	2.7	2.5	ns
Input clock buffer skew	T_{ICKS}	0.25	0.25	0.25	ns
Output clock buffer delay (1)	T_{OCKD}	3.0	2.7	2.5	ns
Output clock buffer skew	T_{OCKS}	0.25	0.25	0.25	ns
GSR buffer	T_{GSR}	12.0	10.5	9.5	ns

Table 7: Clock Buffer AC Characteristics

Notes:
(1) Clock buffer delays are also referred to as latency.
(2) Delays are rounded to nearest tenth of a ns.

Description	Symbol	Speed Grade (Min)			Units
		-E	-F	-G	
Clock min pulse width high	T_{MPH}	2.1	1.9	1.7	ns
Clock min pulse width low	T_{MPL}	2.1	1.9	1.7	ns

Table 8: Minimum Clock Pulse Width

Input and Output Block Switching Characteristics

Description	Symbol	Speed Grade (Max)			Units
		-E	-F	-G	
Input buffer combinatorial delay	T_{INPD}	2.1	1.8	1.6	ns
Input Set-up Time (global clock)	T_{INIS1}	1.0	0.9	0.8	ns
Input Set-up Time (input clock)	T_{INIS2}	1.0	0.9	0.8	ns
Input Hold Time (global clock)	T_{INIH1}	0	0	0	ns
Input Hold Time (input clock)	T_{INIH2}	0	0	0	ns
Input Clock to Output (global clock)	T_{INCO1}	2.0	1.8	1.6	ns
Input Clock to Output (input clock)	T_{INCO2}	2.0	1.8	1.6	ns
Output buffer combinatorial delay	T_{OUTPD}	3.2	2.9	2.6	ns
Output Set-up Time (global clock)	T_{OUTIS1}	2.1	1.9	1.7	ns
Output Set-up Time (output clock)	T_{OUTIS2}	2.1	1.9	1.7	ns
Output Hold Time (global clock)	T_{OUTIH1}	0	0	0	ns
Output Hold Time (output clock)	T_{OUTIH2}	0	0	0	ns
Output Clock to Output (global clock)	T_{OUTCO1}	2.1	1.8	1.6	ns
Output Clock to Output (output clock)	T_{OUTCO2}	2.1	1.8	1.6	ns
Input Set-up Time (GSR)	$T_{INISGSR}$	2.0	1.8	1.6	ns
Output Set-up Time (GSR)	$T_{OUTISGSR}$	4.2	3.8	3.4	ns
Input Flip Flop Reset Delay	T_{INRST}	4.0	3.6	3.2	ns
Output Flip Flop Reset Delay	T_{OUTRST}	4.2	3.6	3.2	ns

Table 9: Input and Output Buffer Parameters (Pin - to - Pin) (1, 2)

Notes:
(1) These delays include all routing up to an active repeater.
(2) All used outputs should be terminated through a 50Ω resistor to a supply that is set to 2V below V_{CC}. All unused outputs should be left electrically disconnected to reduce current consumption.
(3) All unused inputs should be left electrically disconnected. They should not be connected to either V_{EE} or V_{CC}. An internal pull-down resistor will pull unused inputs to a logic "0".
(4) Clock to output delays do not include clock latency.
(5) Delays are rounded to nearest tenth of a ns.

Logic Block Switching Characteristics(1)

Delays include all routing within a 5x7 routing region.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
2-input AND/OR combinatorial delay	$T_{2ASINDC}$	4.6	4.1	3.7	ns
3-input AND/OR combinatorial delay	T_{3ANDC}	4.9	4.3	3.9	ns
4-input AND/OR combinatorial delay	T_{4ANDC}	4.8	4.2	3.8	ns
5-input AND/OR combinatorial delay	T_{5ANDC}	5.3	4.6	4.1	ns
6-input AND/OR combinatorial delay	T_{6ANDC}	5.3	4.6	4.1	ns
2-input XOR combinatorial delay	T_{2XORC}	5.0	4.3	3.9	ns
3-input XOR combinatorial delay	T_{3XORC}	5.4	4.6	4.1	ns
Adder/Multiplier combinatorial delay	T_{ADDC}	5.3	4.6	4.1	ns
4:1 Multiplexer data combinatorial delay	T_{MUXC}	4.4	3.9	3.5	ns
4:1 Multiplexer select delay	T_{MUXS}	5.3	4.6	4.1	ns
2-input AND/OR to flip flop delay	T_{2ANDR}	4.2	3.6	3.2	ns
3-input AND/OR to flip flop delay	T_{3ANDR}	4.5	3.9	3.5	ns
4-input AND/OR to flip flop delay	T_{4ANDR}	4.9	3.8	3.4	ns
5-input AND/OR to flip flop delay	T_{5ANDR}	4.9	4.3	3.9	ns
6-input AND/OR to flip flop delay	T_{6ANDR}	4.9	4.3	3.9	ns
2-input XOR to flip flop delay	T_{2XORR}	4.7	4.0	3.6	ns
3-input XOR to flip flop delay	T_{3XORR}	5.1	4.3	3.9	ns
4:1 Multiplexer data to flip flop	T_{MUXR}	3.5	3.0	2.7	ns
4:1 Multiplexer select to flip flop	T_{MUXSR}	4.4	3.8	3.4	ns
Adder/multiplier to flip flop	T_{ADDCR}	4.4	3.8	3.4	ns
D Flip flop setup time	T_{SU}	0.6	0.5	0.4	ns
T Flip flop setup time	T_{SUT}	0.9	0.8	0.7	ns
Flip flop clock to out (GCLK or QCLK)	T_{COG}	2.0	1.7	1.5	ns
Flip flop clock to out (LCK2)	T_{COL}	5.3	4.6	4.1	ns
GSR set/reset delay	T_{GSR}	3.3	2.9	2.6	ns
LSR set/reset delay	T_{LSR}	5.3	4.7	4.2	ns
Reset Setup Time	T_{SURST}	1.2	1.0	0.8	ns

Table 10: Logic Block Switching Parameters

Notes:
(1) Combinatorial and clock to out delays include all routing and connection buffer delays up to the next logic block input or active repeater as shown in figure 15.
(2) The AND/OR combinatorial delay, XOR combinatorial delay, adder/multiplier delay and 4:1 multiplexer delay include the complete path through the logic block from inputs I1 through I16 through outputs O1 or O2, to the next logic block or active repeater.
(3) The AND/OR to flip flop, XOR to flip flop, 4:1 multiplexer data to flip flop, 4:1 multiplexer select to flip flop and adder/multiplier to flip flop delay includes all elements from inputs I1 through I16 to the D/T input of either flip flop.
(4) Designs may be mapped to paths with different delays.
(5) Delays are rounded to nearest tenth of a ns.

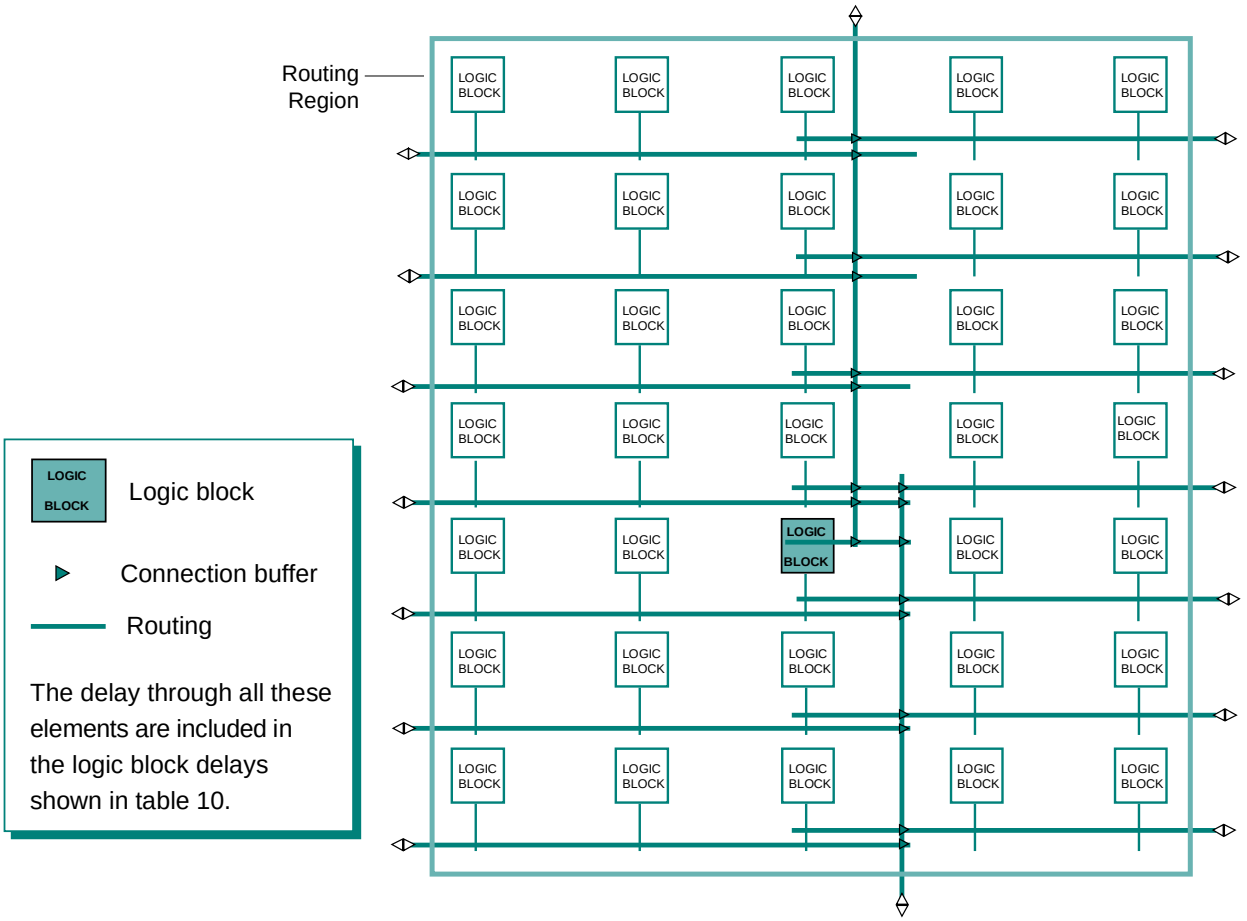


Figure 15: Connection and Routing Delays.

Logic block delays shown in table 10 include all connection buffer and routing delays within a routing region. Additional delays are only incurred when a net must go through an active repeater to reach a block in another routing region. See table 11 for active repeater delays.

Active Repeater Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
Horizontal Active Repeater	T_{HREP}	1.2	1.1	1.0	ns
Vertical Active Repeater	T_{VREP}	1.4	1.2	1.1	ns

Table 11: Active Repeater Parameters

Notes:
(1) Delays are rounded to nearest tenth of a ns.

Timing Diagrams

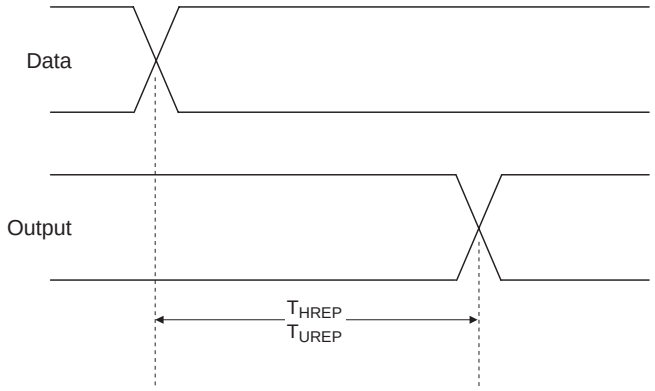


Figure 16: Repeater Delays

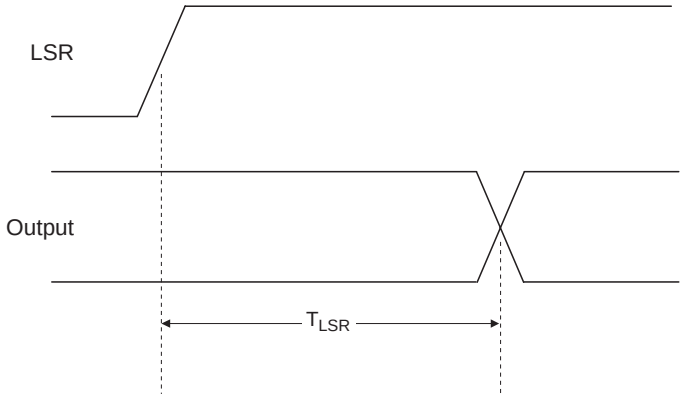


Figure 17: Delay Using Local Set/Reset

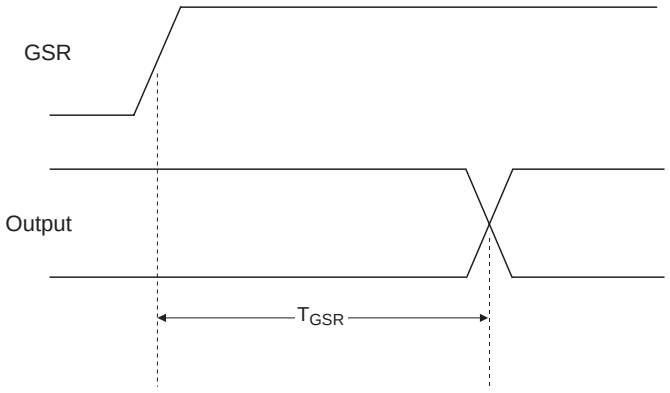


Figure 18: Delay Using Global Set/Reset

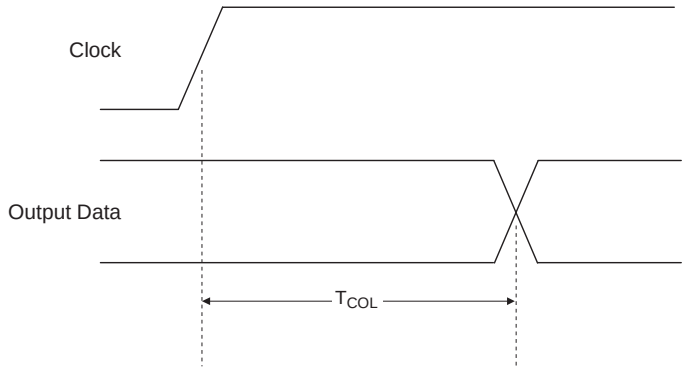


Figure 19: Logic Block Flip Flop Clock to Output Delay Using Local Clock

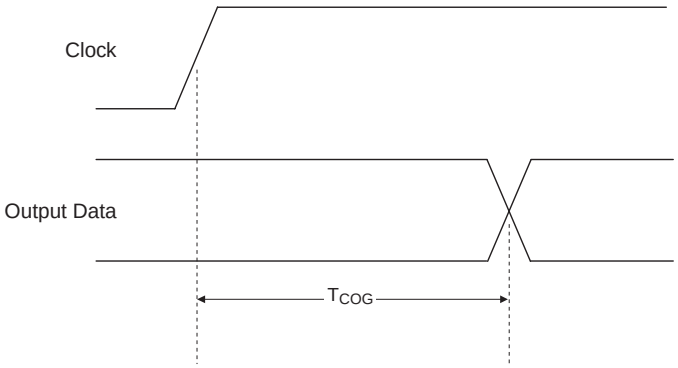


Figure 20: Logic Block Flip Flop Clock to Output Delay Using Global Clock

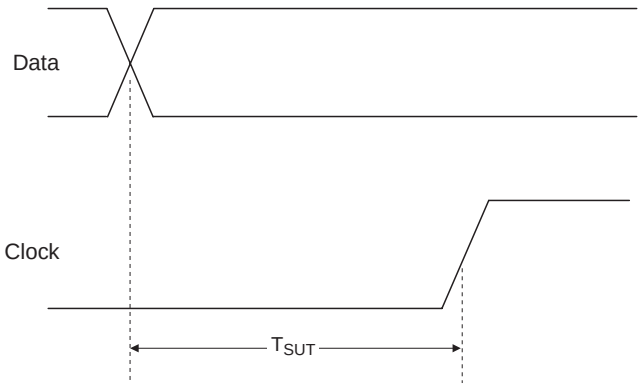


Figure 21: Logic Block T-Flip Flop Setup Time

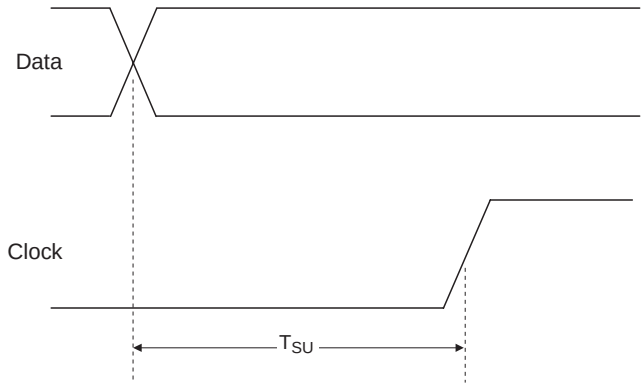


Figure 22: Logic Block D-Flip Flop Setup Time

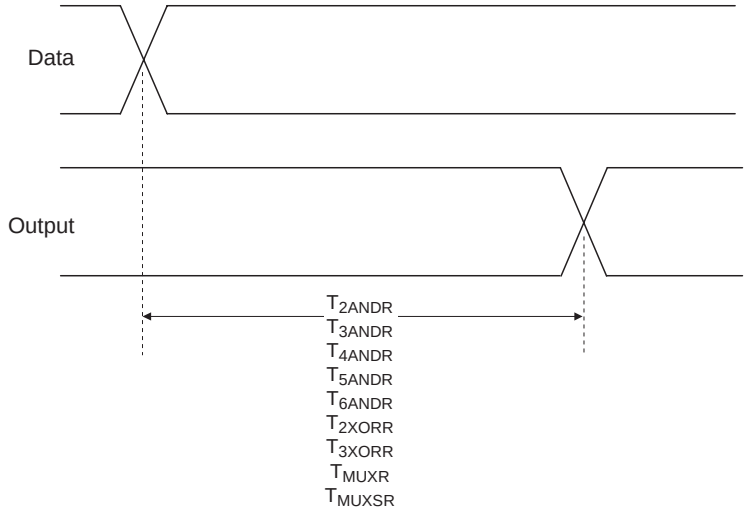


Figure 23: Combinatorial Logic to Flip Flop Delay

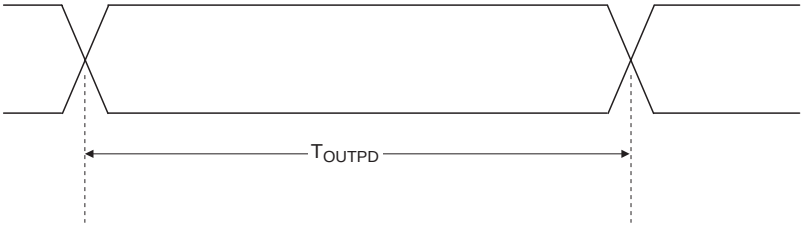


Figure 24: Output Buffer Combinatorial Delay

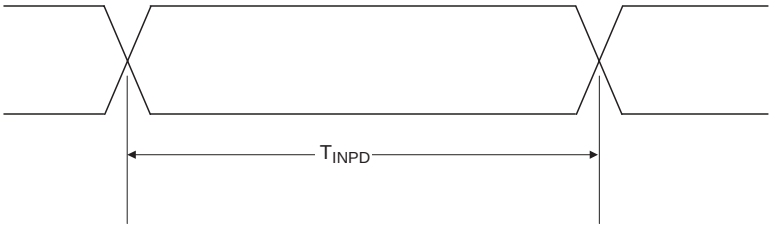


Figure 25: Input Buffer Combinatorial Delay

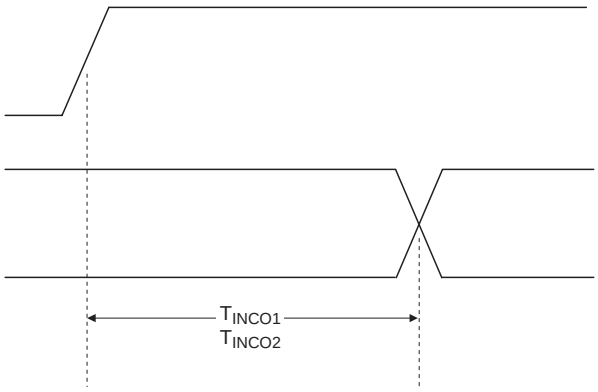


Figure 26: Input Block Flip Flop Clock to Output Delay

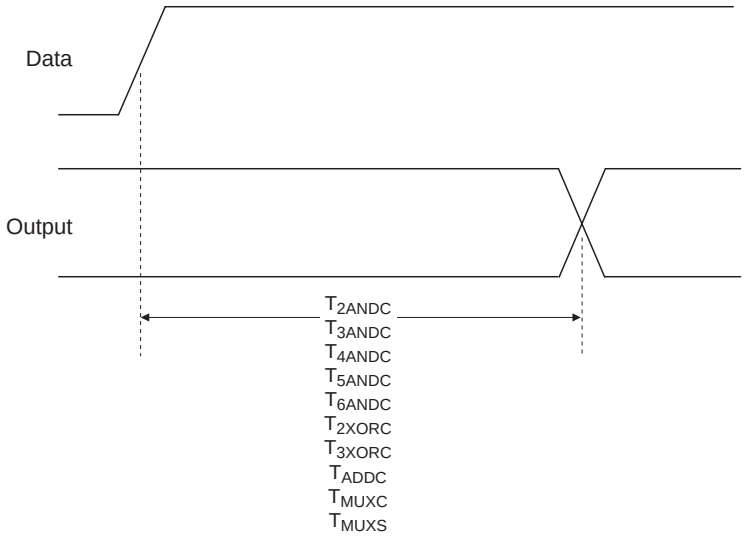


Figure 27: Combinatorial Delay Through Logic Block

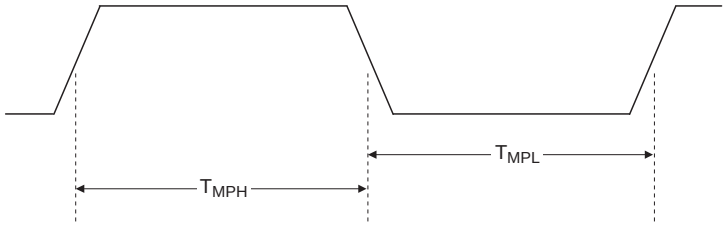


Figure 28: Minimum Clock Pulse High and Low

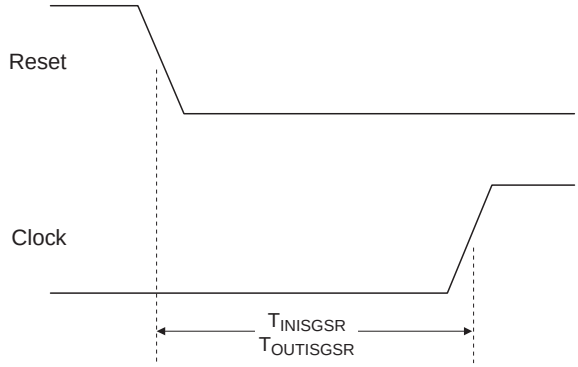


Figure 29: Global Reset Setup Time to Input/Output Block Flip Flop

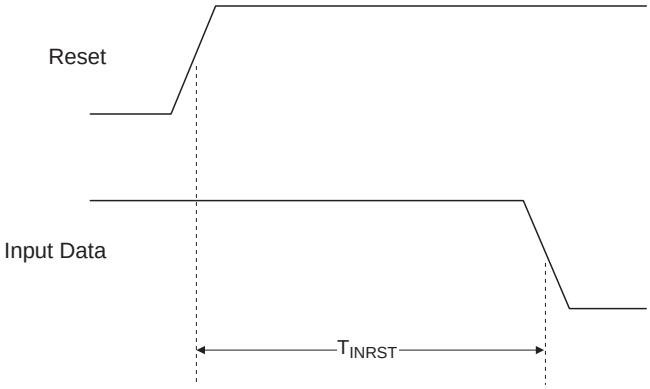


Figure 30: Input Block Flip Flop Reset Delay

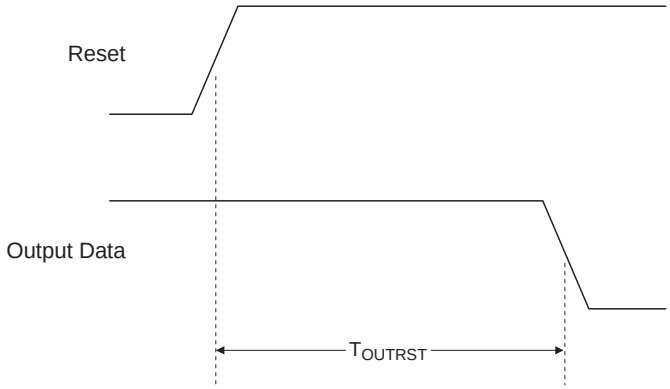


Figure 31: Output Block Flip Flop Reset Delay

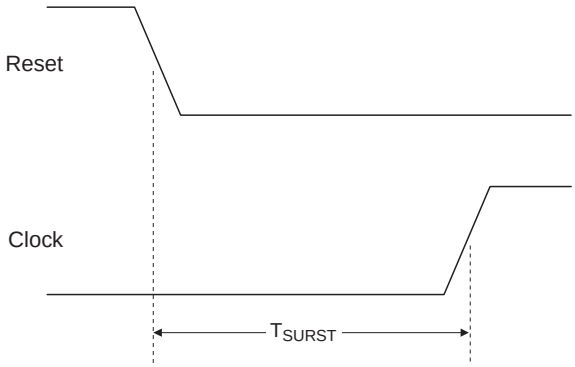


Figure 32: Reset Setup Time to Logic Block Flip Flop

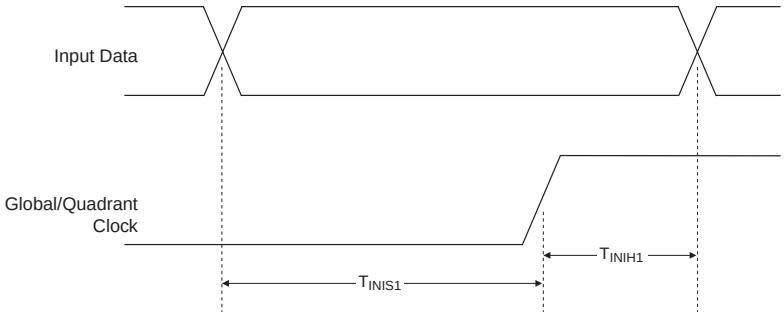


Figure 33: Input Block Flip Flop Setup and Hold Time

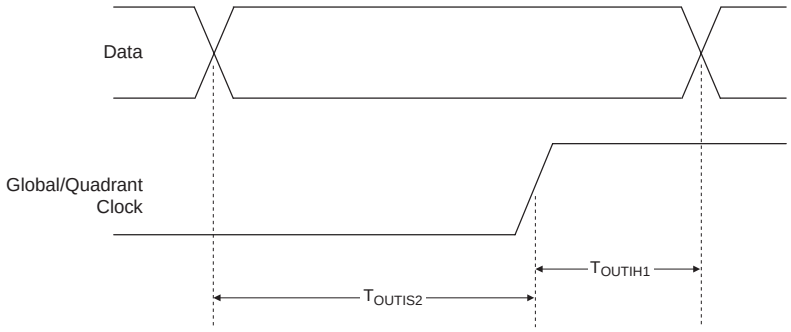


Figure 34: Output Block Flip Flop Setup and Hold Time

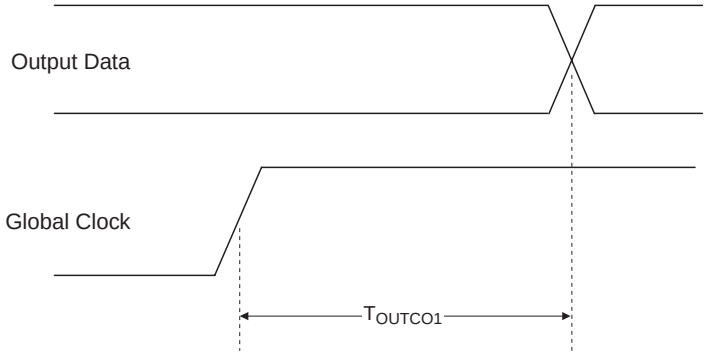


Figure 35: Output Block Flip Flop Clock to Output Delay

Figure 36: Global and Quadrant Clock Buffer Skew

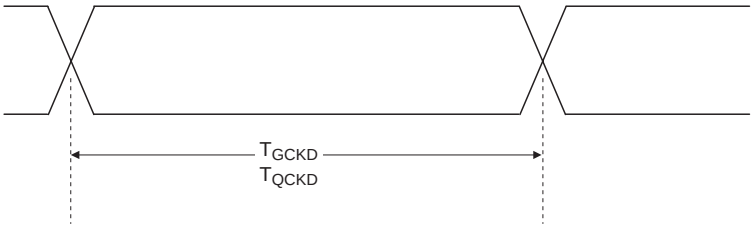


Figure 37: Global and Quadrant Clock Buffer Delay

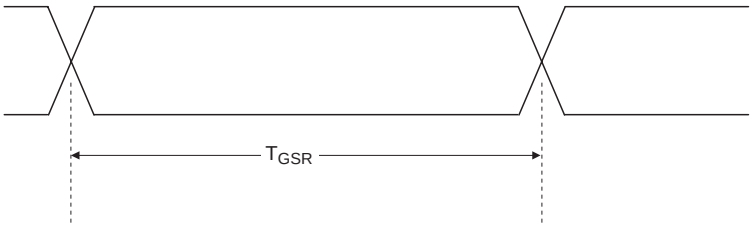


Figure 38: Global Set/Reset Buffer Delay

Pin Description

Pin Description	204 SBGA Ball No.	208 PGA Pin No.	Pin Description	204 SBGA Ball No.	208 PGA Pin No.
RESET	D18	B16	I12B	W14	T12
PCLKI	C19	A17	I13B	Y14	U12
St Pgm	B20	D15	I14B	V13	R11
Sys Done	E18	C16	I15B	W13	T11
PCLKO	D19	B17	I16B	Y13	U11
O0L/BSOUT	C20	E15	I17B/QCK3	V12	R10
O1L	F18	D16	I18B/GRST	W12	T10
O2L/RDY	E19	C17	I19B	Y12	U10
O3L/SEROUT	D20	F15	I20B/GCK2	Y10	U9
O4L	E20	E16	I21B/QCK4	W10	T9
O5L	F19	D17	I22B	V10	U8
O6L	F20	F16	I23B/IBCK	Y9	T8
O7L	G19	G15	I24B	W9	R8
O8L	H18	E17	I25B	V9	U7
O9L	G20	G16	I26B	W8	T7
O10L	H19	F17	I27B	Y7	U6
O11L	J19	H15	I28B	W7	R7
O12L	J18	G17	I29B	Y6	T6
O13L	J20	H16	I30B	W6	U5
O14L	K20	H17	I31B	V7	R6
O15L	K19	J17	I32B	Y5	T5
O16L	L20	J15	I33B	W5	U4
O17L	L19	J16	I34B	V6	T4
O18L	L18	K17	I35B	Y4	U3
O19L	M20	K16	I36B/TDI	W4	R4
O20L	M19	K15	I37B/TMS	Y3	T3
O21L	N20	L17	I38B/TCK	V4	U2
O22L	M18	L16	I36T	C4	A2
O23L	N19	L15	I35T	A3	B3
O24L	P20	M17	O2R	T3	T1
O25L	P19	M16	O3R	W1	R2
O26L	R20	M15	O4R	U2	P3
O27L	T20	N17	O5R	V1	R1
O28L	R19	N16	O6R	R3	P2
O29L	P18	P17	O7R	T2	N3
O30L	U20	N15	O8R	U1	P1
O31L	T19	P16	O9R	T1	N2
O32L	V20	R17	O10R	R2	N1
O33L	R18	P15	O11R	R1	M3
O34L	U19	R16	O12R	N3	M2
O35L	W20	T17	O13R	P2	M1
I1B/OLCK	V19	U17	O14R	P1	L3
I2B	U18	T16	O15R	N2	L2
O0R/TDO	U3	T2	O16R	M2	L1
O1R	V2	U1	O17R	M1	K3
I3B	V17	U16	O18R	L2	K2
I4B	Y18	T15	O19R	L3	K1
I5B	V16	R14	O20R	L1	J2
I6B	W17	U15	O21R	K2	J3
I7B	Y17	T14	O22R	K3	J1
I8B	V15	U14	O23R	K1	H1

Table 12: DL5256 Pin Description

Pin Description	204 SBGA Ball No.	208 PGA Pin No.
I9B	W16	T13
I10B	Y16	U13
I11B	W15	R12
O27R	G1	F1
O28R	G2	G2
O29R	H3	E1
O30R	F1	G3
O31R	E1	F2
O32R	F2	D1
O33R	G3	E2
O34R	D1	F3
O35R	E2	C1
O36R	F3	D2
O37R	C1	E3
O38R	D2	B1
O39R	B1	C2
I38T/ORCK	C2	D3
I37T	D3	B2
I34T	C5	C4
I33T	B4	A3
I32T	A4	B4
I31T	C6	A4
I30T	B5	B5
I29T	A5	C6
I28T	B6	A5
I27T	A6	B6
I26T	C8	C7
I25T	B7	A6
I24T	A7	B7
I23T	B8	A7
I22T	B9	C8
I21T/ITCK	A9	B8
I20T	C10	A8
I19T/QCK2	B10	B9
I18T/GCK1	A10	A9
I17T/M3	C11	A10
I16T/bpsel	A12	B10
I15T/QCK1	B12	C10
I14T/done	C12	A11
I13T/WE	A13	B11
I12T/RB	B13	C11
I11T/D7	A14	A12
I10T/D6	B14	B12
I9T/D5	C14	C12
I8T/D4	B15	A13
I7T/D3	A16	B13
I6T/D2	B16	A14
I5T/D1	C15	B14

Pin Description	204 SBGA Ball No.	208 PGA Pin No.
O24R	J1	H2
O25R	J2	G1
O26R	H2	H3
I4T/D0	A17	A15
I3T/M2	B17	C14
I2T/M1	A18	B15
I1T/M0	C17	A16
V_{CC}	B2	C13
V_{CC}	C13	C15
V_{CC}	C16	C3
V_{CC}	C3	D11
V_{CC}	C7	D13
V_{CC}	C9	D5/D7
V_{CC}	V11	D9
V_{CC}	V14	P10/P12
V_{CC}	V18	P14
V_{CC}	V5	P4/P6
V_{CC}	V8	P8
V_{CC}	W19	R9/R13
V_{CCO}	B19	A1
V_{CCO}	C18	E4/E14
V_{CCO}	E3	F4/F14
V_{CCO}	G18	G4/G14
V_{CCO}	J3	H4/H14
V_{CCO}	K18	J4/J14
V_{CCO}	M3	K4/K14
V_{CCO}	N18	L4/L14
V_{CCO}	P3	M4
V_{CCO}	T18	M14
V_{CCO}	V3	N4
V_{CCO}	W2	N14
V_{EE}	A1/A2	C5
V_{EE}	A8	C9
V_{EE}	A11	D10
V_{EE}	A15	D12
V_{EE}	A19/A20	D14
V_{EE}	B3	D4
V_{EE}	B11/B18	D6
V_{EE}	H1/H20	D8
V_{EE}	N1	P11
V_{EE}	W3	P13
V_{EE}	W11/W18	P5
V_{EE}	Y1/Y2	P7
V_{EE}	Y8	P9
V_{EE}	Y11	R15
V_{EE}	Y15	R3
V_{EE}	Y19/Y20	R5

Table 12: DL5256 Pin Description

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
U	I1B/ L_ock	I3B	I6B	I8B	I10B	I13B	I16B	I19B	I20B/ GCK2	I22B	I25B	I27B	I30B	I33B	I35B	I38B/ TCK	O1R	**U**
T	O35L	I2B	I4B	I7B	I9B	I12B	I15B	I18B/ GRST	I21B/ Q4_ck	I23B/ B_ick	I26B	I29B	I32B	I34B	I37B/ TMS	O0R/ TDO	O2R	**T**
R	O32L	O34L	V_{EE}	I5B	V_{CC}	I11B	I14B	I17B/ Q3_ck	V_{CC}	I24B	I28B	I31B	V_{EE}	I36B/ TDI	V_{EE}	O3R	O5R	**R**
P	O29L	O31L	O33L	V_{CC}	V_{EE}	V_{CC}	V_{EE}	V_{CC}	V_{EE}	V_{CC}	V_{EE}	V_{CC}	V_{EE}	V_{CC}	O4R	O6R	O8R	**P**
N	O27L	O28L	O30L	V_{CCO}										V_{CCO}	O7R	O9R	O10R	**N**
M	O24L	O25L	O26L	V_{CCO}										V_{CCO}	O11R	O12R	O13R	**M**
L	O21L	O22L	O23L	V_{CCO}										V_{CCO}	O14R	O15R	O16R	**L**
K	O18L/ A13	O19L/ A14	O20L/ A15	V_{CCO}										V_{CCO}	O17R	O18R	O19R	**K**
J	O15L/ A10	O17L/ A12	O16L/ A11	V_{CCO}										V_{CCO}	O21R	O20R	O22R	**J**
H	O14L/ A9	O13L/ A8	O11L/ A6	V_{CCO}										V_{CCO}	O26R	O24R	O23R	**H**
G	O12L/ A7	O9L/ A4	O7L/ A2	V_{CCO}										V_{CCO}	O30R	O28R	O25R	**G**
F	O10L/ A5	O6L/ A1	O3L/ SEROUT	V_{CCO}										V_{CCO}	O34R	O31R	O27R	**F**
E	O8L/ A3	O4L	O0L/ BSOUT	V_{CCO}										V_{CCO}	O37R	O33R	O29R	**E**
D	O5L/ A0	O1L	St Pgm	V_{EE}	V_{CC}	V_{EE}	V_{CC}	V_{EE}	V_{CC}	V_{EE}	V_{CC}	V_{EE}	V_{CC}	V_{EE}	I38T/ R_ock	O36R	O32R	**D**
C	O2L/ RDY	Sys Done	V_{CC}	I3T/ M2	V_{CC}	I9T/ D5	I12T/ RB	I15T/ Q1_ck	V_{EE}	I22T	I26T	I29T	V_{EE}	I34T	V_{CC}	O39R	O35R	**C**
B	PCLK O	RESE T	I2T/M1	I5T/ D1	I7T/ D3	I10T/ D6	I13T/ WE	I16T/ bpsel	I19T/ Q2_ck	I21T/ T_ick	I24T	I27T	I30T	I32T	I35T	I37T	O38R	**B**
A	PCLKI	I1T/ M0	I4T/D0	I6T/ D2	I8T/ D4	I11T/ D7	I14T/ done	I17T/ M3	I18T/ GCK1	I20T	I23T	I25T	I28T	I31T	I33T	I36T	V_{CCO}	**A**
	17	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

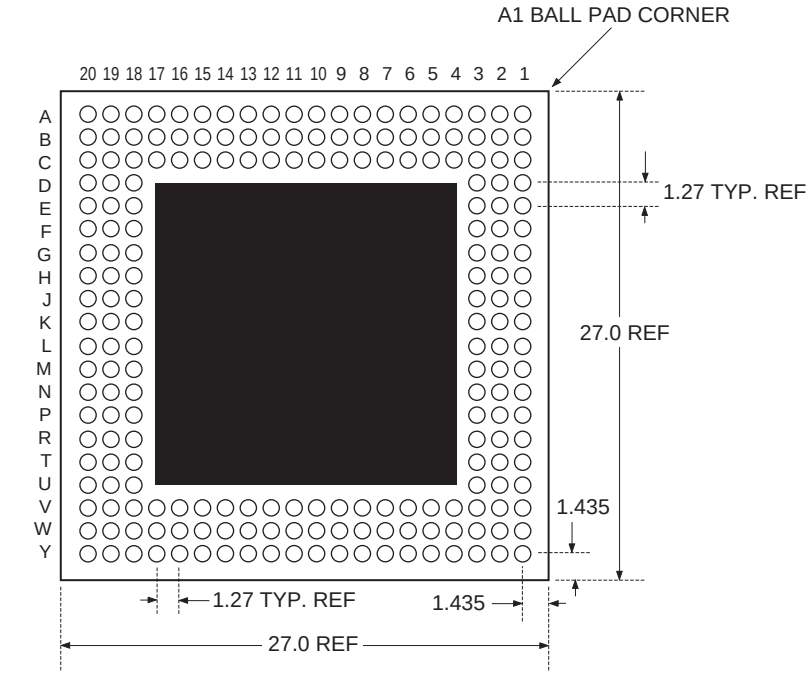
Table 13: DL5256 PGA Package Cross Reference table

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
Y	V_{EE}	V_{EE}	I4B	I7B	I10B	V_{EE}	I13B	I16B	I19B	V_{EE}	I20B/ GCK2	I23B/ B_ick	V_{EE}	I27B	I29B	I23B	I35B	I37B/ TMS	V_{EE}	V_{EE}	Y
W	O35L	V_{CC}	V_{EE}	I6B	I9B	I11B	I12B	I15B	I18B/ GRST	V_{EE}	I21B/ Q4_ck	I24B	I26B	I28B	I30B	I33B	I36B/ TDI	V_{EE}	V_{CCO}	O3R	W
V	O32L	I1B/ L_ock	V_{CC}	I3B	I5B	I8B	V_{CC}	I14B	I17B/ Q3_ck	V_{CC}	I22B	I25B	V_{CC}	I31B	I34B	V_{CC}	I38B/ TCK	V_{CCO}	O1R	O5R	V
U	O30L	O34L	I2B															O0R/ TDO	O4R	O8R	U
T	O27L	O31L	V_{CCO}															O2R	O7R	O9R	T
R	O26L	O28L	O33L															O6R	O10R	O11R	R
P	O24L	O25L	O29L															V_{CCO}	O13R	O14R	P
N	O21L	O23L	V_{CCO}															O12R	O15R	V_{EE}	N
M	O19L/ A14	O20LA 15	O22L															V_{CCO}	O16R	O17R	M
L	O16L/ A11	O17L/ A12	O18L/ A13															O19R	O18R	O20R	L
K	O14L/ A9	O15L/ A10	V_{CCO}															O22R	O21R	O23R	K
J	O13L/ A8	O11L/ A6	O12L/ A7															V_{CCO}	O25R	O24R	J
H	V_{EE}	O10L/ A5	O8L/ A3															O29R	O26R	V_{EE}	H
G	O9L/ A4	O7L/ A2	V_{CCO}															O33R	O28R	O27R	G
F	O6L/ A1	O5L/ A0	OIL															O36R	O32R	O30R	F
E	O4L	O2LR DY	Sys Done															V_{CCO}	O35R	O31R	E
D	O3L/ SEROUT	PCLKO	RESET															I37T	O38R	O34R	D
C	O0L/ BSOUT	PCLKI	V_{CCO}	I1T/M0	V_{CC}	I5T/D1	I9T/D5	V_{CC}	I14T/ done	I17T/ M3	I20T	V_{CC}	I26T	V_{CC}	I31T	I34T	I36T	V_{CC}	I38T/ R_ock	O37R	C
B	St Pgm	V_{CCO}	V_{EE}	I3T/M2	I6T/D2	I8T/D4	I1OT/ D6	I12T/ RB	I15T/ Q1_ck	V_{EE}	I19T/ Q2_ck	I22T	I23T	I25T	I28T	I30T	I33T	V_{EE}	V_{CC}	O39R	B
A	V_{EE}	V_{EE}	I2TM1	I4T/D0	I7T/D3	V_{EE}	I11T/ D7	I13T/ WE	I16T/ bpsel	V_{EE}	I18T/ GCK1	I21T/ T_ick	V_{EE}	I24T	I27T	I29T	I32T	I35T	V_{EE}	V_{EE}	A
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

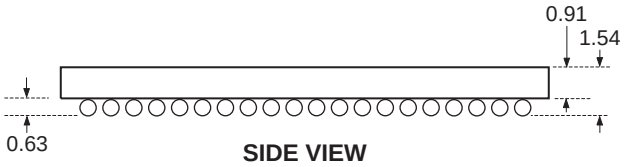
Table 14: DL5256 BGA Package Cross Reference table

Package Drawings

204 Super BGA

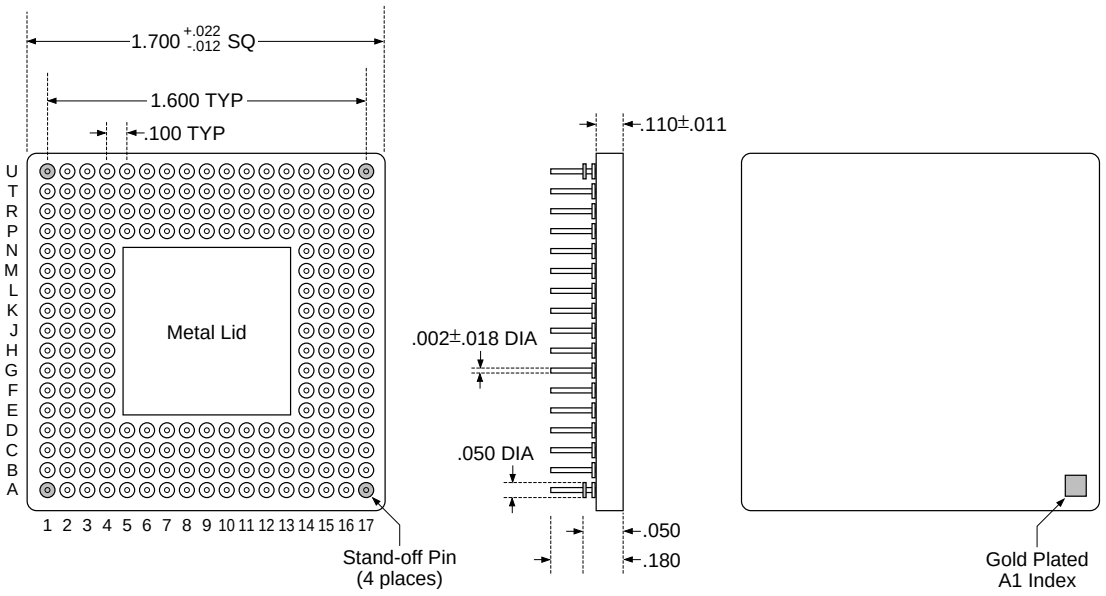


UNIT SHOWN FROM BALL ARRAY SIDE
(Dimensions in mm)

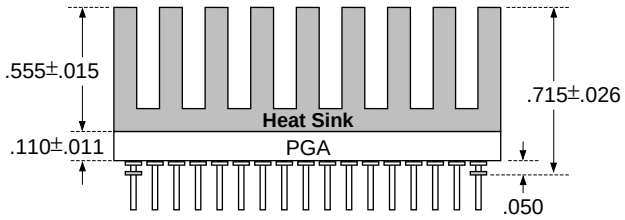


SIDE VIEW

208 Pin Ceramic PGA



208 PGA with Heat Sink



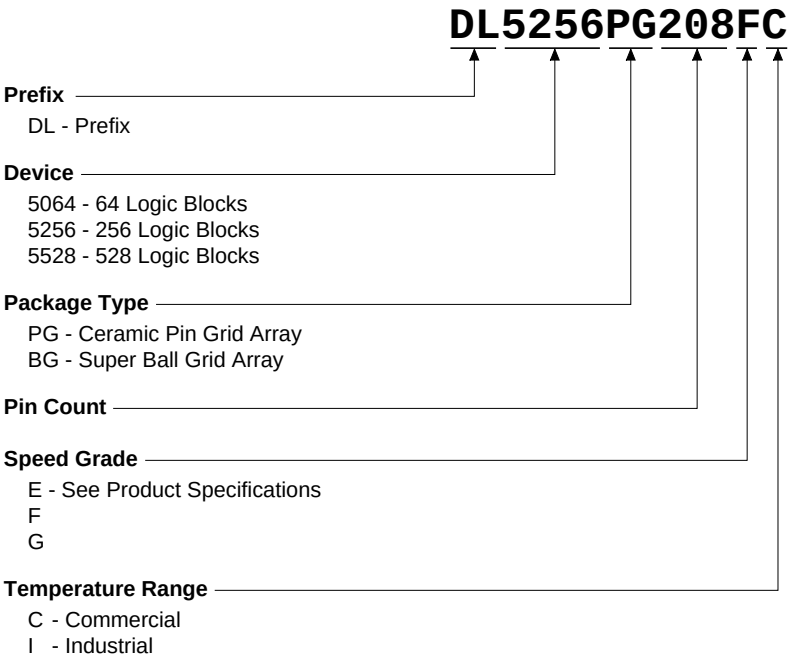
Note:

All Dimensions are in inches

The above illustrated heat sink is for operating at maximum power of 10 watts and requires air flow of 400 lfm. If the expected maximum power is less that 6 watts, a shorter heat sink of .350 inch height can be used for total height of less than .550. This combination can operate under natural convection.

Ordering Information

Order codes are shown below.



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